

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (L<sup>2</sup>-π-MOSV)

## 2SK3387

Switching Regulator, DC-DC Converter and Motor Drive Applications

- 4-V gate drive
- Low drain-source ON resistance:  $R_{DS(ON)} = 0.08 \Omega$  (typ.)
- High forward transfer admittance:  $|Y_{fs}| = 17 \text{ S}$  (typ.)
- Low leakage current:  $I_{DSS} = 100 \mu\text{A}$  ( $V_{DS} = 150 \text{ V}$ )
- Enhancement mode:  $V_{th} = 0.8 \sim 2.0 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 1 \text{ mA}$ )

### Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	150	V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	150	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	DC (Note 1)	$I_D$	A
	Pulse (Note 1)	$I_{DP}$	
Drain power dissipation ( $T_c = 25^\circ\text{C}$ )	$P_D$	100	W
Single pulse avalanche energy (Note 2)	$E_{AS}$	176	mJ
Avalanche current	$I_{AR}$	18	A
Repetitive avalanche energy (Note 3)	$E_{AR}$	10	mJ
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature range	$T_{stg}$	$-55 \sim 150$	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

### Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	1.25	$^\circ\text{C/W}$

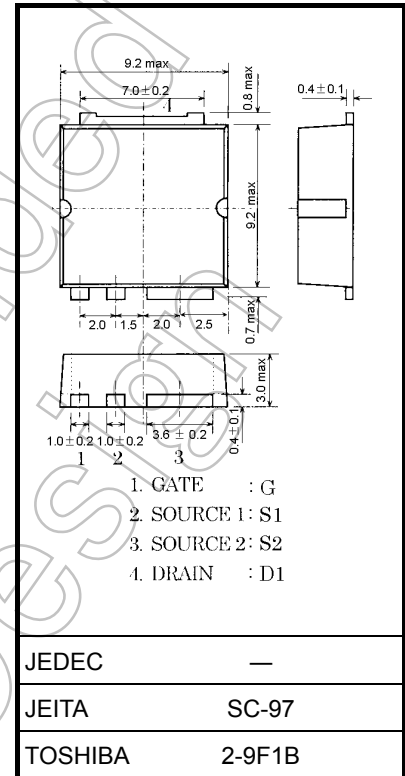
Note 1: Ensure that the channel temperature does not exceed  $150^\circ\text{C}$ .

Note 2:  $V_{DD} = 50 \text{ V}$ ,  $T_{ch} = 25^\circ\text{C}$  (initial),  $L = 800 \mu\text{H}$ ,  $R_G = 25 \Omega$ ,  $I_{AR} = 18 \text{ A}$

Note 3: Repetitive rating: pulse width limited by max junction temperature

This transistor is an electrostatic-sensitive device.  
Please handle with caution.

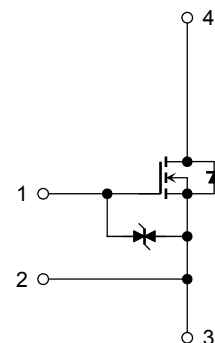
Unit: mm



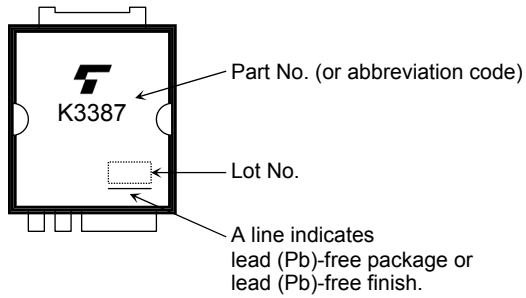
Weight: 0.74 g (typ.)

Notice:

Please use the S1 pin for gate input signal return. Make sure that the main current flows into S2 pin.



## Marking

Electrical Characteristics (Note 4) ( $T_a = 25^\circ\text{C}$ )

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		$I_{GSS}$	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
Drain cut-off current		$I_{DSS}$	$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}$	—	—	100	$\mu\text{A}$
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	150	—	—	V
Gate threshold voltage		$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	0.8	—	2.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 4\text{ V}, I_D = 9\text{ A}$	—	0.09	0.18	$\Omega$
			$V_{GS} = 10\text{ V}, I_D = 9\text{ A}$	—	0.08	0.12	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 9\text{ A}$	10	17	—	S
Input capacitance		$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	1380	—	pF
Reverse transfer capacitance		$C_{rss}$		—	200	—	
Output capacitance		$C_{oss}$		—	610	—	
Switching time	Rise time	$t_r$		—	12	—	ns
	Turn-on time	$t_{on}$		—	20	—	
	Fall time	$t_f$		—	12	—	
	Turn-off time	$t_{off}$		—	68	—	
Total gate charge (gate-source plus gate-drain)		$Q_g$	$V_{DD} \approx 120\text{ V}, V_{GS} = 10\text{ V}, I_D = 18\text{ A}$	—	57	—	nC
Gate-source charge		$Q_{gs}$		—	43	—	nC
Gate-drain ("miller") charge		$Q_{gd}$		—	14	—	nC

Note 4: Connect the S1 and S2 pins together, and ground them except during switching time measurement.

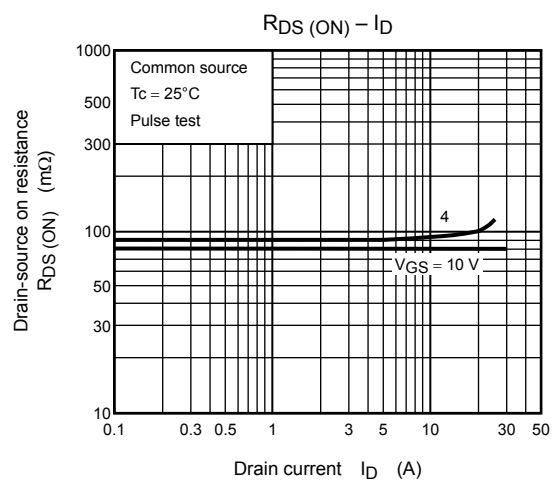
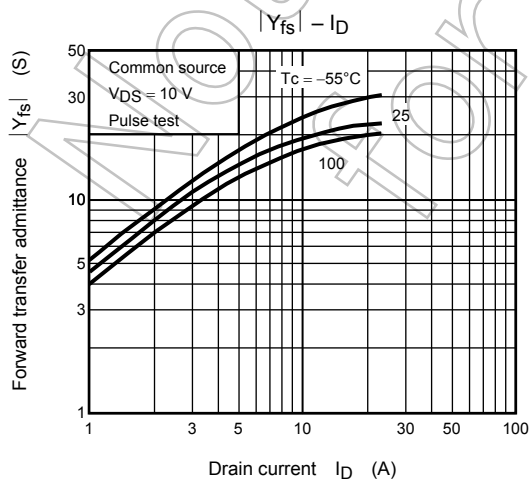
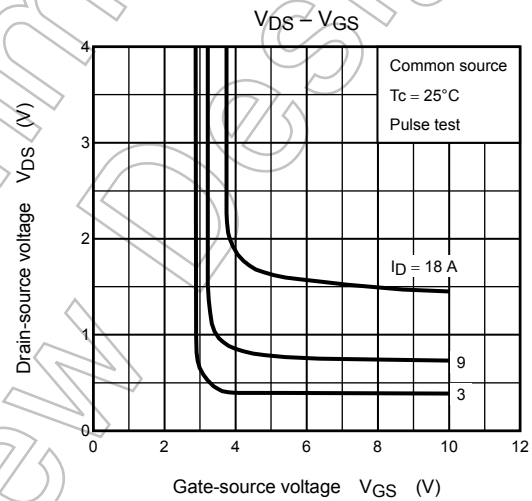
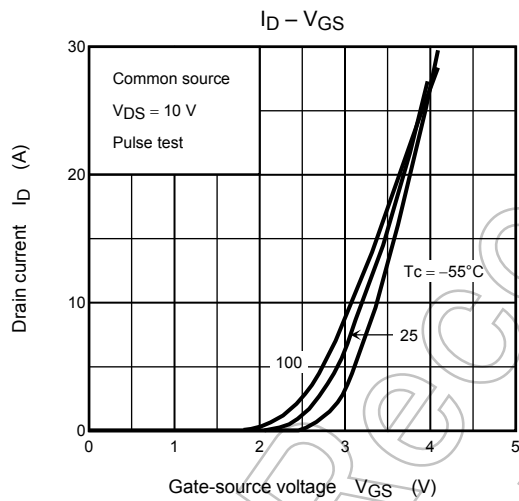
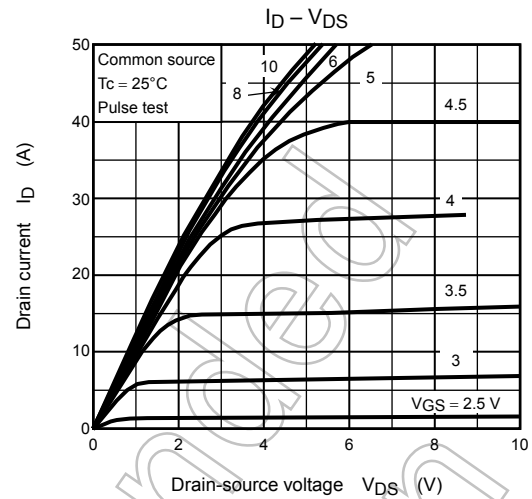
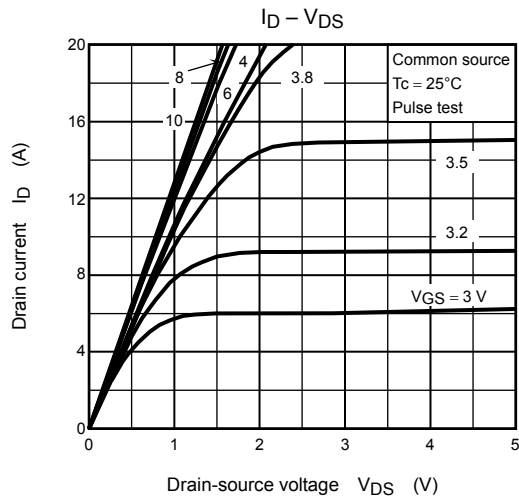
Source-Drain Diode Ratings and Characteristics (Note 5) ( $T_a = 25^\circ\text{C}$ )

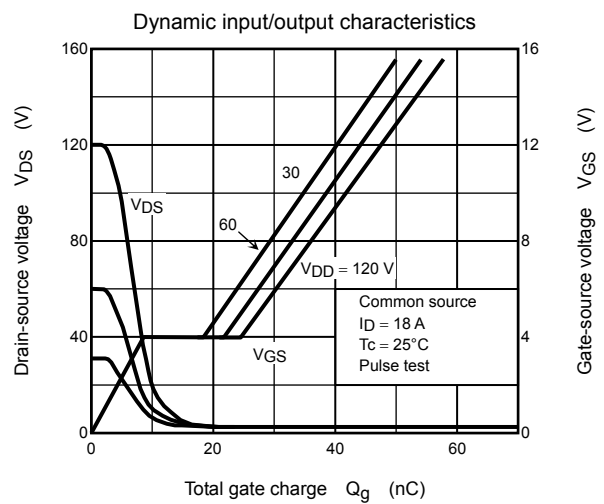
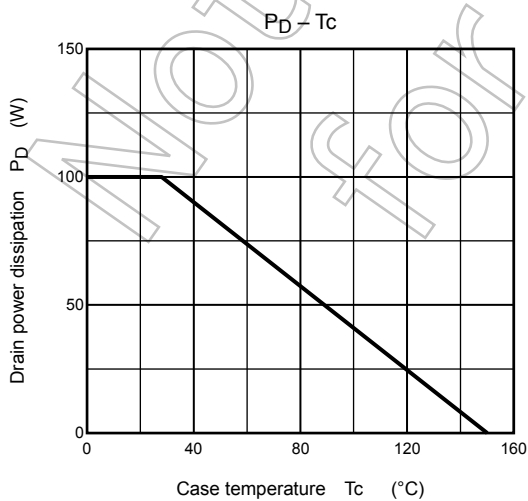
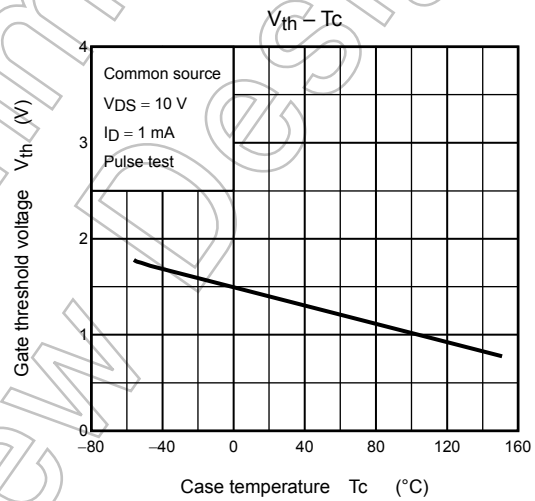
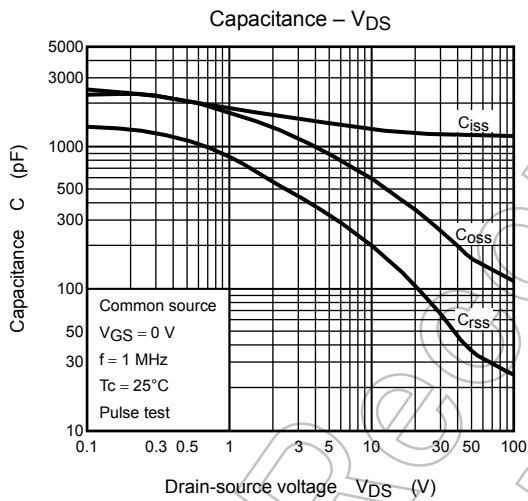
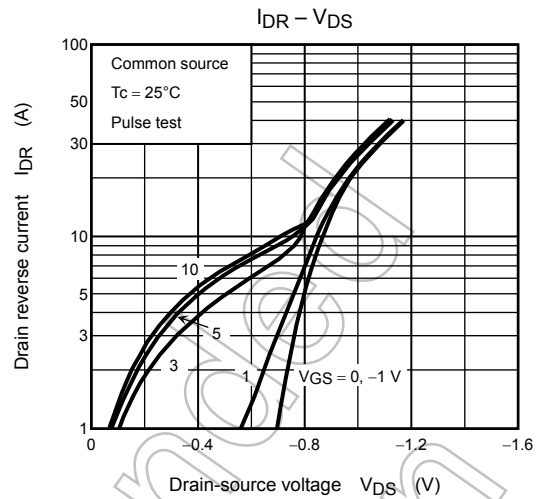
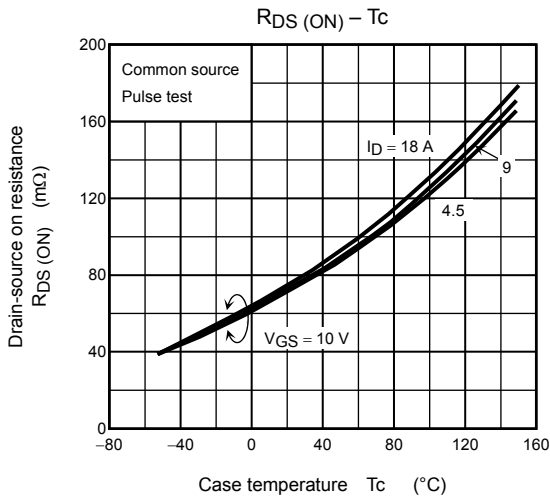
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1, 5)	$I_{DR1}$	—	—	—	18	A
Pulse drain reverse current (Note 1, 5)	$I_{DRP1}$	—	—	—	54	A
Continuous drain reverse current (Note 1, 5)	$I_{DR2}$	—	—	—	1	A
Pulse drain reverse current (Note 1, 5)	$I_{DRP2}$	—	—	—	4	A
Diode forward voltage	$V_{DS2F}$	$I_{DR1} = 18\text{ A}, V_{GS} = 0\text{ V}$	—	—	$-1.7$	V
Reverse recovery time	$t_{rr}$	$I_{DR} = 18\text{ A}, V_{GS} = 0\text{ V},$	—	185	—	ns
Reverse recovery charge	$Q_{rr}$	$dI_{DR}/dt = 100\text{ A}/\mu\text{s}$	—	1.3	—	$\mu\text{C}$

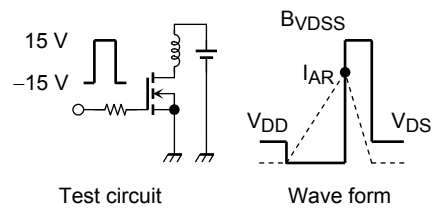
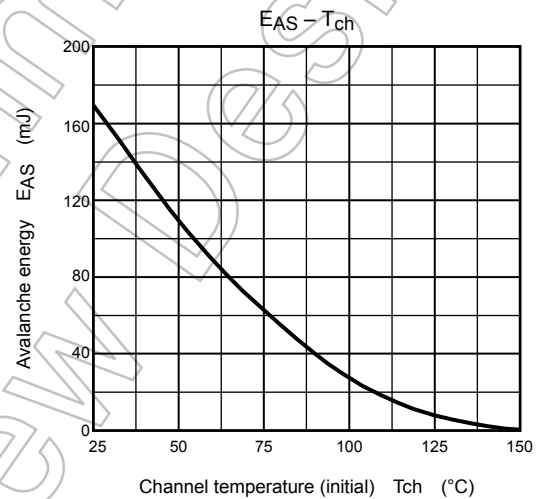
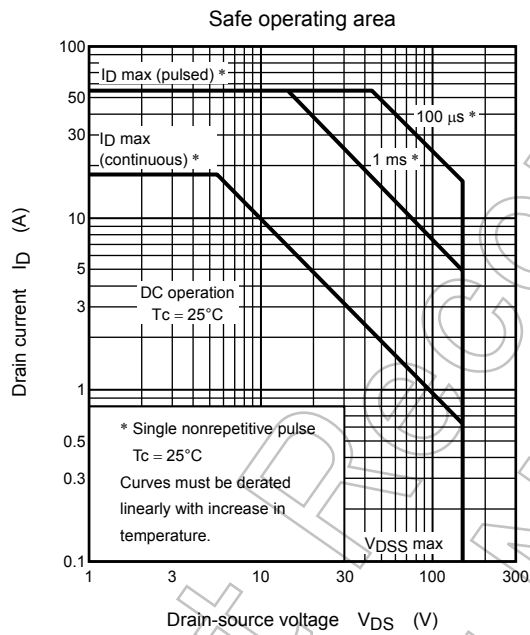
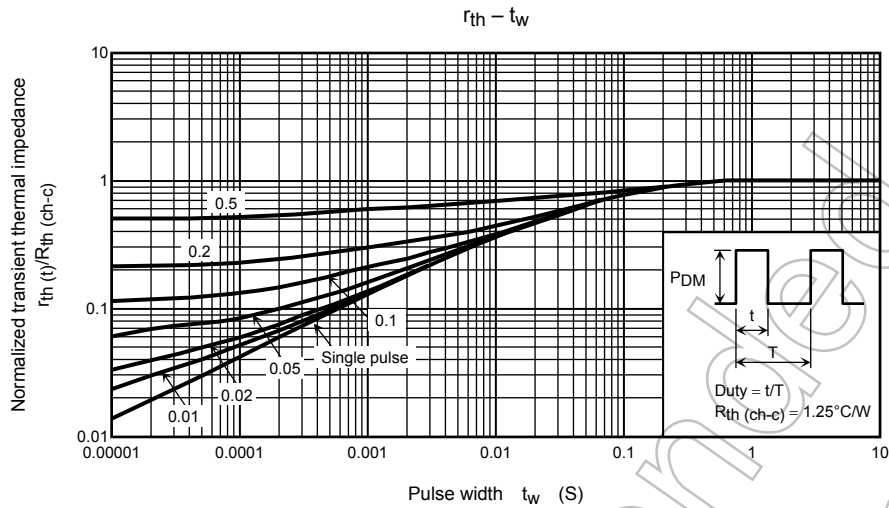
Note 5:  $I_{DR1}$ ,  $I_{DRP1}$ : Current flowing between the drain and the S2 pin. Ensure that the S1 pin is left open.

$I_{DR2}$ ,  $I_{DRP2}$ : Current flowing between the drain and the S1 pin. Ensure that the S2 pin is left open.

Unless otherwise specified, connect the S1 and S2 pins together, and ground them







$$R_G = 25 \, \Omega$$

$$V_{DD} = 50 \, \text{V}, L = 0.8 \, \text{mH}$$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left( \frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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