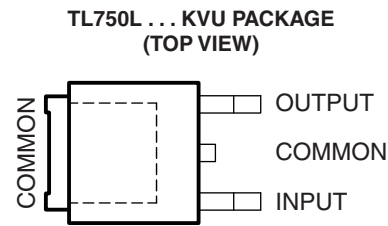
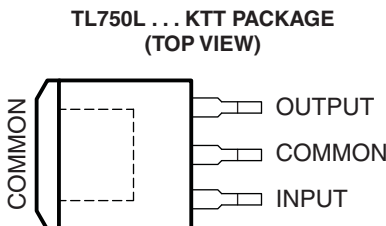
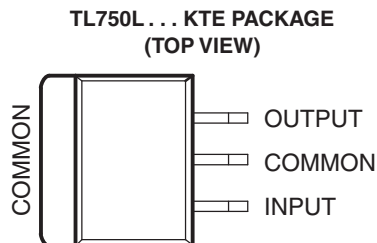
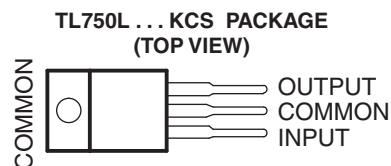
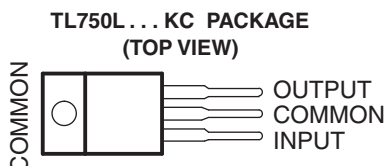
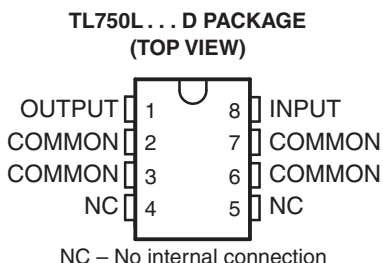


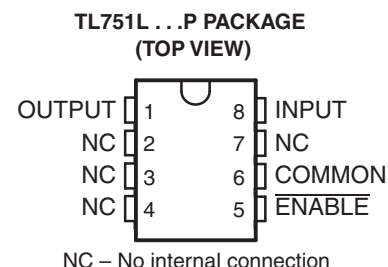
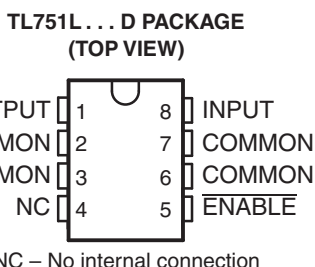
## LOW-DROPOUT VOLTAGE REGULATORS

### FEATURES

- **Very Low Dropout Voltage, Less Than 0.6 V at 150 mA**
- **Very Low Quiescent Current**
- **TTL- and CMOS-Compatible Enable on TL751L Series**
- **60-V Load-Dump Protection**
- **Reverse Transient Protection Down to –50 V**
- **Internal Thermal-Overload Protection**
- **Overvoltage Protection**
- **Internal Overcurrent-Limiting Circuitry**
- **Less Than 500-μA Disable (TL751L Series)**



**TL750L...LP PACKAGE  
(TO-92, TO-226AA)  
(TOP VIEW)**



### DESCRIPTION/ORDERING INFORMATION

The TL750L and TL751L series of fixed-output voltage regulators offer 5-V, 8-V, 10-V, and 12-V options. The TL751L series also has an enable (ENABLE) input. When ENABLE is high, the regulator output is placed in the high-impedance state. This gives the designer complete control over power up, power down, or emergency shutdown.

The TL750L and TL751L series are low-dropout positive-voltage regulators specifically designed for battery-powered systems. These devices incorporate overvoltage and current-limiting protection circuitry, along with internal reverse-battery protection circuitry to protect the devices and the regulated system. The series is fully protected against 60-V load-dump and reverse-battery conditions. Extremely low quiescent current during full-load conditions makes these devices ideal for standby power systems.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# ORDERING INFORMATION<sup>(1)</sup>

T <sub>J</sub>	V <sub>O</sub> TYP AT 25°C	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	5 V	PowerFLEX™ – KTE	Reel of 2000	TL750L05CKTER	TL750L05C
		SOIC – D	Tube of 75	TL750L05CD	50L05C
			Reel of 2500	TL750L05CDR	
			Tube of 75	TL751L05CD	51L05C
			Reel of 2500	TL751L05CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L05CLP	750L05C
			Reel of 2000	TL750L05CLPR	
		TO-220 – KC	Tube of 50	TL750L05CKC	TL750L05C
		TO-220 – KCS	Tube of 50	TL750L05CKCS	TL750L05C
		TO-252 – KVU	Reel of 2500	TL750L05CKVUR	750L05C
		TO-263 – KTT	Reel of 500	TL750L05CKTTR	750L05C
	8 V	SOIC – D	Tube of 75	TL750L08CD	50L08C
			Reel of 2500	TL750L08CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L08CLP	750L08C
	10 V	PDIP – P	Tube of 50	TL751L10CP	TL751L10C
		SOIC – D	Tube of 75	TL750L10CD	50L10C
			Reel of 2500	TL750L10CDR	
			Tube of 75	TL751L10CD	51L10C
			Reel of 2500	TL751L10CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L10CLP	750L10C
			Reel of 2000	TL750L10CLPR	
	12 V	SOIC – D	Tube of 75	TL750L12CD	50L12C
			Reel of 2500	TL750L12CDR	
			Tube of 75	TL751L12CD	51L12C
			Reel of 2500	TL751L12CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L12CLP	750L12C

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).  
(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

DEVICE COMPONENT COUNT	
Transistors	20
JFETs	2
Diodes	5
Resistors	16

## Absolute Maximum Ratings<sup>(1)</sup>

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Continuous input voltage		26	V
	Transient input voltage <sup>(2)</sup>	$T_A = 25^\circ\text{C}$	60	V
	Continuous reverse input voltage		–15	V
	Transient reverse input voltage	$t \leq 100 \text{ ms}$	–50	V
$T_J$	Operating virtual junction temperature		150	$^\circ\text{C}$
	Lead temperature	1,6 mm (1/16 in) for 10 s	260	$^\circ\text{C}$
$T_{\text{stg}}$	Storage temperature range		–65	150
				$^\circ\text{C}$

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The transient input voltage rating applies to the waveform shown in Figure 1.

## Package Thermal Data<sup>(1)</sup>

PACKAGE	BOARD	$\theta_{JC}$	$\theta_{JA}$
PDIP (P)	High K, JESD 51-7	57 $^\circ\text{C}/\text{W}$	85 $^\circ\text{C}/\text{W}$
PowerFLEX™ (KTE)	High K, JESD 51-5	3 $^\circ\text{C}/\text{W}$	23 $^\circ\text{C}/\text{W}$
SOIC (D)	High K, JESD 51-7	39 $^\circ\text{C}/\text{W}$	97 $^\circ\text{C}/\text{W}$
TO-226/TO-92 (LP)	High K, JESD 51-7	55 $^\circ\text{C}/\text{W}$	140 $^\circ\text{C}/\text{W}$
TO-220 (KC)	High K, JESD 51-5	3 $^\circ\text{C}/\text{W}$	19 $^\circ\text{C}/\text{W}$
TO-220 (KCS)	High K, JESD 51-5	3 $^\circ\text{C}/\text{W}$	19 $^\circ\text{C}/\text{W}$
TO-252 (KVU)	High K, JESD 51-5	–	30.3 $^\circ\text{C}/\text{W}$
TO-263 (KTT)	High K, JESD 51-5	18 $^\circ\text{C}/\text{W}$	25.3 $^\circ\text{C}/\text{W}$

- (1) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150 $^\circ\text{C}$  can affect reliability.

## Recommended Operating Conditions

over recommended operating junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_I$	Input voltage	TL75xL05	6	26	V
		TL75xL08	9	26	
		TL75xL10	11	26	
		TL75xL12	13	26	
$V_{IH}$	High-level $\overline{\text{ENABLE}}$ input voltage	TL75xLxx	2	15	V
$V_{IL}^{(1)}$	Low-level $\overline{\text{ENABLE}}$ input voltage	$T_J = 25^\circ\text{C}$ TL75xLxx	–0.3	0.8	V
		$T_J = 0^\circ\text{C to } 125^\circ\text{C}$ TL75xLxx	–0.15	0.8	
$I_O$	Output current	TL75xLxx	0	150	mA
$T_J$	Operating virtual junction temperature	TL75xLxxC	0	125	$^\circ\text{C}$

- (1) The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for  $\overline{\text{ENABLE}}$  voltage levels and temperature only.

## TL75xL05 Electrical Characteristics<sup>(1)</sup>

$V_I = 14\text{ V}$ ,  $I_O = 10\text{ mA}$ ,  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL750L05 TL751L05			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = 6\text{ V to } 26\text{ V}$ , $I_O = 0\text{ to } 150\text{ mA}$	$T_J = 25^\circ\text{C}$	4.8	5	V
		$T_J = 0^\circ\text{C to } 125^\circ\text{C}$	4.75	5.25	
Input regulation voltage	$V_I = 9\text{ V to } 16\text{ V}$		5	10	mV
	$V_I = 6\text{ V to } 26\text{ V}$		6	30	
Ripple rejection	$V_I = 8\text{ V to } 18\text{ V}$ , $f = 120\text{ Hz}$	60	65		dB
Output regulation voltage	$I_O = 5\text{ mA to } 150\text{ mA}$		20	50	mV
Dropout voltage	$I_O = 10\text{ mA}$			0.2	V
	$I_O = 150\text{ mA}$			0.6	
Output noise voltage	$f = 10\text{ Hz to } 100\text{ kHz}$		500		$\mu\text{V}$
Quiescent current	$I_O = 150\text{ mA}$		10	12	mA
	$V_I = 6\text{ V to } 26\text{ V}$ , $I_O = 10\text{ mA}$ , $T_J = 0^\circ\text{C to } 125^\circ\text{C}$		1	2	
	$\overline{\text{ENABLE}} \geq 2\text{ V}$			0.5	

- (1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a  $0.1\text{-}\mu\text{F}$  capacitor across the input and a  $10\text{-}\mu\text{F}$  capacitor, with equivalent series resistance of less than  $0.4\ \Omega$ , across the output.

## TL75xL08 Electrical Characteristics<sup>(1)</sup>

$V_I = 14\text{ V}$ ,  $I_O = 10\text{ mA}$ ,  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL750L08 TL751L08			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = 9\text{ V to } 26\text{ V}$ , $I_O = 0\text{ to } 150\text{ mA}$	$T_J = 25^\circ\text{C}$	7.68	8	V
		$T_J = 0^\circ\text{C to } 125^\circ\text{C}$	7.6	8.4	
Input regulation voltage	$V_I = 10\text{ V to } 17\text{ V}$		10	20	mV
	$V_I = 9\text{ V to } 26\text{ V}$		25	50	
Ripple rejection	$V_I = 11\text{ V to } 21\text{ V}$ , $f = 120\text{ Hz}$	60	65		dB
Output regulation voltage	$I_O = 5\text{ mA to } 150\text{ mA}$		40	80	mV
Dropout voltage	$I_O = 10\text{ mA}$			0.2	V
	$I_O = 150\text{ mA}$			0.6	
Output noise voltage	$f = 10\text{ Hz to } 100\text{ kHz}$		500		$\mu\text{V}$
Quiescent current	$I_O = 150\text{ mA}$		10	12	mA
	$V_I = 9\text{ V to } 26\text{ V}$ , $I_O = 10\text{ mA}$ , $T_J = 0^\circ\text{C to } 125^\circ\text{C}$		1	2	
	$\overline{\text{ENABLE}} \geq 2\text{ V}$			0.5	

- (1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a  $0.1\text{-}\mu\text{F}$  capacitor across the input and a  $10\text{-}\mu\text{F}$  capacitor, with equivalent series resistance of less than  $0.4\ \Omega$ , across the output.

## TL75xL10 Electrical Characteristics<sup>(1)</sup>

 $V_I = 14\text{ V}$ ,  $I_O = 10\text{ mA}$ ,  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL750L10 TL751L10			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = 11\text{ V to } 26\text{ V}$ , $I_O = 0\text{ to } 150\text{ mA}$	$T_J = 25^\circ\text{C}$	9.6	10	V
		$T_J = 0^\circ\text{C to } 125^\circ\text{C}$	9.5	10.5	
Input regulation voltage	$V_I = 12\text{ V to } 19\text{ V}$		10	25	mV
	$V_I = 11\text{ V to } 26\text{ V}$		30	60	
Ripple rejection	$V_I = 12\text{ V to } 22\text{ V}$ , $f = 120\text{ Hz}$	60	65		dB
Output regulation voltage	$I_O = 5\text{ mA to } 150\text{ mA}$		50	100	mV
Dropout voltage	$I_O = 10\text{ mA}$			0.2	V
	$I_O = 150\text{ mA}$			0.6	
Output noise voltage	$f = 10\text{ Hz to } 100\text{ kHz}$		700		$\mu\text{V}$
Quiescent current	$I_O = 150\text{ mA}$		10	12	mA
	$V_I = 11\text{ V to } 26\text{ V}$ , $I_O = 10\text{ mA}$ , $T_J = 0^\circ\text{C to } 125^\circ\text{C}$		1	2	
	$\overline{\text{ENABLE}} \geq 2\text{ V}$			0.5	

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- $\mu\text{F}$  capacitor across the input and a 10- $\mu\text{F}$  capacitor, with equivalent series resistance of less than 0.4  $\Omega$ , across the output.

## TL75xL12 Electrical Characteristics<sup>(1)</sup>

 $V_I = 14\text{ V}$ ,  $I_O = 10\text{ mA}$ ,  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL750L12 TL751L12			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = 13\text{ V to } 26\text{ V}$ , $I_O = 0\text{ to } 150\text{ mA}$	$T_J = 25^\circ\text{C}$	11.52	12	V
		$T_J = 0^\circ\text{C to } 125^\circ\text{C}$	11.4	12.6	
Input regulation voltage	$V_I = 14\text{ V to } 19\text{ V}$		15	30	mV
	$V_I = 13\text{ V to } 26\text{ V}$		20	40	
Ripple rejection	$V_I = 13\text{ V to } 23\text{ V}$ , $f = 120\text{ Hz}$	50	55		dB
Output regulation voltage	$I_O = 5\text{ mA to } 150\text{ mA}$		50	120	mV
Dropout voltage	$I_O = 10\text{ mA}$			0.2	V
	$I_O = 150\text{ mA}$			0.6	
Output noise voltage	$f = 10\text{ Hz to } 100\text{ kHz}$		700		$\mu\text{V}$
Quiescent current	$I_O = 150\text{ mA}$		10	12	mA
	$V_I = 13\text{ V to } 26\text{ V}$ , $I_O = 10\text{ mA}$ , $T_J = 0^\circ\text{C to } 125^\circ\text{C}$		1	2	
	$\overline{\text{ENABLE}} \geq 2\text{ V}$			0.5	

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- $\mu\text{F}$  capacitor across the input and a 10- $\mu\text{F}$  capacitor, with equivalent series resistance of less than 0.4  $\Omega$ , across the output.

## PARAMETER MEASUREMENT INFORMATION

The TL750L, TL751L series are low-dropout regulators. This means that capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and its equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and temperature range. [Figure 1](#) shows the recommended range of ESR for a given load with a 10- $\mu\text{F}$  capacitor on the output.

## TYPICAL CHARACTERISTICS

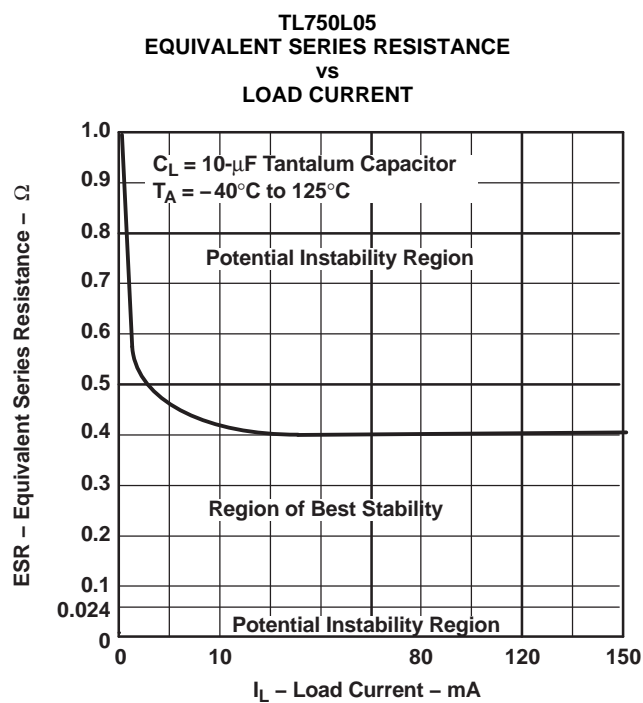


Figure 1.

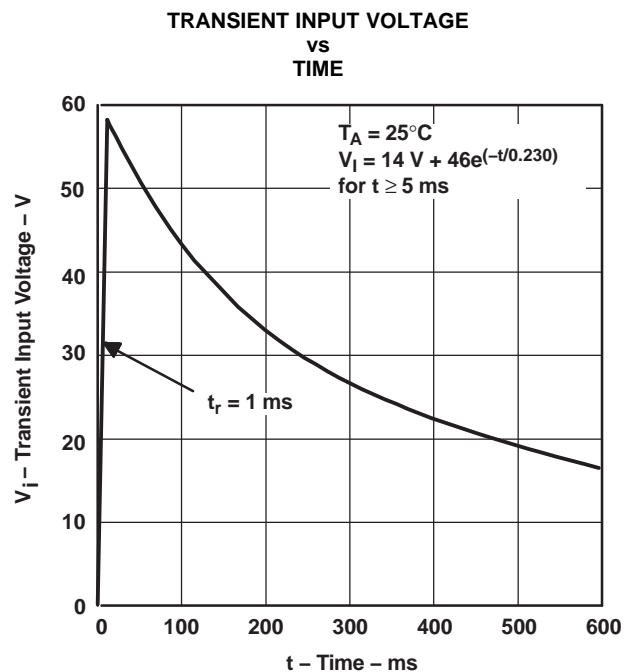


Figure 2.

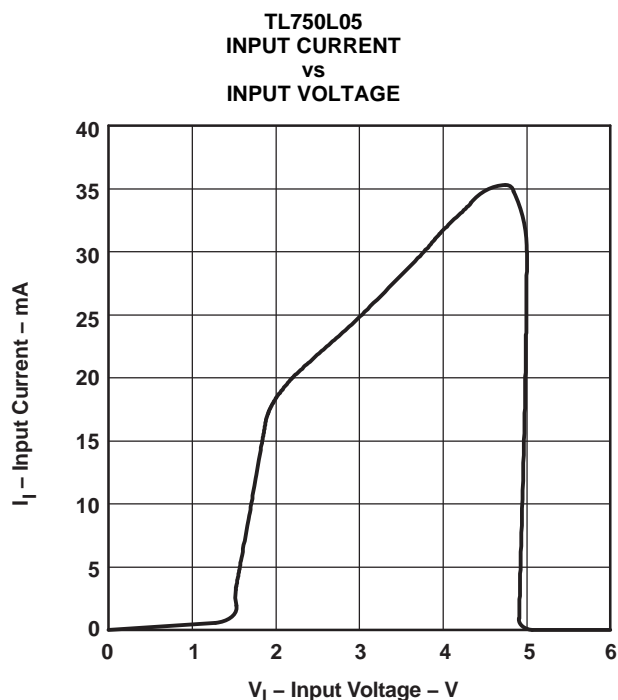


Figure 3.

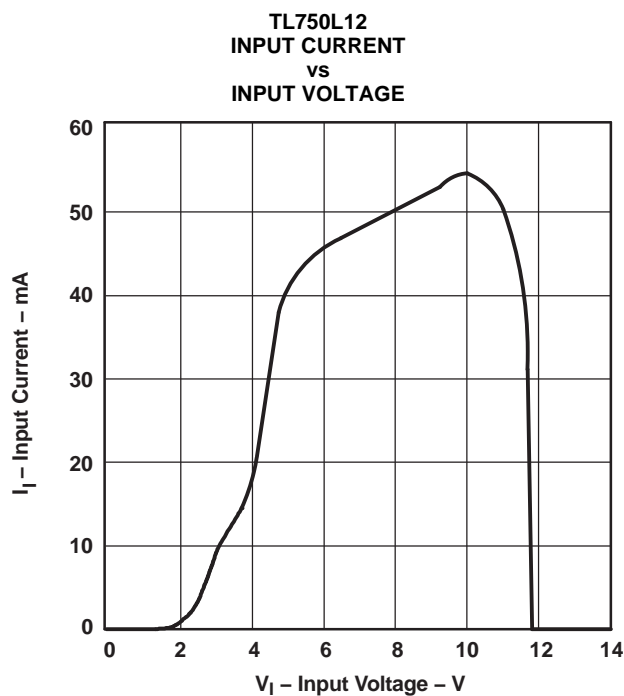


Figure 4.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL750L05CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	50L05C	<a href="#">Samples</a>
TL750L05CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	50L05C	<a href="#">Samples</a>
TL750L05CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	50L05C	<a href="#">Samples</a>
TL750L05CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	50L05C	<a href="#">Samples</a>
TL750L05CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TL750L05C	<a href="#">Samples</a>
TL750L05CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TL750L05C	<a href="#">Samples</a>
TL750L05CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	TL750L05C	<a href="#">Samples</a>
TL750L05CKTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	TL750L05C	<a href="#">Samples</a>
TL750L05CKVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	750L05C	<a href="#">Samples</a>
TL750L05CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	750L05C	<a href="#">Samples</a>
TL750L05CLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	750L05C	<a href="#">Samples</a>
TL750L05CLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	750L05C	<a href="#">Samples</a>
TL750L05CLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	750L05C	<a href="#">Samples</a>
TL750L08CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	50L08C	<a href="#">Samples</a>
TL750L08CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	50L08C	<a href="#">Samples</a>
TL750L08CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	50L08C	<a href="#">Samples</a>
TL750L08CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	50L08C	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL750L08CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	750L08C	<a href="#">Samples</a>
TL750L08CLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	750L08C	<a href="#">Samples</a>
TL750L10CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	50L10C	<a href="#">Samples</a>
TL750L10CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	50L10C	<a href="#">Samples</a>
TL750L10CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	50L10C	<a href="#">Samples</a>
TL750L10CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	50L10C	<a href="#">Samples</a>
TL750L10CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	750L10C	<a href="#">Samples</a>
TL750L10CLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	750L10C	<a href="#">Samples</a>
TL750L12CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	50L12C	<a href="#">Samples</a>
TL750L12CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	50L12C	<a href="#">Samples</a>
TL750L12CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	50L12C	<a href="#">Samples</a>
TL750L12CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	50L12C	<a href="#">Samples</a>
TL750L12CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	750L12C	<a href="#">Samples</a>
TL751L05CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	51L05C	<a href="#">Samples</a>
TL751L05CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	51L05C	<a href="#">Samples</a>
TL751L05CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	51L05C	<a href="#">Samples</a>
TL751L05CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	51L05C	<a href="#">Samples</a>
TL751L10CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	51L10C	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL751L10CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	51L10C	<a href="#">Samples</a>
TL751L10CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 125	TL751L10C	<a href="#">Samples</a>
TL751L12CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	51L12C	<a href="#">Samples</a>
TL751L12CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	51L12C	<a href="#">Samples</a>
TL751L12CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	51L12C	<a href="#">Samples</a>
TL751L12CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	51L12C	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

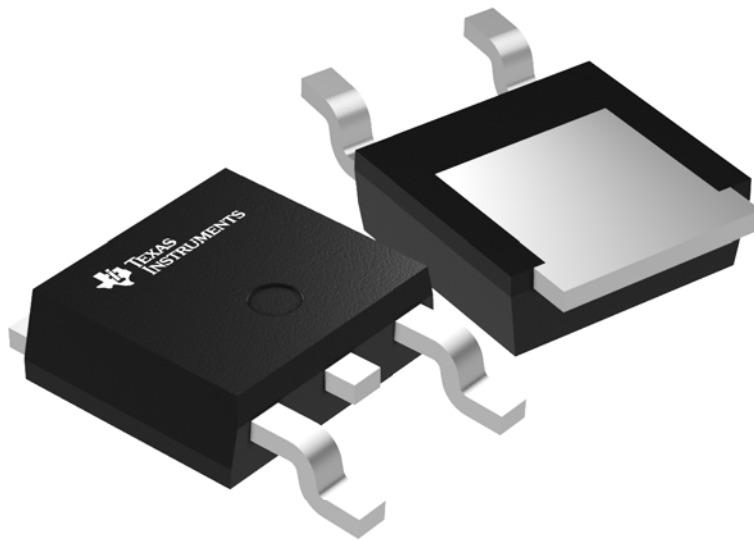
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL750L05CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL750L05CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.1	4.9	16.0	24.0	Q2
TL750L05CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TL750L05CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL750L08CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL750L10CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL750L12CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL751L05CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL751L10CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL751L12CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL750L05CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL750L05CKTTR	DDPAK/TO-263	KTT	3	500	350.0	334.0	47.0
TL750L05CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
TL750L05CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TL750L08CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL750L10CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL750L12CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL751L05CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL751L10CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL751L12CDR	SOIC	D	8	2500	340.5	338.1	20.6



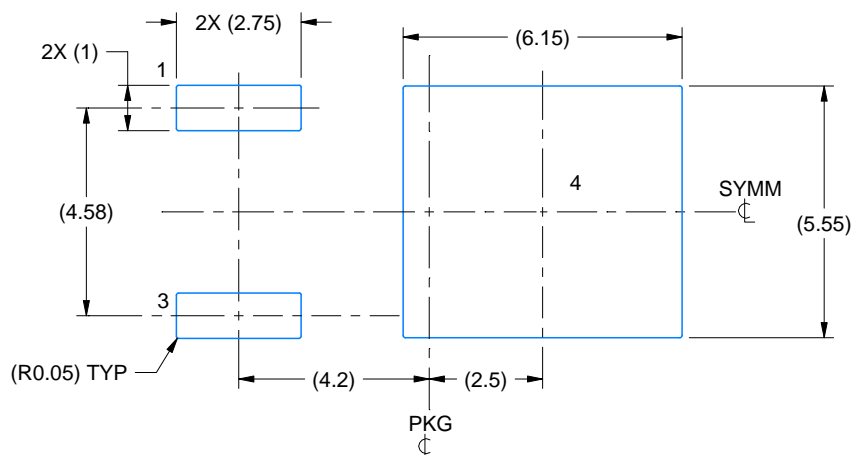
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



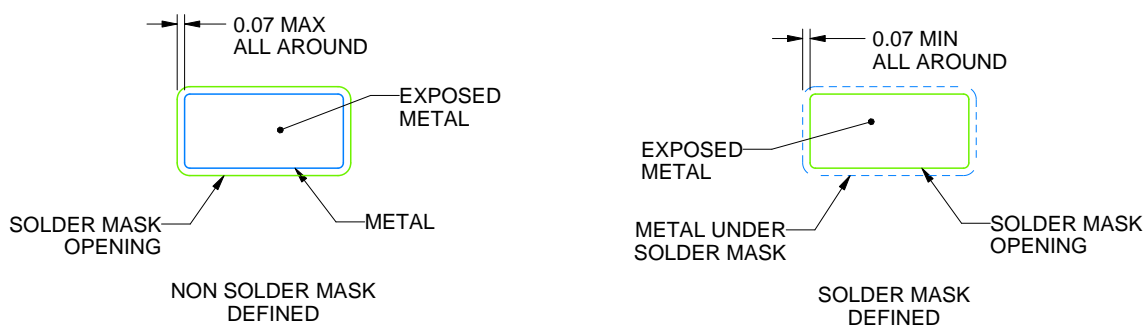
**KVU0003A**

**TO-252 - 2.52 mm max height**

TO-252



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS  
NOT TO SCALE

4218915/A 02/2017

NOTES: (continued)

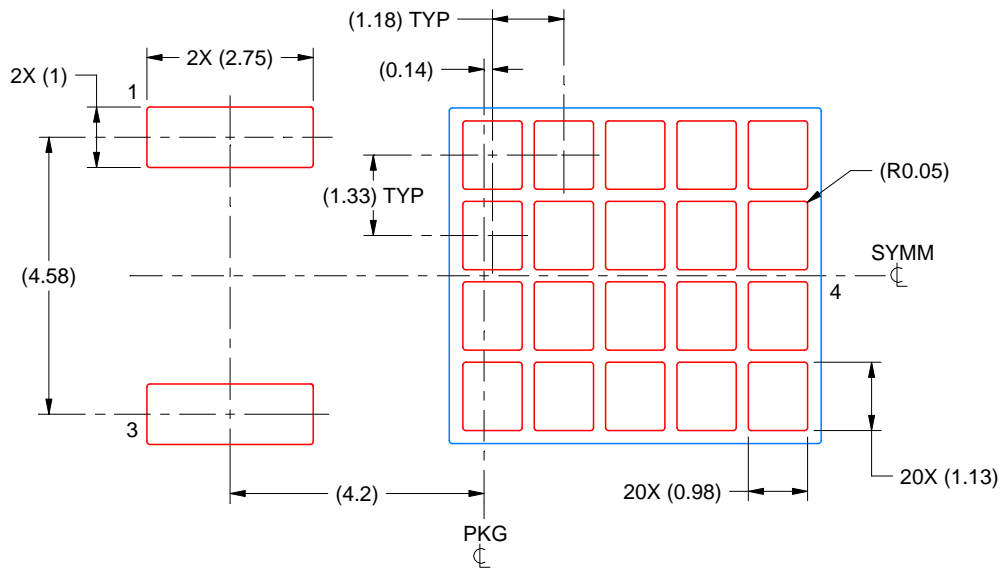
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002([www.ti.com/lit/slm002](http://www.ti.com/lit/slm002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
65% PRINTED SOLDER COVERAGE BY AREA  
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

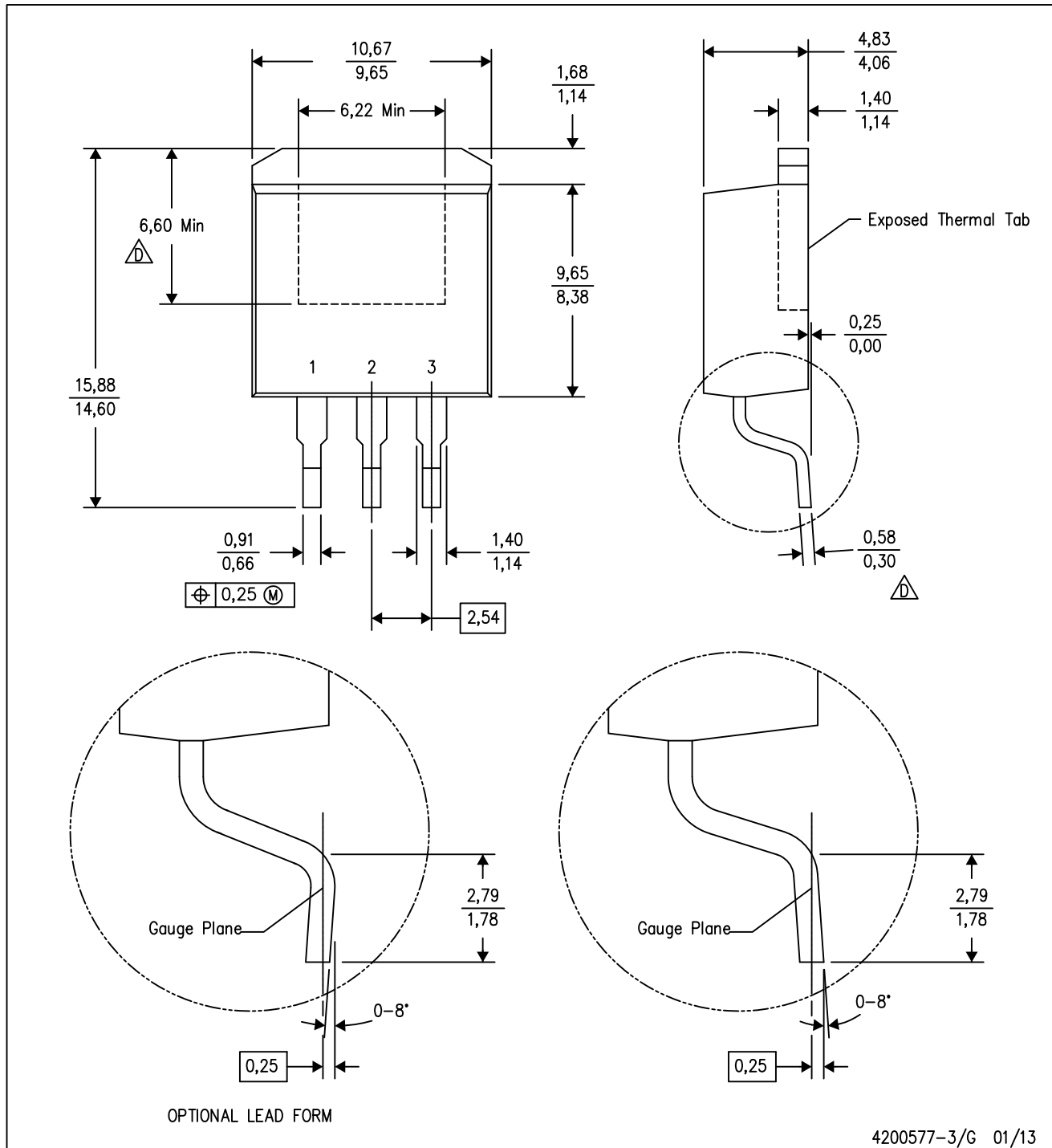


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE

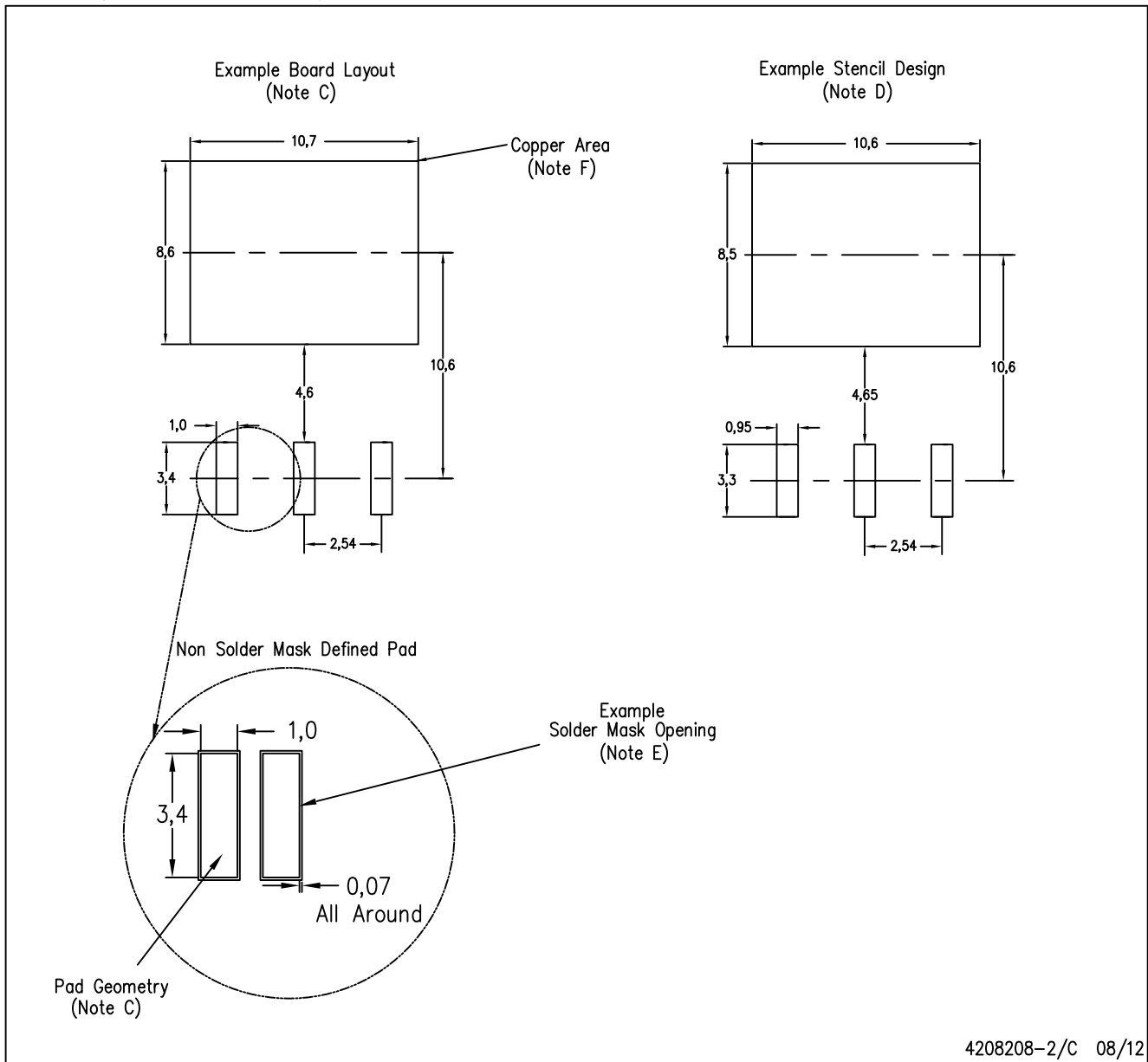


4200577-3/G 01/13

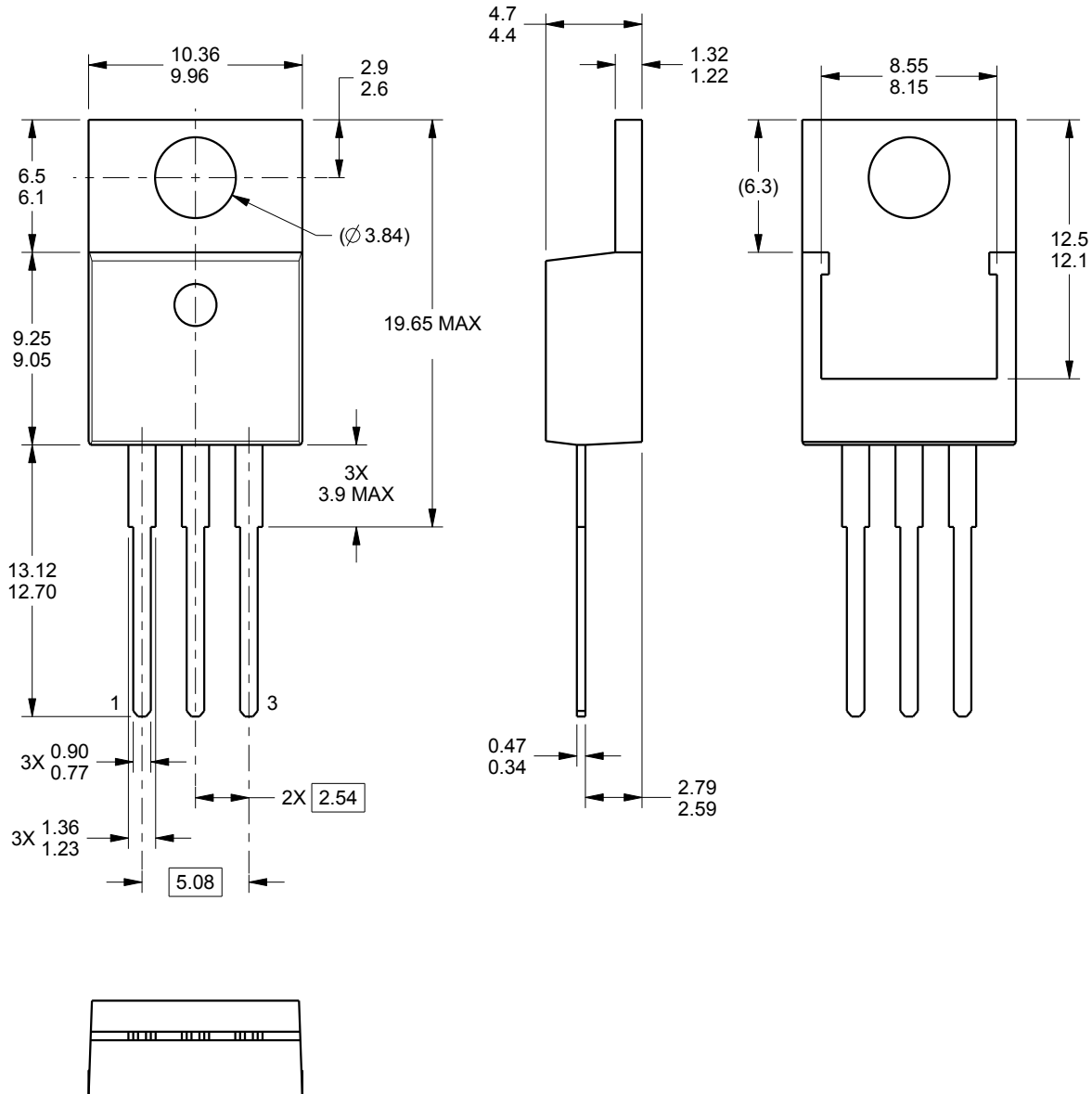
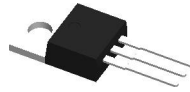
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- Falls within JEDEC TO-263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-SM-782 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
  - This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.



4222214/A 10/2015

## NOTES:

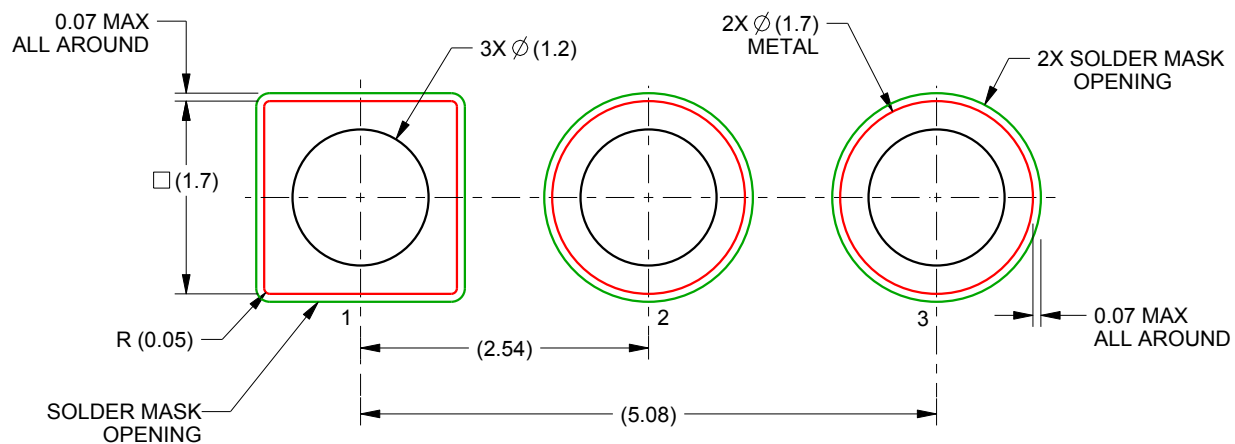
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.

# EXAMPLE BOARD LAYOUT

KCS0003B

TO-220 - 19.65 mm max height

TO-220

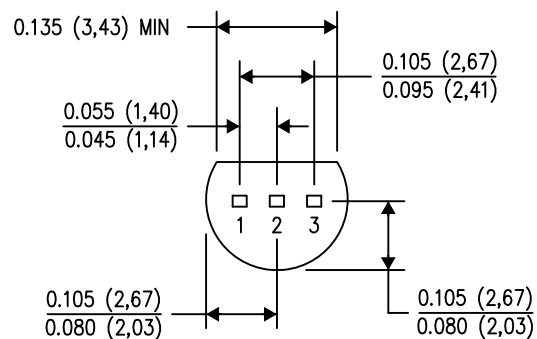
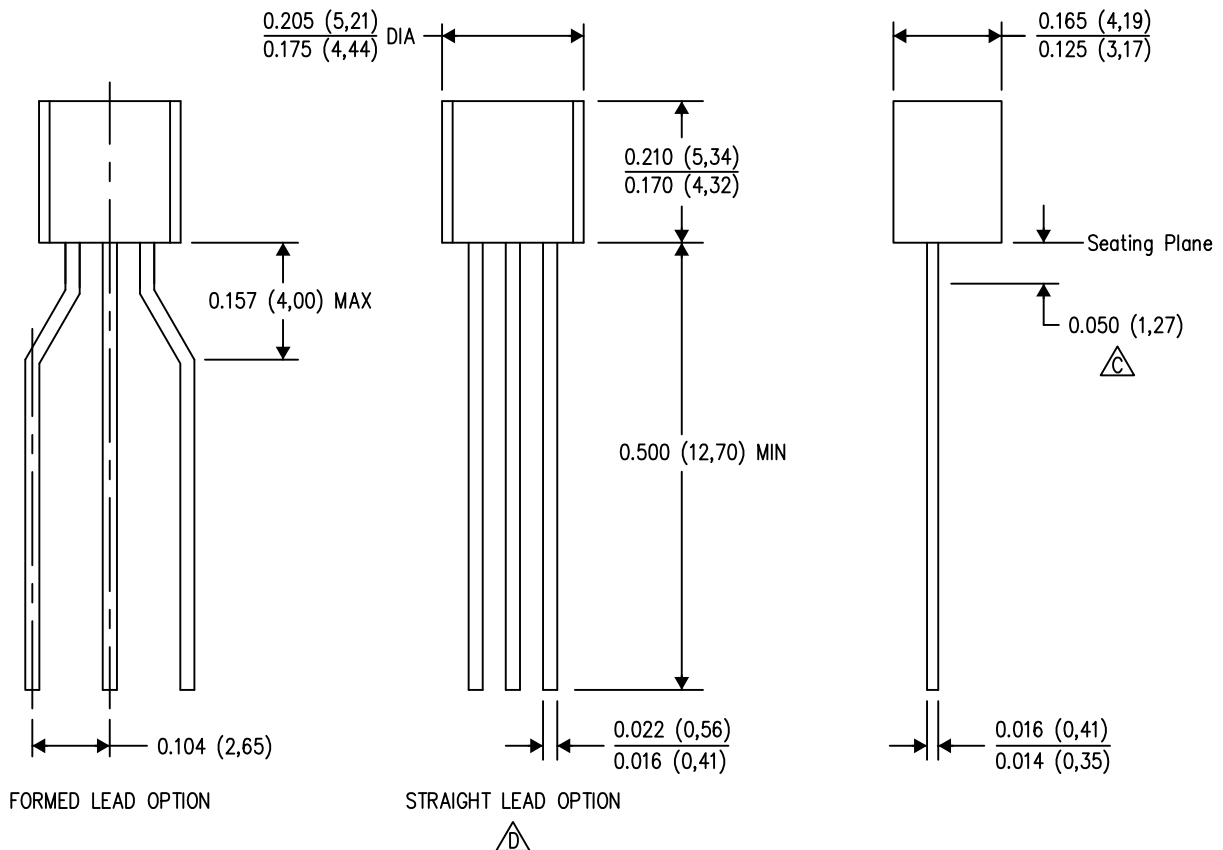


LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 15X

4222214/A 10/2015

LP (O-PBCY-W3)

PLASTIC CYLINDRICAL PACKAGE

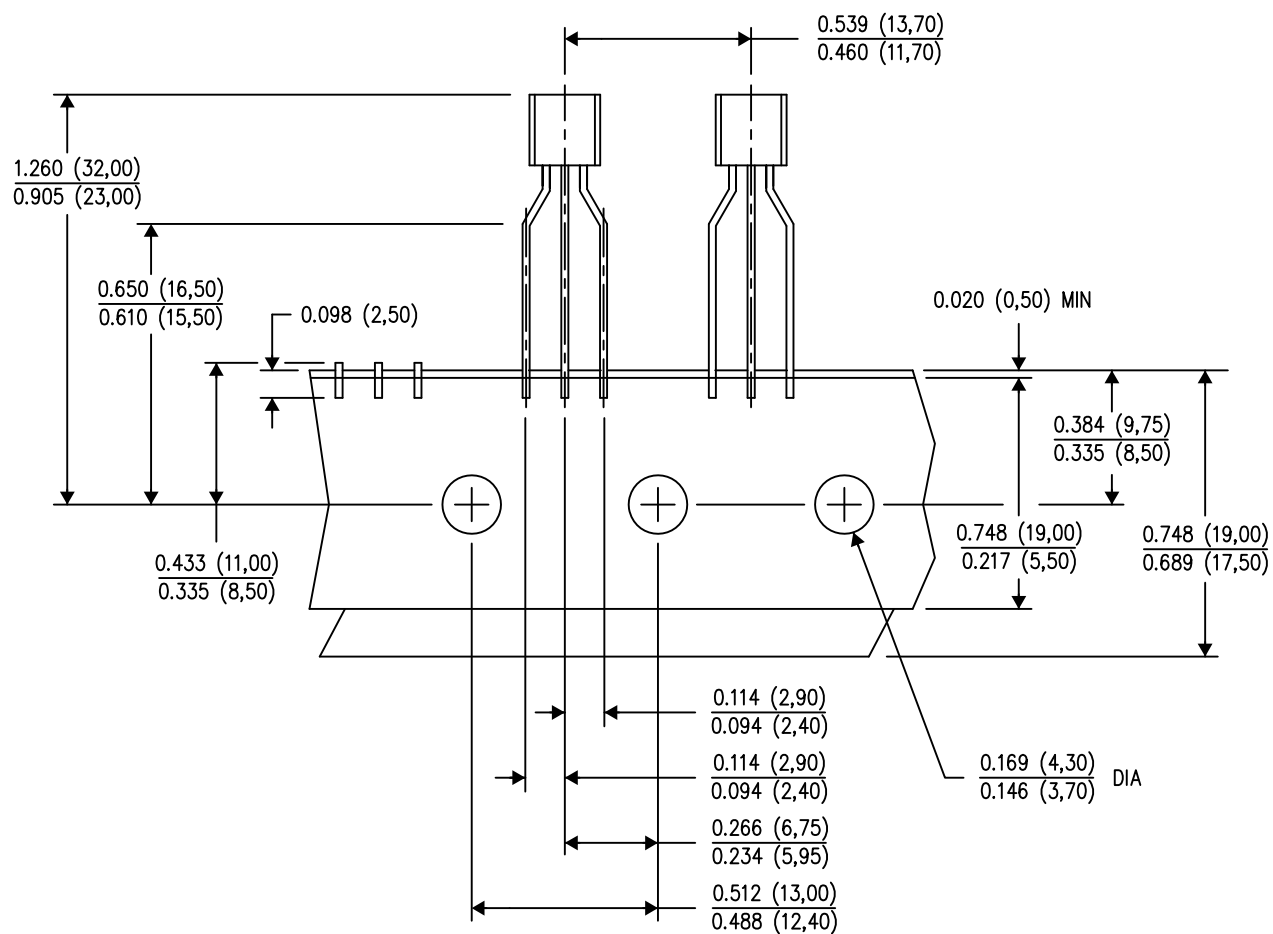


4040001-2/E 08/13

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Lead dimensions are not controlled within this area.
  - D. Falls within JEDEC TO-226 Variation AA (TO-226 replaces TO-92).
  - E. Shipping Method:  
 Straight lead option available in bulk pack only.  
 Formed lead option available in tape & reel or ammo pack.  
 Specific products can be offered in limited combinations of shipping mediums and lead options.  
 Consult product folder for more information on available options.

LP (O-PBCY-W3)

PLASTIC CYLINDRICAL PACKAGE



TAPE &amp; REEL

4040001-3/E 08/13

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Tape and Reel information for the Formed Lead Option package.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

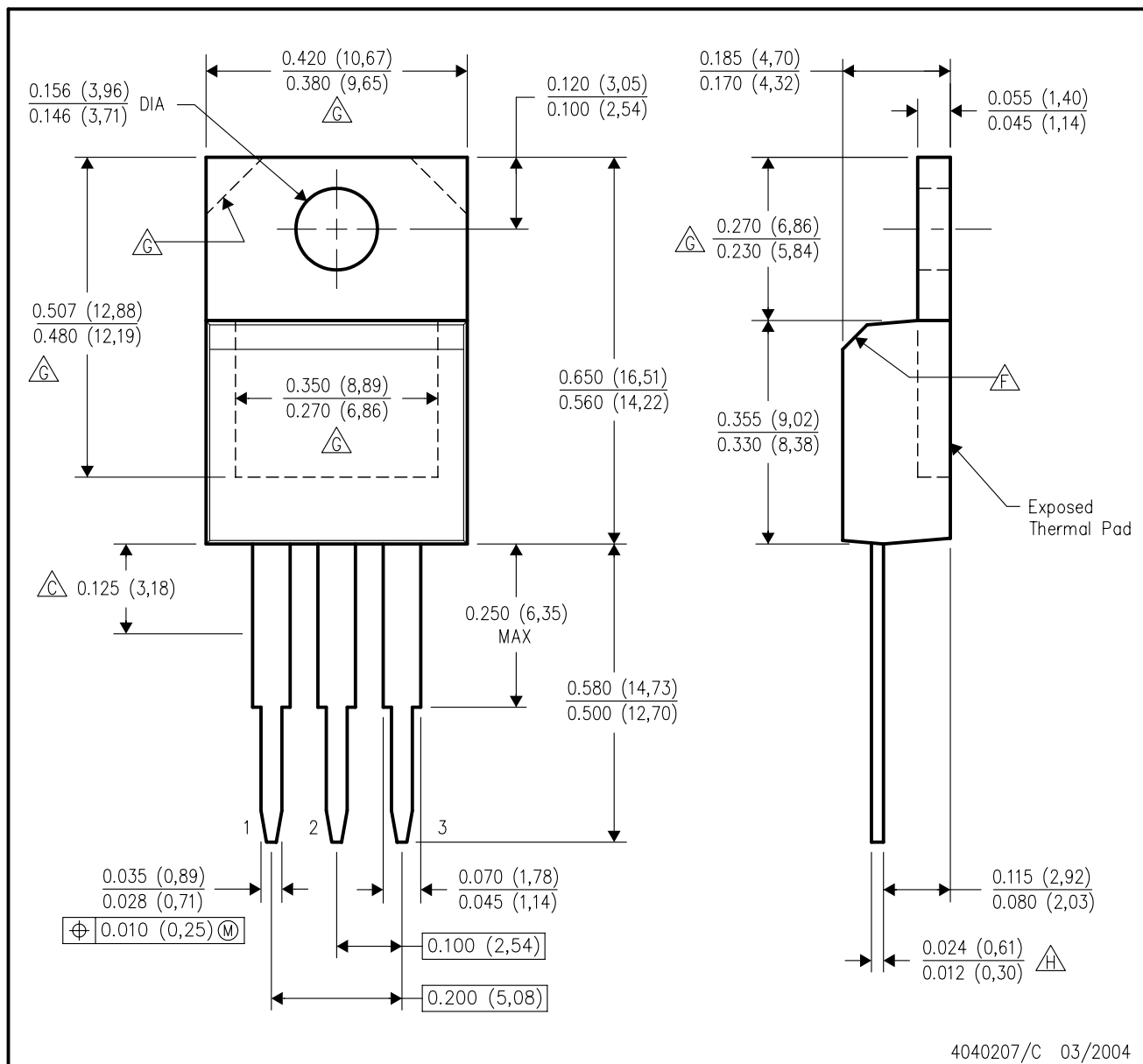


4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## KC (R-PSFM-T3)

## PLASTIC FLANGE-MOUNT PACKAGE

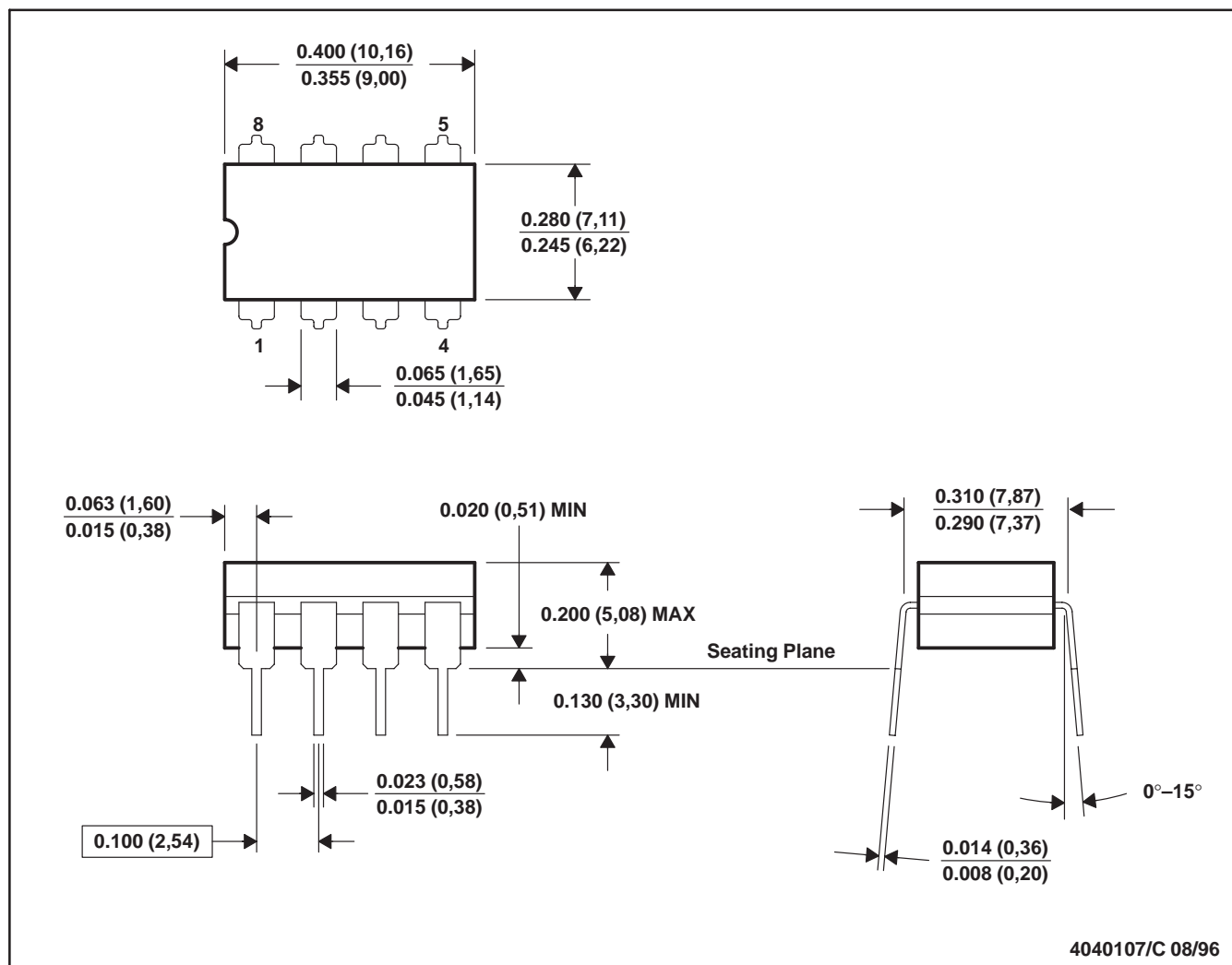


## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. The chamfer is optional.
- G. Thermal pad contour optional within these dimensions.
- H. Falls within JEDEC TO-220 variation AB, except minimum lead thickness.

## JG (R-GDIP-T8)

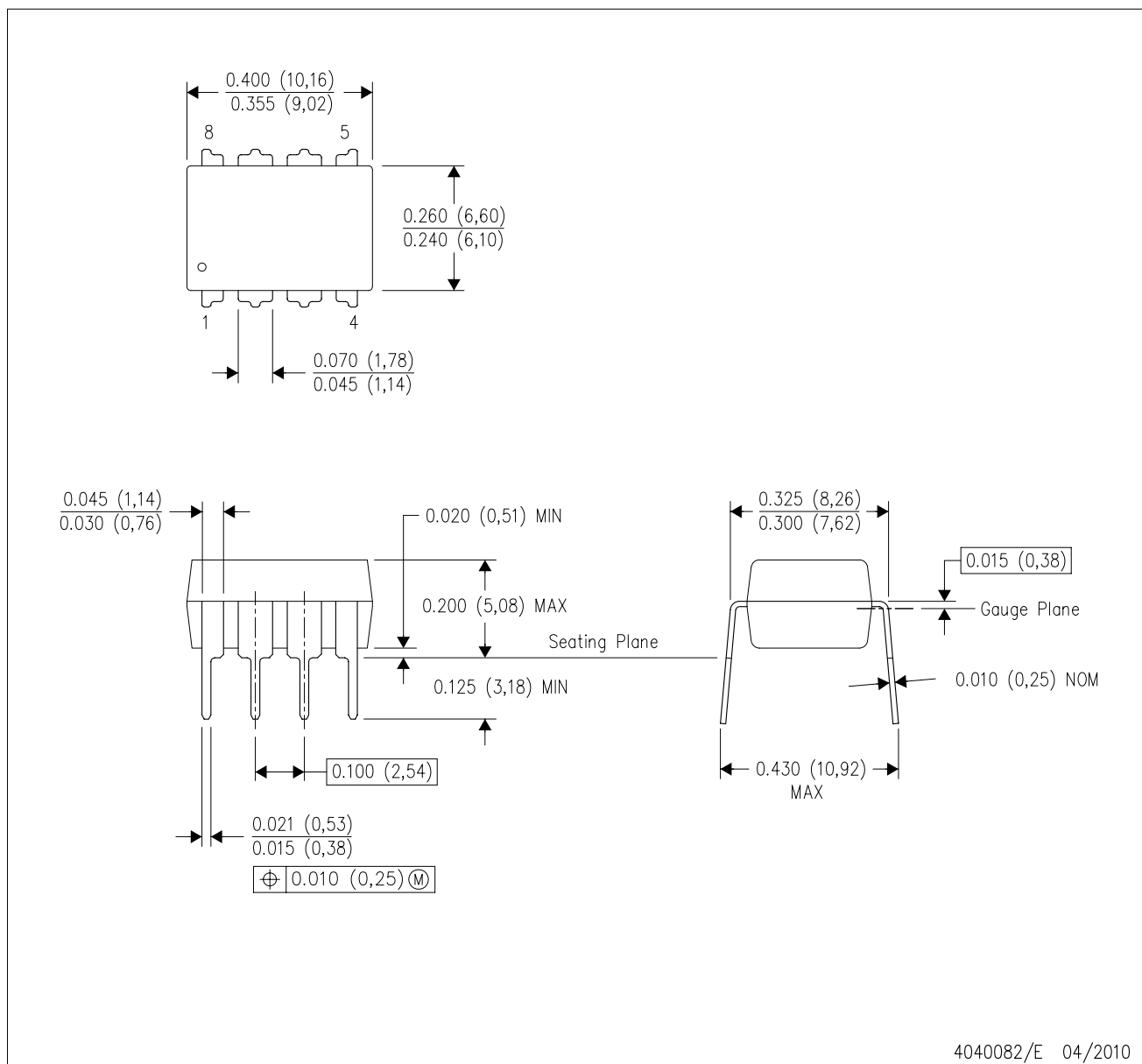
## CERAMIC DUAL-IN-LINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification.
  - E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

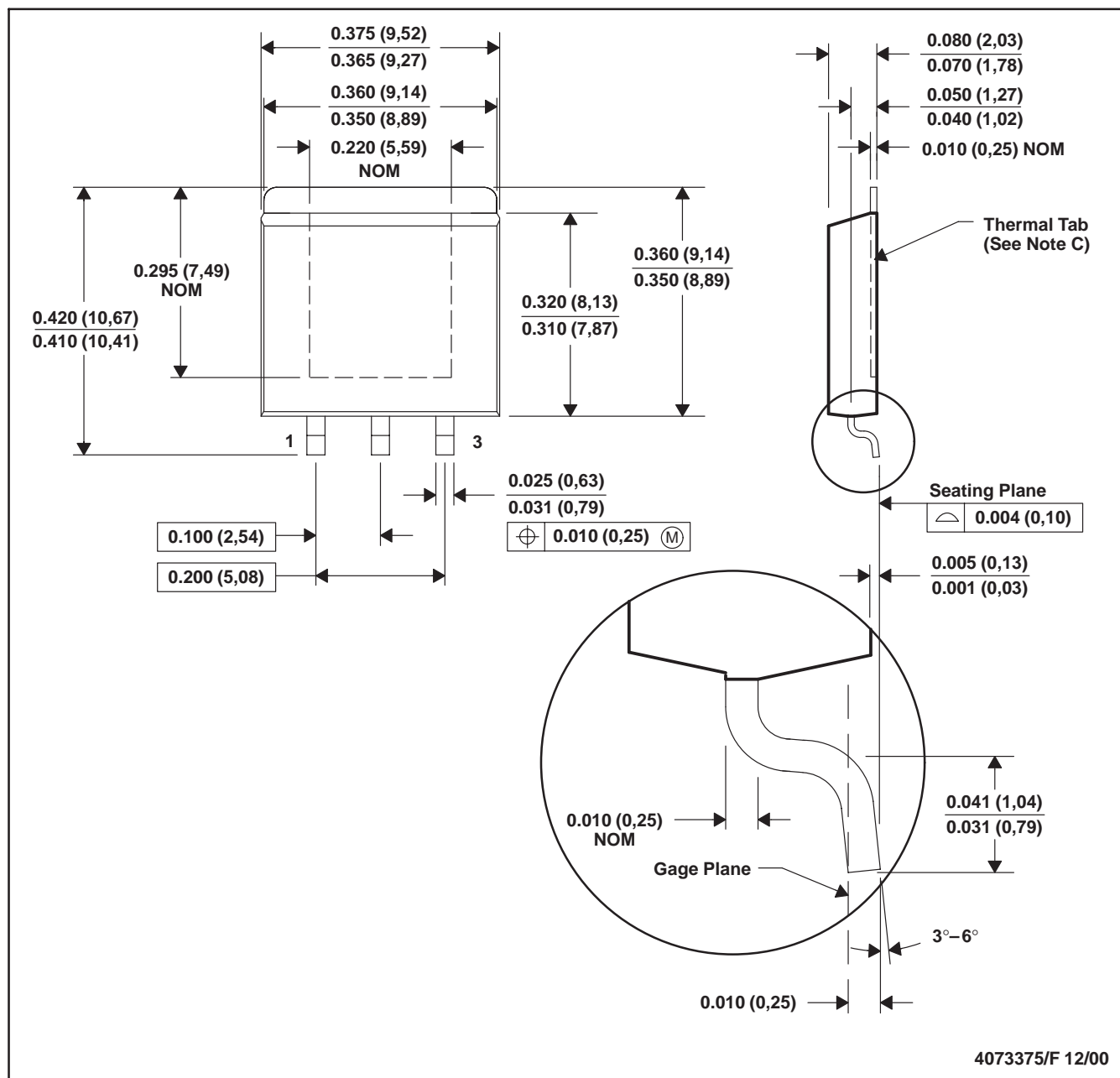
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

## KTE (R-PSFM-G3)

## PowerFLEX™ PLASTIC FLANGE-MOUNT



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - The center lead is in electrical contact with the thermal tab.
  - Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-169

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