Two Channel SATA 3-Gbps Redriver

Check for Samples: SN75LVCP412A

FEATURES

- **Supports SATA 1.5 Gbps and 3.0 Gbps Data Rates**
- **SATA Hot-Plug Capable**
- **Supports Common-Mode Biasing for OOB Signaling with Fast Turn-On**
- **Channel Selectable Output Pre-Emphasis**
- **7dB Fixed Receiver Equalization**
- **Integrated Termination**
- **Low Power**
  - **<200 mW (typ) in Active Mode**
  - **<20 mW (typ) in Auto Low Power Mode**
  - **2.1 mW (max) in Standby Mode**
- **Excellent Jitter and Loss Compensation Capability to Over 20 Inch FR4 Trace**
- **High Protection Against ESD Transient**
  - **HBM: 12000 V**
  - **CDM: 1500 V**
  - **MM: 200 V**
- **IEC 61000-4-2 Qualified (on eSATA connector pins)**
  - **±8 kV Contact Discharge**
  - **±15 kV Air Discharge**
- **20-Pin QFN Package**
- **Pin Compatible to MAX4951**

APPLICATIONS

- **Notebooks, Desktops, Docking Stations, Set Top Box, Servers, and Workstations**

DESCRIPTION

The SN75LVCP412A is a dual channel, single lane SATA redriver and signal conditioner supporting data rates up to 3.0 Gbps that complies with SATA specification revision 2.6.

The SN75LVCP412A operates from a single 3.3-V supply. Integrated 100-Ω line termination with self-biasing make the device suitable for AC coupling. The inputs incorporate an OOB detector which automatically turns the differential outputs off while maintaining a stable output common-mode voltage compliant to SATA link. The device is also designed to handle SSC transmission per the SATA specification.

The SN75LVCP412A handles interconnect losses at both its input and output. The built-in transmitter pre-emphasis feature is capable of applying 0 dB or 2.5 dB of relative amplification at higher frequencies to counter the expected interconnect loss. On the receive side, the device applies a fixed equalization of 7 dB to boost input frequencies near 1.5 GHz. Collectively, the input equalization and output pre-emphasis features of the device work to fully restore SATA signal integrity over extended cable and backplane pathways.

The device is hot-plug capable(1) preventing device damage under *hot*-insertion such as async signal plug/removal, unpowered plug/removal, powered plug/removal, or surprise plug/removal.

(1) *Requires use of AC coupling capacitors at differential inputs and outputs.*

ORDERING INFORMATION(1)

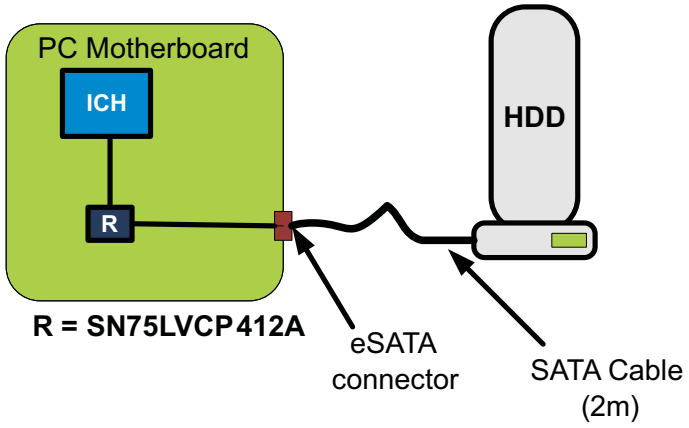
PART NUMBER	PART MARKING	PACKAGE
SN75LVCP412ARTJR	CP412A	20-Pin RTJ Reel (large)
SN75LVCP412ARTJT	CP412A	20-Pin RTJ Reel (small)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

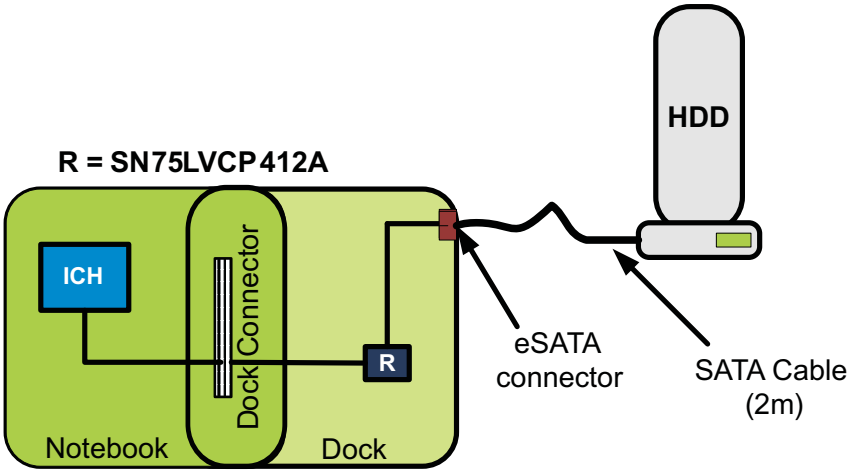
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TYPICAL APPLICATION



In Notebook and Desktop Motherboard



In Notebook Dock

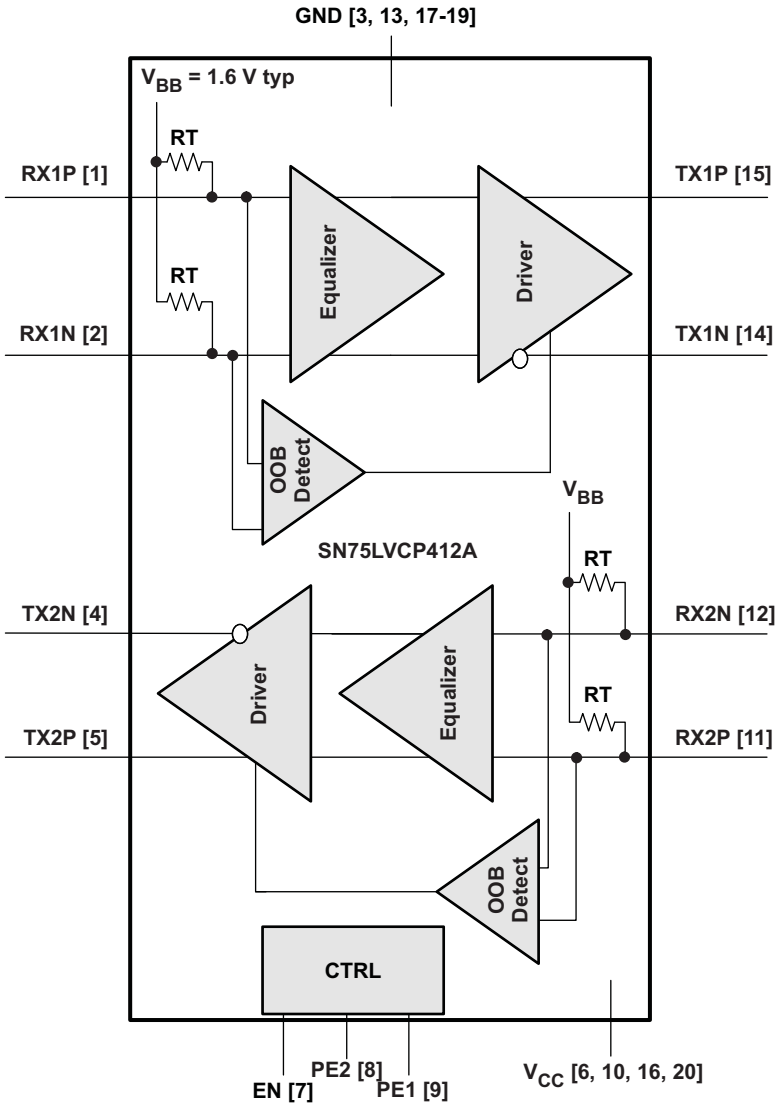


Figure 1. Data Flow Block Diagram

Table 1. Device State

EN	DEVICE STATE	DESCRIPTION
H	Active	ALP enabled (1) (default)
L	Standby	Device in standby mode

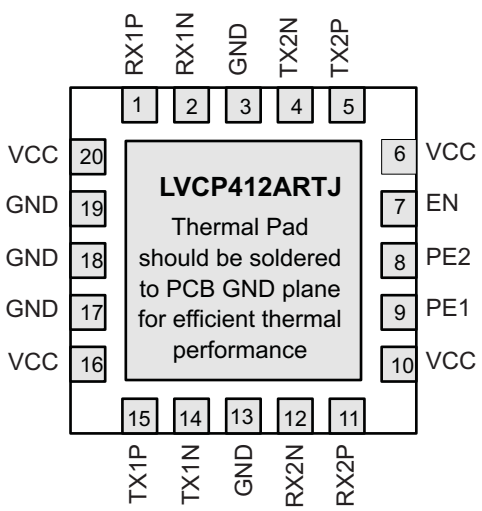
(1) ALP = Auto low power mode

Table 2. Output Pre-Emphasis (Device in active state)

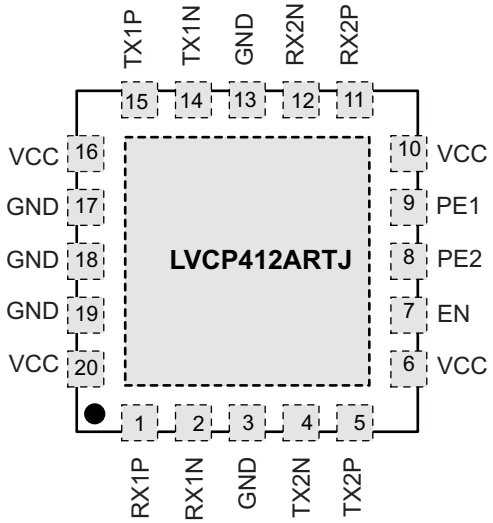
PE1	PE2	FUNCTION
0	**0**	**Normal SATA output (default state); CH 1 and CH 2 → 0 dB**
1	0	CH 1 → 2.5 dB pre-emphasis; CH 2 → 0 dB
0	1	CH 2→ 2.5 dB pre-emphasis; CH 1 → 0 dB
1	1	CH 1 and CH 2 → 2.5 dB pre-emphasis

PIN ASSIGNMENT

BOTTOM VIEW



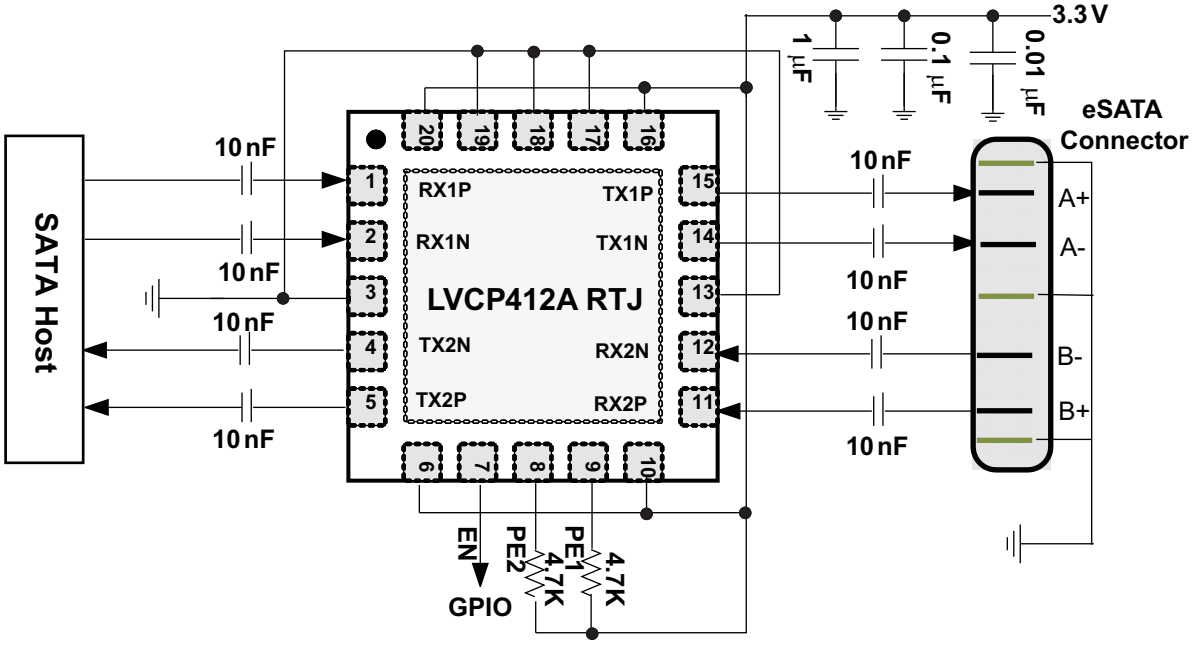
TOP VIEW



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
High Speed Differential I/O			
2	RX_1N	I, CML	Non-inverting and inverting CML differential input for CH 1 and CH 2. These pins are tied to an internal voltage bias by dual termination resistor circuit.
1	RX_1P	I, CML	
12	RX2N	I, CML	
11	RX2P	I, CML	
14	TX_1N	O, CML	Non-inverting and inverting CML differential output for CH 1 and CH 2. These pins are internally tied to voltage bias by termination resistors.
15	TX_1P	O, CML	
4	TX_2N	O, CML	
5	TX_2P	O, CML	
Control Pins			
7	EN	I, LVCMOS	Device enable pin. Internally PU to VCC
9,8	PE1, PE2	I, LVCMOS	Selects pre-emphasis settings for CH 1 and CH 2 perTable 2. Internally PD to GND
Power			
6, 10, 16, 20	VCC	Power	Positive supply should be 3.3V ± 10%
3, 13 17 - 19	GND	Power	Supply ground

DEVICE IMPLEMENTATION



A. Place supply capacitors close to the pin.

B. EN can be left open or tied to supply when no external control is implemented.

C. Output pre-emphasis (PE1, PE2) is shown enabled. Setting depends on device palcement relative to eSATA connector.

DETAILED DESCRIPTION

INPUT EQUALIZATION

Each differential input of the SN75LVCP412A has +7 dB of fixed equalization in its front stage. The equalization amplifies high frequency signals to correct for loss from the transmission channel. The input equalizer is designed to recover a signal even when no eye is present at the receiver and effectively supports FR4 trace at the input anywhere from <4 inches to 20 inches or <10 cm to >50 cm.

OUTPUT PRE-EMPHASIS

The SN75LVCP412A provides single step pre-emphasis from 0 dB to 2.5 dB at each of its differential outputs. Pre-emphasis is controlled independently for each channel and is set by the control pins PE1 and PE2 as shown in the terminal functions table. The pre-emphasis duration is 0.7 UI or 133 ps (typ) at SATA 3-Gbps speed.

LOW POWER MODE

Long battery life has become the single most important differentiator for mobile platforms. The SN75LVCP412A supports this emphasis on low system power by offering the choice of two low power modes, one requires control by SATA host (option 1) and the second (option 2) is completely autonomous whereby the SN75LVCP412A goes into ultra low power mode (<20mW) on its own when no data traffic is detected for longer than 10us. Both low power modes are described below:

- Standby Mode (option 1) (triggered by EN pin when EN = H → L)
  - Standby mode is controlled by the enable (EN) pin. In its default state this pin is internally pulled high. Pulling this pin LOW puts the device in standby mode within 2µs (max). In this mode all active components of the device are driven to their quiescent level and differential outputs are driven to Hi-Z (open). Max power dissipation is 2 mW. Exiting to normal operation requires a maximum latency of 20 µs.
- Auto Low Power Mode (option 2) (triggered when a given channel is in the electrical idle state for > 10 µs and EN = H)
  - The device enters and exits low power mode by actively monitoring the input signal (V_{IDp-p}) level on each

of its channels independently. When the input signal of either or both channels is in the electrical idle state, i.e. V_{IDp-p} <50 mV and stays in this state for > 10 µs, the associated channel(s) enters the low power state. In this state, the output of the associated channel(s) is held to TX VCM and the device selectively shuts off some circuitry to lower power by > 90% (typ) of its normal operating power. Exit time from auto low power mode is less than 50 ns max.

OUT-OF-BAND (OOB) SUPPORT

The squelch detector circuit within the device enables full detection of OOB signaling as specified in SATA specification 2.6. Differential signal amplitude at the receiver input of 50 mV_{p-p} or less is not detected as an activity and hence is not passed to the output. Differential signal amplitude of 150 mV_{p-p} or more is detected as an activity and therefore passed to the output indicating activity. Squelch circuit on/off time is 8 ns max. While in squelch mode outputs are held to VCM_{TX}.

DEVICE POWER

The SN75LVCL412A is designed to operate from a single 3.3-V supply. Always practice proper power supply sequencing procedures. Apply V_{CC} first before any input signals are applied to the device. The power-down sequence is in reverse order.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply voltage range(2)	V_{CC}	–0.5 to 4	V
Voltage range	Differential I/O	–0.5 to 4	V
	Control I/O	–0.5 to V_{CC} + 0.5	
Electrostatic discharge	Human body model(3)	±12000	V
	Charged-device model(4)	±1500	
	Machine model(5)	±200	
Continuous power dissipation		See Dissipation Rating Table	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A.
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \le 25°C$	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
20-pin QFN (RTJ)	Low-K	1176 mW	11.76 mW/°C	470 mW
	High-K	2631 mW	26.3 mW/°C	1052 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance			10		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			60		°C/W
$R_{\theta JP}$	Junction-to-pad thermal resistance			15.2		°C/W

(1) The maximum rating is simulated under 3.6-V V_{CC}.

RECOMMENDED OPERATING CONDITIONS

with typical values measured at V_{CC} = 3.3 V, T_A = 25°C; all temperature limits are assured by design

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage		3	3.3	3.6	V
$C_{COUPLING}$	Coupling capacitor			12		nF
T_A	Operating free-air temperature		0		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE						
P_{Active}	Device power dissipation	EN, PE1, PE2 in default state, K28.5 pattern at 3 Gbps, V_{ID} = 700 mV_{p-p}		185	280	mW
I_{CC}	Supply current, active	EN, PE1, PE2 in default state, K28.5 pattern at 3 Gbps, V_{ID} = 700 mV_{p-p}		56	78	mA
P_{SDWN}	Standby power	EN = 0V		1.3	2.1	mW
I_{CCSDWN}	Shutdown current	EN = 0V		380	560	µA
P_{ALP}	ALP (auto low power) supply current	Auto low power conditions met		17	24	mW
I_{CC-ALP}	ALP (auto low power) supply current	Auto low power conditions met		5.0	6.5	mA
	Maximum data rate				3.0	Gbps
t_{PDelay}	Propagation delay	Measured using K28.5 pattern, See Figure 2		300	500	ps
t_{ENB}	Device enable time	ENB = 0 → 1			5	µs
t_{DIS}	Device disable time	ENB = 1 → 0			1	µs
$AutoLP_{ENTRY}$	ALP entry time	Electrical Idle at Input, See Figure 2		17		µs
$AutoLP_{EXIT}$	ALP exit time	After first signal activity, See Figure 2		25	50	ns
V_{OOB}	Input OOB threshold	See Figure 3	50	100	150	mV_{p-p}
t_{OOB1}	OOB mode enter	See Figure 3		5	8	ns
t_{OOB2}	OOB mode exit	See Figure 3		5	8	ns
CONTROL LOGIC						
V_{IH}	High-level input voltage		1.4			V
V_{IL}	Low-level input voltage				0.5	V
V_{INHYS}	Input hysteresis			100		mV
I_{IH}	High-level input current				10	µA
I_{IL}	Low-level input current				10	µA
RECEIVER AC/DC						
Z_{DiffRX}	Differential input impedance		85	100	115	Ω
Z_{SERX}	Single-ended input impedance		40			Ω
VCM_{RX}	Common-mode voltage			1.6		V
RL_{DiffRX}	Differential mode return loss	f = 150 MHz–300 MHz	18			dB
		f = 300 MHz–600 MHz	14			
		f = 600 MHz–1.2 GHz	10			
		f = 1.2 GHz–2.4 GHz	8			
		f = 2.4 GHz–3.0 GHz	3			

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

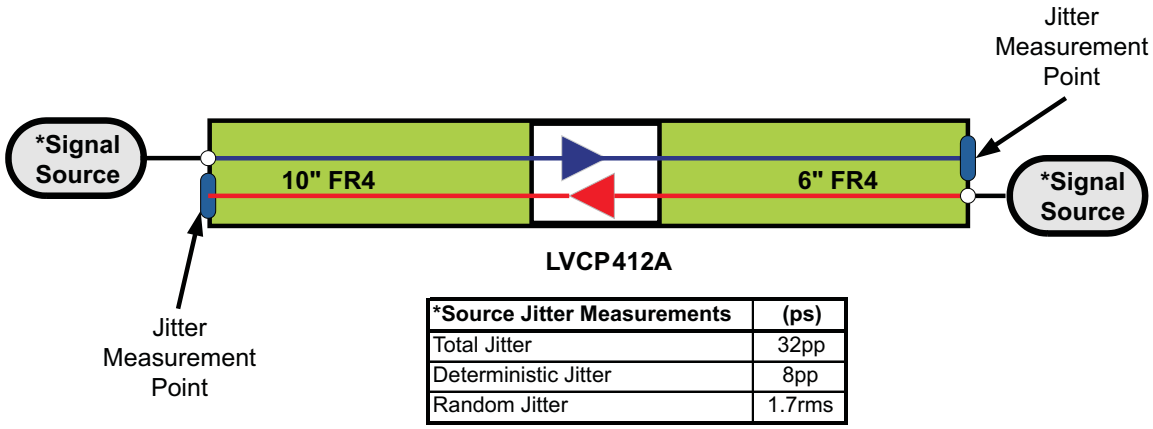
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
RL_{CMRX}	Common-mode return loss	f = 150 MHz–300 MHz	5			dB
		f = 300 MHz–600 MHz	5			
		f = 600 MHz–1.2 GHz	2			
		f = 1.2 GHz–2.4 GHz	1			
		f = 2.4 GHz–3.0 GHz	1			
V_{DiffRX}	Differential input voltage PP	f = 750 MHz–1.5 GHz	200		2000	mV/pp
IB_{RX}	Impedance balance	f = 150 MHz–300 MHz	30			dB
		f = 300 MHz–600 MHz	30			
		f = 600 MHz–1.2 GHz	20			
		f = 1.2 GHz–2.4 GHz	10			
		f = 2.4 GHz–3.0 GHz	4			
$T_{20\text{-}80RX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal	67		136	ps
T_{skewRX}	Differential skew	Difference between the single-ended mid-point of the RX+ signal rising/falling edge, and the single-ended mid-point of the RX– signal falling/rising edge			50	ps
TRANSMITTER AC/DC						
Z_{DiffTX}	Pair differential Impedance		85		115	Ω
Z_{SETX}	Single-ended input impedance		40			Ω
RL_{DiffTX}	Differential mode return loss	f = 150 MHz–300 MHz	14			dB
		f = 300 MHz–600 MHz	8			
		f = 600 MHz–1.2 GHz	6			
		f = 1.2 GHz–2.4 GHz	6			
		f = 2.4 GHz–3.0 GHz	3			
RL_{CMTX}	Common-mode return loss	f = 150 MHz–300 MHz	5			dB
		f = 300 MHz–600 MHz	5			
		f = 600 MHz–1.2 GHz	2			
		f = 1.2 GHz–2.4 GHz	1			
		f = 2.4 GHz–3.0 GHz	1			
IB_{TX}	Impedance balance	f = 150 MHz–300 MHz	30			dB
		f = 300 MHz–600 MHz	20			
		f = 600 MHz–1.2 GHz	10			
		f = 1.2 GHz–2.4 GHz	10			
		f = 2.4 GHz–3.0 GHz	4			
$Diff_{VppTX}$	Differential output voltage PP	f = 1.5 GHz, PE1/PE2 = 0	400	585	700	mV/pp
$Diff_{VppTX\_PE}$	Differential output voltage PP	f = 1.5 GHz, PE1/PE2 = 1	600	790	965	mV/pp
	Output pre-emphasis	At 1.5 GHz when enabled		2.5		dB
t_{PE}	Pre-emphasis width	At 3 Gbps, See Figure 6		0.5		UI
VCM_{TX}	Common-mode voltage			1.97		V
VCM_{TX_AC}	AC CM voltage active mode	Max amount of AC CM signal at TX		20	50	$mV_{p\text{-}p}$
$T_{20\text{-}80TX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal, PE2, PE1 = 0 V	67	83	136	ps
T_{skewTX}	Differential skew	Difference between the single-ended mid-point of the TX+ signal rising/falling edge, and the single-ended mid-point of the TX– signal falling/rising edge		7	20	ps

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
JITTER (with pre-emphasis disabled at device pin+2" loadboard trace)						
TJ_{TX}	Total jitter(1)	UI = 333 ps, +K28.5 control character, PE2, PE1 = 0 V, V_{ID} = 500 mV_{p-p}		35	67	ps_{p-p}
DJ_{TX}	Deterministic jitter(1)	UI = 333 ps, +K28.5 control character, PE2, PE1 = 0 V, V_{ID} = 500 mV_{p-p}		10	33	ps_{p-p}
RJ_{SD}	Random jitter(1)	UI = 333 ps, +K28.7 control character, PE2, PE1 = 0 V, V_{ID} = 500 mV_{p-p}		1.8	2.0	ps-rms
JITTER (with pre-emphasis enabled and measured as shown in Fig 1)						
TJ_{TX}	Total jitter(1)	UI = 333 ps, +K28.5 control character, PE2, PE1 = VCC, V_{ID} = 500 mV_{p-p}		40	100	ps_{p-p}
DJ_{TX}	Deterministic jitter(1)	UI = 333 ps, +K28.5 control character, PE2, PE1 = VCC, V_{ID} = 500 mV_{p-p}		15	67	ps_{p-p}
RJ_{SD}	Random jitter(1)	UI = 333 ps, +K28.7 control character, PE2, PE1 = VCC, V_{ID} = 500 mV_{p-p}		1.8	2.0	ps-rms

(1) T_J = (14.1×RJ_{SD} + DJ) where RJ_{SD} is one standard deviation value of RJ Gaussian distribution. T_J measurement is at the SATA connector and includes jitter generated at the package connection on the printed circuit board, and at the board interconnect.



*Source Jitter Measurements	(ps)
Total Jitter	32pp
Deterministic Jitter	8pp
Random Jitter	1.7rms

Figure 2. Jitter Measurement Setup

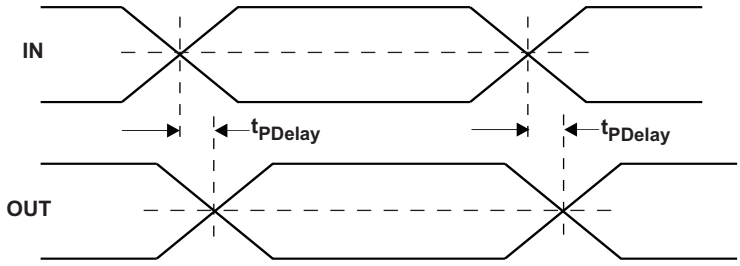


Figure 3. Propagation Delay Timing Diagram

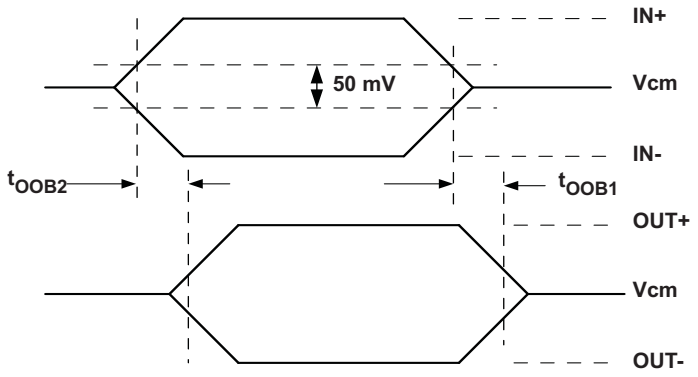


Figure 4. OOB Enter and Exit Timing

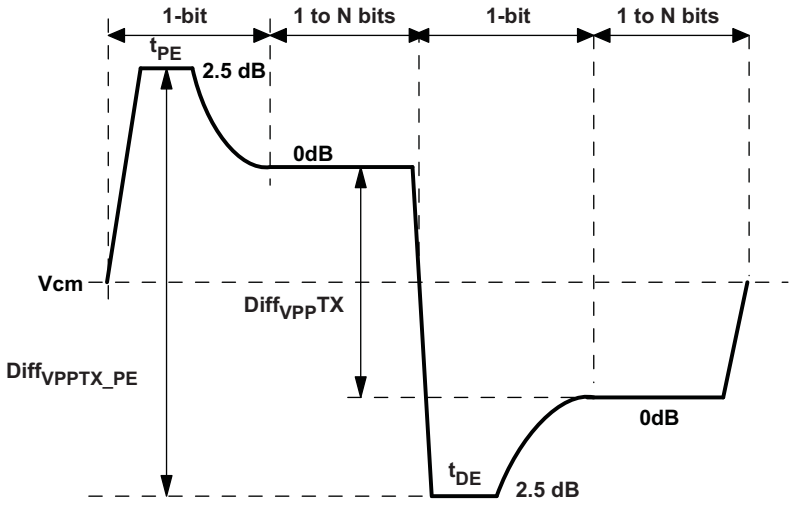


Figure 5. TX Differential Output with 2.5 dB Pre-Emphasis Step

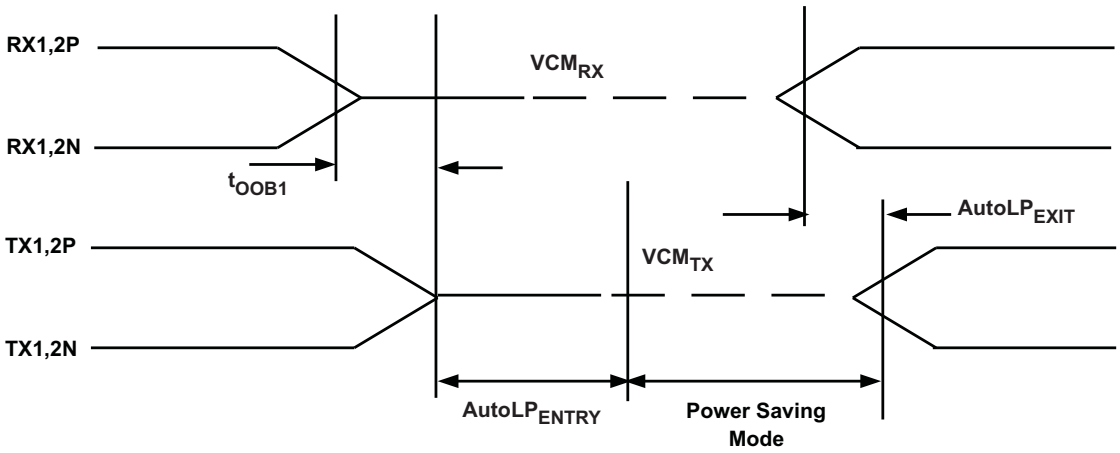


Figure 6. Auto Low Power Mode Timing

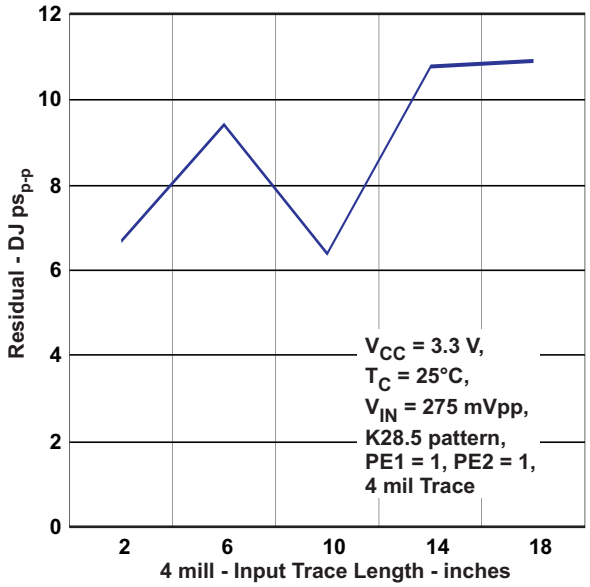


Figure 7. Residual DJ vs Input Trace Length Output Trace Fixed at 2"

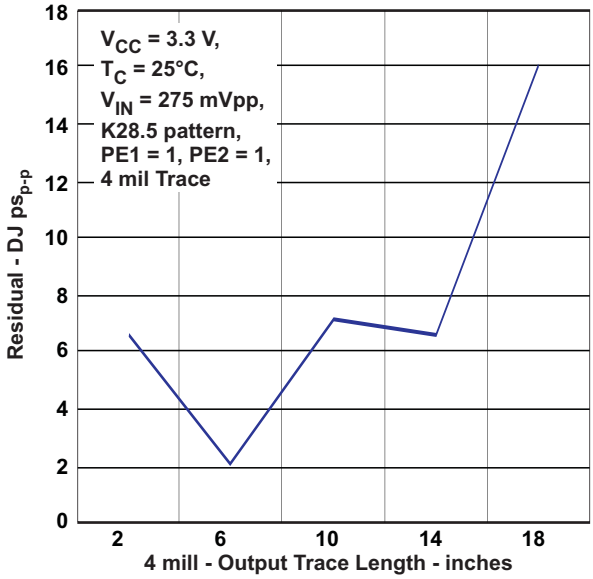


Figure 8. Residual DJ vs Output Trace Length Input Trace Fixed at 2"

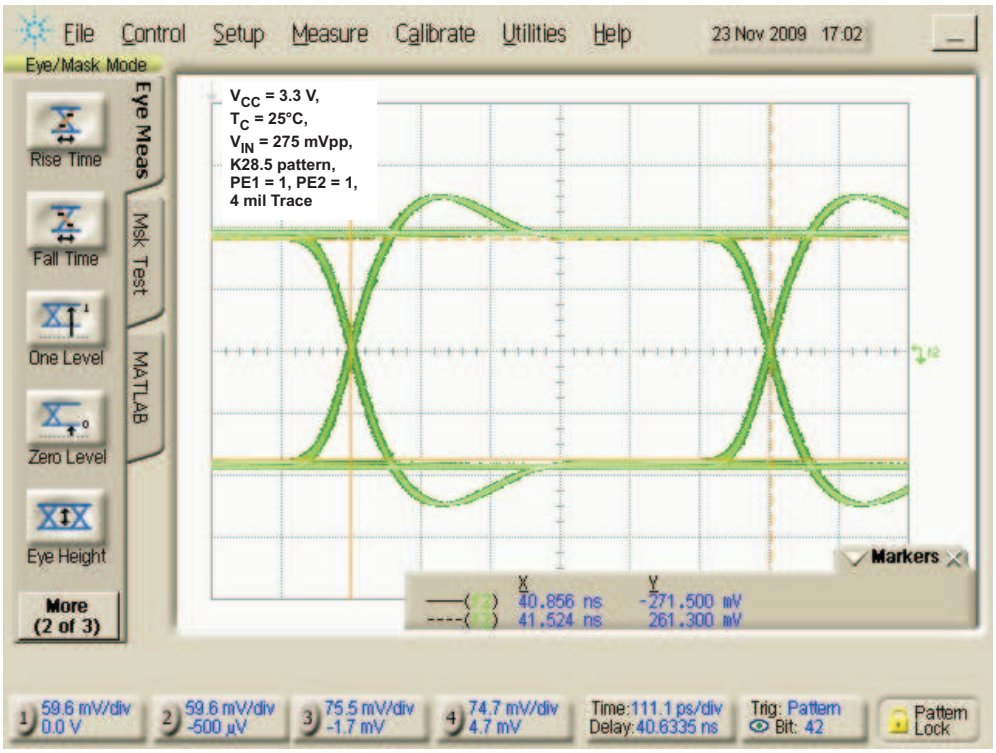


Figure 9. Eye Pattern, 1.5 Gbps, Input = 2", Output = 2"

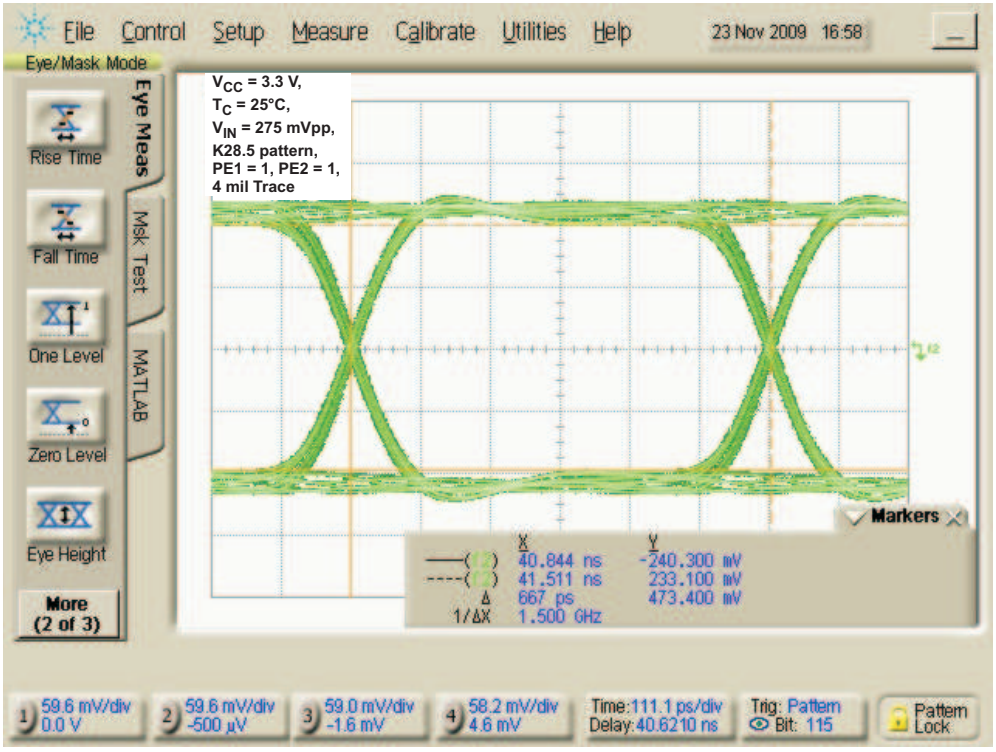


Figure 10. Eye Pattern, 1.5 Gbps, Input = 2", Output = 6"

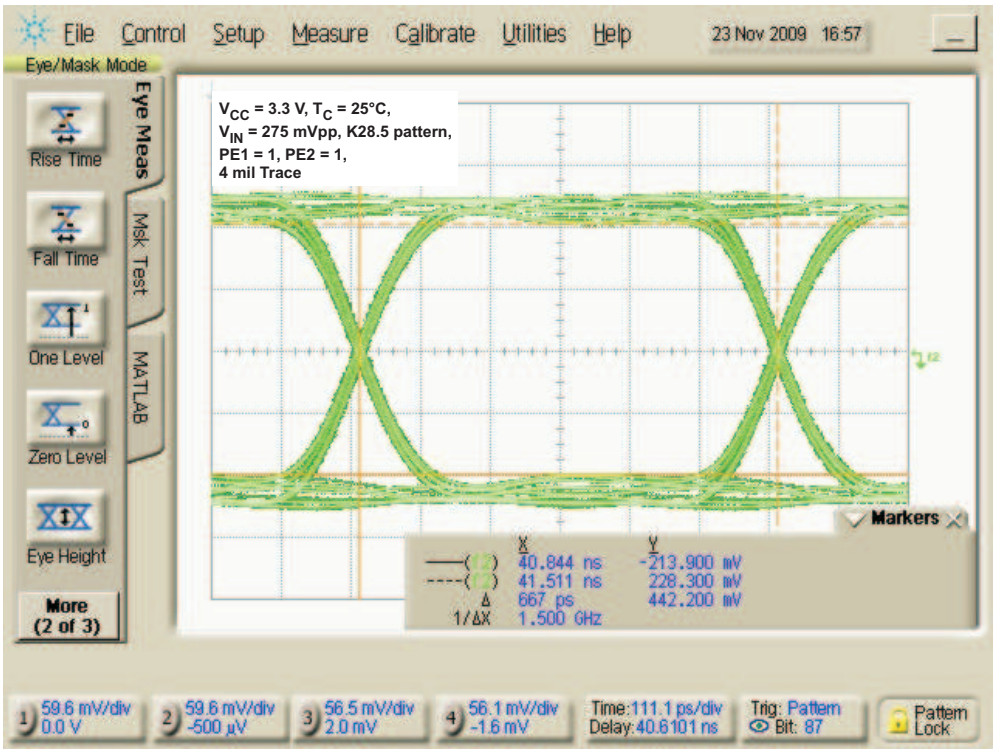


Figure 11. Eye Pattern, 1.5 Gbps, Input = 2", Output = 10"

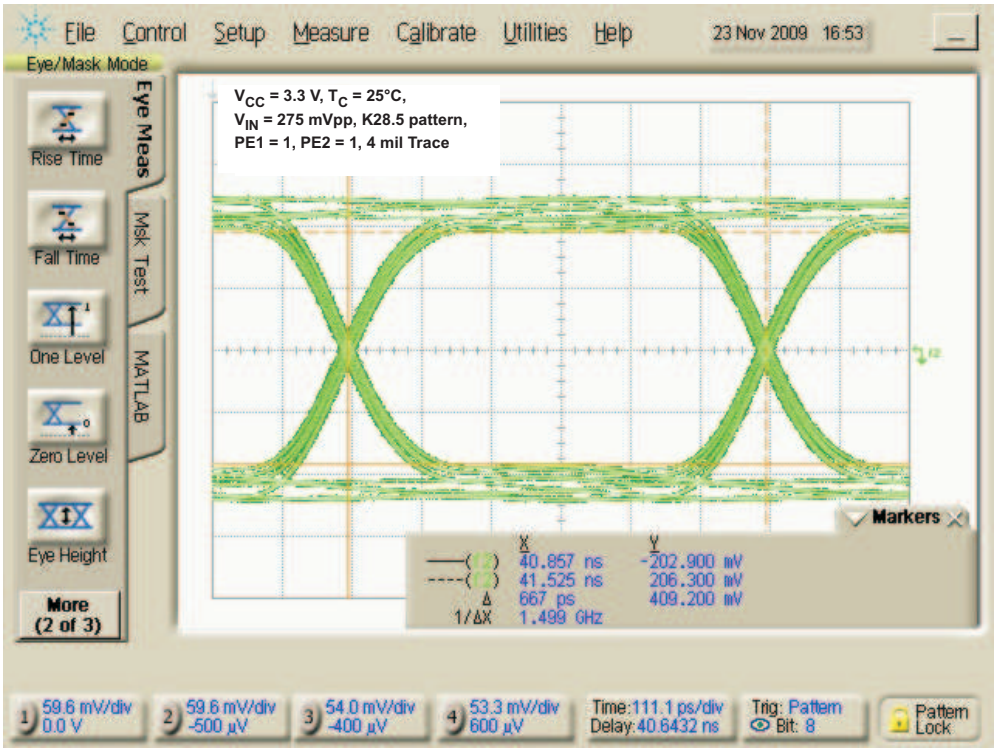


Figure 12. Eye Pattern, 1.5 Gbps, Input = 2", Output = 14"

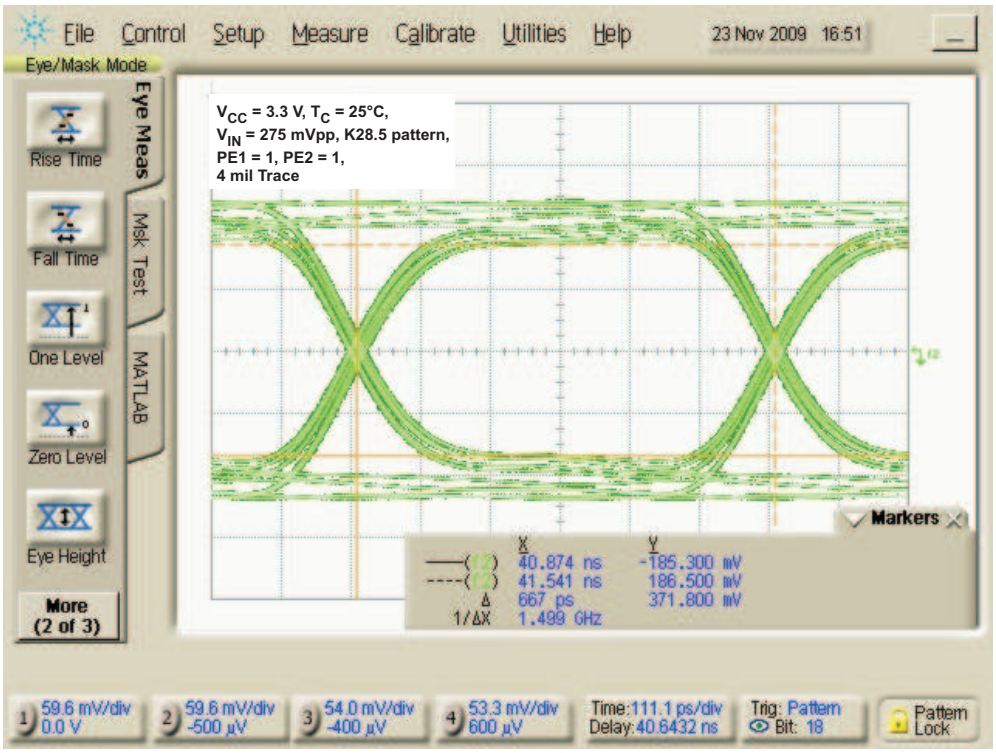


Figure 13. Eye Pattern, 1.5 Gbps, Input = 2", Output = 18"

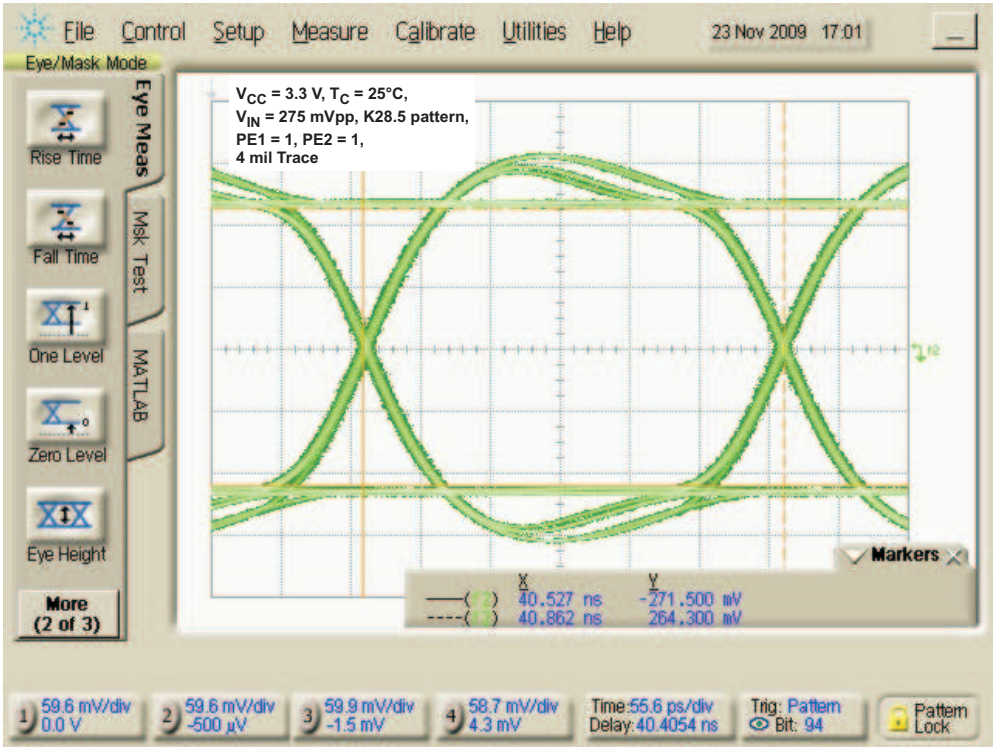


Figure 14. Eye Pattern, 3.0 Gbps, Input = 2", Output = 2"

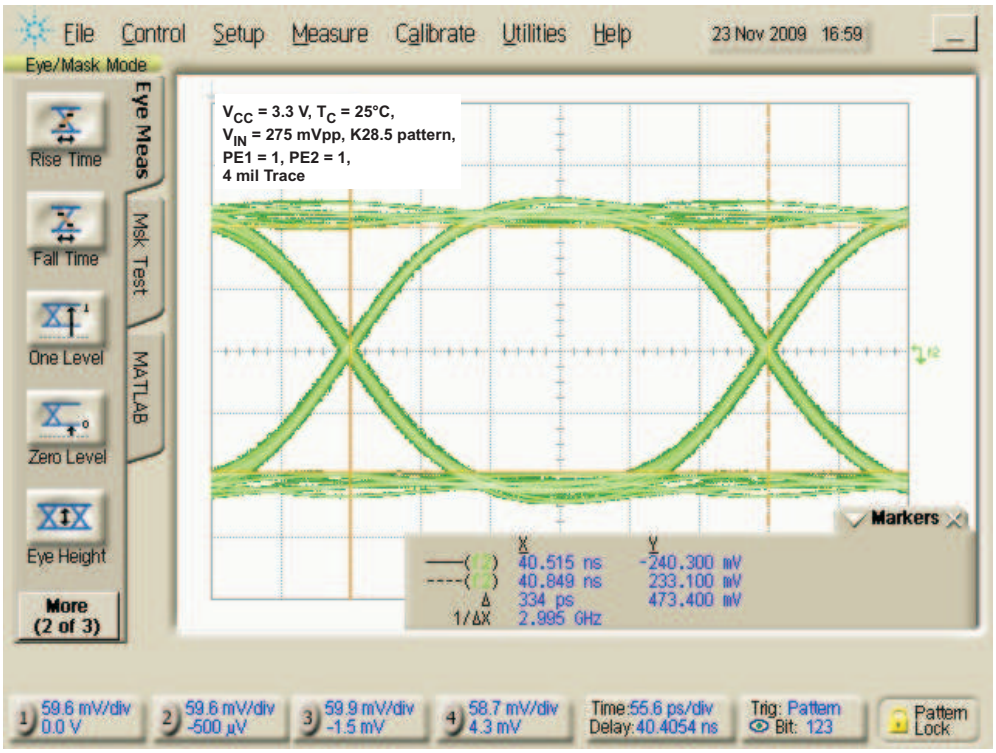


Figure 15. Eye Pattern, 3.0 Gbps, Input = 2", Output = 6"

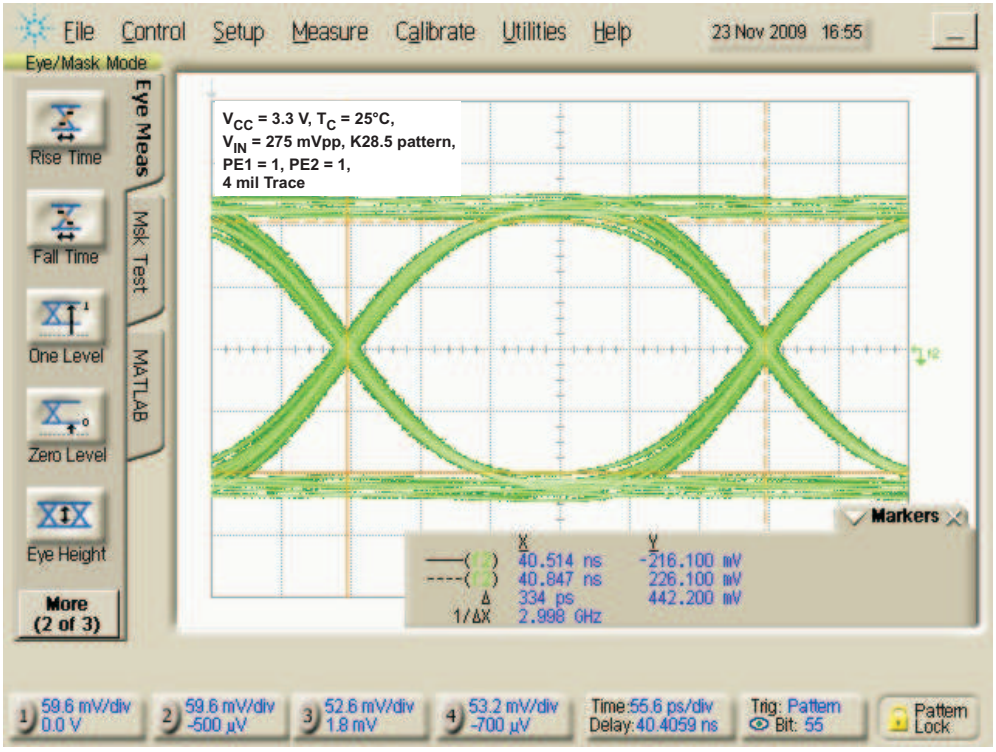


Figure 16. Eye Pattern, 3.0 Gbps, Input = 2", Output = 10"

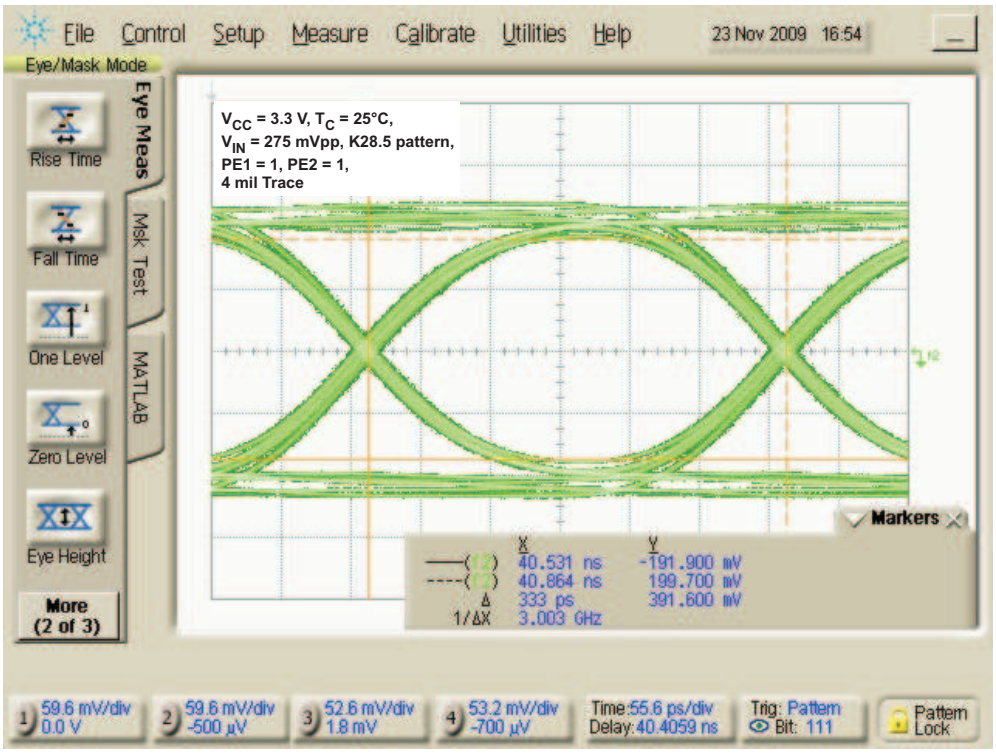


Figure 17. Eye Pattern, 3.0 Gbps, Input = 2", Output = 14"

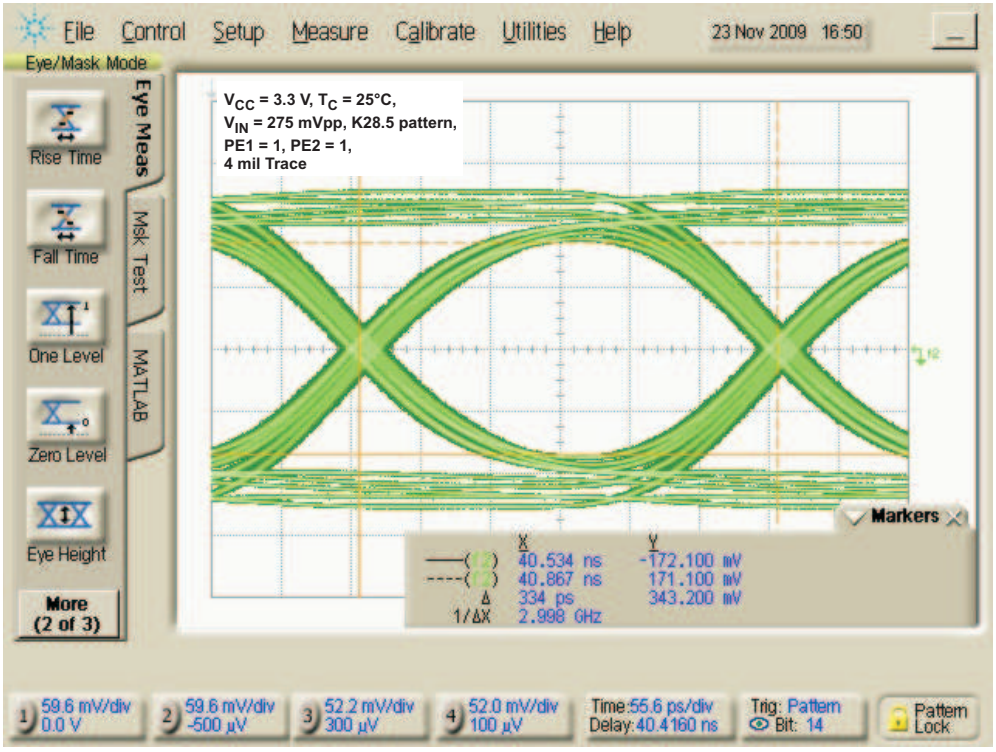


Figure 18. Eye Pattern, 3.0 Gbps, Input = 2", Output = 18"

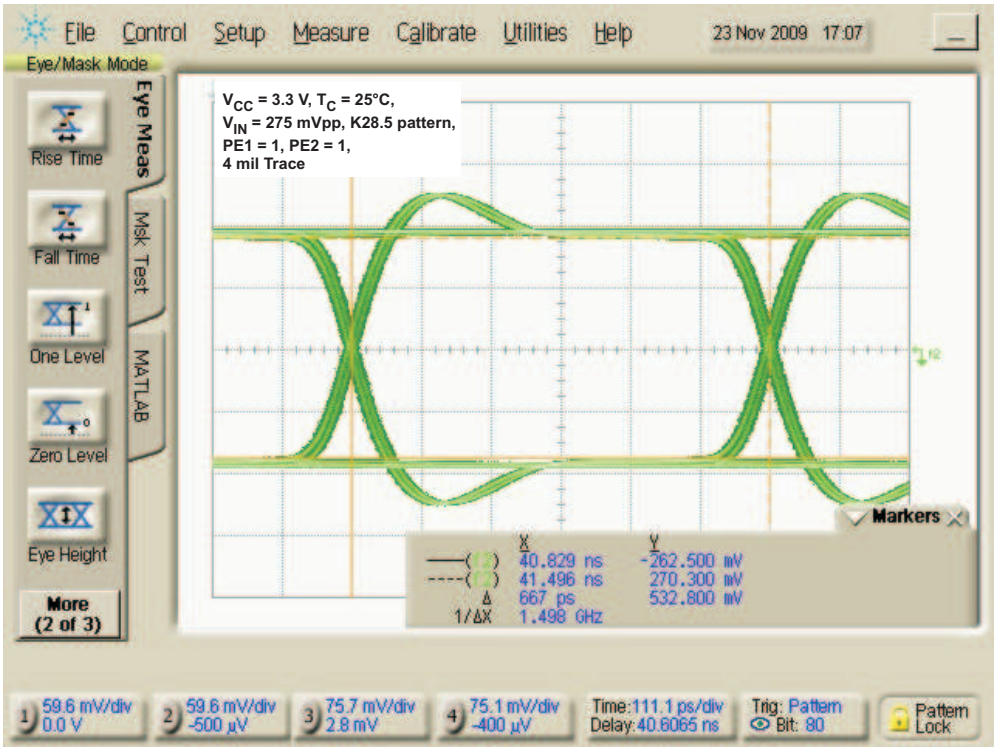


Figure 19. Eye Pattern, 1.5 Gbps, Input = 6", Output = 2"

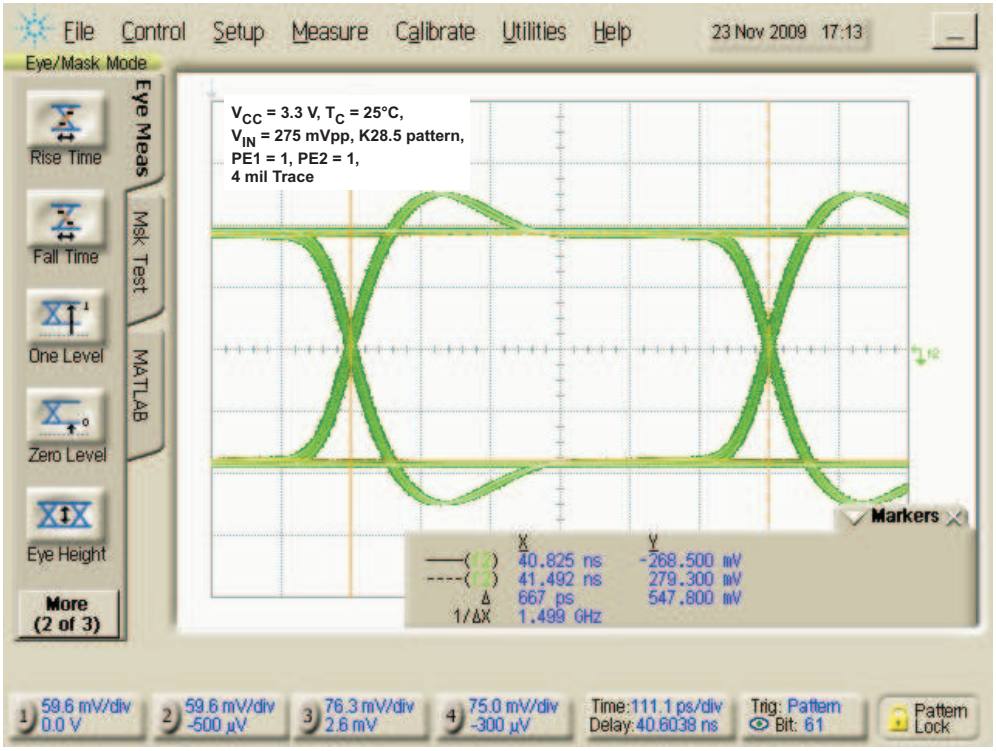


Figure 20. Eye Pattern, 1.5 Gbps, Input = 10", Output = 2"

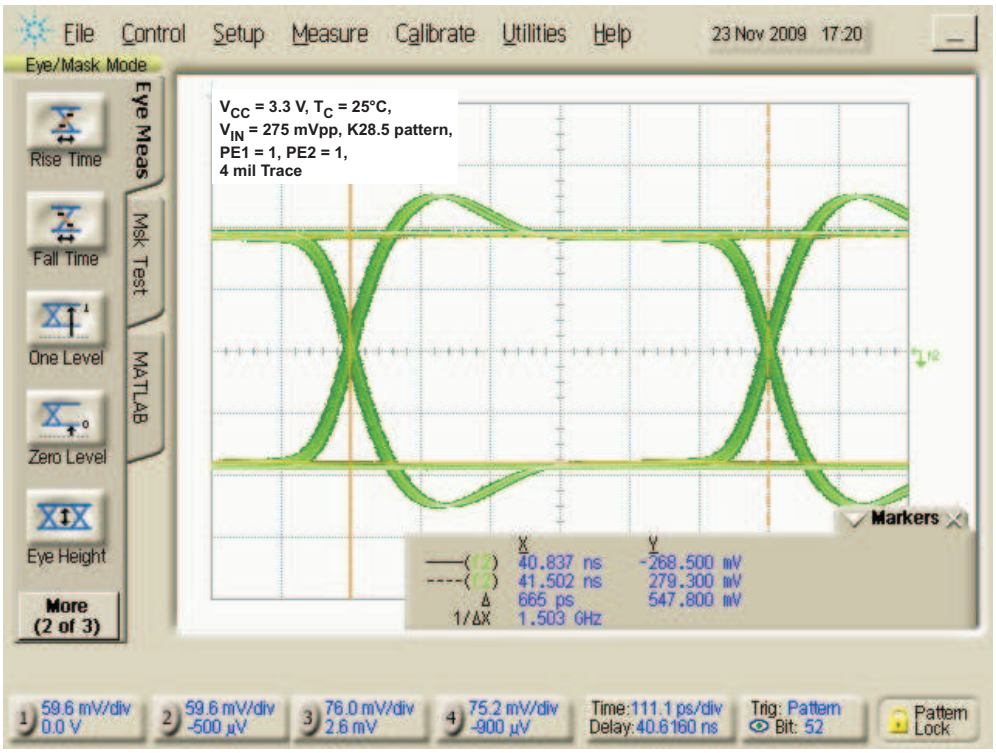


Figure 21. Eye Pattern, 1.5 Gbps, Input = 14", Output = 2"

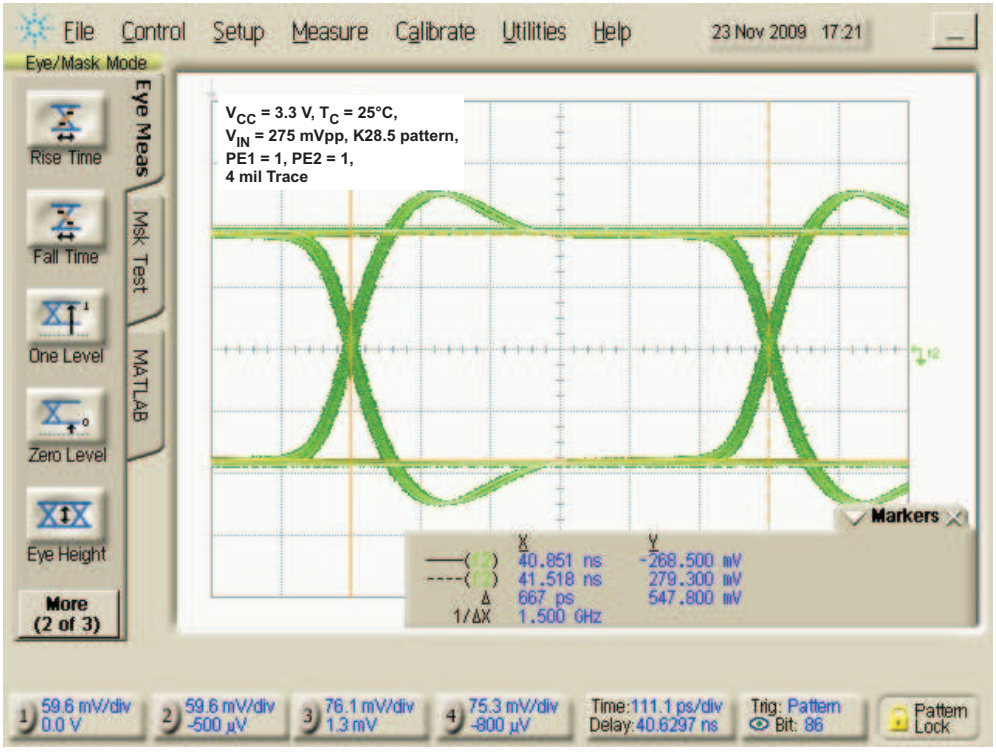


Figure 22. Eye Pattern, 1.5 Gbps, Input = 18", Output = 2"

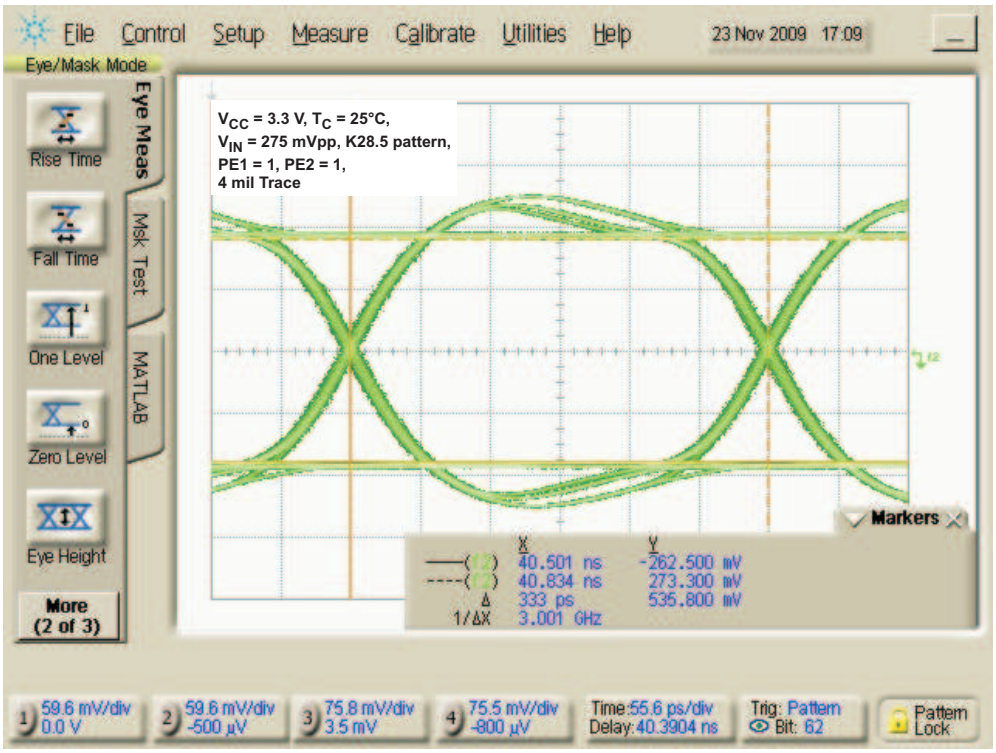


Figure 23. Eye Pattern, 3.0 Gbps, Input = 6", Output = 2"

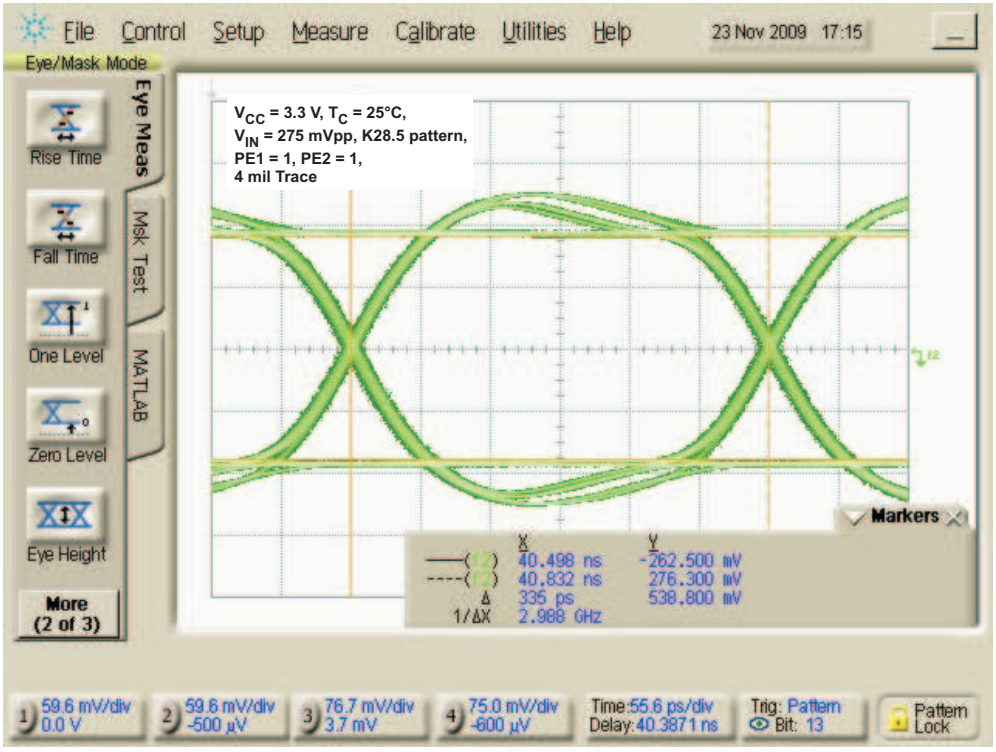


Figure 24. Eye Pattern, 3.0 Gbps, Input = 10", Output = 2"

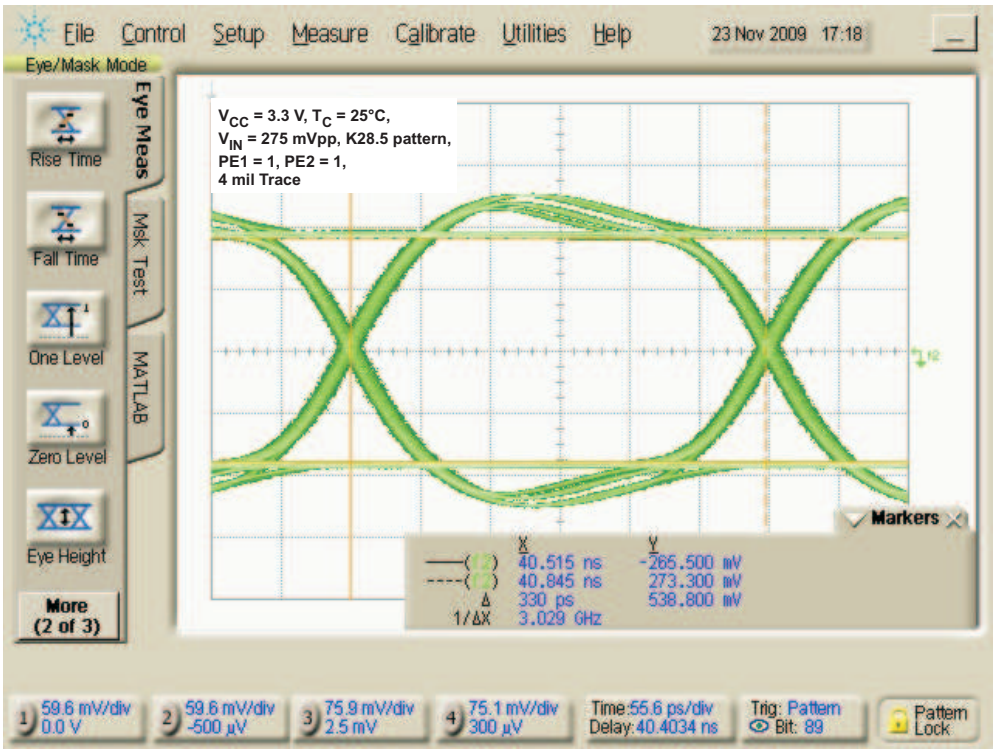


Figure 25. Eye Pattern, 3.0 Gbps, Input = 14", Output = 2"

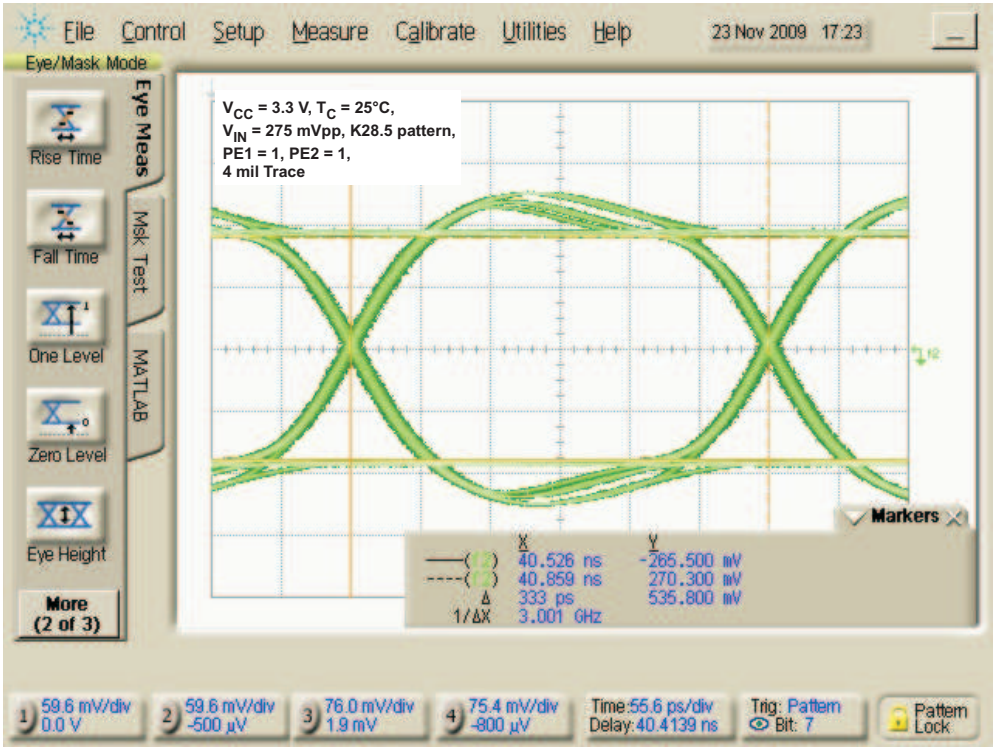
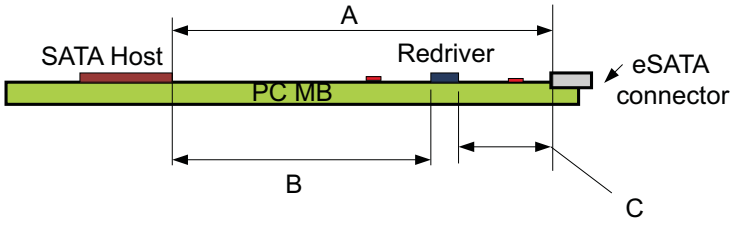
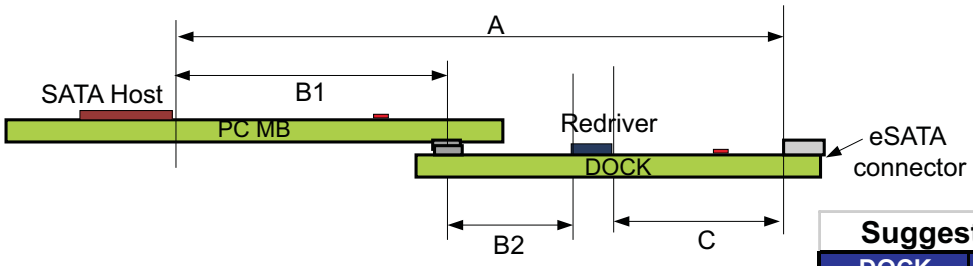


Figure 26. Eye Pattern, 3.0 Gbps, Input = 18", Output = 2"



Redriver on PC Motherboard

Suggested Trace Lengths		
PC MB	TYP* (inch)	MAX* (inch)
B	4 to 16	18
C	2 to 4	6
A	6 to 20	24



Redriver on Dock Board

Suggested Trace Lengths		
DOCK	TYP* (inch)	MAX* (inch)
B = (B1+B2)	8 to 14	16
C	2 to 4	6
A	10 to 18	22

A. Trace lengths are suggested values based on TI lab measurements (taken with output pre-emphasis enabled on both channels) to meet SATA loss and jitter specifications.

B. Actual trace length supported by the SN75LVCP412A may be more or less than suggestedvalues and depend on board layout, number of connectors used in the SATA signal path, and SATA host and esata connector design.

Figure 27. Suggested Trace Length for LVCP412A in PC MB and Dock

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVCP412ARTJR	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	CP412A	Samples
SN75LVCP412ARTJT	ACTIVE	QFN	RTJ	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	CP412A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

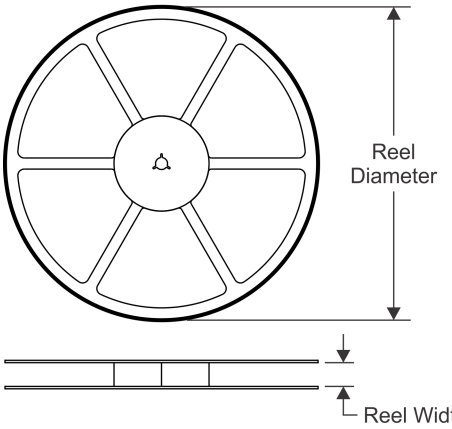
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

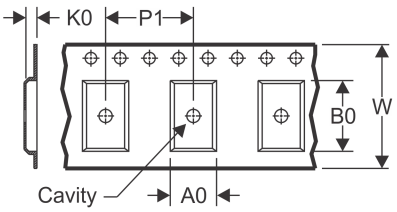
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

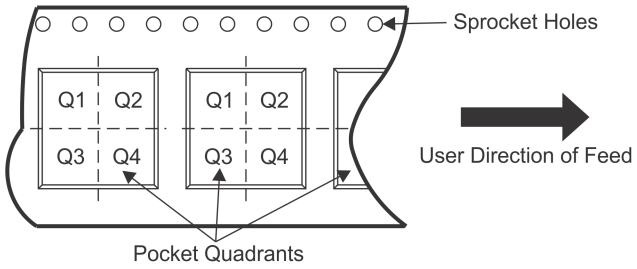


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

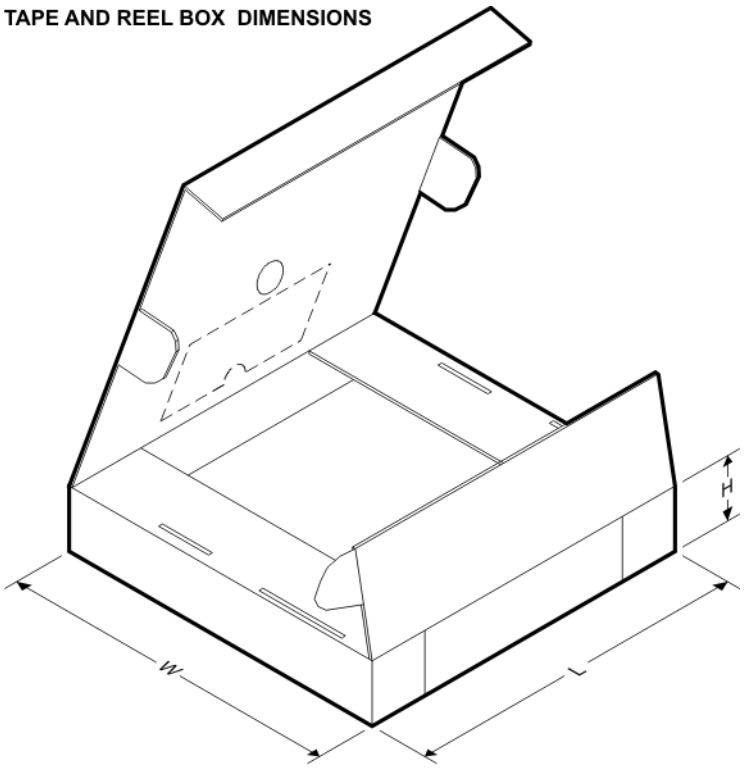
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVCP412ARTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN75LVCP412ARTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

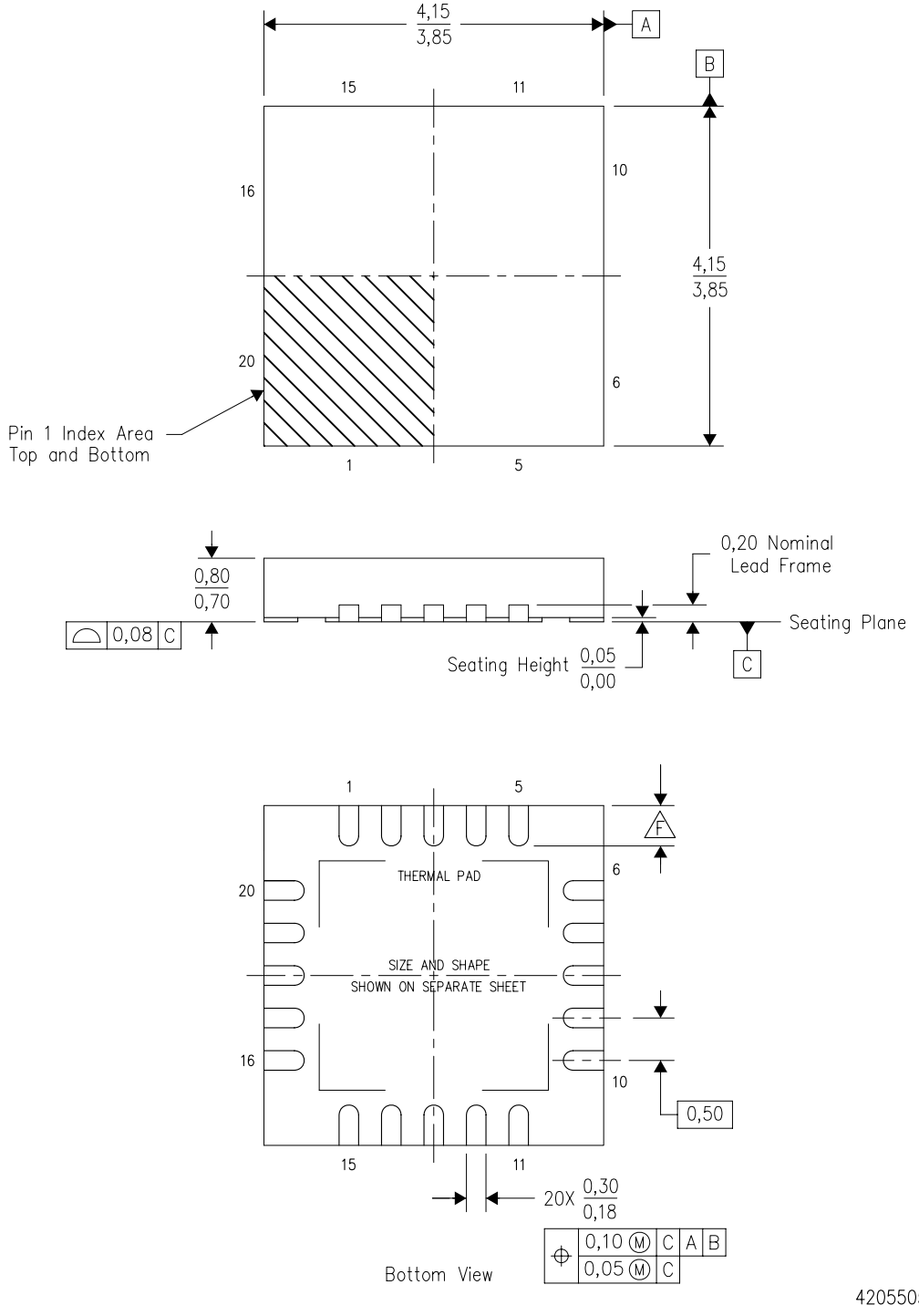
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVCP412ARTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
SN75LVCP412ARTJT	QFN	RTJ	20	250	210.0	185.0	35.0

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

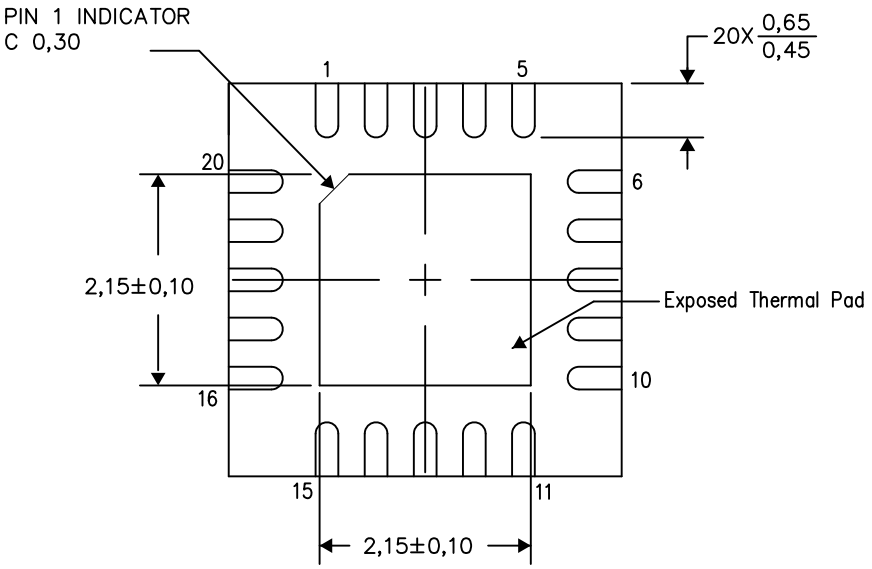
RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



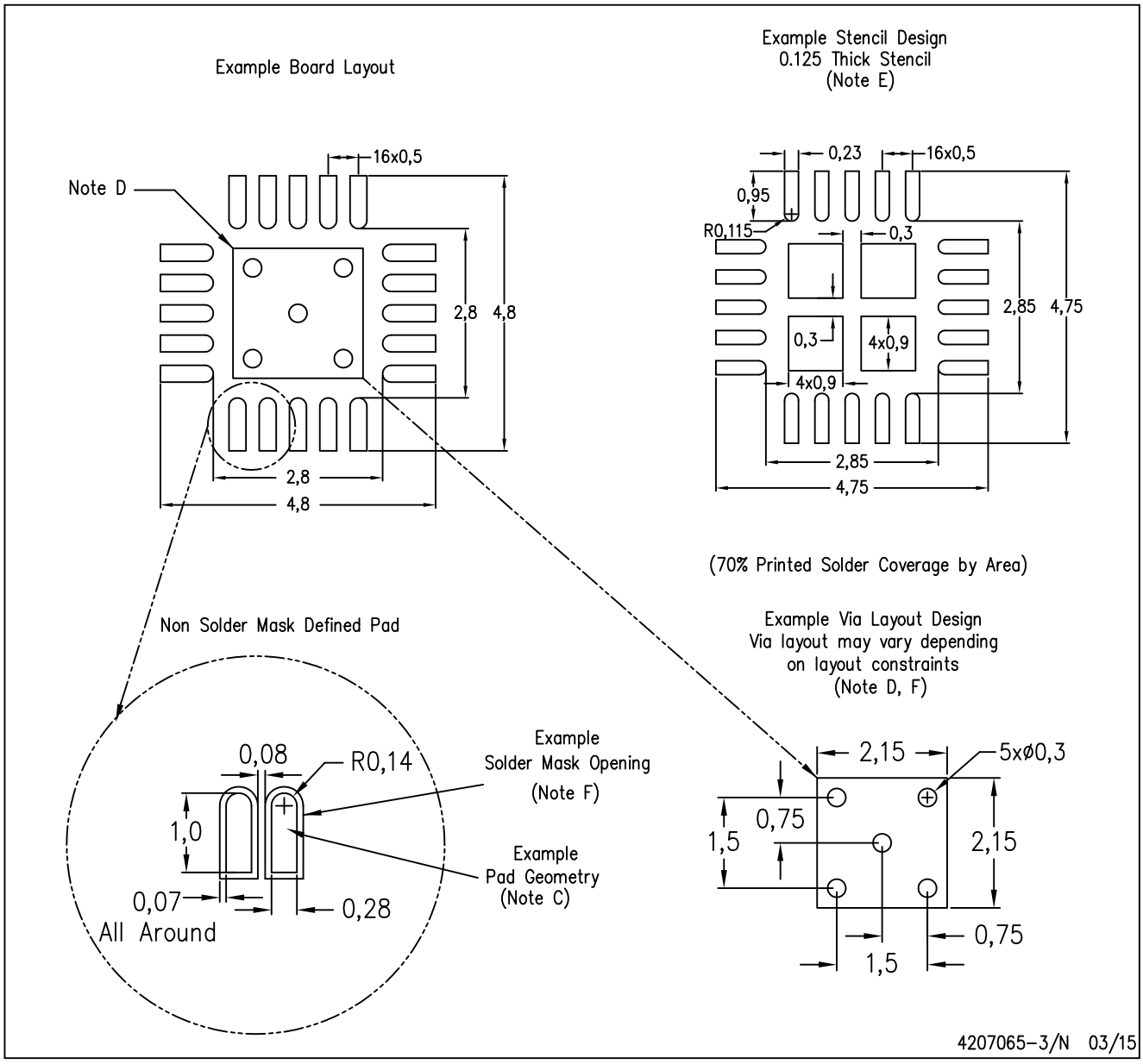
Bottom View

Exposed Thermal Pad Dimensions

4206256–3/V 05/15

NOTE: All linear dimensions are in millimeters

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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