600-mA, HIGH-EFFICIENCY MicroSiP™ STEP-DOWN CONVERTER (PROFILE <1.0mm)

Check for Samples: TPS82670, TPS82671, TPS82672, TPS82673, TPS82674, TPS82675, TPS82676, TPS82677, TPS826711

FEATURES

- **90% Efficiency at 5.5MHz Operation**
- **17µA Quiescent Current**
- **Wide V_{IN} Range From 2.3V to 4.8V**
- **5.5MHz Regulated Frequency Operation**
- **Spread Spectrum, PWM Frequency Dithering**
- ***Best in Class* Load and Line Transient**
- **±2% Total DC Voltage Accuracy**
- **Automatic PFM/PWM Mode Switching**
- **Low Ripple Light-Load PFM Mode**
- **≥35dB V_{IN} PSRR (1kHz to 10kHz)**
- **Internal Soft Start, 120-µs Start-Up Time**
- **Integrated Active Power-Down Sequencing (Optional)**
- **Current Overload and Thermal Shutdown Protection**
- **Sub 1-mm Profile Solution**
- **Total Solution Size <6.7 mm²**

APPLICATIONS

- **Cell Phones, Smart-Phones**
- **Digital TV, WLAN, GPS and Bluetooth™ Applications**
- **POL Applications**

DESCRIPTION

The TPS8267x device is a complete 600mA, DC/DC step-down power supply intended for low-power applications. Included in the package are the switching regulator, inductor and input/output capacitors. No additional components are required to finish the design.

The TPS8267x is based on a high-frequency synchronous step-down dc-dc converter optimized for battery-powered portable applications. The MicroSiP™ DC/DC converter operates at a regulated 5.5-MHz switching frequency and enters the power-save mode operation at light load currents to maintain high efficiency over the entire load current range.

The PFM mode extends the battery life by reducing the quiescent current to 17µA (typ) during light load operation. For noise-sensitive applications, the device has PWM spread spectrum capability providing a lower noise regulated output, as well as low noise at the input. These features, combined with high PSRR and AC load regulation performance, make this device suitable to replace a linear regulator to obtain better power conversion efficiency.

The TPS8267x is packaged in a compact (2.3mm x 2.9mm) and low profile (1.0mm) BGA package suitable for automated assembly by standard surface mount equipment.

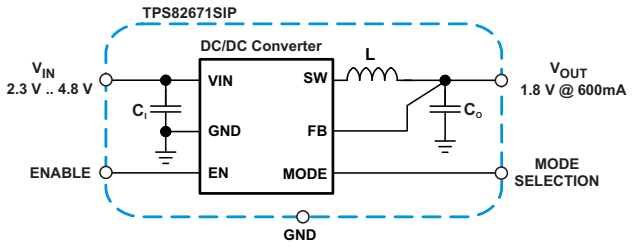


Figure 1. Typical Application

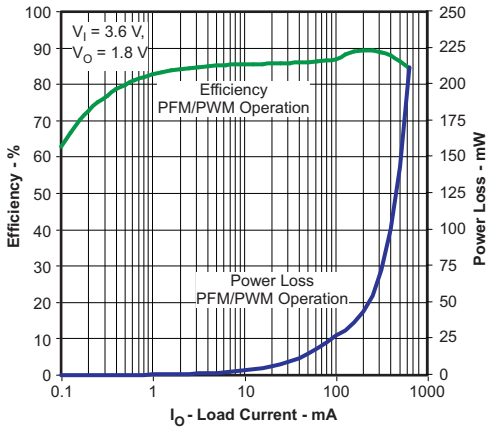


Figure 2. Efficiency vs. Load Current

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

MicroSiP is a trademark of Texas Instruments.
Bluetooth is a trademark of Bluetooth SIG, Inc.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION (1)

T_A	PART NUMBER	OUTPUT VOLTAGE(2)	DEVICE SPECIFIC FEATURE	ORDERING(3)	PACKAGE MARKING
-40°C to 85°C	TPS82670	1.86V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage Output Capacitor Discharge	TPS82670SIP	YK
	TPS82671	1.8V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage	TPS82671SIP	RA
	TPS826711	1.8V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage Output Capacitor Discharge	TPS826711SIP	YW
	TPS82672	1.5V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage	TPS82672SIP	WD
	TPS82673	1.26V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage Output Capacitor Discharge	TPS82673SIP	YL
	TPS82674	1.2V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage Output Capacitor Discharge	TPS82674SIP	SW
	TPS82675	1.2V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage	TPS82675SIP	RB
	TPS82676	1.1V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage Output Capacitor Discharge	TPS82676SIP	TU
	TPS82677	1.2V	Output Capacitor Discharge	TPS82677SIP	SK
	TPS82678(4)	1.35V	PWM Spread Spectrum Modulation Output Capacitor Discharge	TPS82678SIP	TN

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Internal tap points are available to facilitate output voltages in 25mV increments.
(3) The SIP package is available in tape and reel. Add a R suffix (e.g. TPS82671SIPR) to order quantities of 3000 parts. Add a T suffix (e.g. TPS82671SIPT) to order quantities of 250 parts.
(4) Product Preview

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
V_I	Voltage at VIN(2)(3)	–0.3	6	V
	Voltage at VOUT(3)	–0.3	3.6	V
	Voltage at EN, MODE (3)	–0.3	V_{IN} + 0.3	V
	Power dissipation	Internally limited		
T_A	Operating temperature range(4)	–40	85	°C
T_{INT} (max)	Maximum internal operating temperature		125	°C
T_{stg}	Storage temperature range	–55	125	°C
ESD rating (5)	Human body model		2	kV
	Charge device model		1	kV
	Machine model		200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Operation above 4.8V input voltage for extended periods may affect device reliability.
(3) All voltage values are with respect to network ground terminal.
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating temperature ($T_{INT(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum internal temperature of 105°C.
(5) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TPS8267xSIP	UNITS
		SIP	
		8 PINS	
θ_{JA}	Junction-to-ambient (top) thermal resistance	125	°C/W
	Junction-to-ambient (bottom) thermal resistance	70	
θ_{JCtop}	Junction-to-case (top) thermal resistance		
θ_{JB}	Junction-to-board thermal resistance		
ψ_{JT}	Junction-to-top characterization parameter		
ψ_{JB}	Junction-to-board characterization parameter		
θ_{JCbot}	Junction-to-case (bottom) thermal resistance		

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal data have been measured using TI's 4-layer evaluation board.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range		2.3		4.8(1)	V
I_O	Output current range	TPS82671 to TPS826711	0		600	mA
	Additional output capacitance (PFM/PWM operation)(2)	TPS82670 to TPS82676 TPS826711		0	2.5	µF
		TPS82677, TPS82678		0	4	µF
	Additional output capacitance (PWM operation)(2)			0	7	µF
T_A	Ambient temperature		–40		+85	°C
T_J	Operating junction temperature		–40		+125	°C

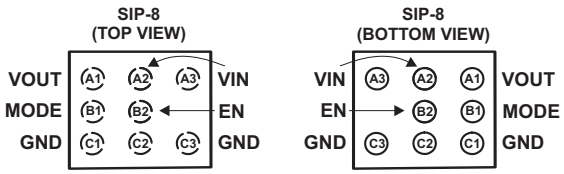
(1) Operation above 4.8V input voltage for extended periods may affect device reliability.
(2) In certain applications larger capacitor values can be tolerable, see *output capacitor selection* section for more details.

ELECTRICAL CHARACTERISTICS

Minimum and maximum values are at V_{IN} = 2.3V to 5.5V, V_{OUT} = 1.8V, EN = 1.8V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V, V_{OUT} = 1.8V, EN = 1.8V, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_Q	Operating quiescent current		I_O = 0mA. Device not switching		17	40	µA
			I_O = 0mA. PWM operation		5.8		mA
I_{SD}	Shutdown current		EN = GND		0.5	5	µA
UVLO	Undervoltage lockout threshold				2.05	2.1	V
PROTECTION							
	Thermal shutdown				140		°C
	Thermal shutdown hysteresis				10		°C
I_{LIM}	Peak Input Current Limit				1100		mA
I_{SC}	Input current limit under short-circuit conditions		V_O shorted to ground		13.5		mA
ENABLE, MODE							
V_{IH}	High-level input voltage			1.0			V
V_{IL}	Low-level input voltage					0.4	V
I_{lkg}	Input leakage current		Input connected to GND or VIN		0.01	1.5	µA
OSCILLATOR							
f_{SW}	Oscillator frequency		I_O = 0mA. PWM operation	4.9	5.45	6.0	MHz
OUTPUT							
V_{OUT}	Regulated DC output voltage	TPS82670, TPS82671, TPS826711, TPS82672, TPS82673, TPS82674, TPS82675, TPS82676, TPS82678	2.5V ≤ V_I ≤ 4.8V, 0mA ≤ I_O ≤ 600 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			2.5V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 600 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			2.5V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 600 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
		TPS82677, TPS82678	2.5V ≤ V_I ≤ 4.8V, 0mA ≤ I_O ≤ 600 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			2.5V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 600 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
	Line regulation		V_I = V_O + 0.5V (min 2.5V) to 5.5V, I_O = 200 mA		0.23		%/V
	Load regulation		I_O = 0mA to 600 mA. PWM operation		–0.00085		%/mA
	Feedback input resistance				480		kΩ
ΔV_O	Power-save mode ripple voltage	TPS82671	I_O = 1mA, V_O = 1.8V		19		mV_{PP}
		TPS82674, TPS82675	I_O = 1mA, V_O = 1.2V		16		mV_{PP}
		TPS82676	I_O = 1mA, V_O = 1.1V		16		mV_{PP}
		TPS82677	I_O = 1mA, V_O = 1.2V		25		mV_{PP}
		TPS82678	I_O = 1mA, V_O = 1.35V		TBD		mV_{PP}
	Start-up time	TPS82671, TPS826711	I_O = 0mA, Time from active EN to V_O		120		µs
r_{DIS}	Discharge resistor for power-down sequence	TPS82670, TPS826711, TPS82673, TPS82674, TPS82676, TPS82677, TPS82678	Device featuring active discharge		70	150	Ω

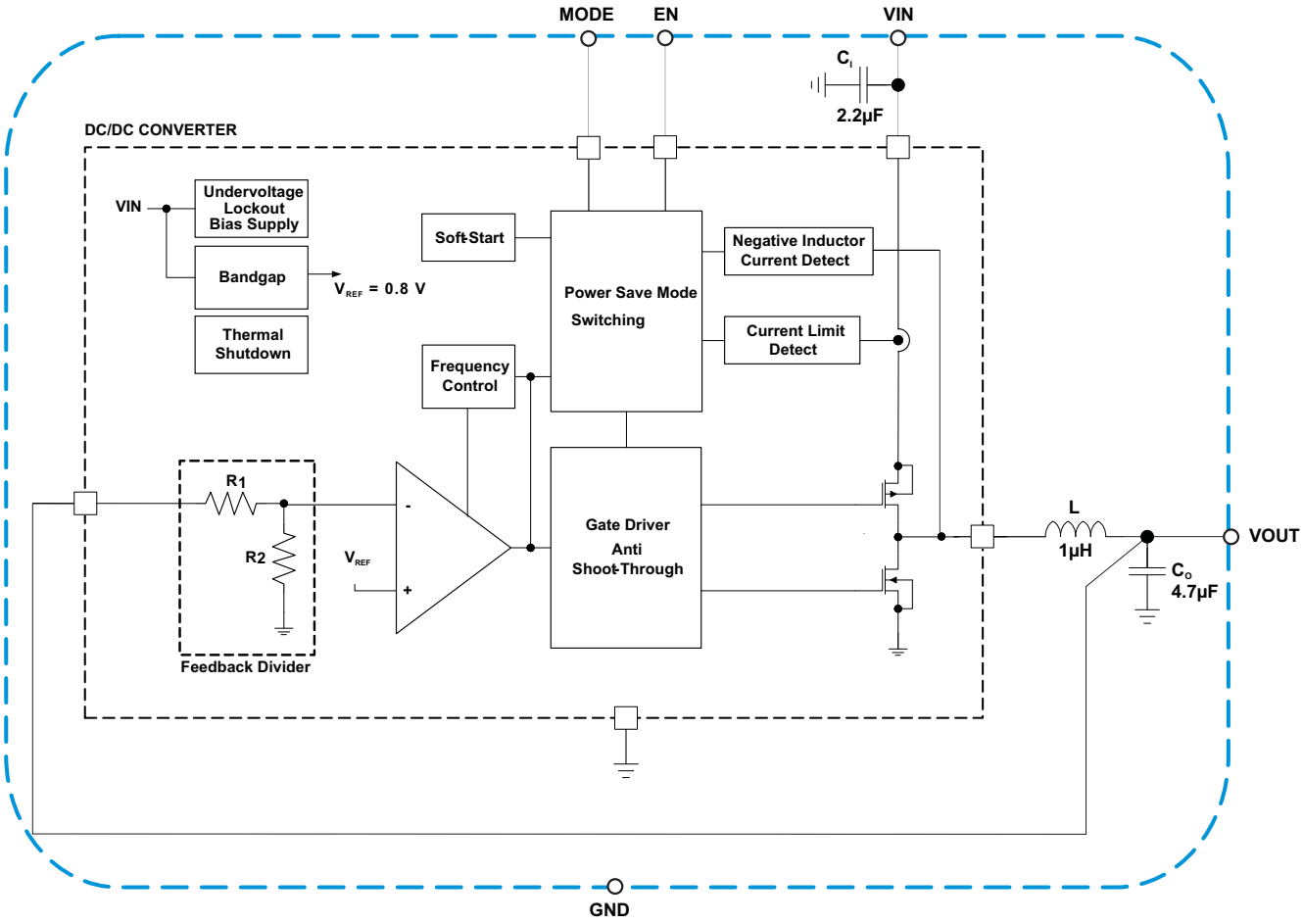
PIN ASSIGNMENTS



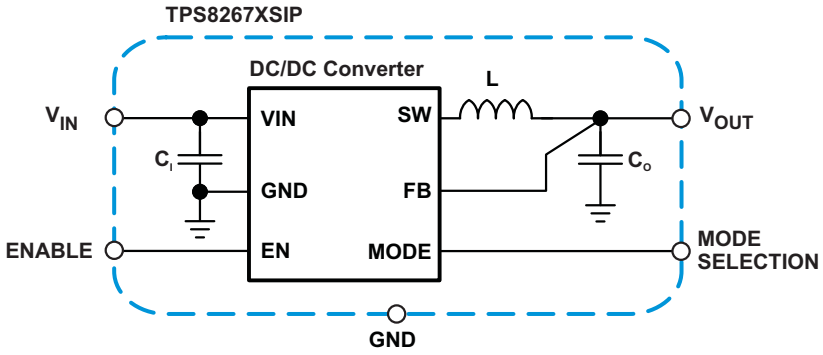
PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
VOUT	A1	O	Power output pin. Apply output load between this pin and GND.
VIN	A2, A3	I	The VIN pins supply current to the TPS8267x internal regulator.
EN	B2	I	This is the enable pin of the device. Connect this pin to ground to force the converter into shutdown mode. Pull this pin to V_I to enable the device. This pin must not be left floating and must be terminated.
MODE	B1	I	This is the mode selection pin of the device. This pin must not be left floating and must be terminated. MODE = LOW: The device is operating in regulated frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents. MODE = HIGH: Low-noise mode is enabled and regulated frequency PWM operation is forced.
GND	C1, C2, C3	–	Ground pin.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Load current	3, 4
		vs Input voltage	5
	Peak-to-peak output ripple voltage	vs Load current	6, 7, 8
V_O	DC output voltage	vs Load current	9, 10, 11
	Combined line/load transient response		12, 13
	Load transient response		14, 15, 16, 17 18, 19, 20
	AC load transient response		21
	Load transient response		22, 23, 24, 25 26, 27, 28
	AC load transient response		29
	PFM/PWM boundaries	vs Input voltage	30, 31
I_Q	Quiescent current	vs Input voltage	32
f_s	PWM switching frequency	vs Input voltage	33
	Start-up		34, 35
PSRR	Power supply rejection ratio	vs. Frequency	36
	Spurious output noise (PFM mode)	vs. Frequency	37
	Spurious output noise (PWM mode)	vs. Frequency	38
	Output spectral noise density	vs. Frequency	39

EFFICIENCY vs LOAD CURRENT

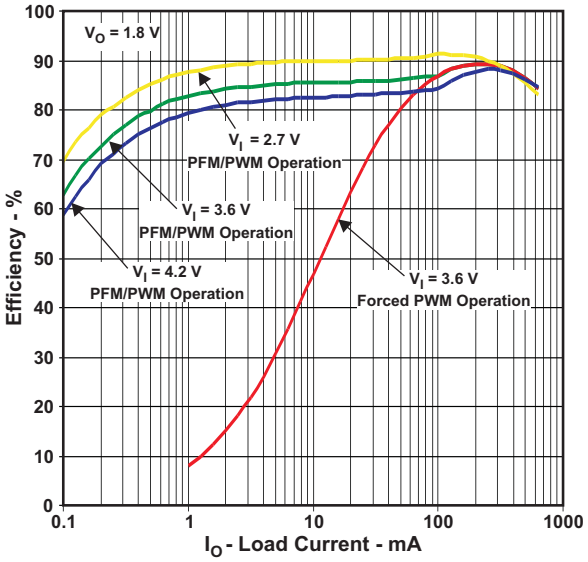


Figure 3.

EFFICIENCY vs LOAD CURRENT

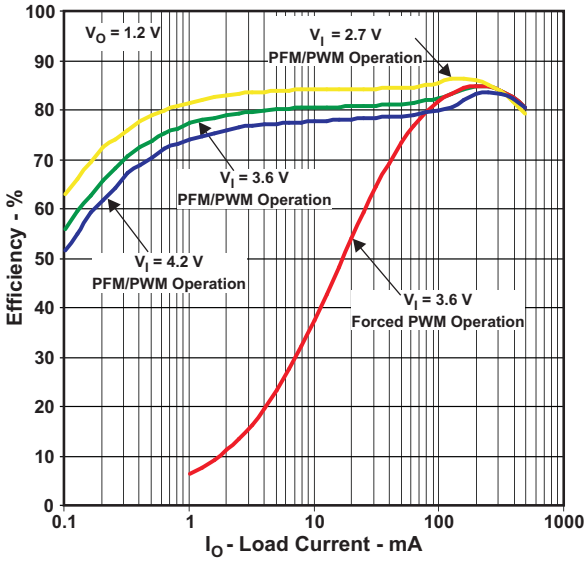


Figure 4.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY vs INPUT VOLTAGE

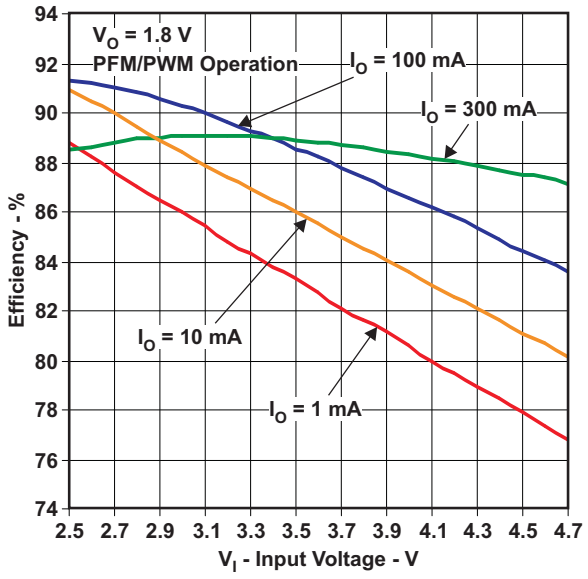


Figure 5.

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE vs LOAD CURRENT

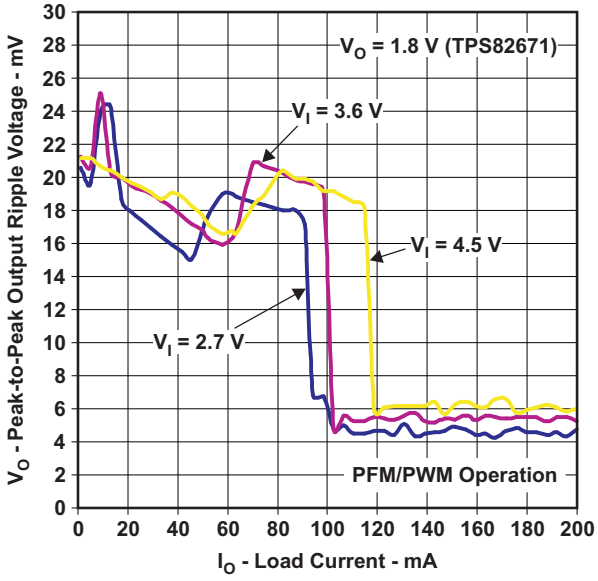


Figure 6.

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE vs LOAD CURRENT

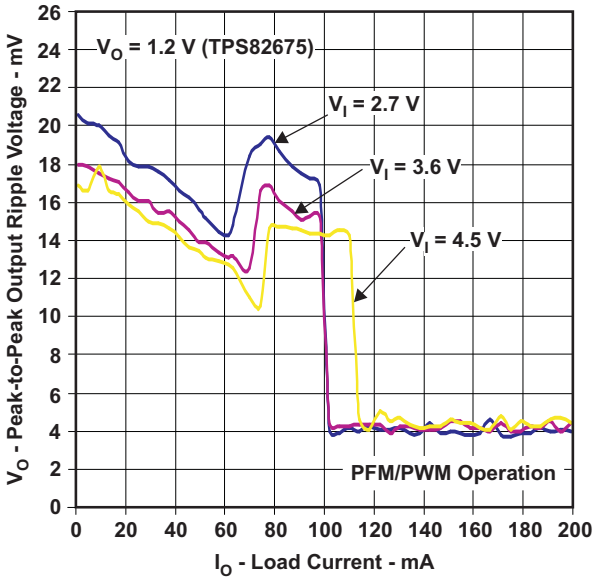


Figure 7.

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE vs LOAD CURRENT

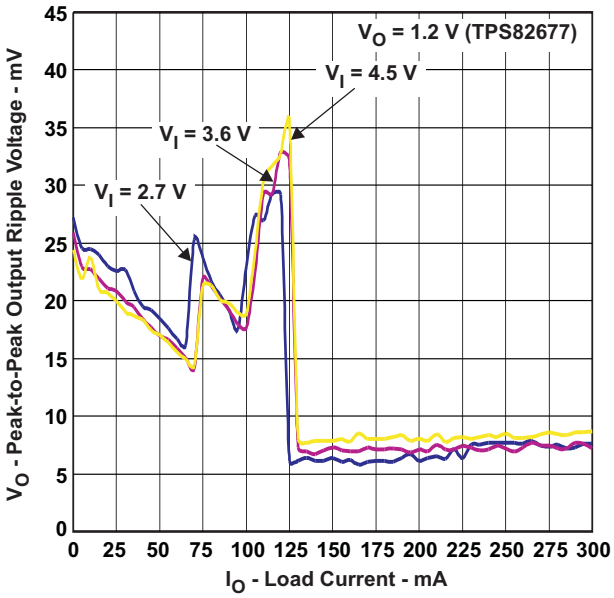


Figure 8.

TYPICAL CHARACTERISTICS (continued)

DC OUTPUT VOLTAGE
vs
LOAD CURRENT

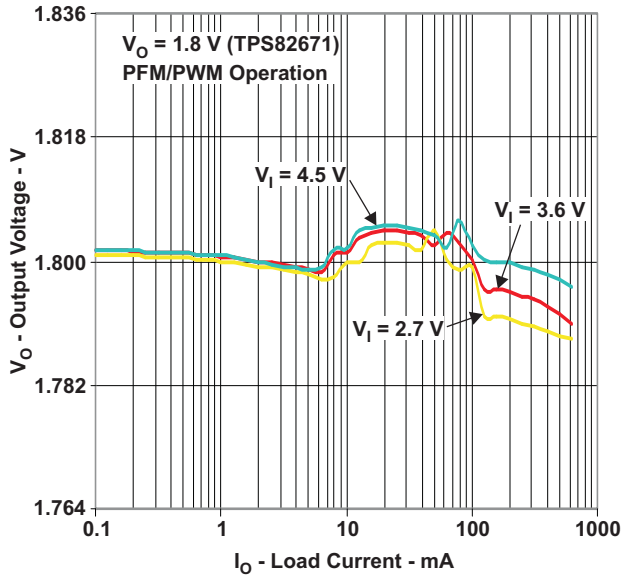


Figure 9.

DC OUTPUT VOLTAGE
vs
LOAD CURRENT

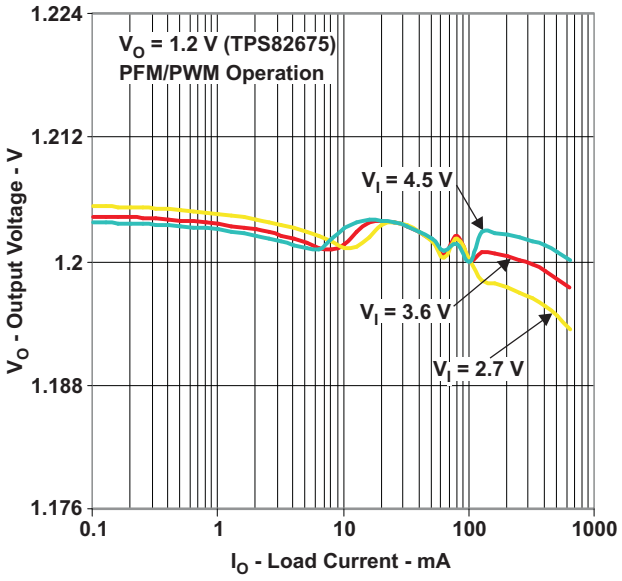


Figure 10.

DC OUTPUT VOLTAGE
vs
LOAD CURRENT

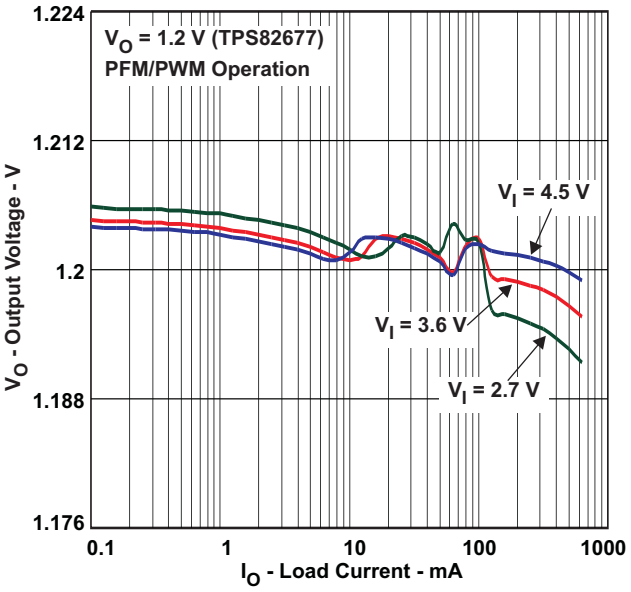


Figure 11.

COMBINED LINE/LOAD TRANSIENT RESPONSE

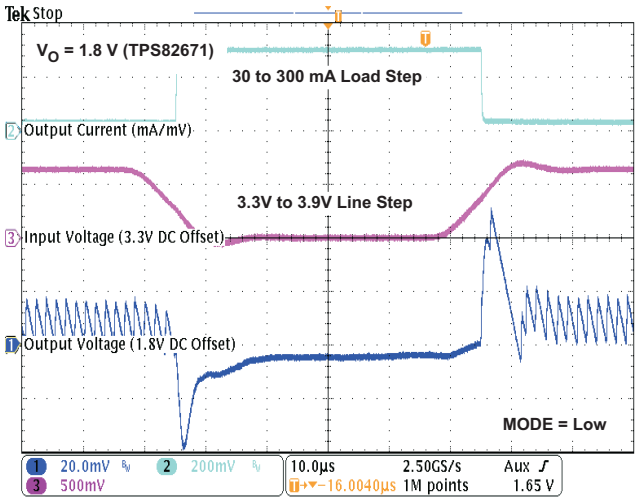


Figure 12.

TYPICAL CHARACTERISTICS (continued)

COMBINED LINE/LOAD TRANSIENT RESPONSE

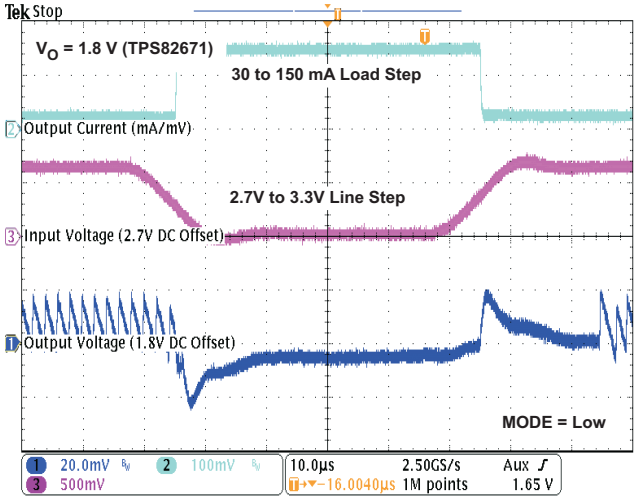


Figure 13.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

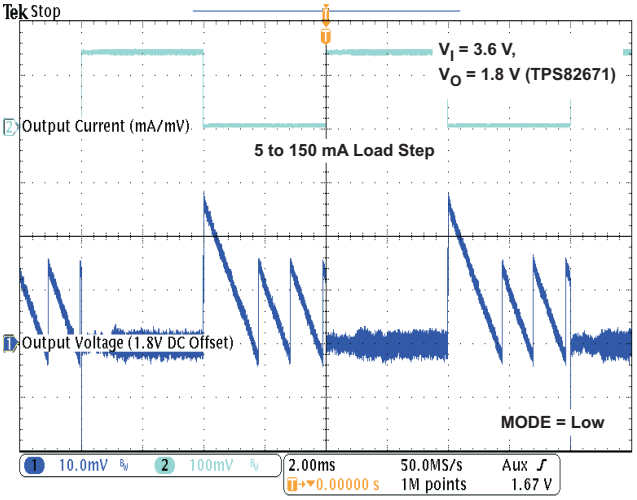


Figure 14.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

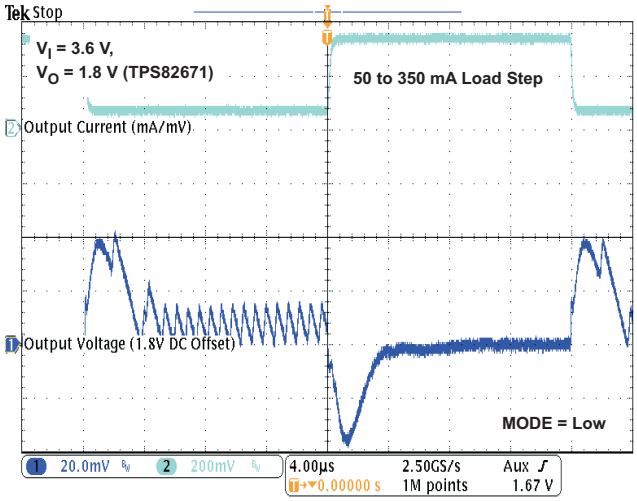


Figure 15.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

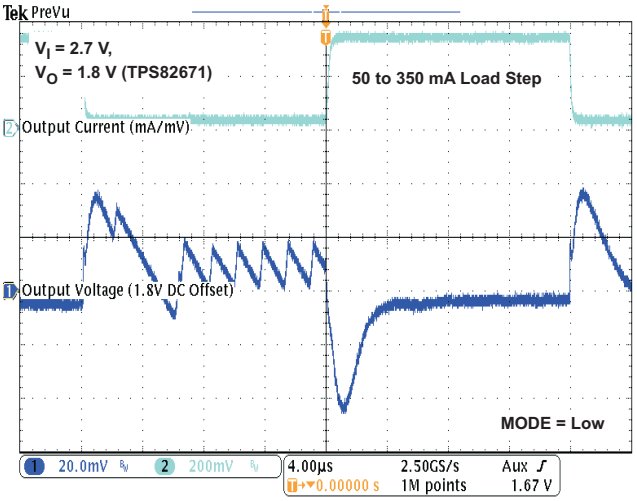


Figure 16.

TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

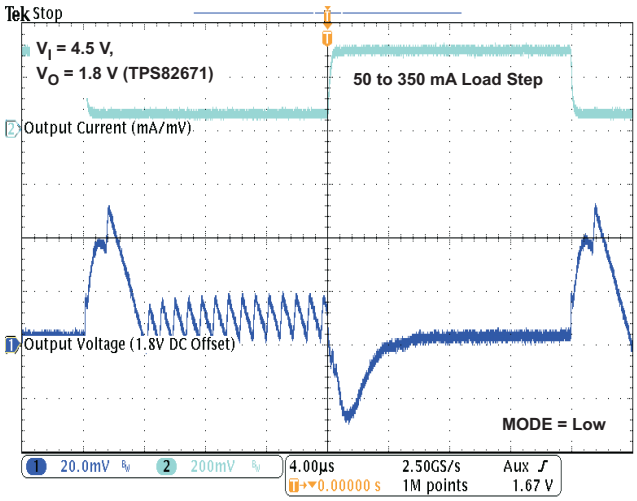


Figure 17.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

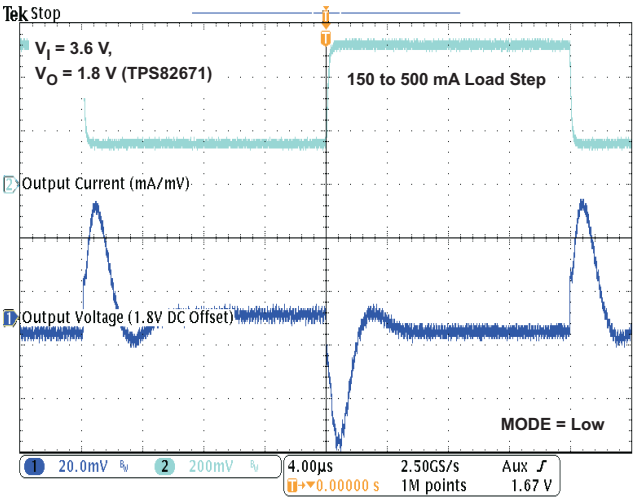


Figure 18.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

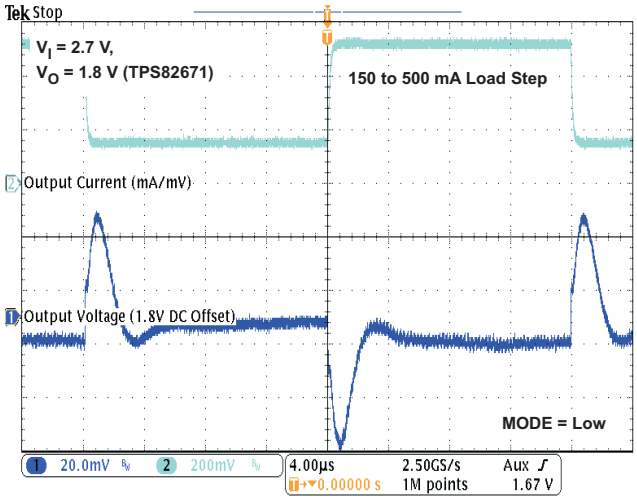


Figure 19.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

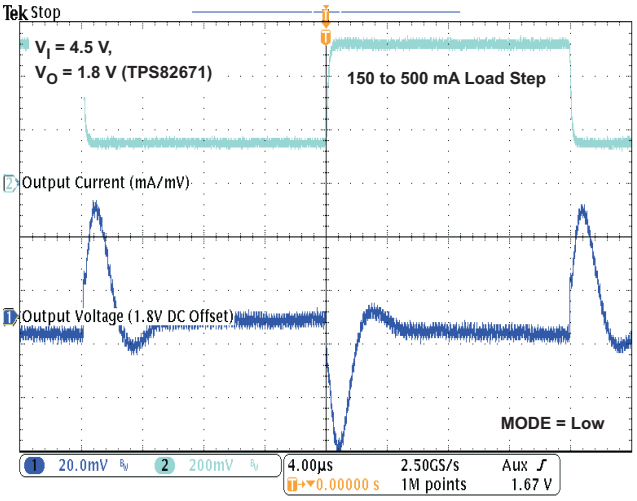


Figure 20.

TYPICAL CHARACTERISTICS (continued)

AC LOAD TRANSIENT RESPONSE

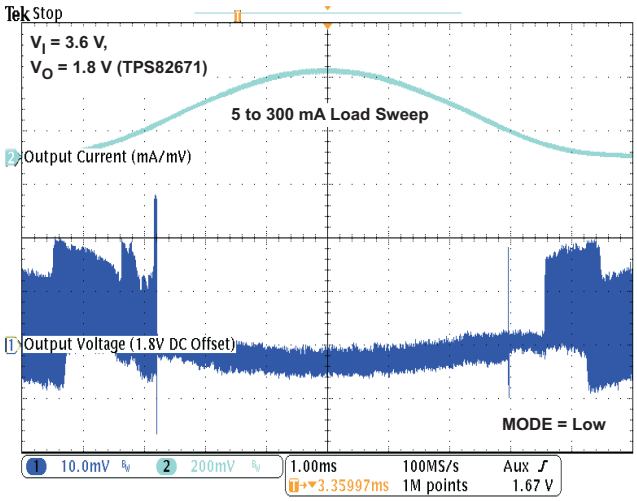


Figure 21.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

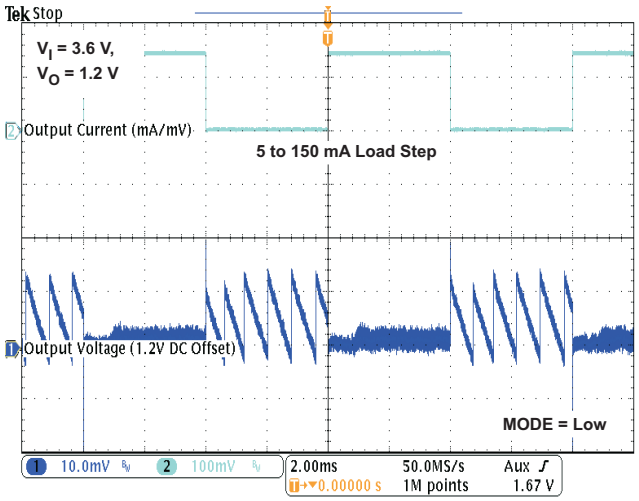


Figure 22.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

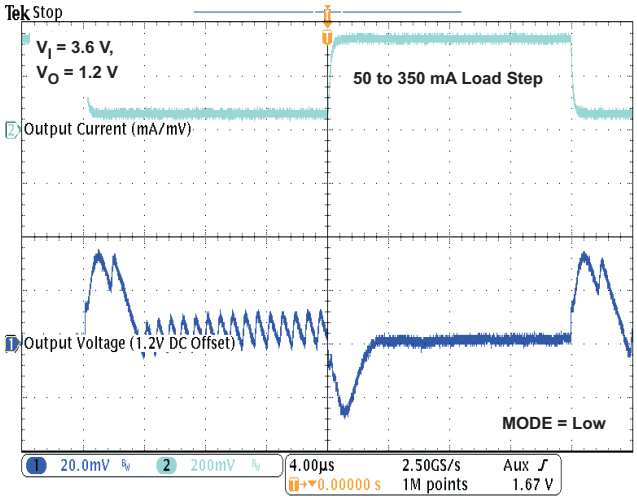


Figure 23.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

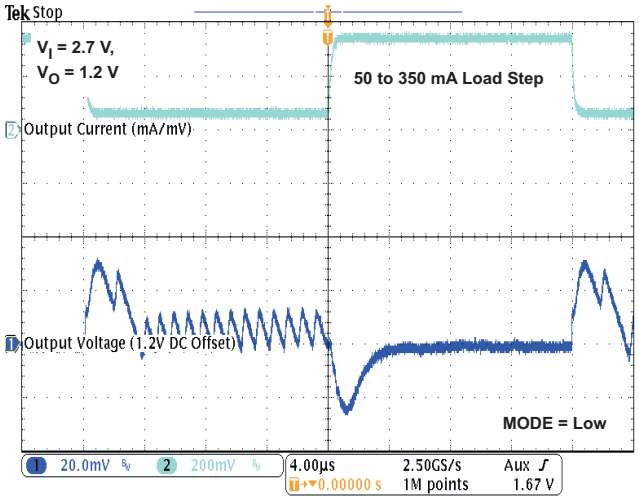


Figure 24.

TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

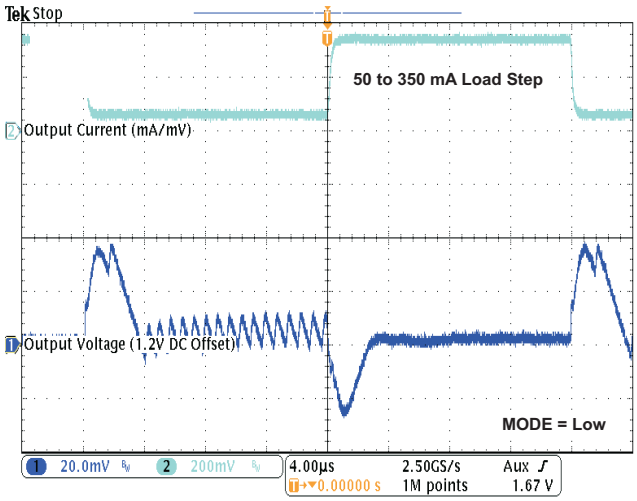


Figure 25.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

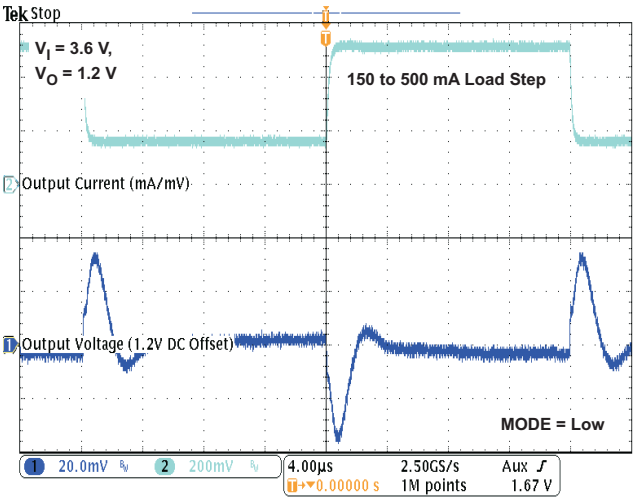


Figure 26.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

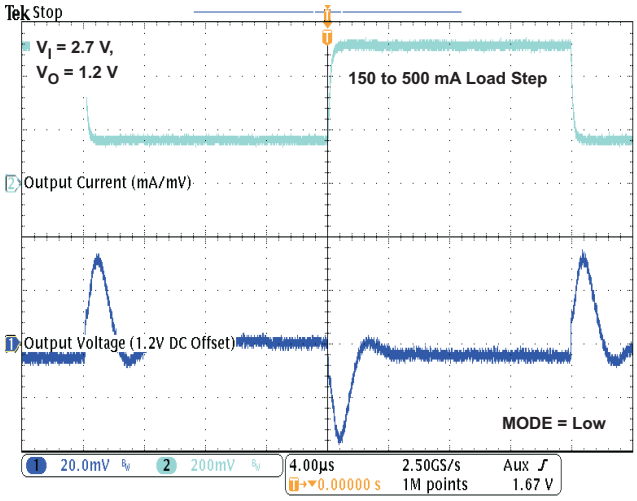


Figure 27.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

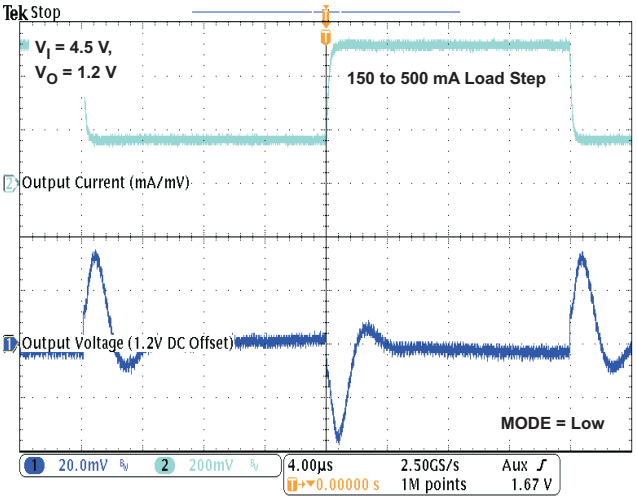


Figure 28.

TYPICAL CHARACTERISTICS (continued)

AC LOAD TRANSIENT RESPONSE

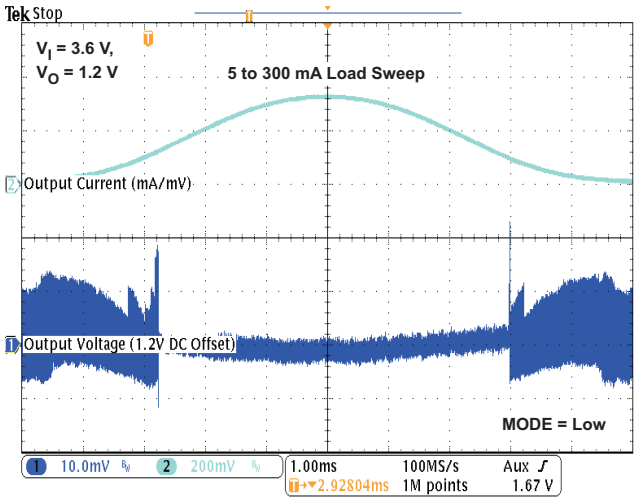


Figure 29.

PFM/PWM BOUNDARIES

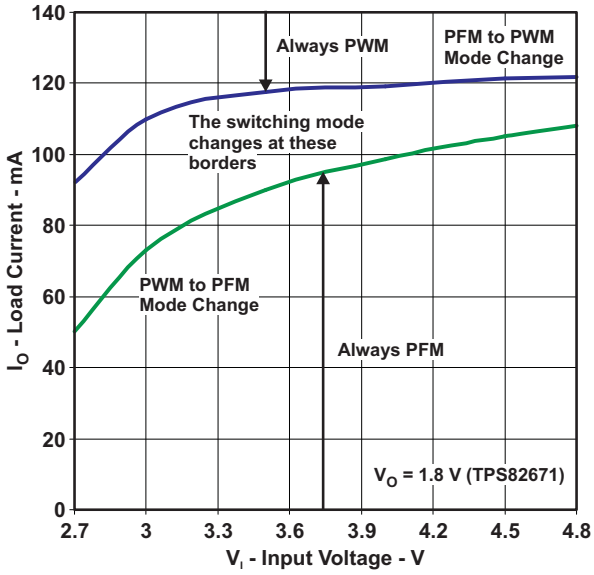


Figure 30.

PFM/PWM BOUNDARIES

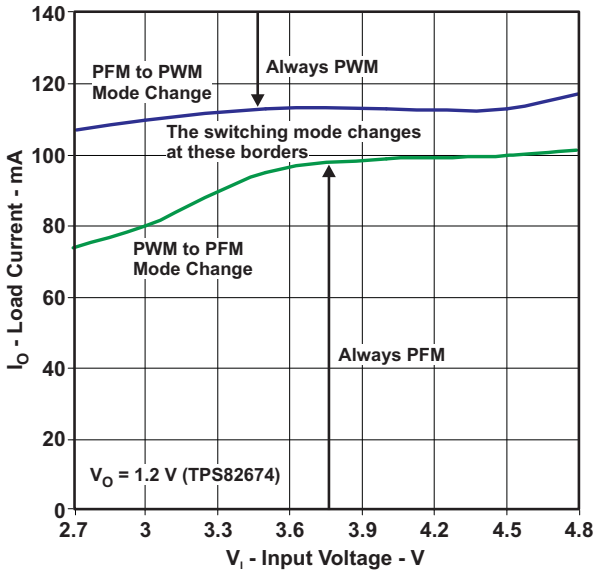


Figure 31.

QUIESCENT CURRENT vs INPUT VOLTAGE

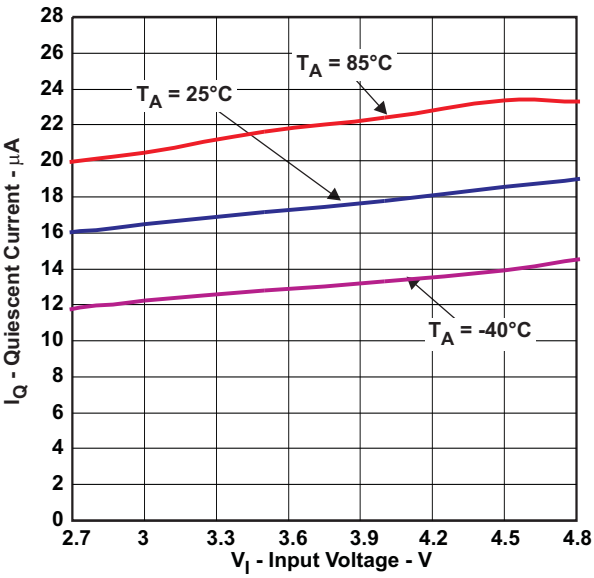


Figure 32.

TYPICAL CHARACTERISTICS (continued)

PWM SWITCHING FREQUENCY vs INPUT VOLTAGE

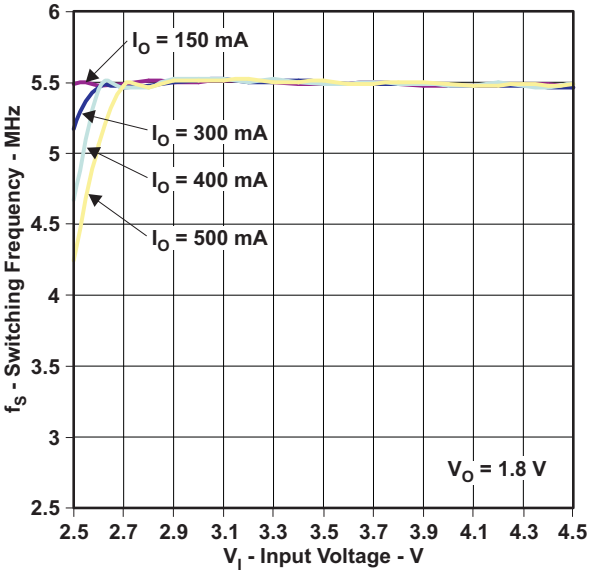


Figure 33.

START-UP

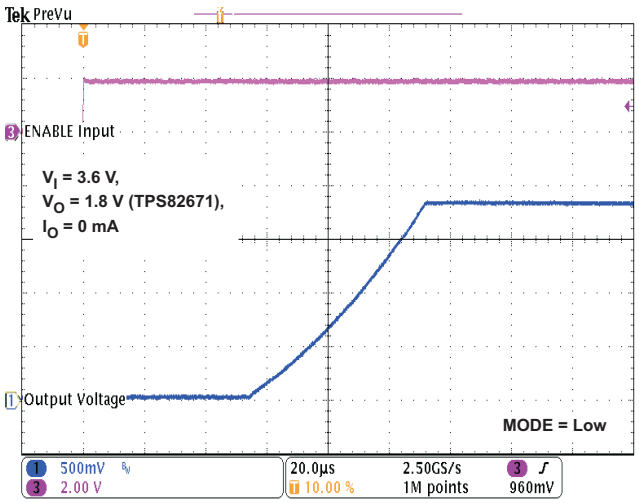


Figure 34.

START-UP

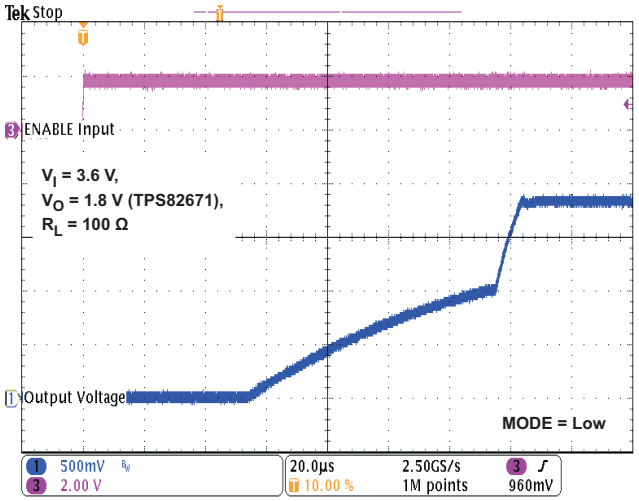


Figure 35.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

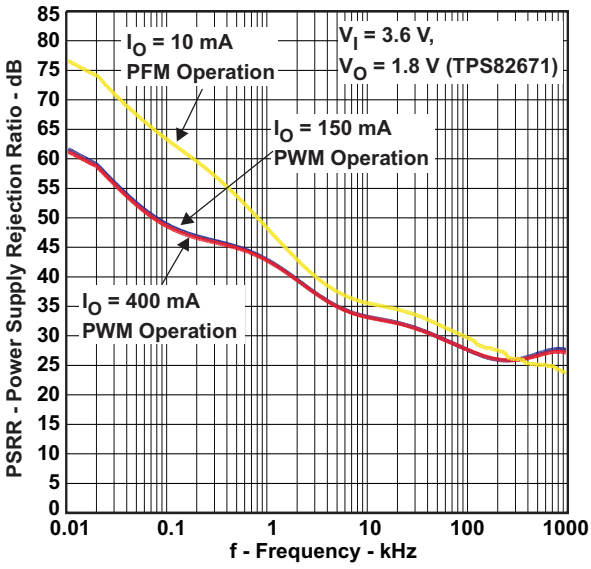


Figure 36.

TYPICAL CHARACTERISTICS (continued)

SPURIOUS OUTPUT NOISE (PFM MODE) vs FREQUENCY

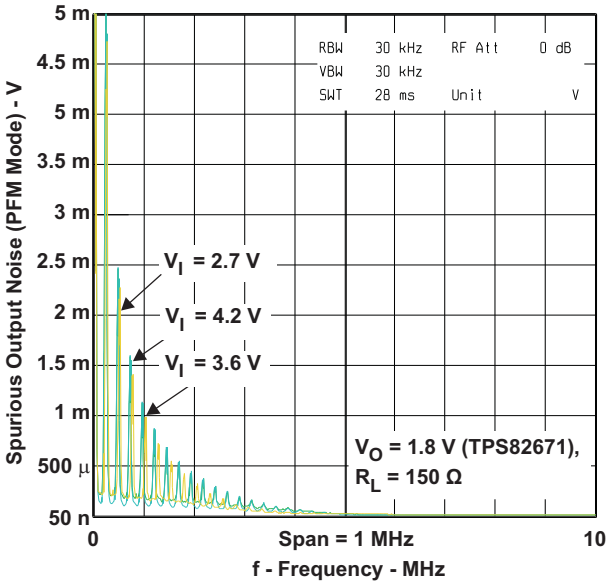


Figure 37.

SPURIOUS OUTPUT NOISE (PWM MODE) vs FREQUENCY

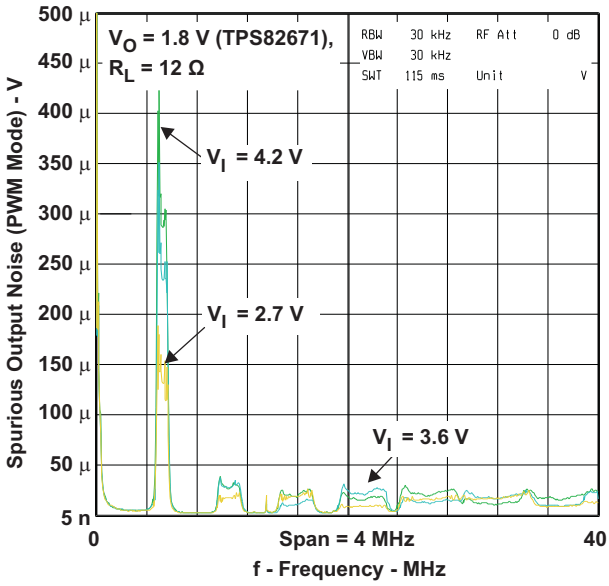


Figure 38.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

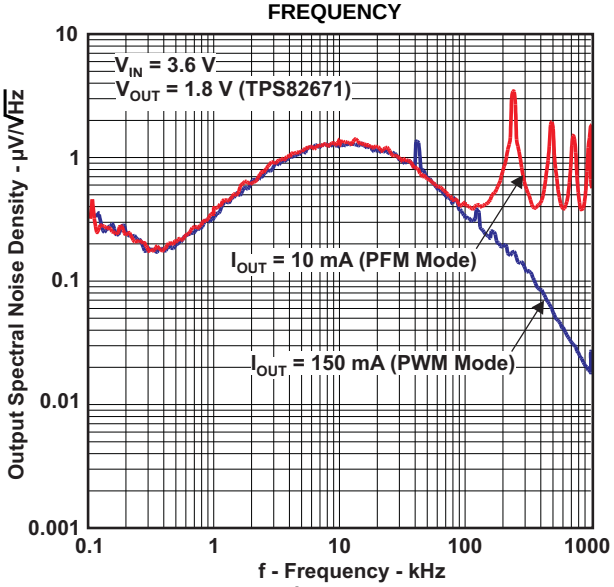


Figure 39.

DETAILED DESCRIPTION

OPERATION

The TPS8267x is a stand-alone, synchronous, step-down converter. The converter operates at a regulated 5.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS8267x converter operates in power-save mode with pulse frequency modulation (PFM).

The converter uses a unique frequency-locked ring-oscillating modulator to achieve *best-in-class* load and line response. One key advantage of the non-linear architecture is that there is no traditional feed-back loop. The loop response to change in V_O is essentially instantaneous, which explains the transient response. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency lock loop (FLL) holds the switching frequency constant over a large range of operating conditions.

Combined with *best-in-class* load and line-transient response characteristics, the low quiescent current of the device (approximately 17µA) helps to maintain high efficiency at light load while that current preserves a fast transient response for applications that require tight output regulation.

The TPS8267x integrates an input current limit to protect the device against heavy load or short circuits and features an undervoltage lockout circuit to prevent the device from misoperation at low input voltages. Fully functional operation is permitted down to 2.1V input voltage.

POWER-SAVE MODE

If the load current decreases, the converter enters power-save mode automatically. During power-save mode, the converter operates in discontinuous current, (DCM) single-pulse PFM mode, which produces a low output ripple compared with other PFM architectures.

When in power-save mode, the converter resumes its operation when the output voltage falls below the nominal voltage. The converter ramps up the output voltage with a minimum of one pulse and goes into power-save mode when the output voltage is within its regulation limits.

The IC exits PFM mode and enters PWM mode when the output current can no longer be supported in PFM mode. As a consequence, the DC output voltage is typically positioned approximately 0.5% above the nominal output voltage. The transition between PFM and PWM is seamless.

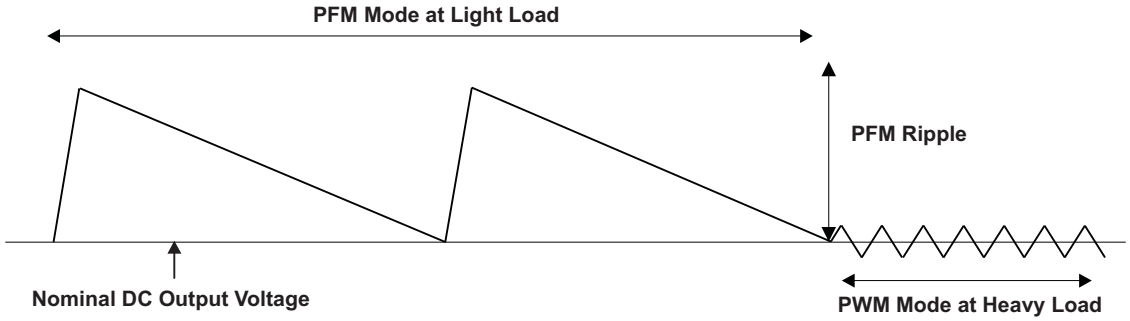


Figure 40. Operation in PFM Mode and Transfer to PWM Mode

MODE SELECTION

The MODE pin selects the operating mode of the device. Connecting the MODE pin to GND enables the automatic PWM and power-save mode operation. The converter operates in regulated frequency PWM mode at moderate to heavy loads, and operates in PFM mode during light loads. This type of operation maintains high efficiency over a wide load current range.

Pulling the MODE pin high forces the converter to operate in PWM mode even at light-load currents. The advantage is that the converter modulates its switching frequency according to a spread spectrum PWM modulation technique that allows simple filtering of the switching harmonics in noise-sensitive applications. In this mode, the efficiency is lower when compared to the power-save mode during light loads.

For additional flexibility, it is possible to switch from power-save mode to PWM mode during operation. This type of operation allows efficient power management by adjusting the operation of the converter to the specific system requirements.

SPREAD SPECTRUM, PWM FREQUENCY DITHERING

The goal of spread spectrum architecture is to spread out the emitted RF energy over a larger frequency range so that any resulting electromagnetic interference (EMI) is similar to white noise. The end result is a spectrum that is continuous and lower in peak amplitude. Spread spectrum makes it easier to comply with EMI standards. It also makes it easier to comply with the power supply ripple requirements in cellular and non-cellular wireless applications. Radio receivers are typically susceptible to narrowband noise that is focused on specific frequencies.

Switching regulators can be particularly troublesome in applications where electromagnetic interference (EMI) is a concern. Switching regulators operate on a cycle-by-cycle basis to transfer power to an output. In most cases, the frequency of operation is either fixed or regulated, based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

The spread spectrum architecture varies the switching frequency by approximately ±10% of the nominal switching frequency, thereby significantly reduces the peak radiated and conducting noise on both the input and output supplies. The frequency dithering scheme is modulated with a triangle profile and a modulation frequency f_m.

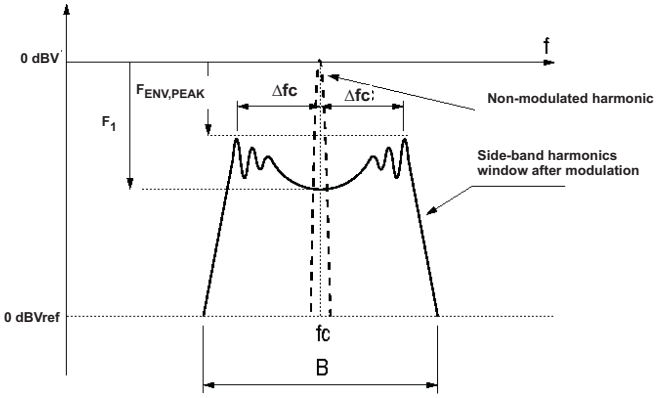


Figure 41. Spectrum of a Frequency Modulated Sin. Wave with Sinusoidal Variation in Time

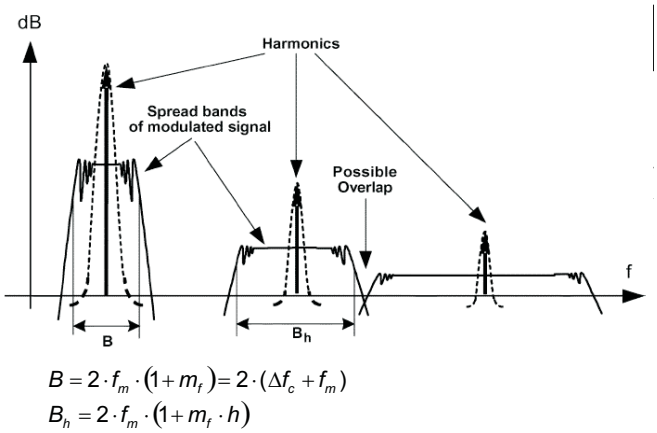


Figure 42. Spread Bands of Harmonics in Modulated Square Signals (1)

Figure 41 and Figure 42 show that after modulation the sideband harmonic is attenuated when compared to the non-modulated harmonic, and when the harmonic energy is spread into a certain frequency band. The higher the modulation index (*mf*) the larger the attenuation.

$$m_f = \frac{\delta \times f_c}{f_m} \quad (1)$$

With:

f_c is the carrier frequency (i.e. nominal switching frequency)
f_m is the modulating frequency (approx. 0.016*f_c)
δ is the modulation ratio (approx 0.1)

$$\delta = \frac{\Delta f_c}{f_c} \quad (2)$$

(1) Spectrum illustrations and formulae (Figure 41 and Figure 42) copyright IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 47, NO.3, AUGUST 2005. See REFERENCES Section for full citation.

The maximum switching frequency is limited by the process and by the parameter modulation ratio (δ), together with f_m, which is the bandwidth of the side-band harmonics around the carrier frequency f_c. The bandwidth of a frequency modulated waveform is approximately given by the Carson's rule and can be summarized as:

$$B = 2 \times f_m \times (1 + m_f) = 2 \times (\Delta f_c + f_m) \quad (3)$$

f_m < RBW: The receiver is not able to distinguish individual side-band harmonics; so, several harmonics are added in the input filter and the measured value is higher than expected in theoretical calculations.

f_m > RBW: The receiver is able to properly measure each individual side-band harmonic separately, so that the measurements match the theoretical calculations.

SOFT START

The TPS8267x has an internal soft-start circuit that limits the in-rush current during start-up. This circuit limits input voltage drop when a battery or a high-impedance power source is connected to the input of the MicroSiP™ DC/DC converter.

The soft-start system progressively increases the switching on-time from a minimum pulse-width of 35ns as a function of the output voltage. This mode of operation continues for approximately 100µs after the enable. If the output voltage does not reach its target value within the soft-start time, the soft-start transitions to a second mode of operation.

If the output voltage rises above approximately 0.5V, the converter increases the input current limit and thus enables the power supply to come up properly. The start-up time mainly depends on the capacitance present at the output node and the load current.

ENABLE

The TPS8267x device starts operation when EN is set high and starts up with the soft start as previously described. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN pin low forces the device into shutdown. In this mode, all internal circuits are turned off and the V_{IN} current reduces to the device leakage current, which is typically a few hundred nanoamps.

The TPS8267x device can actively discharge the output capacitor when it turns off. The integrated discharge resistor has a typical resistance of 100 Ω. The required time to ramp down the output voltage depends on the load current and the capacitance present at the output node.

APPLICATION INFORMATION

INPUT CAPACITOR SELECTION

Because of the pulsating input current nature of the buck converter, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interference in other circuits in the system.

For most applications, the input capacitor that is integrated into the TPS8267x should be sufficient. If the application exhibits a noisy or erratic switching frequency, experiment with additional input ceramic capacitance to find a remedy.

The TPS8267x uses a tiny ceramic input capacitor. When a ceramic capacitor is combined with trace or cable inductance, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the part. In this circumstance, additional "bulk" capacitance, such as electrolytic or tantalum, should be placed between the input of the converter and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_I.

OUTPUT CAPACITOR SELECTION

The advanced, fast-response, voltage mode, control scheme of the TPS8267x allows the use of a tiny ceramic output capacitor (C_O). For most applications, the output capacitor integrated in the TPS8267x is sufficient.

At nominal load current, the device operates in PWM mode; the overall output voltage ripple is the sum of the voltage step that is caused by the output capacitor ESL and the ripple current that flows through the output capacitor impedance. At light loads, the output capacitor limits the output ripple voltage and provides holdup during large load transitions.

The TPS8267x is designed as a Point-Of-Load (POL) regulator, to operate stand-alone without requiring any additional capacitance. Adding a 2.2µF ceramic output capacitor (X7R or X5R dielectric) generally works from a converter stability point of view, but does not necessarily help to minimize the output ripple voltage.

For best operation (i.e. optimum efficiency over the entire load current range, proper PFM/PWM auto transition), the TPS8267xSIP requires a minimum output ripple voltage in PFM mode. The typical output voltage ripple is ca. 1% of the nominal output voltage V_O. The PFM pulses are time controlled resulting in a PFM output voltage ripple and PFM frequency that depends (first order) on the capacitance seen at the MicroSiP™ DC/DC converter's output.

In applications requiring additional output bypass capacitors located close to the load, care should be taken to ensure proper operation. If the converter exhibits marginal stability or erratic switching frequency, experiment with additional low value series resistance (e.g. 50 to 100mΩ) in the output path to find a remedy.

Because the damping factor in the output path is directly related to several resistive parameters (e.g. inductor DCR, power-stage $r_{DS(on)}$, PWB DC resistance, load switches $r_{DS(on)}$ …) that are temperature dependant, the converter small and large signal behavior must be checked over the input voltage range, load current range and temperature range.

The easiest sanity test is to evaluate, directly at the converter’s output, the following aspects:

- PFM/PWM efficiency
- PFM/PWM and forced PWM load transient response

During the recovery time from a load transient, the output voltage can be monitored for settling time, overshoot or ringing that helps judge the converter’s stability. Without any ringing, the loop has usually more than 45° of phase margin.

LAYOUT CONSIDERATION

In making the pad size for the SiP LGA balls, it is recommended that the layout use non-solder-mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 43 shows the appropriate diameters for a MicroSiP™ layout.

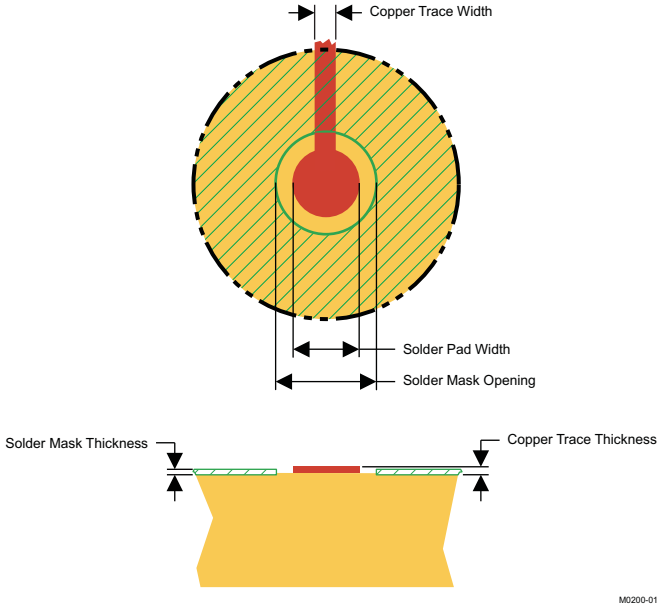


Figure 43. Recommended Land Pattern Image and Dimensions

SOLDER PAD DEFINITIONS (1)(2)(3)(4)	COPPER PAD	SOLDER MASK (5) OPENING	COPPER THICKNESS	STENCIL (6) OPENING	STENCIL THICKNESS
Non-solder-mask defined (NSMD)	0.30mm	0.360mm	1oz max (0.032mm)	0.34mm diameter	0.1mm thick

(1) Circuit traces from non-solder-mask defined PWB lands should be 75µm to 100µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and affect reliability.
(2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
(3) Recommend solder paste is Type 3 or Type 4.
(4) For a PWB using a Ni/Au surface finish, the gold thickness should be less than 0.5mm to avoid a reduction in thermal fatigue performance.
(5) Solder mask thickness should be less than 20 µm on top of the copper circuit pattern.
(6) For best solder stencil performance use laser cut stencils with electro polishing. Chemically etched stencils give inferior solder paste volume control.

SURFACE MOUNT INFORMATION

The TPS8267x MicroSiP™ DC/DC converter uses an open frame construction that is designed for a fully automated assembly process and that features a large surface area for pick and place operations. See the "Pick Area" in the package drawings.

Package height and weight have been kept to a minimum thereby to allow the MicroSiP™ device to be handled similarly to a 0805 component.

See JEDEC/IPC standard J-STD-20b for reflow recommendations.

THERMAL INFORMATION

The die temperature of the TPS8267x must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the TPS8267x.

To estimate the junction temperature, approximate the power dissipation within the TPS8267x by applying the typical efficiency stated in this datasheet to the desired output power; or, by taking a power measurement if you have an actual TPS8267x device and TPS82671EVM evaluation module. Then calculate the internal temperature rise of the TPS8267x above the surface of the printed circuit board by multiplying the TPS8267x power dissipation by the thermal resistance.

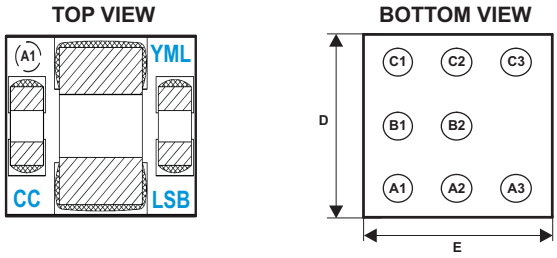
The actual thermal resistance of the TPS8267x to the printed circuit board depends on the layout of the circuit board, but the thermal resistance given in the Thermal Information Table can be used as a guide.

Three basic approaches for enhancing thermal performance are listed below:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

PACKAGE SUMMARY

SIP PACKAGE



Code:

- CC — Customer Code (device/voltage specific)
- YML — Y: Year, M: Month, L: Lot trace code
- LSB — L: Lot trace code, S: Site code, B: Board locator

MicroSiP™ DC/DC MODULE PACKAGE DIMENSIONS

The TPS8267x device is available in an 8-bump ball grid array (BGA) package. The package dimensions are:

- D = 2.30 ±0.05 mm
- E = 2.90 ±0.05 mm

REFERENCES

"EMI Reduction in Switched Power Converters Using Frequency Modulation Techniques", in *IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 4, NO. 3, AUGUST 2005, pp 569-576* by Josep Balcells, Alfonso Santolaria, Antonio Orlandi, David González, Javier Gago.

REVISION HISTORY

Note: Page numbers of current version may differ form previous versions.

Changes from Original (October 2010) to Revision A **Page**

- Added devices TPS82677 and TPS82678 to Header info 1
- Added TPS82678 to Ordering Info table and removed "Product Preview" attribute from TPS82677 2
- Changed graph for Figure 8 8
- Changed graph for Figure 11 9
- Added copyright attribution for spectrum illustrations 18

Changes from Revision A (April 2011) to Revision B **Page**

- Added TPS82676 part number to the data sheet header 1
- Deleted product preview attribute fromTPS82676 device in the Ordering Information table. 2

Changes from Revision B (August 2011) to Revision C **Page**

- Added device TPS82672 to Header info 1
- Deleted Product Preview annotation from device TPS82672 in Ordering Info table 2

Changes from Revision C (November 2011) to Revision D **Page**

- Added devices TPS82670, TPS82673, and TPS82674 to Header 1
- Changed the TPS82678SIP Package Marking From: TT To: TN in the Ordering Information table 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS82670SIPR	ACTIVE	uSiP	SIP	8	3000	TBD	Call TI	Call TI	-40 to 85	YK TXI670	Samples
TPS82670SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	YK TXI670	Samples
TPS826711SIPR	ACTIVE	uSiP	SIP	8	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	YW TXI671	Samples
TPS826711SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	YW TXI671	Samples
TPS82671SIPR	ACTIVE	uSiP	SIP	8	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	RA TXI671	Samples
TPS82671SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	RA TXI671	Samples
TPS82672SIPR	ACTIVE	uSiP	SIP	8	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	WD TXI672	Samples
TPS82672SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	WD TXI672	Samples
TPS82673SIPR	ACTIVE	uSiP	SIP	8	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	YL TXI673	Samples
TPS82673SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	YL TXI673	Samples
TPS82675SIPR	ACTIVE	uSiP	SIP	8	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	RB TXI675	Samples
TPS82675SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	RB TXI675	Samples
TPS82676SIPR	ACTIVE	uSiP	SIP	8	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	TU TXI676	Samples
TPS82676SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	TU TXI676	Samples
TPS82677SIPR	ACTIVE	uSiP	SIP	8	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	SK TXI677	Samples
TPS82677SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	SK TXI677	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

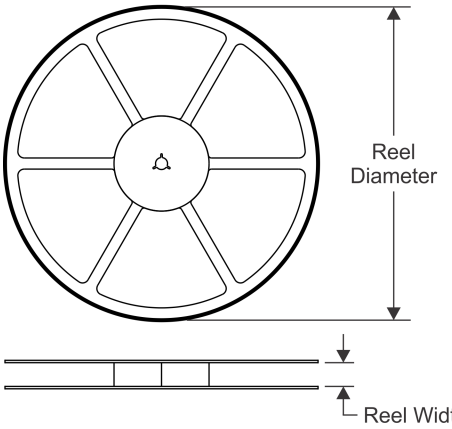
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

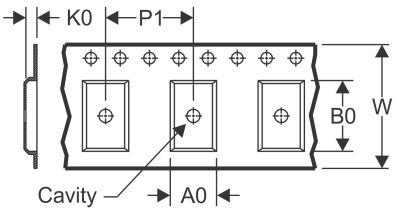
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

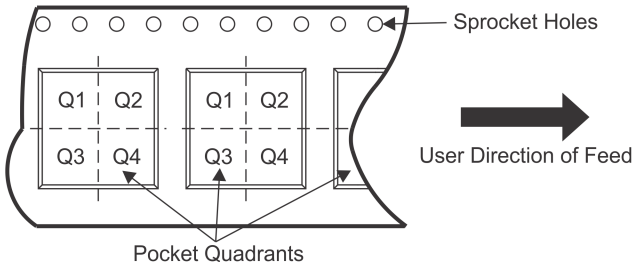


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

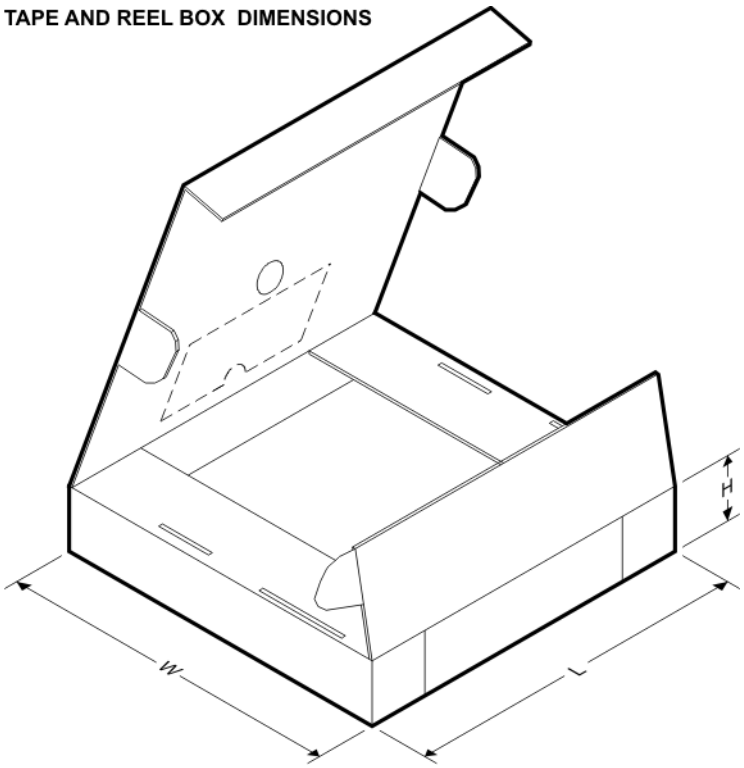
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS826711SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82671SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82672SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82673SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82675SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82676SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82677SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2

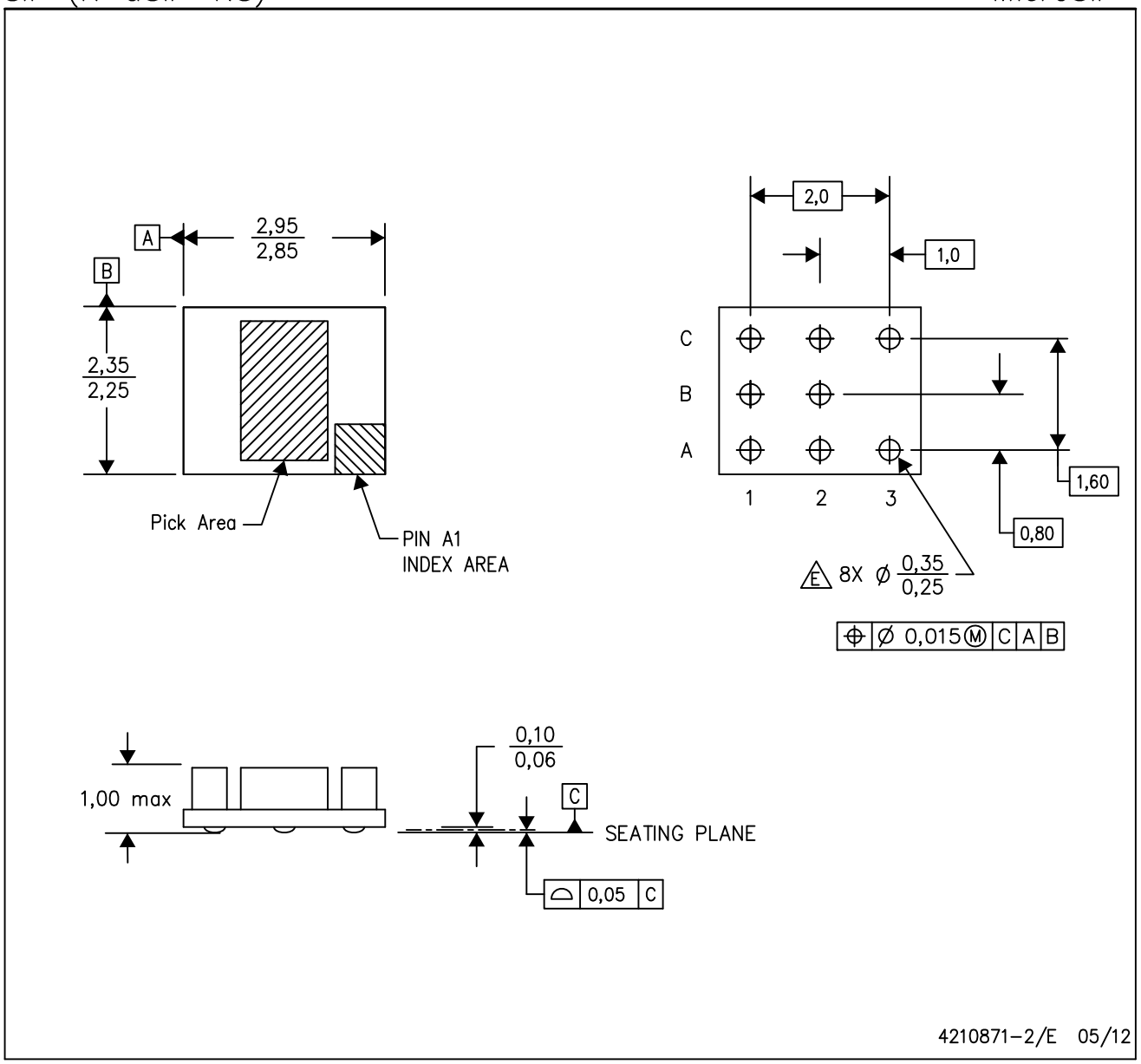
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS826711SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS82671SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS82672SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS82673SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS82675SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS82676SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS82677SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0

SIP (R–uSiP–N8) MicroSiP™



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. MicroSiP™ package configuration – Micro System in Package.
D. Reference Product Data Sheet for array population. 3 x 3 matrix pattern is shown for illustration only.
E. This package contains Pb–free balls.

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