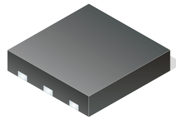


Single-Channel High-Speed Low-Side Gate Driver (with 4-A Peak Source and 8-A Peak Sink)

Check for Samples: UCC27511, UCC27512

FEATURES

- **Low-Cost Gate-Driver Device Offering Superior Replacement of NPN and PNP Discrete Solutions**
- **4-A Peak Source and 8-A Peak Sink Asymmetrical Drive**
- **Strong Sink Current Offers Enhanced Immunity Against Miller Turnon**
- **Split Output Configuration (allows easy and independent adjustment of turnon and turnoff speeds) in the UCC27511**
- **Fast Propagation Delays (13-ns typical)**
- **Fast Rise and Fall Times (9-ns and 7-ns typical)**
- **4.5 to 18-V Single Supply Range**
- **Outputs Held Low During VDD UVLO (ensures glitch-free operation at power up and power down)**
- **TTL and CMOS Compatible Input-Logic Threshold, (independent of supply voltage)**
- **Hysteretic-Logic Thresholds for High-Noise Immunity**
- **Dual-Input Design (choice of an inverting (IN- pin) or non-inverting (IN+ pin) driver configuration)**
  - **Unused Input Pin can be Used for Enable or Disable Function**
- **Output Held Low when Input Pins are Floating**
- **Input Pin Absolute Maximum Voltage Levels Not Restricted by VDD Pin Bias Supply Voltage**
- **Operating Temperature Range of –40°C to +140°C**
- **6-Pin DBV (SOT-23) and 6-Pin DRS (3mm × 3 mm WSON with exposed thermal pad) Package Options**

APPLICATIONS

- **Switch-Mode Power Supplies**
- **DC-to-DC Converters**
- **Companion Gate-Driver Devices for Digital Power Controllers**
- **Solar Power, Motor Control, UPS**
- **Gate Driver for Emerging Wide Band-Gap Power Devices (such as GaN)**

DESCRIPTION

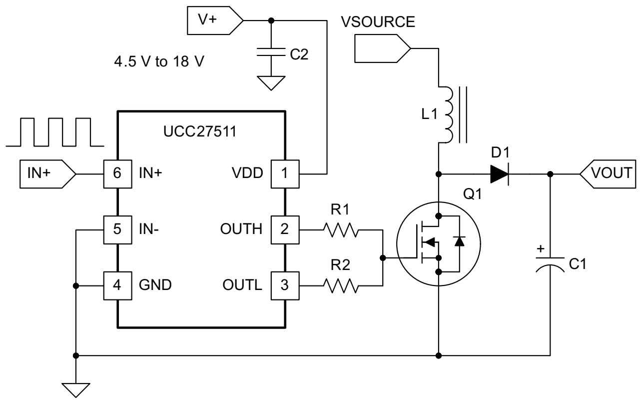
The UCC27511 and UCC27512 single-channel high-speed low-side gate-driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, UCC27511 and UCC27512 are capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay typically 13 ns.

The UCC27511 and UCC27512 provides 4-A source, 8-A sink (asymmetrical drive) peak-drive current capability. Strong sink capability in asymmetrical drive boosts immunity against parasitic, Miller turnon effect. The UCC27511 device also features a unique split output configuration where the gate-drive current is sourced through OUTH pin and sunk through OUTL pin. This unique pin arrangement allows the user to apply independent turnon and turnoff resistors to the OUTH and OUTL pins respectively and easily control the switching slew rates.

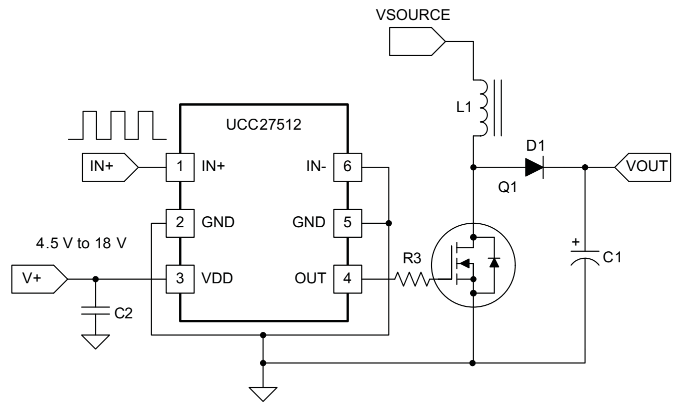
UCC27511 and UCC27512 are designed to operate over a wide VDD range of 4.5 to 18 V and wide temperature range of –40°C to +140°C. Internal Undervoltage Lockout (UVLO) circuitry on VDD pin holds output low outside VDD operating range. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging wide band-gap power-switching devices such as GaN power-semiconductor devices.

TYPICAL APPLICATION DIAGRAMS

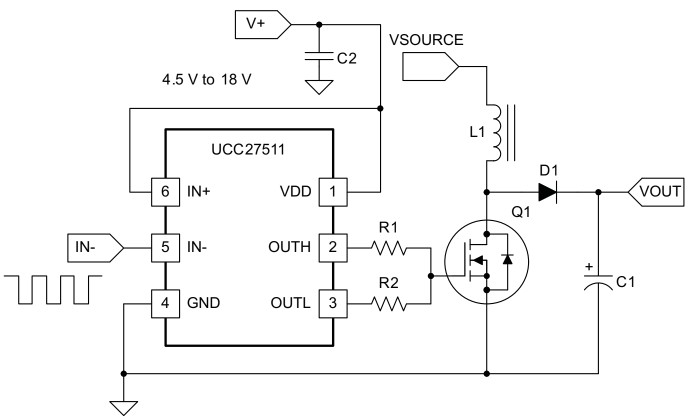
Non-Inverting Input



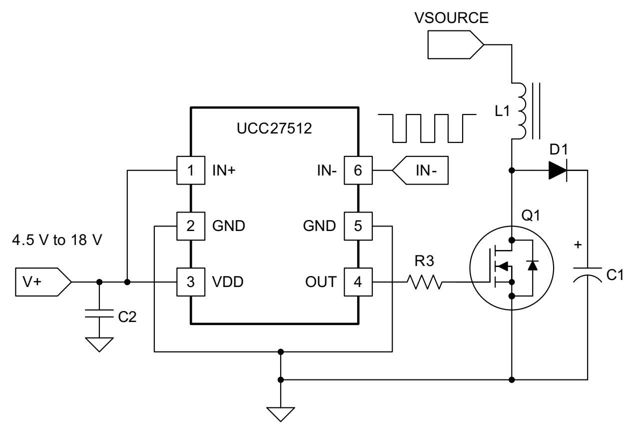
Non-Inverting Input



Inverting Input



Inverting Input



DESCRIPTION (CONTINUED)

UCC27511 features a dual-input design which offers flexibility of implementing both inverting (IN- pin) and non-inverting (IN+ pin) configuration with the same device. Either IN+ or IN- pin can be used to control the state of the driver output. The unused input pin can be used for enable and disable functions. For safety purpose, internal pullup and pulldown resistors on the input pins ensure that outputs are held low when input pins are in floating condition. Hence the unused input pin is not left floating and must be properly biased to ensure that driver output is in enabled for normal operation.

The input pin threshold of the UCC27511 device is based on TTL and CMOS-compatible low-voltage logic which is fixed and independent of the VDD supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION(1)(2)

PART NUMBER	PACKAGE	PEAK CURRENT (SOURCE/SINK)	INPUT THRESHOLD LOGIC	OPERATING TEMPERATURE RANGE, T_A
UCC27511DBV	SOT-23 6 pin	4-A/8-A (Asymmetrical Drive)	CMOS/TTL-Compatible (low voltage, independent of VDD bias voltage)	-40°C to 140°C
UCC27512DRS	3 mm x 3 mm WSON, 6 pin	4-A/8-A (Asymmetrical Drive)	CMOS/TTL-Compatible (low voltage, independent of VDD bias voltage)	

(1) For the most current package and ordering information, see Package Option Addendum at the end of this document.
(2) All packages use Pb-Free lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations. DRS package is rated MSL level 2.

Table 2. UCC2751x Product Family Summary

PART NUMBER	PACKAGE	PEAK CURRENT (SOURCE/SINK)	INPUT THRESHOLD LOGIC
UCC27511DBV	SOT-23, 6 pin	4-A/8-A (Asymmetrical Drive)	CMOS/TTL-Compatible (low voltage, independent of VDD bias voltage)
UCC27512DRS	3 mm x 3 mm WSON, 6 pin		
UCC27516DRS (1)	3 mm x 3 mm WSON, 6 pin	4-A/4-A (Symmetrical Drive)	
UCC27517DBV (1)	SOT-23, 5 pin		
UCC27518DBV (1)	SOT-23, 5 pin		CMOS (follows VDD bias voltage)
UCC27519DBV (1)	SOT-23, 5 pin		

(1) Visit www.ti.com for the latest product datasheet.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range	VDD	-0.3	20	V
OUTH voltage, (UCC27511)		-0.3	VDD + 0.3	
OUTL voltage, (UCC27511)	DC	-0.3	20	
	Repetitive pulse less than 200 ns(4)	-2	20	
OUT voltage, (UCC27512)	DC	-0.3	VDD + 0.3	
	Repetitive pulse less than 200 ns(4)	-2	VDD + 0.3	
Output continuous current (OUTH source current and OUTL sink current)	I_{OUT_DC} (source)		0.3	A
	I_{OUT_DC} (sink)		0.6	
Output pulsed current (0.5 µs) (OUTH source current and OUTL sink current)	I_{OUT_pulsed}(source)		4	
	I_{OUT_pulsed}(sink)		8	
IN+, IN-(5)		-0.3	20	V
ESD	Human Body Model, HBM		4000	
	Charged Device Model, CDM		1000	
Operating virtual junction temperature range, T_J		-40	150	°C
Storage temperature range, T_{STG}		-65	150	
Lead temperature	Soldering, 10 sec.		300	
	Reflow		260	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into and negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
(4) Values are verified by characterization on bench.
(5) Maximum voltage on input pins is not restricted by the voltage on the VDD pin.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, VDD	4.5	12	18	V
Operating junction temperature range	-40		140	°C
Input voltage, IN+ and IN-	0		18	V

THERMAL INFORMATION

THERMAL METRIC		UCC27511	UCC27512	UNITS
		SOT-23 (DBV)	[(1)]WSON	
		6 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance[(2)]	217.8	85.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[(3)]	97.6	100.1	
θ_{JB}	Junction-to-board thermal resistance[(4)]	72.2	58.6	
ψ_{JT}	Junction-to-top characterization parameter[(5)]	8.6	7.5	
ψ_{JB}	Junction-to-board characterization parameter[(6)]	71.6	58.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[(7)]	n/a	23.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

NOTE

Under identical power dissipation conditions, the DRS package will allow to maintain a lower die temperature than the DBV. θ_{JA} metric should be used for comparison of power dissipation capability between different packages (Refer to the APPLICATION INFORMATION Section).

ELECTRICAL CHARACTERISTICS

VDD = 12 V, T_A = T_J = -40°C to 140°C, 1-µF capacitor from VDD to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNITS
BIAS Currents							
$I_{DD(off)}$	Startup current	VDD = 3.4 V	IN+ = VDD, IN- = GND	40	100	160	µA
			IN+ = IN- = GND or IN+ = IN- = VDD	25	75	145	
			IN+ = GND, IN- = VDD	20	60	115	
Under Voltage Lockout (UVLO)							
V_{ON}	Supply start threshold	T_A = 25°C		3.91	4.20	4.5	V
		T_A = -40°C to 140°C		3.70	4.20	4.65	
V_{OFF}	Minimum operating voltage after supply start			3.45	3.9	4.35	
V_{DD_H}	Supply voltage hysteresis			0.2	0.3	0.5	
Inputs (IN+, IN-)							
V_{IN_H}	Input signal high threshold	Output high for IN+ pin, Output low for IN- pin			2.2	2.4	V
V_{IN_L}	Input signal low threshold	Output low for IN+ pin, Output high for IN- pin		1.0	1.2		
V_{IN_HYS}	Input signal hysteresis				1.0		
Source/Sink Current							
$I_{SRC/SNK}$	Source/sink peak current(1)	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz			-4/+8		A
Outputs (OUTH, OUTL, OUT)							
V_{DD}-V_{OH}	High output voltage	VDD = 12 V I_{OUTH} = -10 mA			50	90	mV
		VDD = 4.5 V I_{OUTH} = -10 mA			60	130	
V_{OL}	Low output voltage	VDD = 12 I_{OUTL} = 10 mA			5	6.5	
		VDD = 4.5 V I_{OUTL} = 10 mA			5.5	10	
R_{OH}	Output pull-up resistance(2)	VDD = 12 V I_{OUTH} = -10 mA			5.0	7.5	Ω
		VDD = 4.5 V I_{OUTH} = -10 mA			5.0	11.0	
R_{OL}	Output pull-down resistance	VDD = 12 V I_{OUTL} = 10 mA			0.375	0.650	
		VDD = 4.5 V I_{OUTL} = 10 mA			0.45	0.750	

(1) Ensured by Design.
(2) R_{OH} represents on-resistance of P-Channel MOSFET in pull-up structure of the UCC27511 and UCC27512's output stage.

ELECTRICAL CHARACTERISTICS (continued)

VDD = 12 V, T_A = T_J = -40°C to 140°C, 1-µF capacitor from VDD to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Switching Time						
t_R	Rise time(3)	VDD = 12 V C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together		8	12	ns
		VDD = 4.5 V C_{LOAD} = 1.8 nF		16	22	
t_F	Fall time(3)	VDD = 12 V C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together		7	11	
		VDD=4.5V C_{LOAD} = 1.8 nF		7	11	
t_{D1}	IN+ to output propagation delay(3)	VDD = 12 V 5-V input pulse C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together	4	13	23	
		VDD = 4.5 V 5-V input pulse C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together	4	15	26	
t_{D2}	IN- to output propagation delay(3)	VDD = 12 V C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together	4	13	23	
		VDD = 4.5 V C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together	4	19	30	

(3) See timing diagrams in Figure 1, Figure 2, Figure 3 and Figure 4.

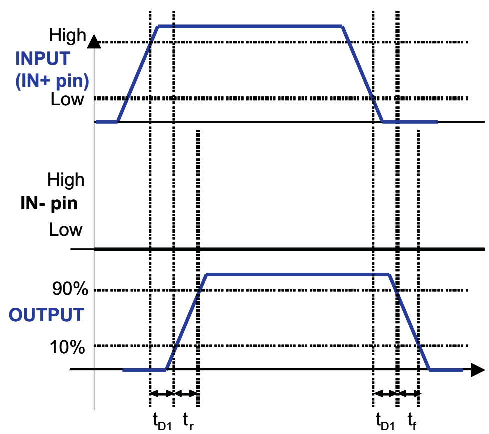


Figure 1. Non-Inverting Configuration (PWM Input To IN+ pin (IN- Pin Tied To GND), Output Represents OUTH And OUTL Pins Tied Together In The UCC27511)

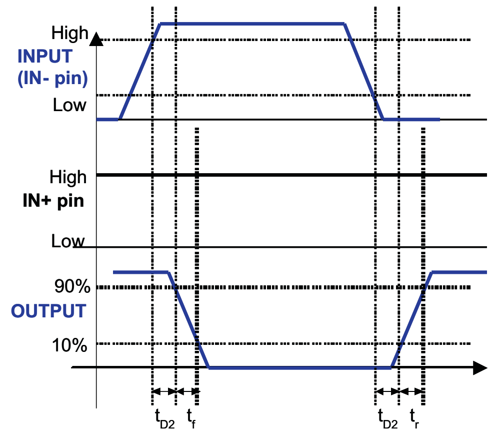


Figure 2. Inverting Configuration (PWM Input to IN- Pin (IN+ Pin Tied To VDD), Output Represents OUTH And OUTL Pins Tied Together In The UCC27511)

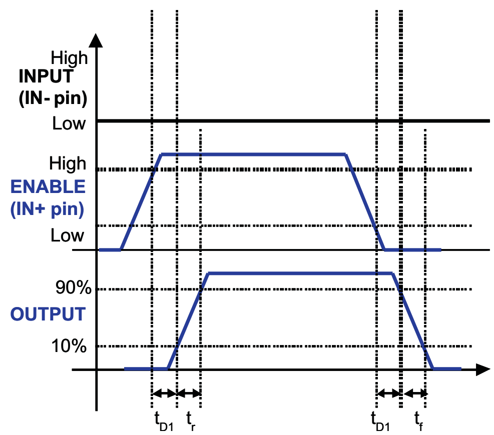


Figure 3. Enable And Disable Function Using IN+ Pin (Enable And Disable Signal Applied To IN+ Pin, PWM Input To IN- Pin, Output Represents OUTH And OUTL Pins Tied Together In The UCC27511)

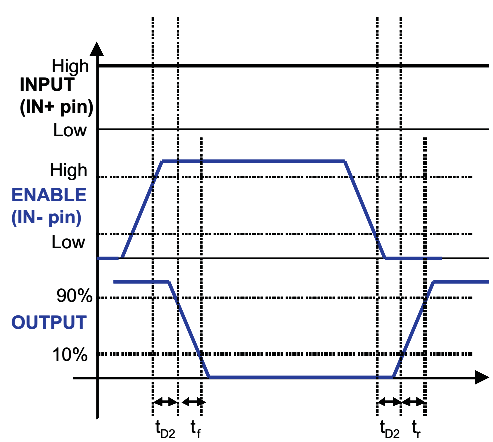
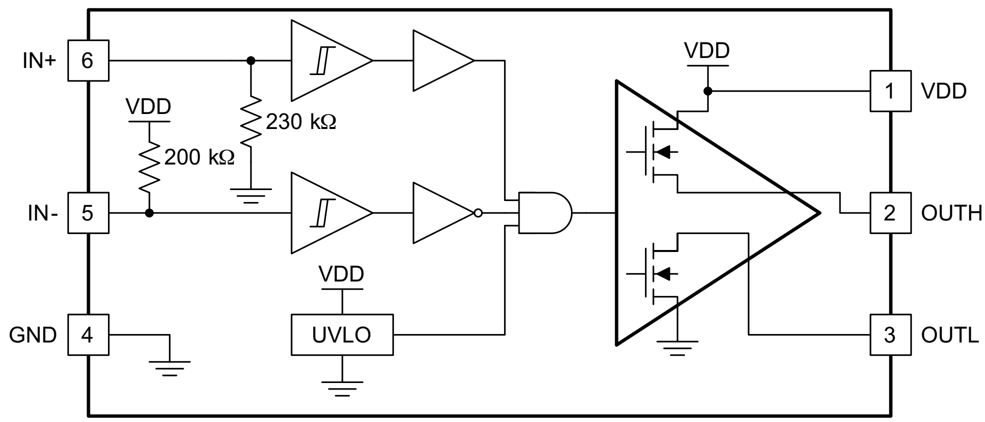


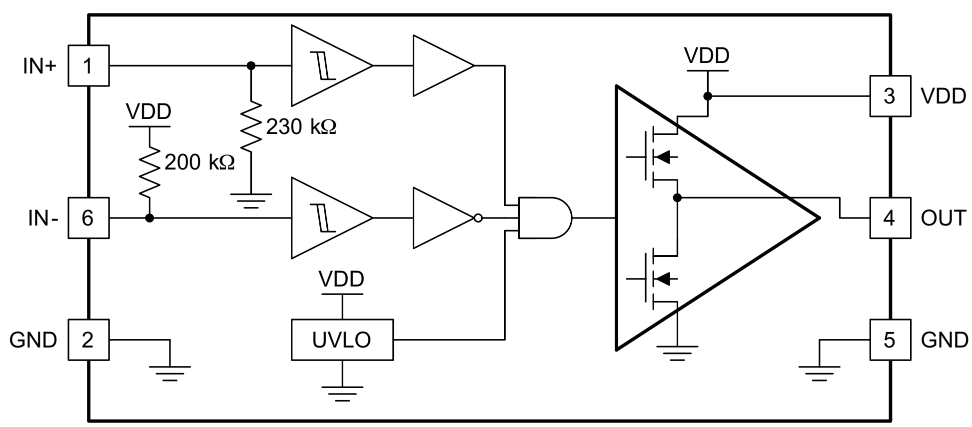
Figure 4. Enable And Disable Function Using IN- Pin (Enable And Disable Signal Applied To IN- Pin, PWM Input To IN+ Pin, Output Represents OUTH And OUTL Pins Tied Together In The UCC27511)

DEVICE INFORMATION

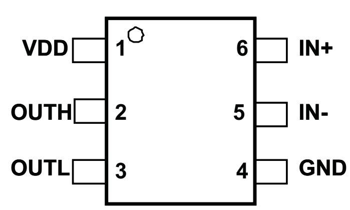
UCC27511 Functional Block Diagram



UCC27512 Functional Block Diagram



SOT-23 DBV
(Top View)



DRS Package
(Top View)

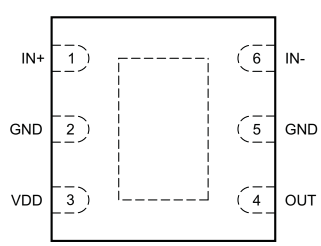


Table 3. UCC27511 TERMINAL FUNCTIONS

TERMINAL		I/O	FUNCTION
PIN NUMBER	NAME		
1	VDD	I	**Bias supply input.**
2	OUTH	O	**Sourcing current output of driver**. Connect resistor between OUTH and Gate of power-switching device to adjust turnon speed.
3	OUTL	O	**Sinking current output of driver.** Connect resistor between OUTL and Gate of power-switching device to adjust turnoff speed.
4	GND	-	**Ground:** All signals referenced to this pin.
5	IN-	I	**Inverting input:** When the driver is used in non-inverting configuration, connect IN- to GND in order to enable output, OUT held LOW if IN- is unbiased or floating
6	IN+	I	**Non-inverting input:** When the driver is used in inverting configuration, connect IN+ to VDD in order to enable output, OUT held LOW if IN+ is unbiased or floating

Table 4. UCC27512 TERMINAL FUNCTIONS

TERMINAL		I/O	FUNCTION
PIN NUMBER	NAME		
1	IN+	I	**Non-inverting input:** When the driver is used in inverting configuration, connect IN+ to VDD in order to enable output, OUT held LOW if IN+ is unbiased or floating.
2, 5	GND	-	**Ground:** All signals referenced to this pin. TI recommends to connect pin 2 and pin 5 on PCB as close to the device as possible.
3	VDD	I	**Bias supply input.**
4	OUT	O	**Sourcing/sinking current output of driver.**
6	IN-	I	**Inverting input:** When the driver is used in non-inverting configuration, connect IN- to GND in order to enable output, OUT held LOW if IN- is unbiased or floating.

Table 5. Device Logic Table

IN+ PIN	IN- PIN	OUTH PIN	OUTL PIN	OUT (OUTH and OUTL pins tied together in the UCC27511)
L	L	High impedance	L	L
L	H	High impedance	L	L
H	L	H	High impedance	H
H	H	High impedance	L	L
x(1)	Any	High impedance	L	L
Any	x(1)	High impedance	L	L

(1) x = Floating Condition

TYPICAL CHARACTERISTICS

START-UP CURRENT vs TEMPERATURE

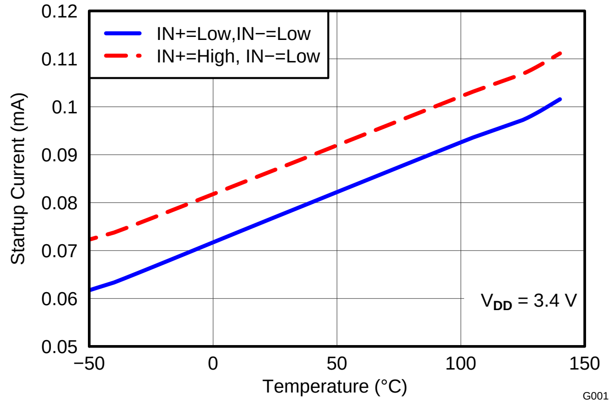


Figure 5.

OPERATING SUPPLY CURRENT vs TEMPERATURE (Output Switching)

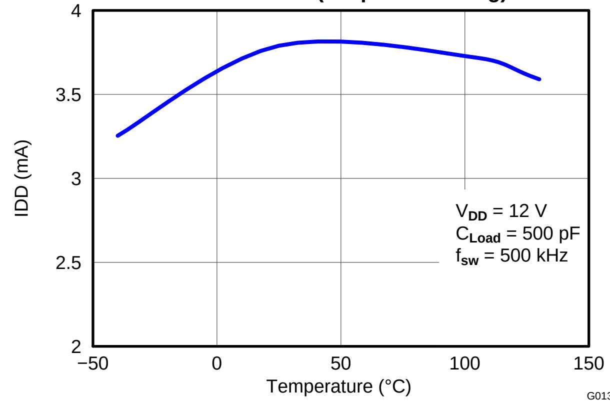


Figure 6.

SUPPLY CURRENT vs TEMPERATURE (Output in DC On/Off condition)

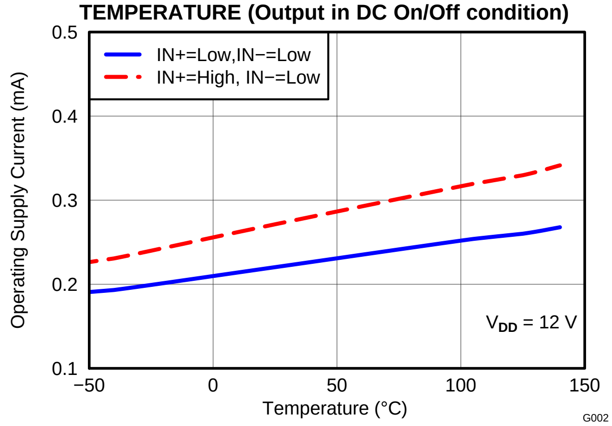


Figure 7.

UVLO THRESHOLD VOLTAGE vs TEMPERATURE

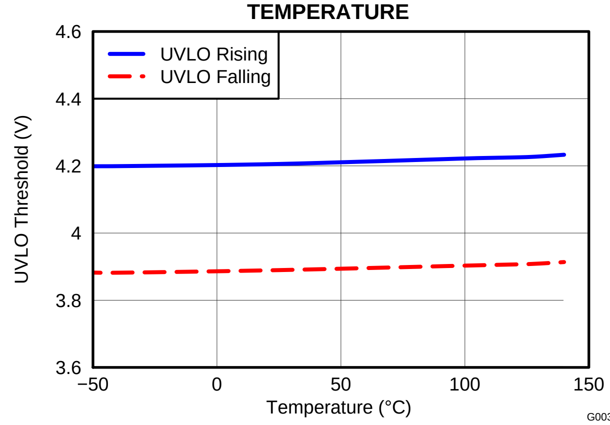


Figure 8.

INPUT THRESHOLD vs TEMPERATURE

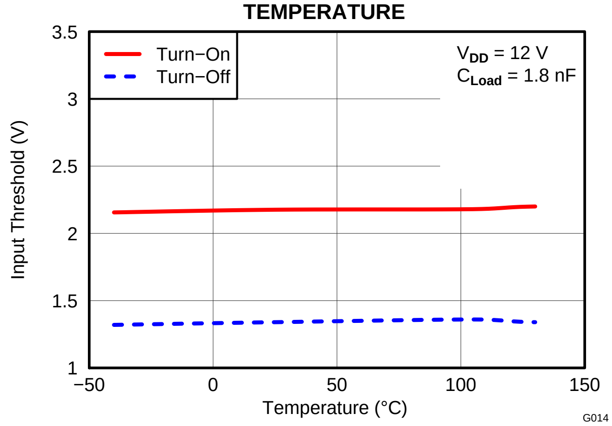


Figure 9.

OUTPUT PULL-UP RESISTANCE vs TEMPERATURE

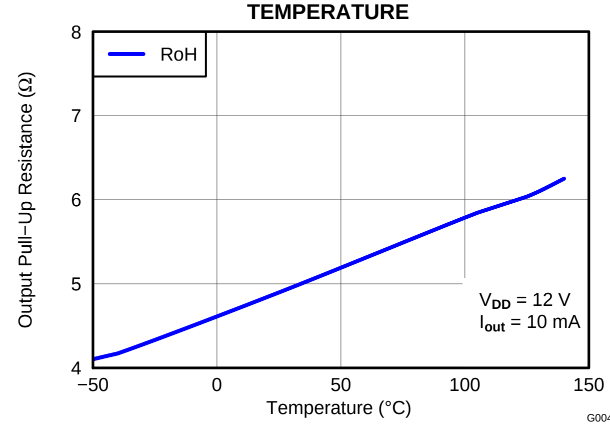


Figure 10.

TYPICAL CHARACTERISTICS (continued)

OUTPUT PULL-DOWN RESISTANCE vs TEMPERATURE

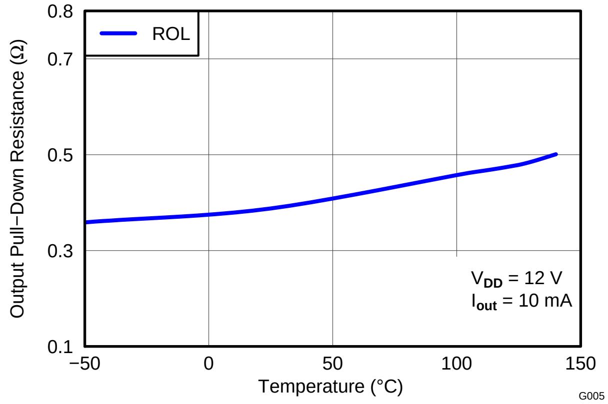


Figure 11.

RISE TIME vs TEMPERATURE

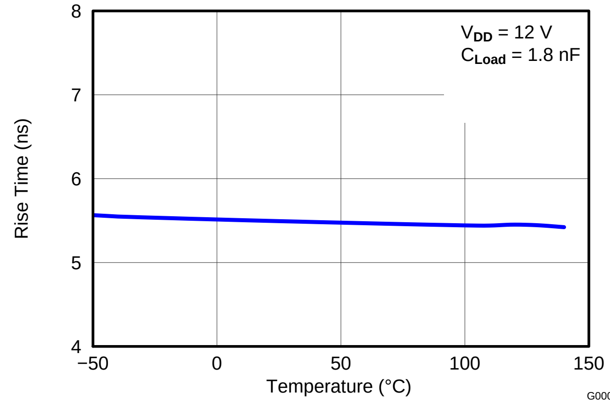


Figure 12.

FALL TIME vs TEMPERATURE

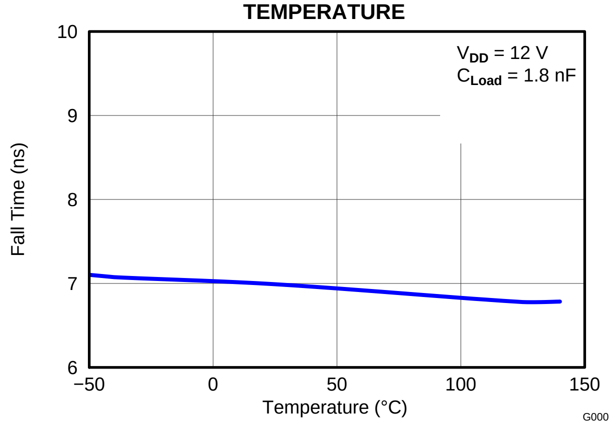


Figure 13.

INPUT TO OUTPUT PROPAGATION DELAY vs TEMPERATURE

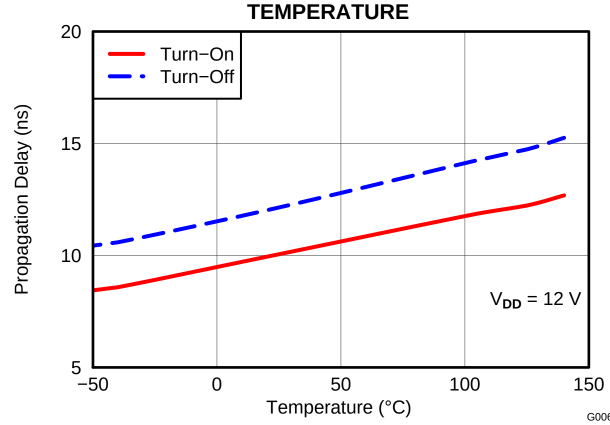


Figure 14.

OPERATING SUPPLY CURRENT vs FREQUENCY

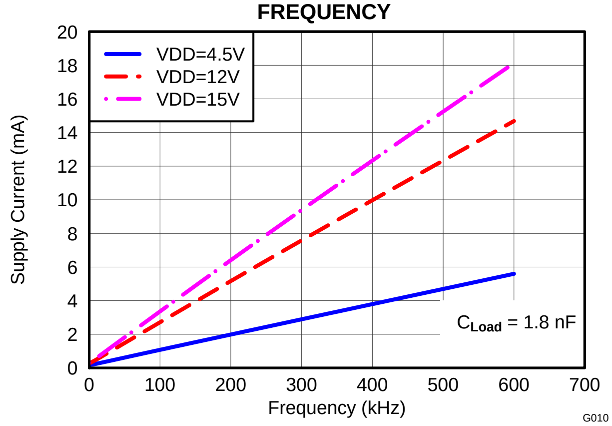


Figure 15.

PROPAGATION DELAYS vs SUPPLY VOLTAGE

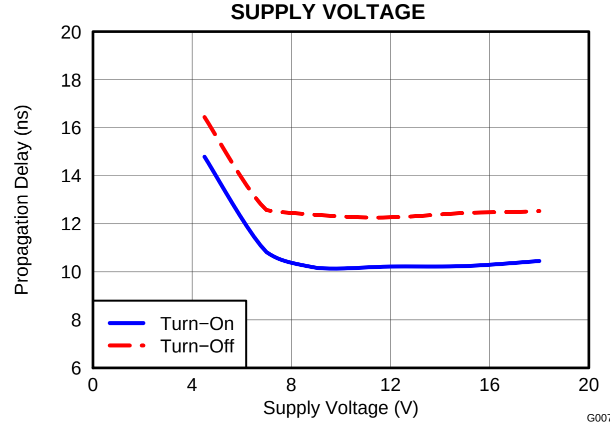


Figure 16.

TYPICAL CHARACTERISTICS (continued)

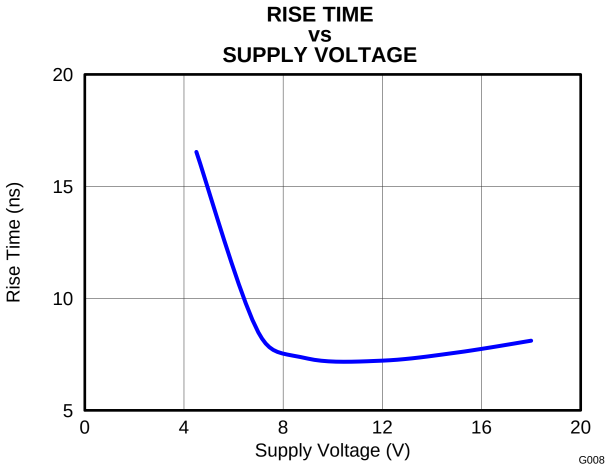


Figure 17.

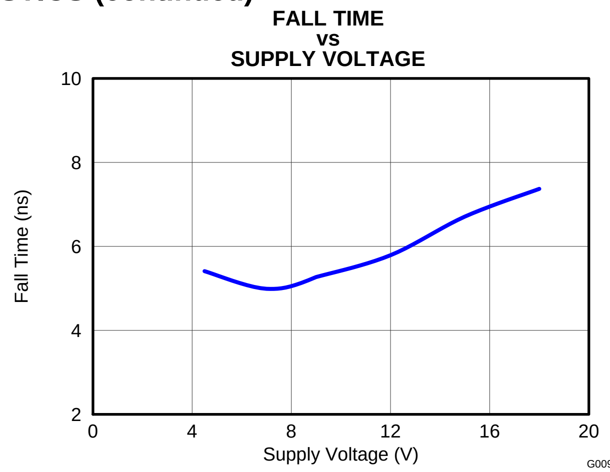


Figure 18.

APPLICATION INFORMATION

Introduction

High-current gate-driver devices are required in switching-power applications for a variety of reasons. In order to effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver employs between the PWM output of controllers and the gates of the power-semiconductor devices. Further, gate drivers are indispensable when having the PWM controller directly drive the gates of the switching devices is impossible. With advent of digital power, this situation will be often encountered since the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power since they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself. Finally, emerging wide band-gap power device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. In summary gate-driver devices are extremely important components in switching power combining benefits of high-performance low-cost component count and board-space reduction and simplified system design.

UCC2751x Product Family

The UCC2751x family of gate-driver products (Table 6) represent Texas Instruments' latest generation of single-channel low-side high-speed gate-driver devices featuring high-source/sink current capability, industry best-in-class switching characteristics and a host of other features (Table 7) all of which combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

Table 6. UCC2751x Product Family Summary

PART NUMBER	PACKAGE	PEAK CURRENT (SOURCE/SINK)	INPUT THRESHOLD LOGIC
UCC27511DBV	SOT-23, 6 pin	4-A/8-A (Asymmetrical Drive)	CMOS/TTL-Compatible (low voltage, independent of VDD bias voltage)
UCC27512DRS	3 mm x 3 mm WSON, 6 pin		
UCC27516DRS (1)	3 mm x 3 mm WSON, 6 pin	4-A/4-A (Symmetrical Drive)	
UCC27517DBV (1)	SOT-23, 5 pin		
UCC27518DBV (1)	SOT-23, 5 pin		CMOS (follows VDD bias voltage)
UCC27519DBV (1)	SOT-23, 5 pin		

(1) Visit www.ti.com for the latest product datasheet.

Table 7. UCC2751x Features and Benefits

FEATURE	BENEFIT
High Source and Sink Current Capability 4 A and 8 A (Asymmetrical) – UCC27511 and UCC27512 4 A and 4 A (Symmetrical) – UCC27511 and UCC27512	High current capability offers flexibility in employing UCC2751x family of devices to drive a variety of power switching devices at varying speeds
Best-in-class 13-ns (typ) Propagation delay	Extremely low pulse-transmission distortion
Expanded VDD Operating range of 4.5 V to 18 V	Flexibility in system design Low VDD operation ensures compatibility with emerging wide band-gap power devices such as GaN
Expanded Operating Temperature range of -40°C to 140°C (See ELECTRICAL CHARACTERISTICS table)	
VDD UVLO Protection	Outputs are held low in UVLO condition, which ensures predictable glitch-free operation at power up and power down
Outputs held low when input pins (INx) in floating condition	Safety feature, especially useful in passing abnormal condition tests during safety certification
Ability of input pins (and enable pin in UCC27518/9) to handle voltage levels not restricted by VDD pin bias voltage	System simplification, especially related to auxiliary bias supply architecture
Split output structure in UCC27511 and UCC27512 (OUTH, OUTL)	Allows independent optimization of turnon and turnoff speeds
Strong sink current (8 A) and low pulldown impedance (0.375 Ω) in UCC27511 and UCC27512	High immunity to C x dV/dt Miller turnon events
CMOS/TTL compatible input-threshold logic with wide hysteresis in UCC27511, UCC27512, UCC27516 and UCC27517	Enhanced noise immunity, while retaining compatibility with microcontroller logic-level input signals (3.3 V, 5 V) optimized for digital power
CMOS input threshold logic in UCC27518/9 (VIN_H – 70% VDD, VIN_L – 30% VDD)	Well suited for slow input-voltage signals, with flexibility to program delay circuits (RCD)

Typical Application Diagram

Typical application diagrams of UCC27511 and UCC27512 devices are shown below illustrating use in non-inverting and inverting driver configurations. The UCC27511 device features a unique split output configuration where the gate-drive current is sourced through OUTH pin and sunk through OUTL pin. This unique pin arrangement allows user to apply independent turn-on and turn-off resistors to the OUTH and OUTL pins respectively and easily control the turn-on and turn-off switching dV/dt. This pin arrangement, along with the low pulldown impedance of the output driver stage, is especially handy in applications where a high C x dV/dt Miller turnon immunity is needed (such as with GaN power switches, SR MOSFETs etc) and OUTL pin can be directly tied to the gate of the power device.

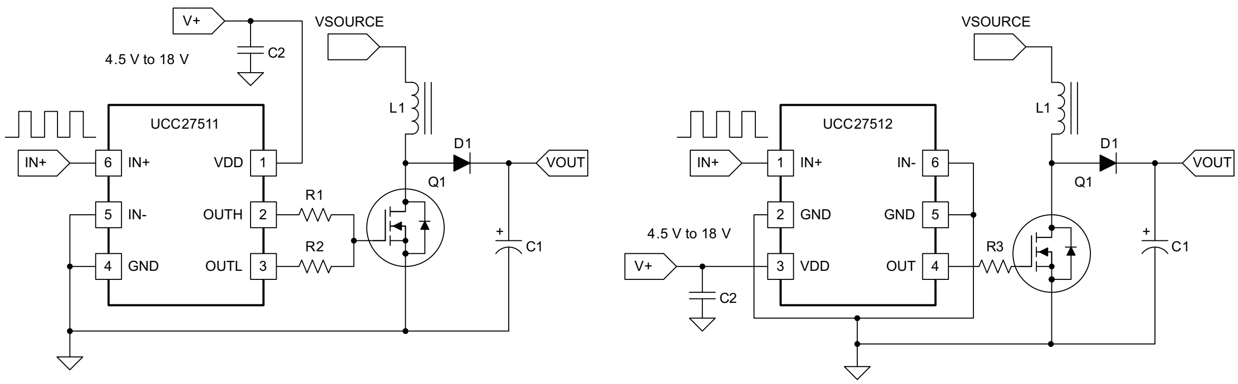


Figure 19. Using Non-Inverting Input (IN- Is Grounded To Enable Output)

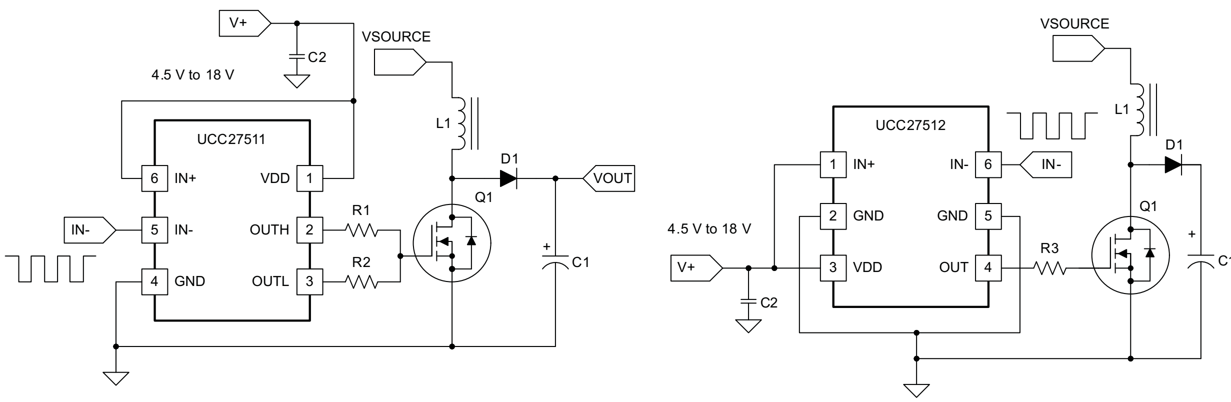


Figure 20. Using Inverting Input (IN+ Is Tied To VDD Enable Output)

NOTE

The UCC27516 features two ground pins, pin 2 and pin 5. TI recommends to tie both pins together using PCB trace as close as possible to the device.

VDD and Undervoltage Lockout

The UCC2751X devices have internal Undervoltage LockOut (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition (for example when V_{DD} voltage less than V_{ON} during power up and when V_{DD} voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300-mV typical hysteresis. This hysteresis prevents chatter when low V_{DD} supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide band-gap power-semiconductor devices.

For example, at power up, the UCC2751X driver output remains LOW until the V_{DD} voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. In the non-inverting operation (PWM signal applied to IN+ pin) shown in Figure 21, the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. In the inverting operation (PWM signal applied to IN- pin) shown in Figure 22 the output remains LOW until the UVLO threshold is reached, and then the output is out-phase with the input. In both cases, the unused input pin must be properly biased to enable the output. Note that in these devices the output turns to high state only if IN+ pin is high and IN- pin is low after the UVLO threshold is reached.

Since the driver draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD-bypass capacitors are recommended to prevent noise problems. The use of surface-mount components is highly recommended. A 0.1-µF ceramic capacitor should be located as close as possible to the VDD to GND pins of the gate driver. In addition, a larger capacitor (such as 1 µF) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

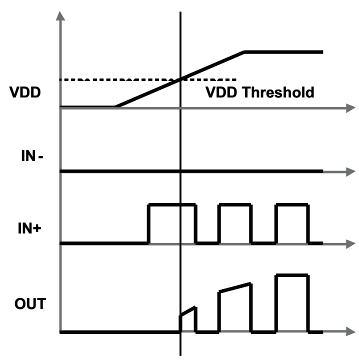


Figure 21. Power-Up (Non-Inverting Drive)

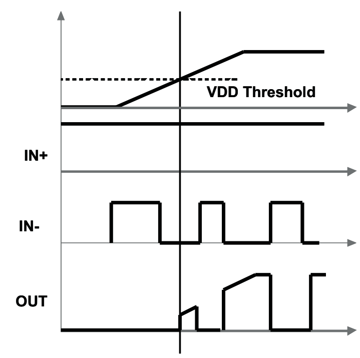


Figure 22. Power-Up (Inverting Drive)

Operating Supply Current

The UCC27511 and UCC27512 feature very low quiescent I_{DD} currents. The typical operating-supply current in Undervoltage LockOut (UVLO) state and fully-on state (under static and switching conditions) are summarized in Figure 5, Figure 6 and Figure 7. The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, refer Figure 7) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current due to switching, and finally any current related to pullup resistors on the unused input pin. For example, when the inverting input pin is pulled low additional current is drawn from VDD supply through the pullup resistors (refer to DEVICE INFORMATION for the device Block Diagram). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

A complete characterization of the IDD current as a function of switching frequency at different VDD bias voltages under 1.8-nF switching load is provided in Figure 15. The strikingly linear variation and close correlation with theoretical value of average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to its high-speed characteristics.

Input Stage

The input pins of the UCC27511 and UCC27512 devices are based on a TTL/CMOS compatible input-threshold logic that is independent of the VDD supply voltage. With typically high threshold = 2.2 V and typically low threshold = 1.2 V, the logic-level thresholds can be conveniently driven with PWM control signals derived from 3.3-V and 5-V digital-power controllers. Wider hysteresis (typ 1 V) offers enhanced noise immunity compared to traditional TTL-logic implementations, where the hysteresis is typically less than 0.5 V. These devices also feature tight control of the input-pin threshold-voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance on these pins reduces loading and increases switching speed.

The device features an important safety function wherein, whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This is achieved using VDD-pullup resistors on all the inverting inputs (IN- pin) or GND-pulldown resistors on all the non-inverting input pins (IN+ pin), (refer to DEVICE INFORMATION for the device Block Diagram).

The device also features a dual-input configuration with two input pins available to control the state of the output. The user has the flexibility to drive the device using either a non-inverting input pin (IN+) or an inverting input pin (IN-). The state of the output pin is dependent on the bias on both the IN+ and IN- pins. Refer to the input/output logic truth table (Table 5) and the Typical Application Diagrams, (Figure 19 and Figure 20), for additional clarification.

When an input pin has been chosen for PWM drive, the other input pin (the *unused* input pin) must be properly biased in order to enable the output. As mentioned earlier, the *unused* input pin cannot remain in a floating condition because whenever any input pin is left in a floating condition the output is disabled for safety purposes. Alternatively, the *unused* input pin can effectively be used to implement an enable/disable function, as explained below.

- In order to drive the device in a non-inverting configuration, apply the PWM-control input signal to IN+ pin. In this case, the *unused* input pin, IN-, must be biased low (such as tied to GND) in order to enable the output.
  - Alternately, the IN- pin is used to implement the enable/disable function using an external logic signal. OUT is disabled when IN- is biased high and OUT is enabled when IN- is biased low.
- In order to drive the device in an inverting configuration, apply the PWM-control input signal to IN- pin. In this case, the *unused* input pin, IN+, must be biased high (such as tied to VDD) in order to enable the output.
  - Alternately, the IN+ pin is used to implement the enable/disable function using an external logic signal. OUT is disabled when IN+ is biased low and OUT is enabled when IN+ is biased high.
- Finally, note that the output pin can be driven into a high state ONLY when IN+ pin is biased high and IN- input is biased low.

The input stage of the driver is preferably driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a mechanical socket or PCB layout is not optimal:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. The differential voltage between input pins and GND is modified and triggers an unintended change of output state because of fast 13-ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage.
- 1-V input-threshold hysteresis boosts noise immunity compared to most other industry standard drivers.
- In the worst case, when a slow input signal is used and PCB layout is not optimal, adding a small capacitor (1 nF) between input pin and ground very close to the driver device may be necessary which helps to convert the differential mode noise with respect to the input-logic circuitry into common-mode noise and avoid unintended change of output state.

If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate-driver device package and transferring it into the external resistor.

Enable Function

As mentioned earlier, an enable/disable function is easily implemented in UCC27511 and UCC27512 using the *unused* input pin. When IN+ is pulled down to GND or IN- is pulled down to VDD, the output is disabled. Thus IN+ pin can be used like an enable pin that is based on active-high logic, while IN- can be used like an enable pin that is based on active-low logic.

Output Stage

The output stage of the UCC27511 and UCC27512 devices are illustrated in Figure 23. OUTH and OUTL are internally connected and pinned out as OUT pin in the UCC27512 . The UCC27511 and UCC27512 devices feature a unique architecture on the output stage which delivers the highest peak-source current when it is most needed during the Miller plateau region of the power switch turnon transition (when the power switch drain/collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate-driver device is able to deliver a brief boost in the peak-sourcing current enabling fast turn on.

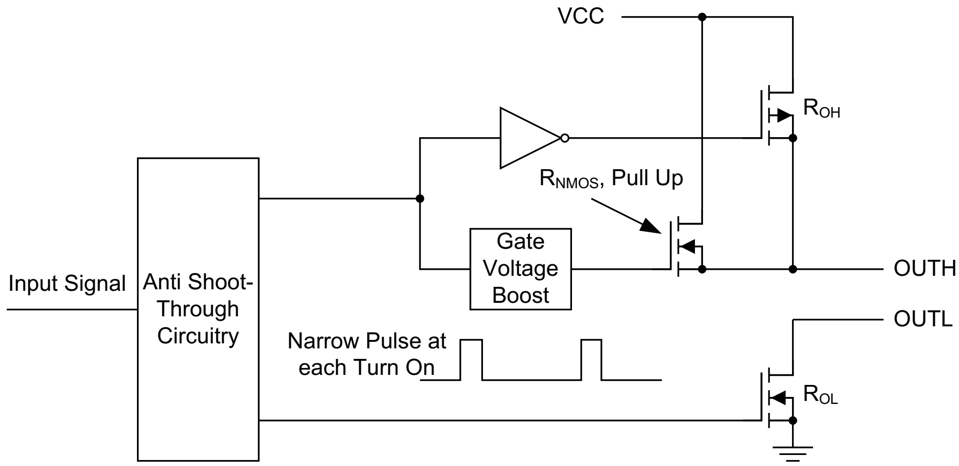


Figure 23. UCC2751X Gate Driver Output Structure

The R_{OH} parameter (see ELECTRICAL CHARACTERISTICS) is a DC measurement and it is representative of the on-resistance of the P-Channel device only, since the N-Channel device is turned on only during output change of state from low to high. Thus the effective resistance of the hybrid pullup stage is much lower than what is represented by R_{OH} parameter. The pulldown structure is composed of a N-Channel MOSFET only. The R_{OL} parameter (see ELECTRICAL CHARACTERISTICS), which is also a DC measurement, is representative of true impedance of the pull-down stage in the device. In UCC27511 and UCC27512, the effective resistance of the hybrid pullup structure is approximately 2.7 x R_{OL}.

The UCC27511 and UCC27512 are capable of delivering 4-A source, 8-A sink (asymmetrical drive) at VDD = 12 V. Strong sink capability in asymmetrical drive results in a very low pulldown impedance in the driver output stage which boosts immunity against parasitic, Miller turnon (C x dV/dt turn on) effect, especially where low gate-charge MOSFETs or emerging wide band-gap GaN-power switches are used.

An example of a situation where Miller turnon is a concern is synchronous rectification (SR). In SR application, the dV/dt occurs on MOSFET drain when the MOSFET is already held in off state by the gate driver. The current discharging the C_{GD} Miller capacitance during this dV/dt is shunted by the pulldown stage of the driver. If the pulldown impedance is not low enough then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turnon. This phenomenon is illustrated in Figure 24. UCC27511 and UCC27512 offers a best-in-class, 0.375-Ω (typ) pulldown impedance boosting immunity against Miller turnon.

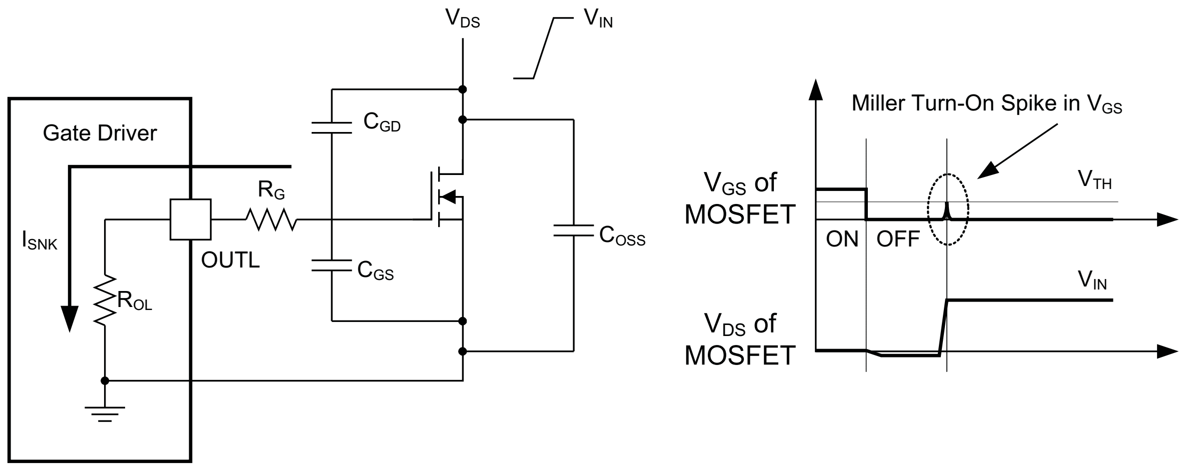


Figure 24. Very Low Pull-Down Impedance In UCC27511, 4-A/8-A Asymmetrical Drive (Output Stage Mitigates Miller Turnon Effect)

Figure 25 and Figure 26 illustrate typical switching characteristics of UCC27511.

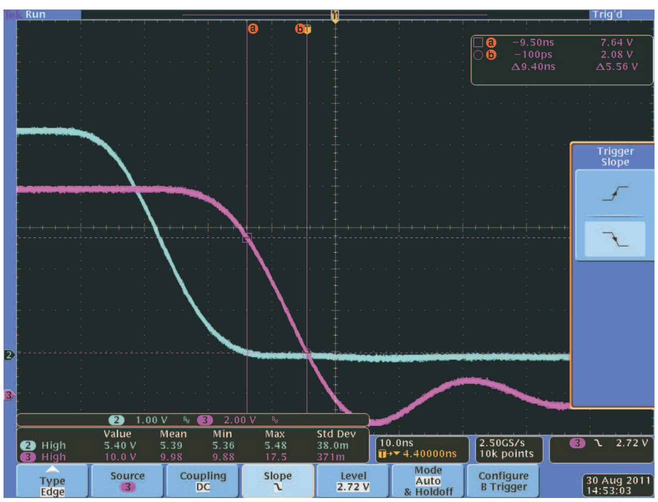


Figure 25. Typical Turnon Waveform (VDD = 10 V, C_L = 1 nF)

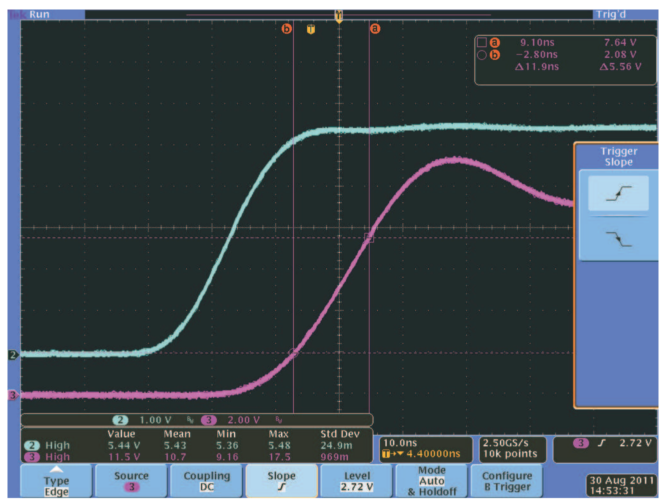


Figure 26. Typical Turnoff Waveform (VDD = 10 V, C_L = 1 nF)

The driver-output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low dropout. The presence of the MOSFET-body diodes also offers low impedance to switching overshoots and undershoots. In many cases, external Schottky diode clamps are eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

Power Dissipation

Power dissipation of the gate driver has two portions as shown in Equation 1.

$$P_{DISS} = P_{DC} + P_{SW} \tag{1}$$

The DC portion of the power dissipation is $P_{DC} = I_Q$ x VDD where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through etc). The UCC27511 and UCC27512 features very low quiescent currents (less than 1 mA, refer Figure 7) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible.

The power dissipated in the gate-driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out).
- Switching frequency.
- Use of external gate resistors.

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 2.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

Where

- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver (2)

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by Equation 3.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW}$$

where

- f_{SW} is the switching frequency (3)

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, determine the power that must be dissipated when charging a capacitor which is calculated using the equation, $Q_G = C_{LOAD}$ x V_{DD}, to provide Equation 4 for power.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \tag{4}$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated in Equation 5.

$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right)$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pull-up structure) = 2.7 x R_{OL} (5)

Low Propagation Delays

The UCC27511 and UCC27512 driver devices feature best-in-class input-to-output propagation delay of 13 ns (typ) at VDD = 12 V, which promises the lowest level of pulse transmission distortion available from industry-standard gate-driver devices for high-frequency switching applications. As seen in Figure 14, there is very little variation of the propagation delay with temperature and supply voltage as well, offering typically less than 20-ns propagation delays across the entire range of application conditions.

Thermal Information

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the section of the datasheet. For detailed information regarding the table, please refer to the Application Note from Texas Instruments entitled *IC Package Thermal Metrics* (SPRA953).

The UCC27511 and UCC27512 devices are offered in SOT-23, 6-pin package (DBV) and 3 mm × 3 mm, WSON 6-pin package with exposed thermal pad (DRS), respectively. The thermal information table summarizes the thermal performance metrics related to the two packages. θ_{JA} metric should be used for comparison of power dissipation between different packages. Under identical power-dissipation conditions, the DRS package will maintain a lower die temperature than the DBV. The ψ_{JT} and ψ_{JB} metrics are used when estimating the die temperature during actual application measurements.

The DRS is a better thermal package overall because it has the exposed thermal pad and is able to sink heat to the PCB better than the DBV. The thermal pad in DRS package provides designers with an ability to create an excellent heat removal sub-system from the vicinity of the device, thus helping to maintain a lower junction temperature. This pad should be soldered to the copper on the printed circuit board directly underneath the device package. Then a printed circuit board designed with thermal lands and thermal vias completes a very efficient heat-removal subsystem. In such a design, the heat is extracted from the semiconductor junction through the thermal pad, which is then efficiently conducted away from the location of the device on the PCB through the thermal network. This helps to maintain a lower board temperature near the vicinity of the device leading to an overall lower device-junction temperature.

In comparison, for the DBV package, heat removal occurs primarily through the leads of the device and the PCB traces connected to the leads.

Note that the exposed pad in DRS package is not directly connected to any leads of the package, but is electrically and thermally connected to the substrate of the device which is the ground of the device. TI recommends to externally connect the exposed pads to GND in PCB layout for better EMI immunity.

PCB Layout

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27511 and UCC27512 gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak-current capability is even higher (4-A/8-A peak current is at VDD = 12 V). Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit-layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the VDD-bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD during turnon of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turnon and turnoff current-loop paths (driver device, power MOSFET and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances – during turnon and turnoff transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller etc at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.
- In noisy environments, tying the unused Input pin of UCC27511 and UCC27512 to VDD (in case of IN+) or GND (in case of IN-) using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output may be necessary.
- The UCC27512 device offers two ground pins, pin 2 and pin 5. Shorting the two pins together using the PCB trace is extremely important. The shortest trace should be located as close as possible to the device.

REVISION HISTORY

Changes from Revision D (May 2013) to Revision E	Page
• Changed OUTL in the ABS Max Ratings table to show DC and Repetitive pulse values	4

Changes from Revision C (June 2012) to Revision D	Page
• Added 0.05 to P_{SW} equation in the *Power Dissipation* section.	20

Changes from Revision B (March, 2012) to Revision C	Page
• Added UCC27512 device throughout.	1
• Added 6-Pin DRS package feature.	1
• Added UCC27512DRS ordering information.	3
• Added OUT voltage ab max ratings for the UCC27512.	4
• Changed ESD ratings of Human Body Model, HBM from 2000 V to 4000 V.	4
• Changed ESD ratings of Charged Device Model, CDM SOT-23 from 500 V to 1000 V.	4
• Added (1)	4
• Added UCC27512 Thermal Information.	5
• Added power dissipation conditions note to Thermal Information section.	5
• Added UCC27512 Functional Block Diagram.	9
• Added DRS pinout for the UCC27512.	9
• Added UCC27512 TERMINAL FUNCTIONS table.	10
• Added UCC27512 application diagrams.	15
• Added Typical Application Diagram note.	15
• Added Output stage text.	18
• Added Thermal Information description.	21
• Added PCB layout bullet.	22

(1) Values are verified by characterization on bench.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27511DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7511	Samples
UCC27511DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7511	Samples
UCC27512DRSR	ACTIVE	SON	DRS	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27512	Samples
UCC27512DRST	ACTIVE	SON	DRS	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27512	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC27512 :

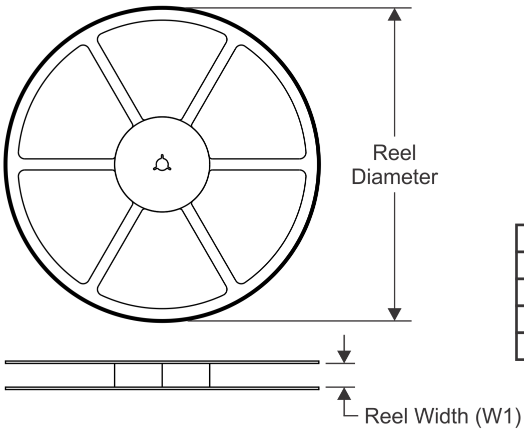
- Enhanced Product: UCC27512-EP

NOTE: Qualified Version Definitions:

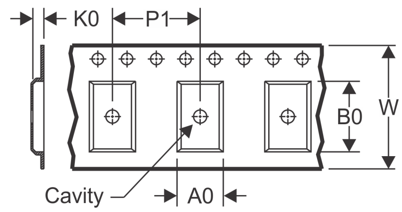
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

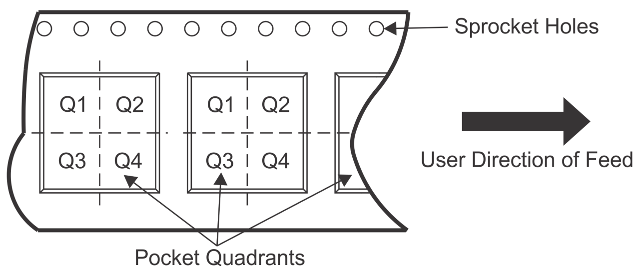


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

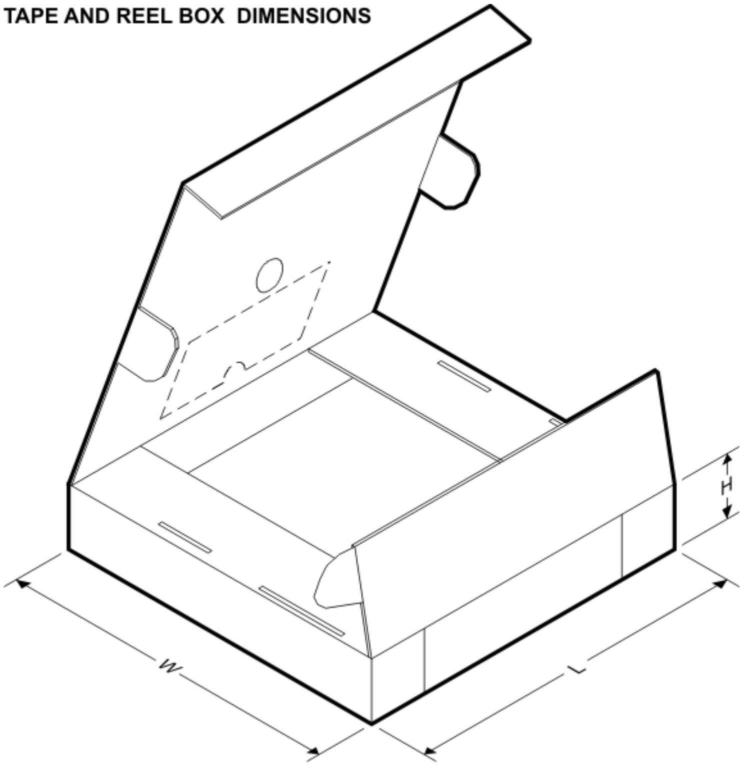
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27511DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27511DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27512DRSR	SON	DRS	6	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27512DRST	SON	DRS	6	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

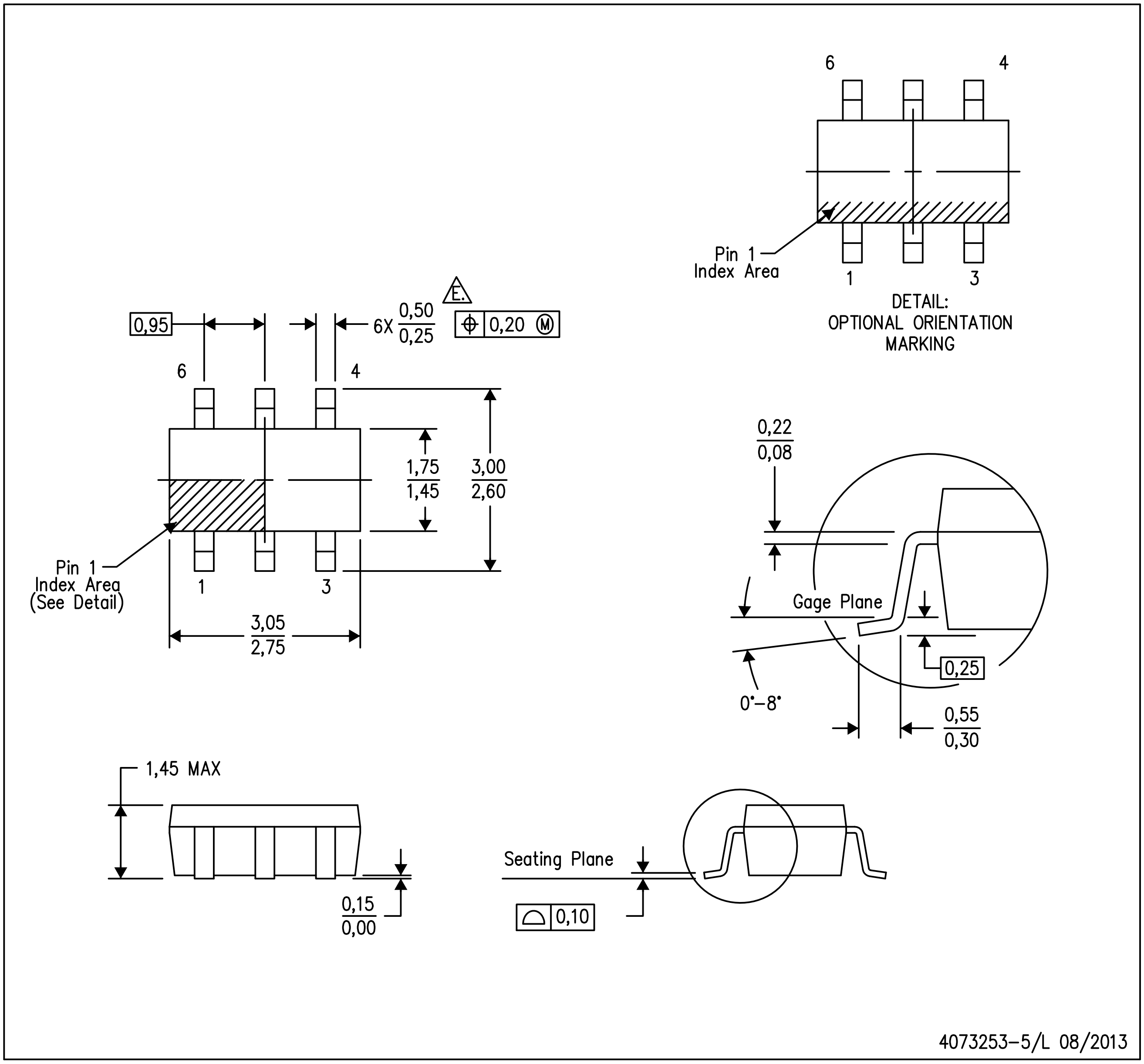
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

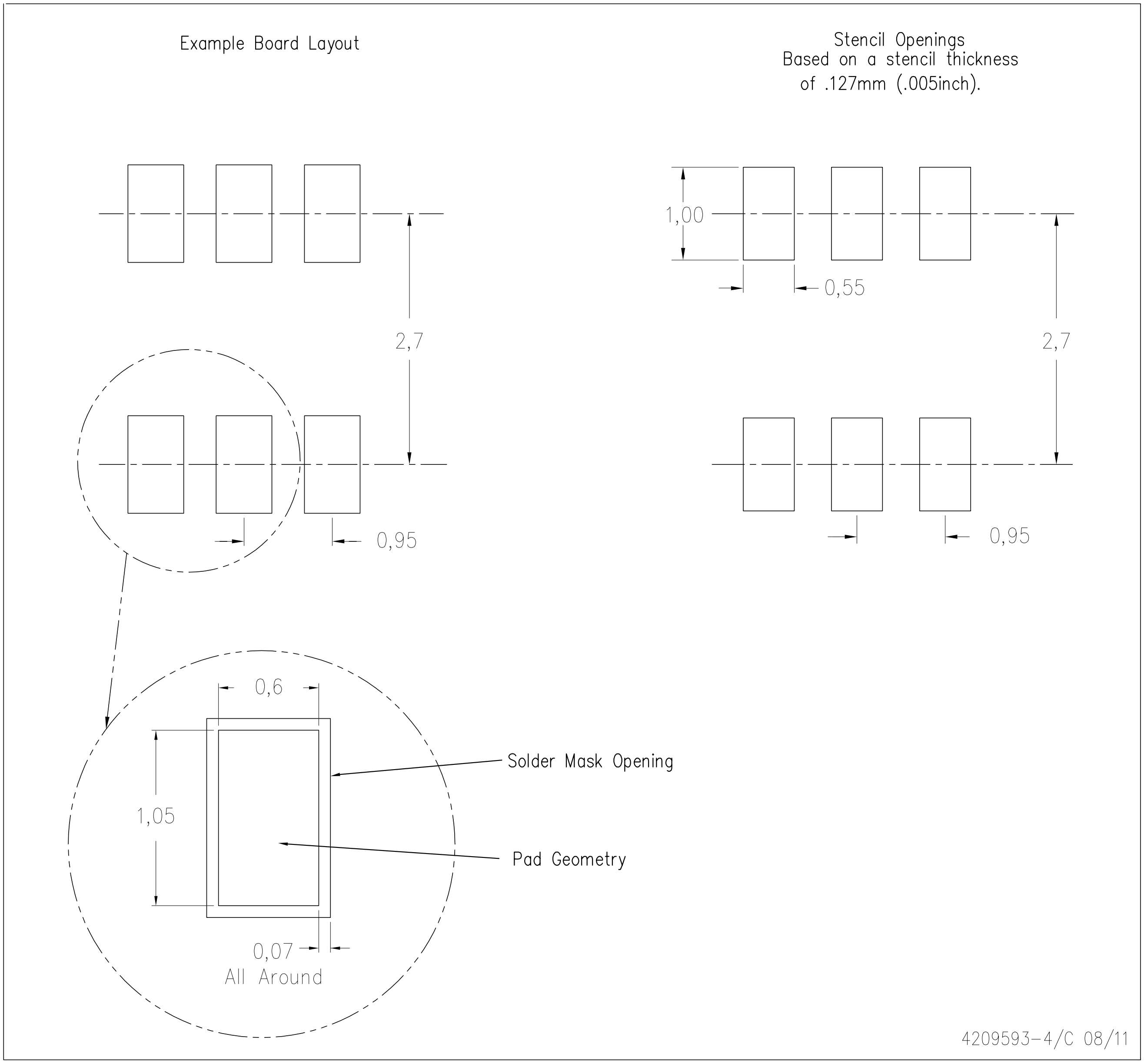
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27511DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
UCC27511DBVT	SOT-23	DBV	6	250	203.0	203.0	35.0
UCC27512DRSR	SON	DRS	6	3000	367.0	367.0	35.0
UCC27512DRST	SON	DRS	6	250	210.0	185.0	35.0

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



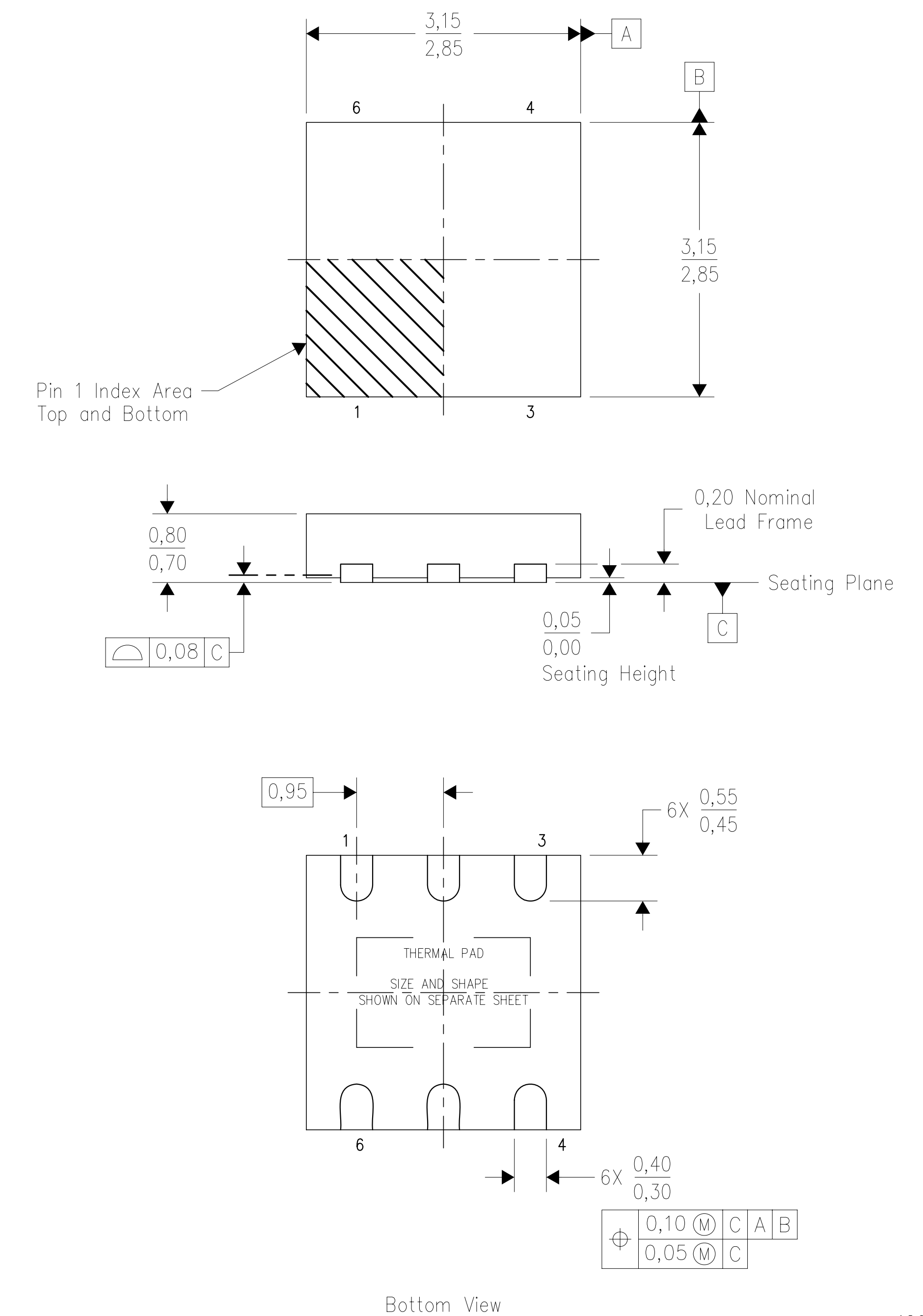
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DRS (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

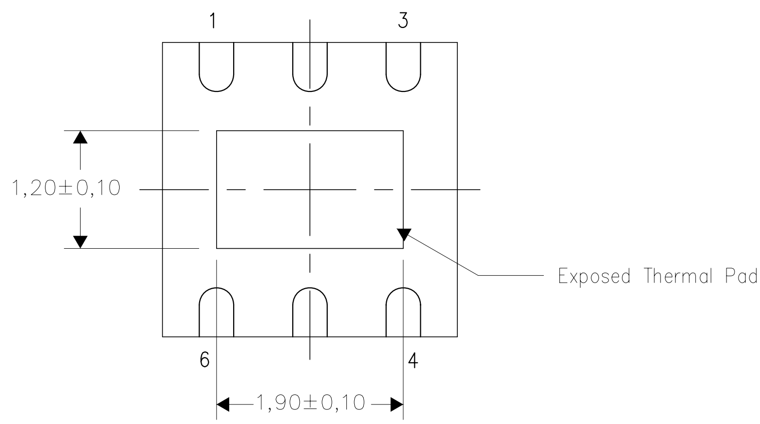
DRS (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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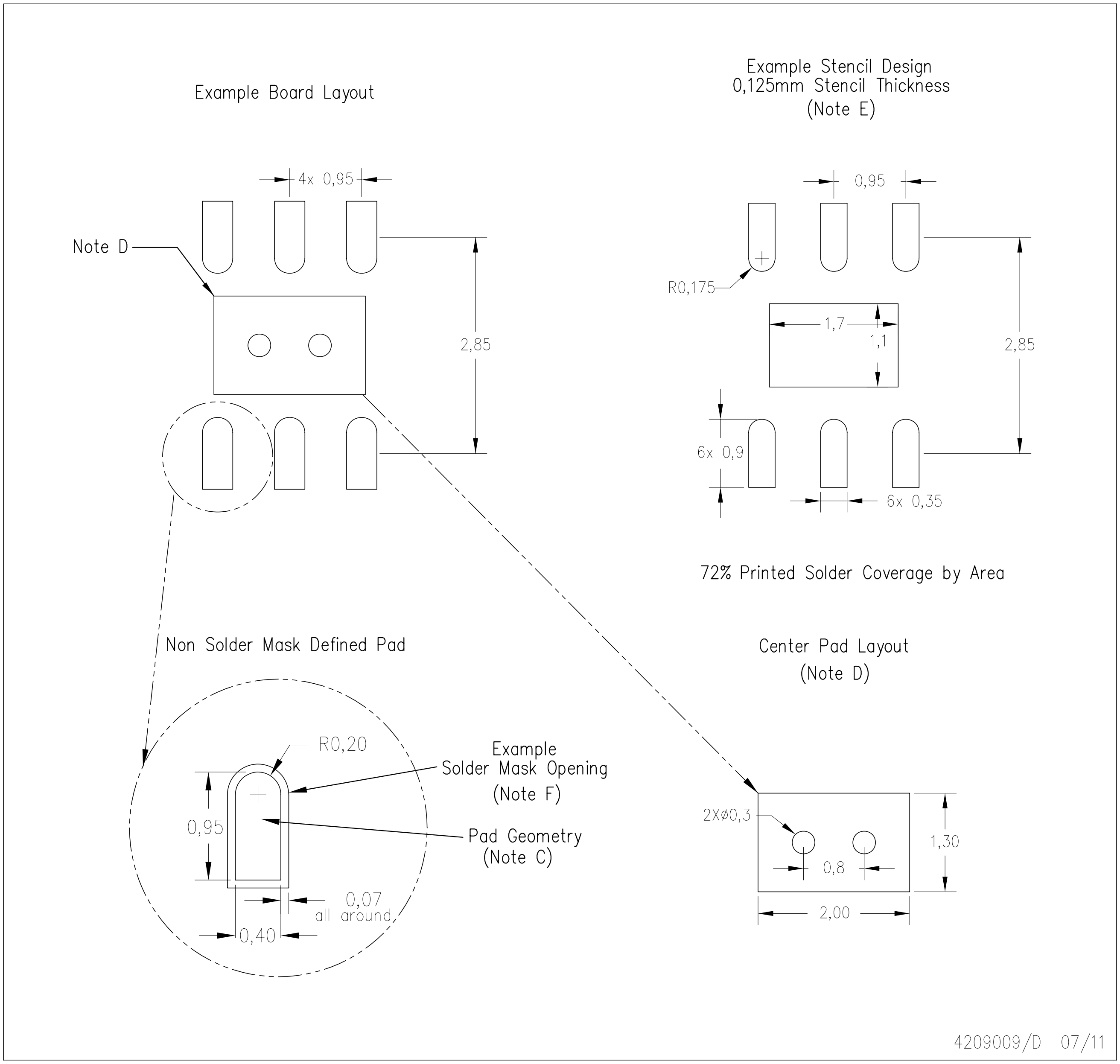
NOTE: All linear dimensions are in millimeters

DRS (S−PWSON−N6) PLASTIC SMALL OUTLINE NO−LEAD



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC−7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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