MAX232E Dual RS-232 Driver and Receiver With IEC61000-4-2 Protection

1 Features

- Meets or Exceeds TIA/RS-232-F and ITU Recommendation V.28
- ESD Protection for RS-232 Bus Pins
  - ±15-kV Human-Body Model (HBM)
  - ±8-kV IEC61000-4-2, Contact Discharge
  - ±15-kV IEC61000-4-2, Air-Gap Discharge
- Operates From a Single 5-V Power Supply With 1-µF Charge-Pump Capacitors
- Operates up to 250 kbit/s
- Two Drivers and Two Receivers
- Low Supply Current: 8 mA Typical

2 Applications

- TIA/RS-232-F
- Battery-Powered Systems
- Terminals
- Modems
- Computers

3 Description

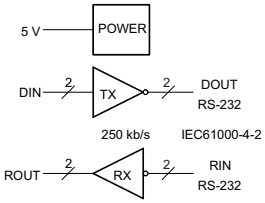
The MAX232E is a dual driver and receiver that includes a capacitive voltage generator to supply RS-232-F compliant voltage levels from a single 5-V supply. Each receiver converts RS-232 inputs to 5-V TTL/CMOS levels. This receiver has a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into TIA/RS-232-F levels.

Device Information[1]

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)
MAX232ECD MAX232EID	SOIC (16)	9.90 mm × 3.91 mm
MAX232ECDW MAX232EIDW	SOIC WIDE (16)	10.30 mm × 7.50 mm
MAX232ECN MAX232EIN	PDIP (16)	19.30 mm × 6.35 mm
MAX232ECPW MAX232EIPW	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

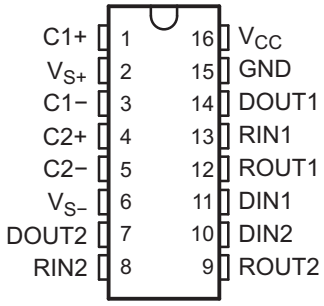
Changes from Revision B (November 2009) to Revision C **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted "±30-V Input Levels" from *Features* ... 1
- Deleted *Ordering Information* table; see POA at the end of the data sheet ... 1
- Added MIN value ±3 to "Receiver input voltage (RIN1, RIN2) row in *Recommended Operating Conditions* ... 4
- Changed $R_{\theta JA}$ values in *Thermal Information* ... 4
- Deleted table note 3 from *Receiver Section Electrical Characteristics* ... 5
- Added a new row to the *Function Table for Each Receiver* ... 10

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5 Pin Configuration and Functions

D, DW, N, or PW Package
Add 16-Pin SOIC, PDIP, or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	C1+	—	Positive lead of C1 capacitor
2	V_{S+}	O	Positive charge pump output for storage capacitor only
3	C1–	—	Negative lead of C1 capacitor
4	C2+	—	Positive lead of C2 capacitor
5	C2–	—	Negative lead of C2 capacitor
6	V_{S-}	O	Negative charge pump output for storage capacitor only
7	DOUT2	O	RS-232 line data output (to remote RS-232 system)
8	RIN2	I	RS-232 line data input (from remote RS-232 system)
9	ROUT2	O	Logic data output (to UART)
10	DIN2	I	Logic data input (from UART)
11	DIN1	I	Logic data input (from UART)
12	ROUT1	O	Logic data output (to UART)
13	RIN1	I	RS-232 line data input (from remote RS-232 system)
14	DOUT1	O	RS-232 line data output (to remote RS-232 system)
15	GND	—	Ground
16	V_{CC}	—	Supply voltage—connect to external 5-V power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Input supply voltage (2)		–0.3	6	V
V_{S+}	Positive output supply voltage		V_{CC} – 0.3	15	V
V_{S-}	Negative output supply voltage		–0.3	–15	V
V_I	Input voltage	Driver	–0.3	V_{CC} + 0.3	V
		Receiver		±30	
V_O	Output voltage	DOUT	V_{S-} – 0.3	V_{S+} + 0.3	V
		ROUT	–0.3	V_{CC} + 0.3	
	Short-circuit duration	DOUT	Unlimited		
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 7, 8, 13, and 14	±15000	V
			Other pins	±3000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1500	
		IEC61000-4-2, air-gap discharge	Pins 7, 8, 13, and 14	±15000	
		IEC61000-4-2, contact discharge		±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (DIN1, DIN2)		2			V
V_{IL}	Low-level input voltage (DIN1, DIN2)				0.8	V
	Receiver input voltage (RIN1, RIN2)		±3		±30	V
T_A	Operating free-air temperature	MAX232EC	0		70	°C
		MAX232EI	–40		85	

6.4 Thermal Information

THERMAL METRIC(1)(2)(3)		MAX232E				UNIT
		D (SOIC)	DW (SOIC)	N (PDIP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.8	73.4	43.3	101.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.4	35.1	30	29.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.4	38.3	23.3	47.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Maximum power dissipation is a function of $T_J(max)$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

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Thermal Information (continued)

THERMAL METRIC(1)(2)(3)		MAX232E				UNIT
		D (SOIC)	DW (SOIC)	N (PDIP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
ψ_{JT}	Junction-to-top characterization parameter	5.8	9.4	14.4	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.1	37.7	23.2	46.6	°C/W

6.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 10)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.5 V	All outputs open, T_A = 25°C		8	10	mA

(1) Test conditions are C1 – C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.

6.6 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER			TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	R_L = 3 kΩ to GND		5	7		V
V_{OL}	Low-level output voltage(3)	DOUT	R_L = 3 kΩ to GND			–7	–5	V
r_o	Output resistance	DOUT	V_{S+} = V_{S-} = 0,	V_O = ±2 V	300			Ω
I_{OS}(4)	Short-circuit output current	DOUT	V_{CC} = 5.5 V,	V_O = 0		±10		mA
I_{IS}	Short-circuit input current	DIN	V_I = 0				200	µA

(1) Test conditions are C1 – C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
(4) Not more than one output should be shorted at a time.

6.7 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER			TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	ROUT	I_{OH} = –1 mA		3.5			V
V_{OL}	Low-level output voltage	ROUT	I_{OL} = 3.2 mA				0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	RIN	V_{CC} = 5 V	T_A = 25°C		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	RIN	V_{CC} = 5 V	T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	RIN	V_{CC} = 5 V		0.2	0.5	1	V
r_i	Receiver input resistance	RIN	V_{CC} = 5 V	T_A = 25°C	3	5	7	kΩ

(1) Test conditions are C1 – C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.

6.8 Switching Characteristics: Driver

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ, See Figure 6			30	V/µs
SR(t)	Driver transition region slew rate	R_L = 3 kΩ, C_L = 2.5 nF See Figure 7		3		V/µs
	Data rate	One DOUT switching		250		kbit/s

(1) Test conditions are C1 – C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

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6.9 Switching Characteristics: Receiver

V_{CC} = 5 V, T_A = 25°C (see Figure 5)

PARAMETER		TEST CONDITIONS(1)	TYP	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	C_L = 50 pF	500	ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	C_L = 5 0pF	500	ns

(1) Test conditions are C1 – C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

6.10 Typical Characteristics

T_A = 25 °C

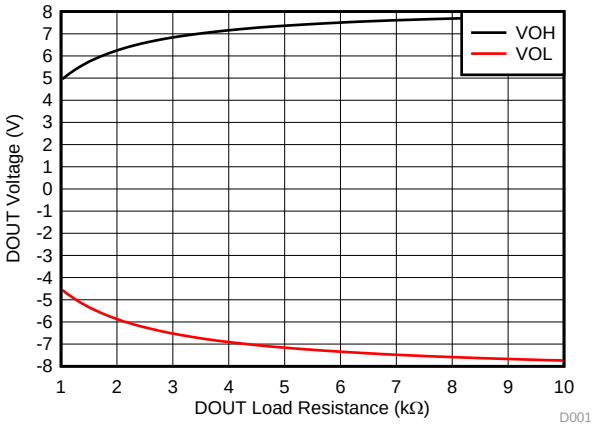


Figure 1. Driver Output Voltage vs Load Resistance

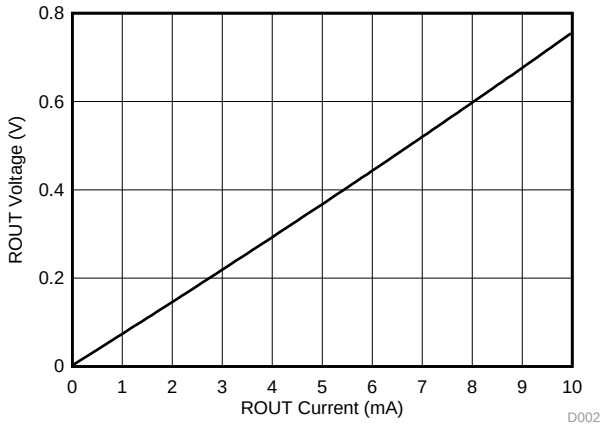


Figure 2. Receiver Low Output Voltage vs Load Current

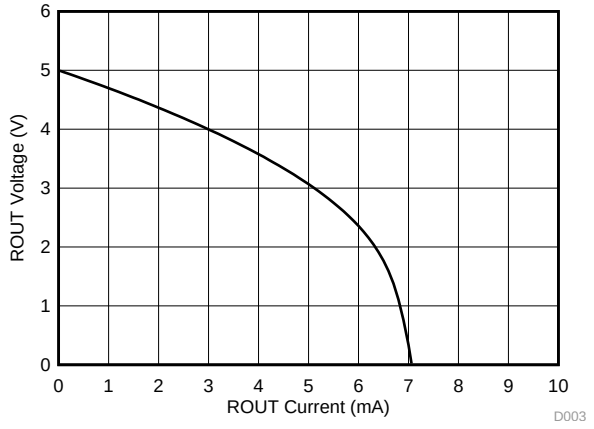


Figure 3. Receiver High Output Voltage vs Load Current

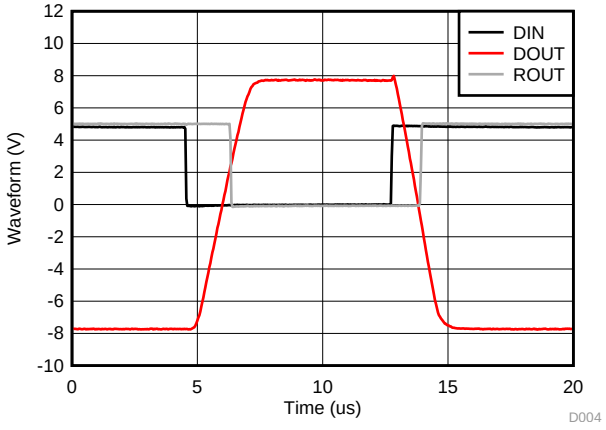
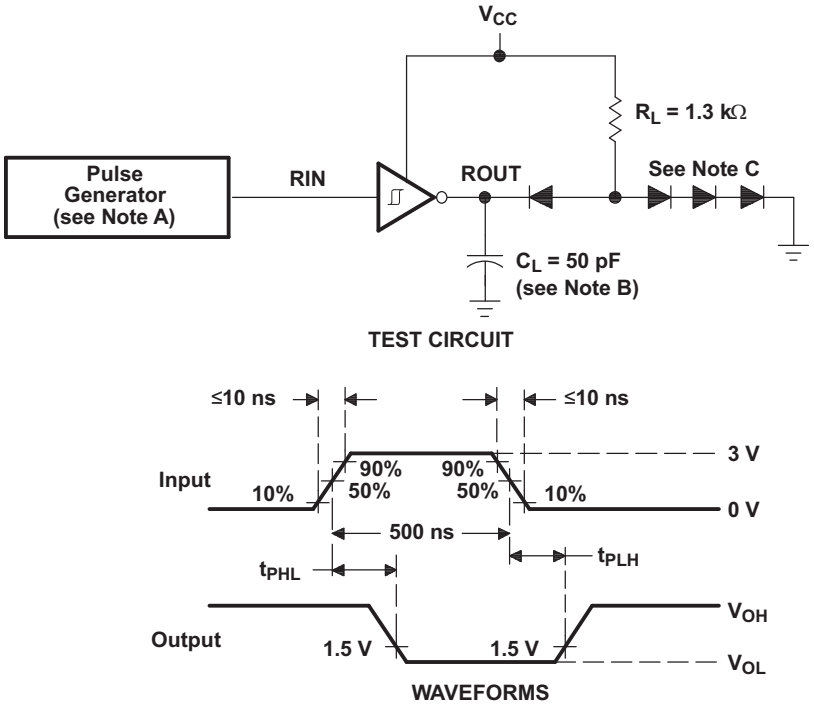


Figure 4. Loopback Waveforms
Data Rate 120 kbit/s

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7 Parameter Measurement Information



A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.

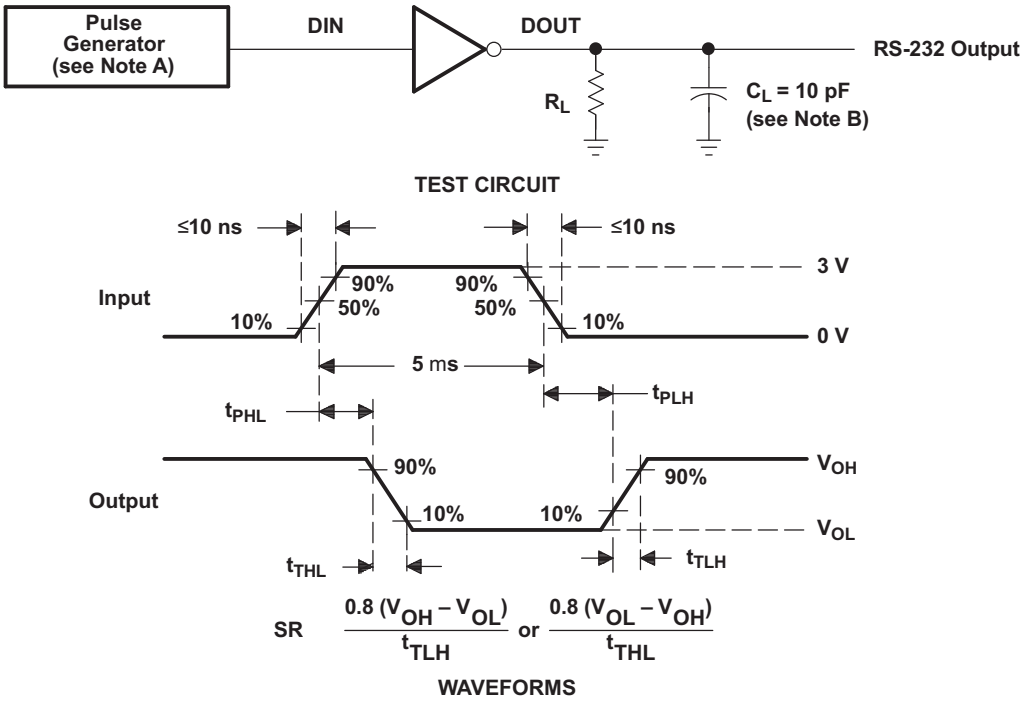
B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064 or equivalent.

Figure 5. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements

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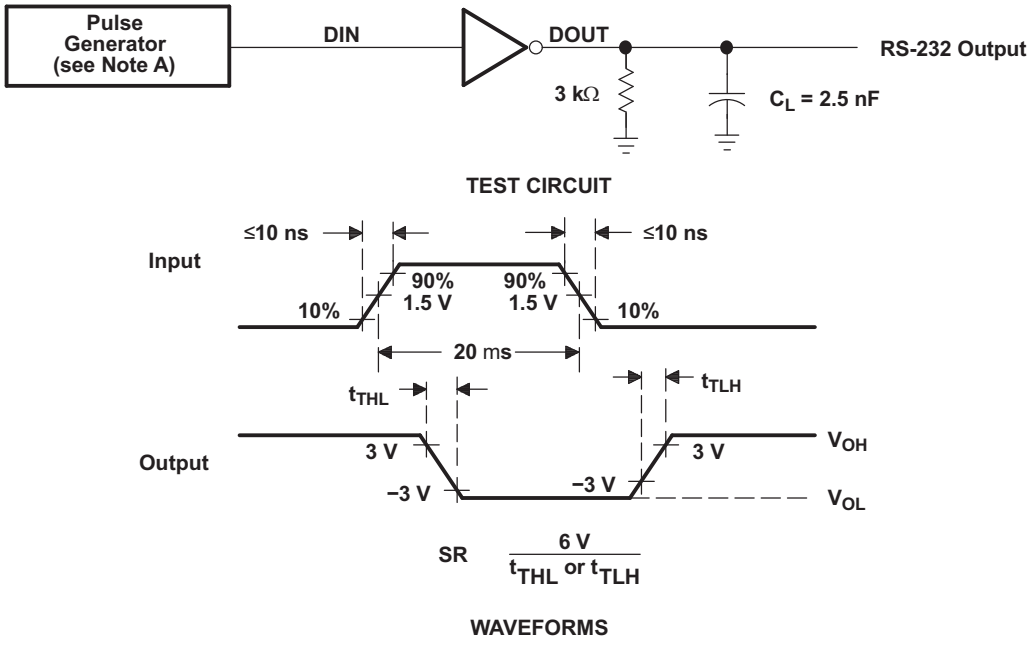
Parameter Measurement Information (continued)



A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.

B. C_L includes probe and jig capacitance.

Figure 6. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5-µs Input)



A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.

Figure 7. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20-µs Input)

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8 Detailed Description

8.1 Overview

The MAX232E device is a dual driver and receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5-V supply. All RS-232 pins have 15-kV HBM and IEC61000-4-2 Air-Gap discharge protection. RS-232 pins also have 8-kV IEC61000-4-2 contact discharge protection. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have shorted and open fail safe. The receiver can accept up to ±30-V inputs and decode inputs as low as ±3 V. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. Outputs are protected against shorts to ground.

8.2 Functional Block Diagram

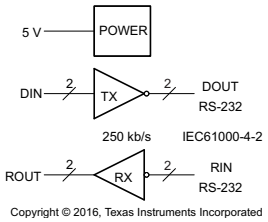


Figure 8. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Power

The power block increases and inverts the 5-V supply for the RS-232 driver using a charge pump that requires four 1-µF external capacitors.

8.3.2 RS-232 Driver

Two drivers interface standard logic level to RS-232 levels. Internal pullup resistors on DIN inputs ensures a high input when the line is high impedance.

8.3.3 RS-232 Receiver

Two receivers interface RS-232 levels to standard logic levels. An open or shorted to ground input results in a high output on ROUT.

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8.4 Device Functional Modes

8.4.1 V_{CC} Powered by 5 V

The device is in normal operation.

8.4.2 V_{CC} Unpowered

When MAX232E is unpowered, it can be safely connected to an active remote RS-232 device.

8.4.3 Truth Tables

Table 1 and Table 2 list the functions of this device.

Table 1. Function Table for Each Driver(1)

INPUT DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

Table 2. Function Table for Each Receiver(1)

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level, Open = input disconnected or connected driver off

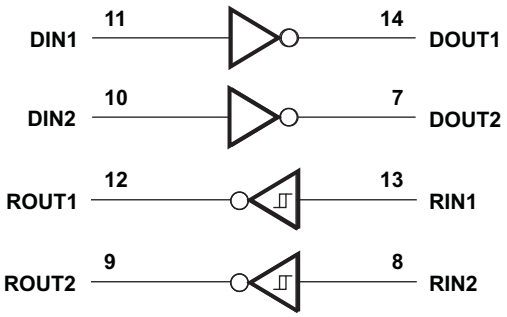


Figure 9. Logic Diagram (Positive Logic)

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9 Applications and Implementation

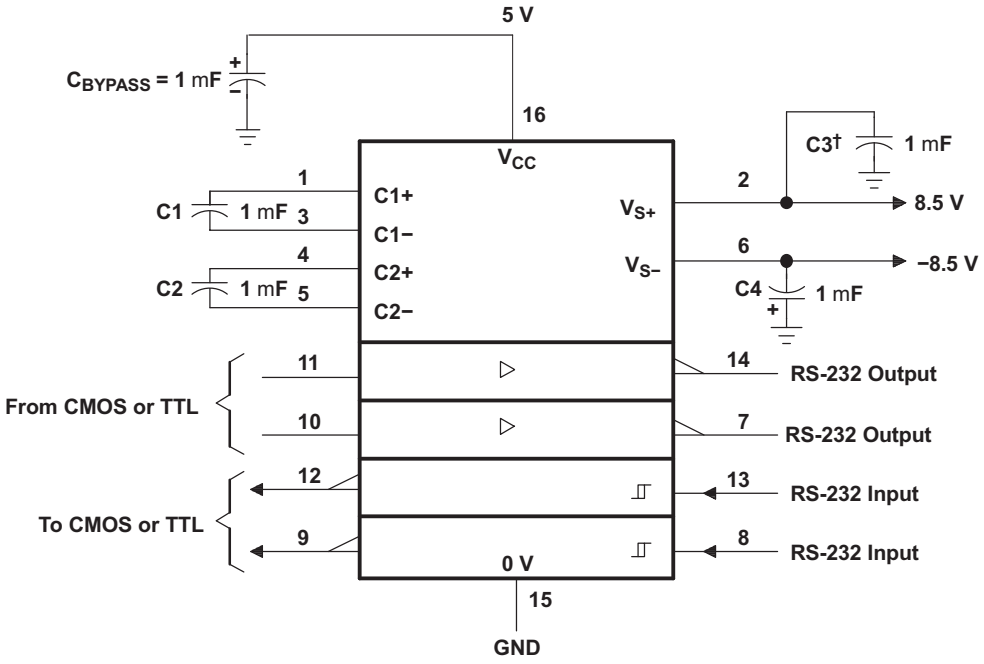
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

For proper operation add capacitors as shown in Figure 10. Pins 9 through 12 connect to UART or general purpose logic lines. RS-232 lines on pins 7, 8, 13, and 14 connect to a connector or cable.

9.2 Typical Application



† C3 can be connected to V_{CC} or GND.

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Resistor values shown are nominal.

Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 10. Typical Operating Circuit

9.2.1 Design Requirements

- V_{CC} minimum is 4.5 V and maximum is 5.5 V.
- Maximum recommended bit rate is 250 kbit/s.

9.2.2 Detailed Design Procedure

The capacitor type used for C1–C4 is not critical for proper operation. The MAX232E requires 1-µF capacitors, although capacitors up to 10 µF can be used without harm. Ceramic dielectrics are suggested for capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (for example, 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V–.

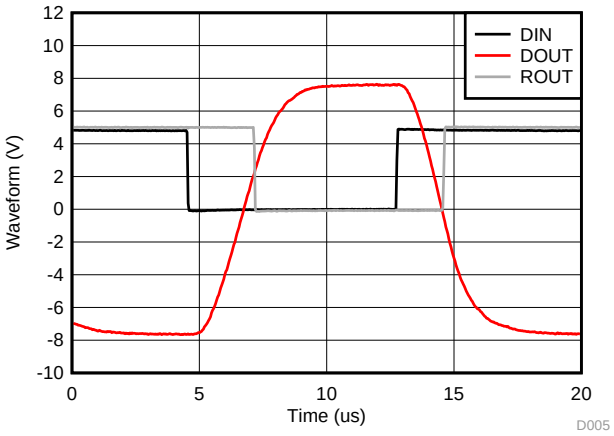
Typical Application (continued)

Use larger capacitors (up to 10 µF) to reduce the output impedance at V_{S+} and $V_{S–}$.

Bypass V_{CC} to ground with at least 1 µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

9.2.3 Application Curve

Loopback waveform connects DOUT to RIN.



Date Rate = 120 kbit/s, C_L = 1 nF

Figure 11. Loopback Waveforms

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10 Power Supply Recommendations

The V_{CC} voltage should be connected to the same power source used for logic device connected to DIN and ROUT pins. V_{CC} should be between 4.5 V and 5.5 V.

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. Make the impedance from MAX232E ground pin and circuit board's ground plane as low as possible for best ESD performance. Use wide metal and multiple vias on both sides of ground pin.

11.2 Layout Example

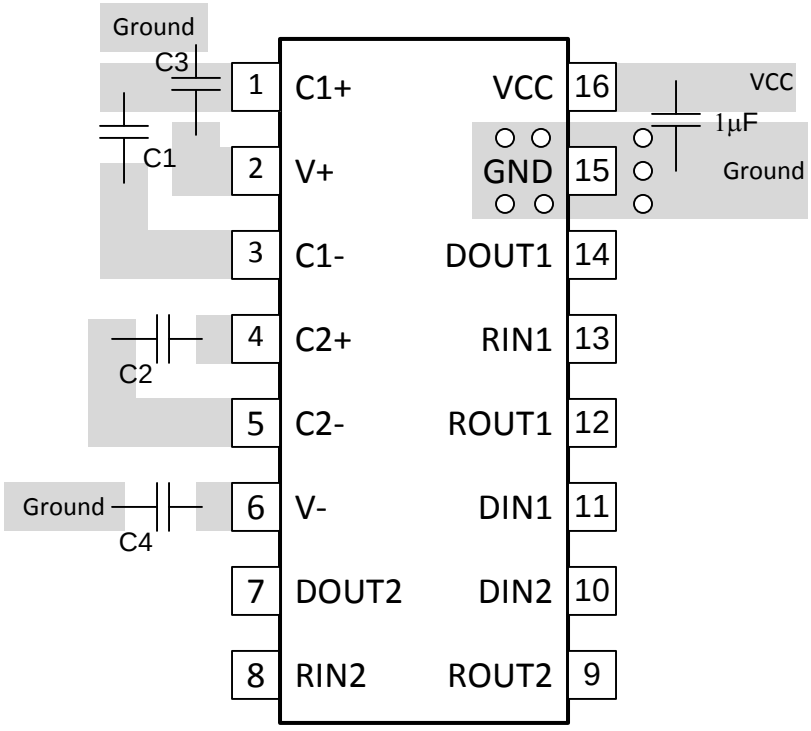


Figure 12. MAX232E Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX232ECD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232EC	Samples
MAX232ECDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232EC	Samples
MAX232ECDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232EC	Samples
MAX232ECDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	MAX232EC	Samples
MAX232ECDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232EC	Samples
MAX232ECDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232EC	Samples
MAX232ECN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	MAX232ECN	Samples
MAX232ECNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	MAX232ECN	Samples
MAX232ECPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA232EC	Samples
MAX232ECPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	MA232EC	Samples
MAX232ECPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA232EC	Samples
MAX232EID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	Samples
MAX232EIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	Samples
MAX232EIDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	Samples
MAX232EIDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	Samples
MAX232EIDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	Samples
MAX232EIDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX232EIN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	MAX232EIN	Samples
MAX232EINE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	MAX232EIN	Samples
MAX232EIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB232EI	Samples
MAX232EIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB232EI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

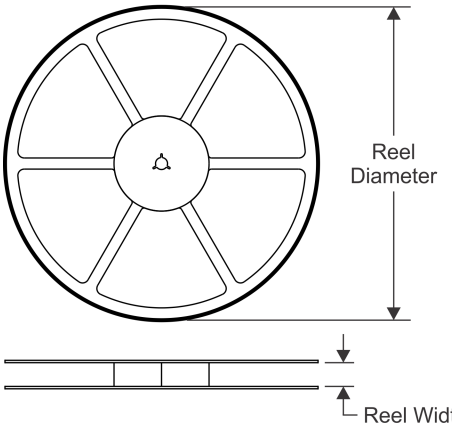
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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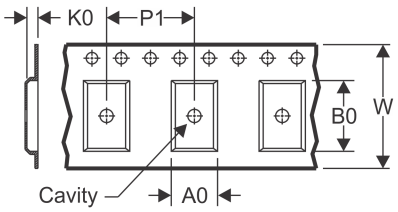
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

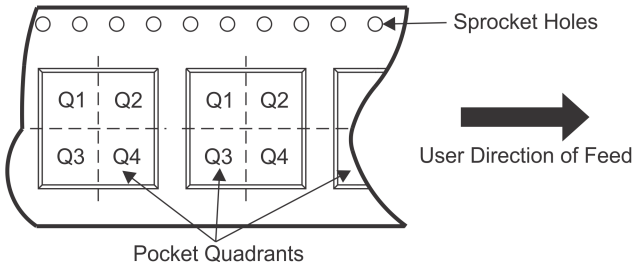


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

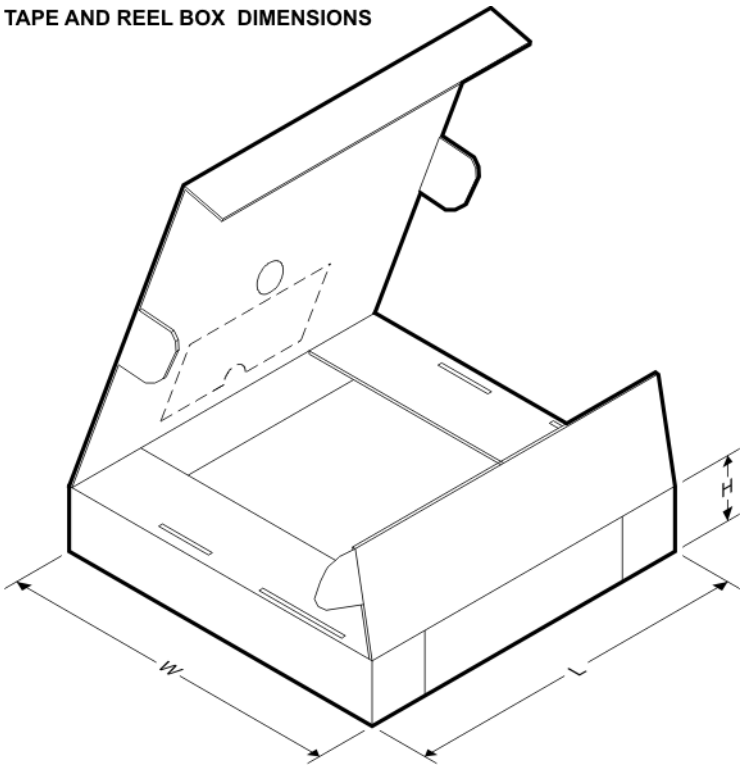
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232ECDWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX232ECPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

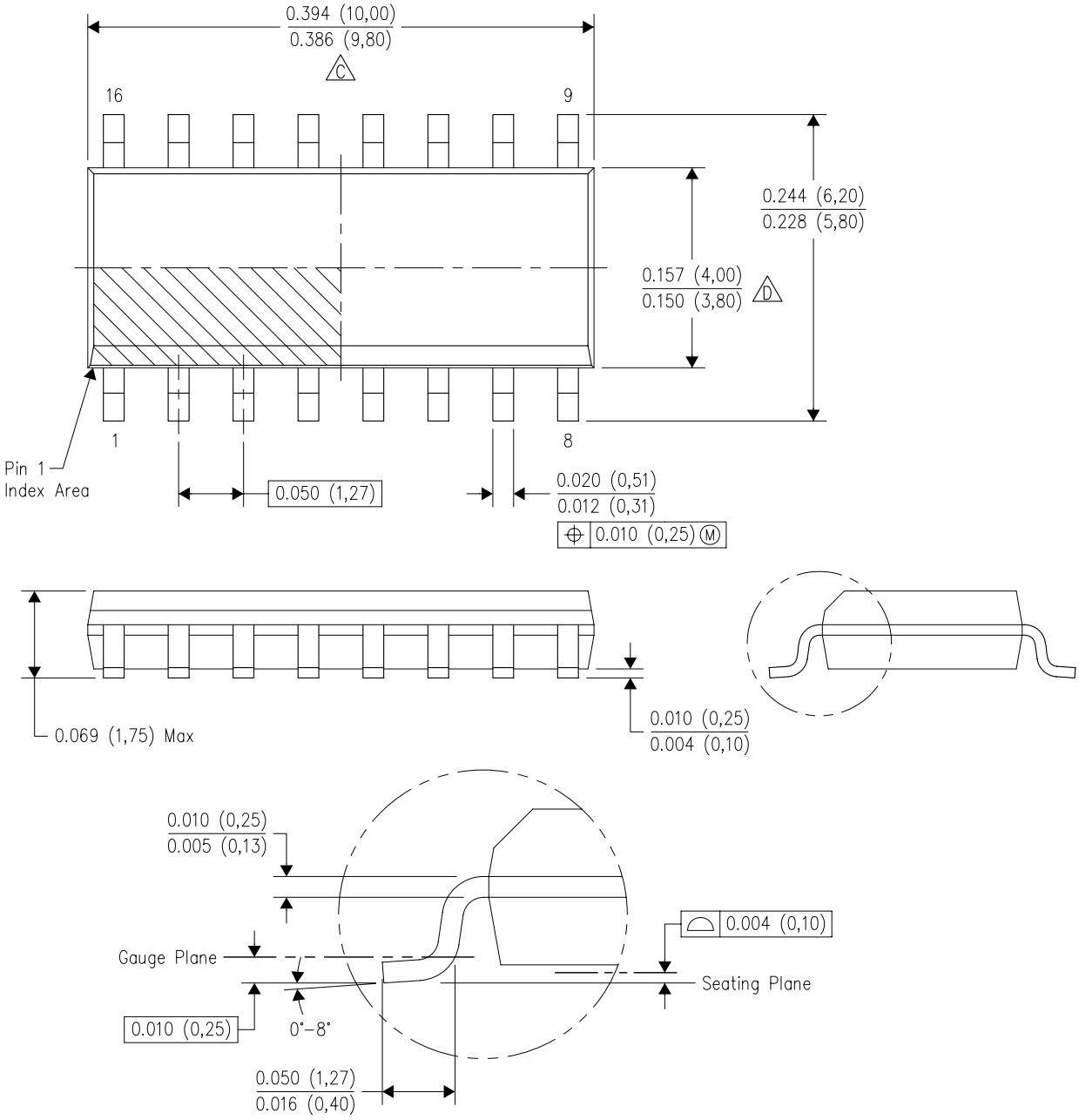
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

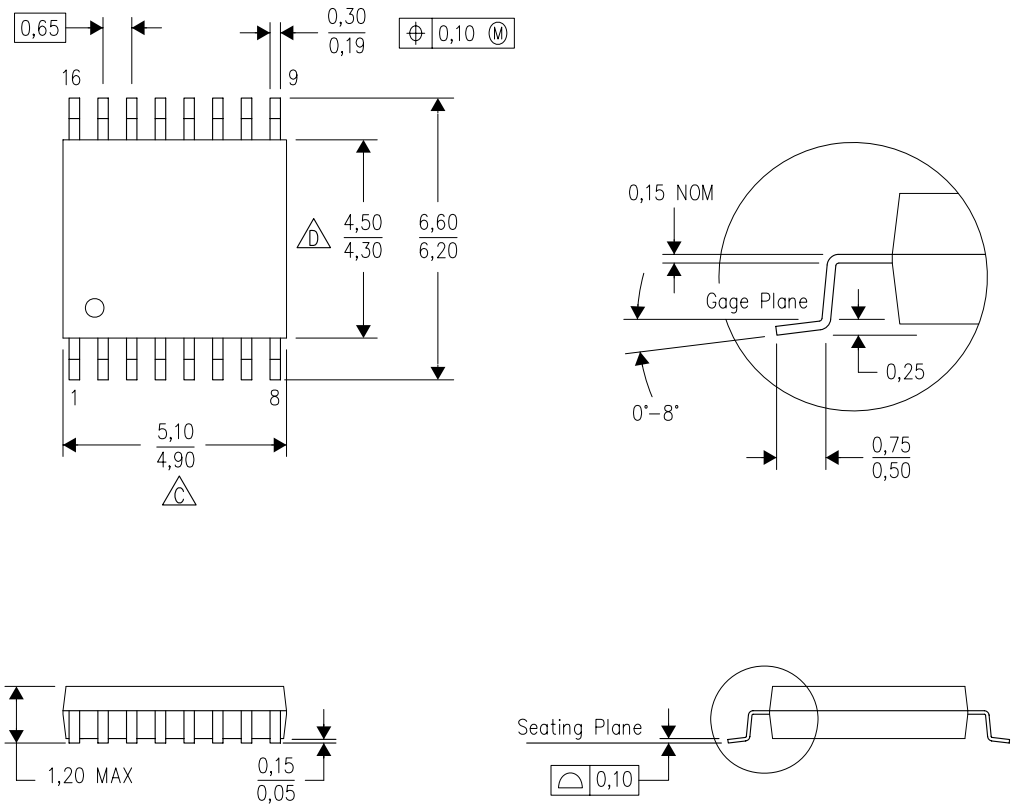
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX232ECDR	SOIC	D	16	2500	367.0	367.0	38.0
MAX232ECDWR	SOIC	DW	16	2000	367.0	367.0	38.0
MAX232ECDWRG4	SOIC	DW	16	2000	367.0	367.0	38.0
MAX232ECPWR	TSSOP	PW	16	2000	364.0	364.0	27.0
MAX232ECPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
MAX232ECPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
MAX232EIDR	SOIC	D	16	2500	367.0	367.0	38.0
MAX232EIDWR	SOIC	DW	16	2000	367.0	367.0	38.0
MAX232EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

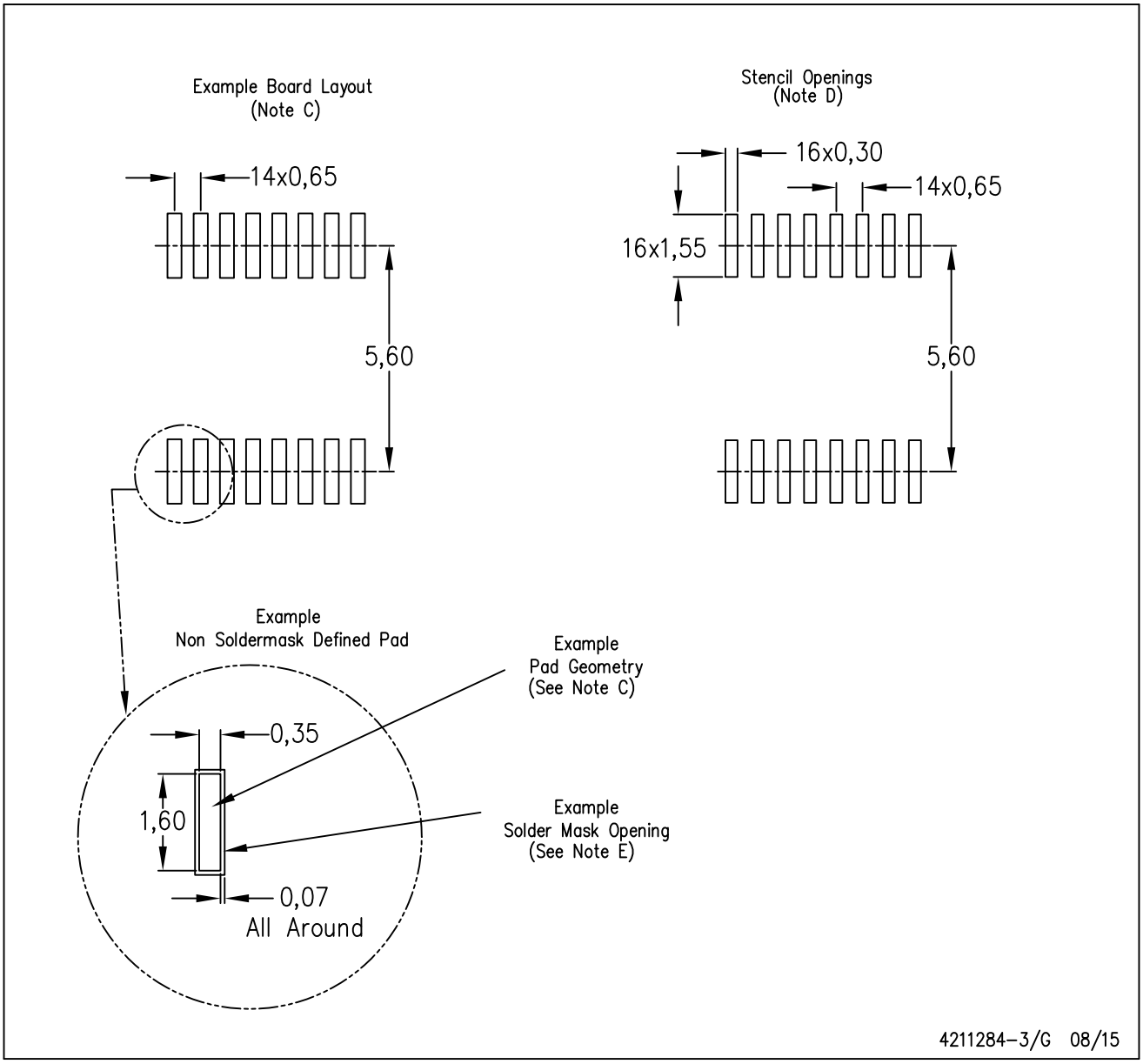
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE

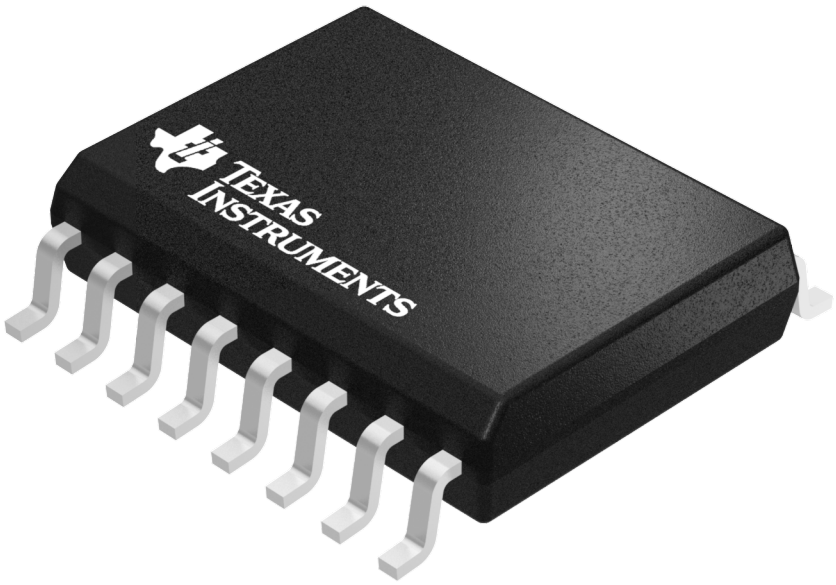


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

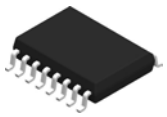
GENERIC PACKAGE VIEW

DW 16 SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

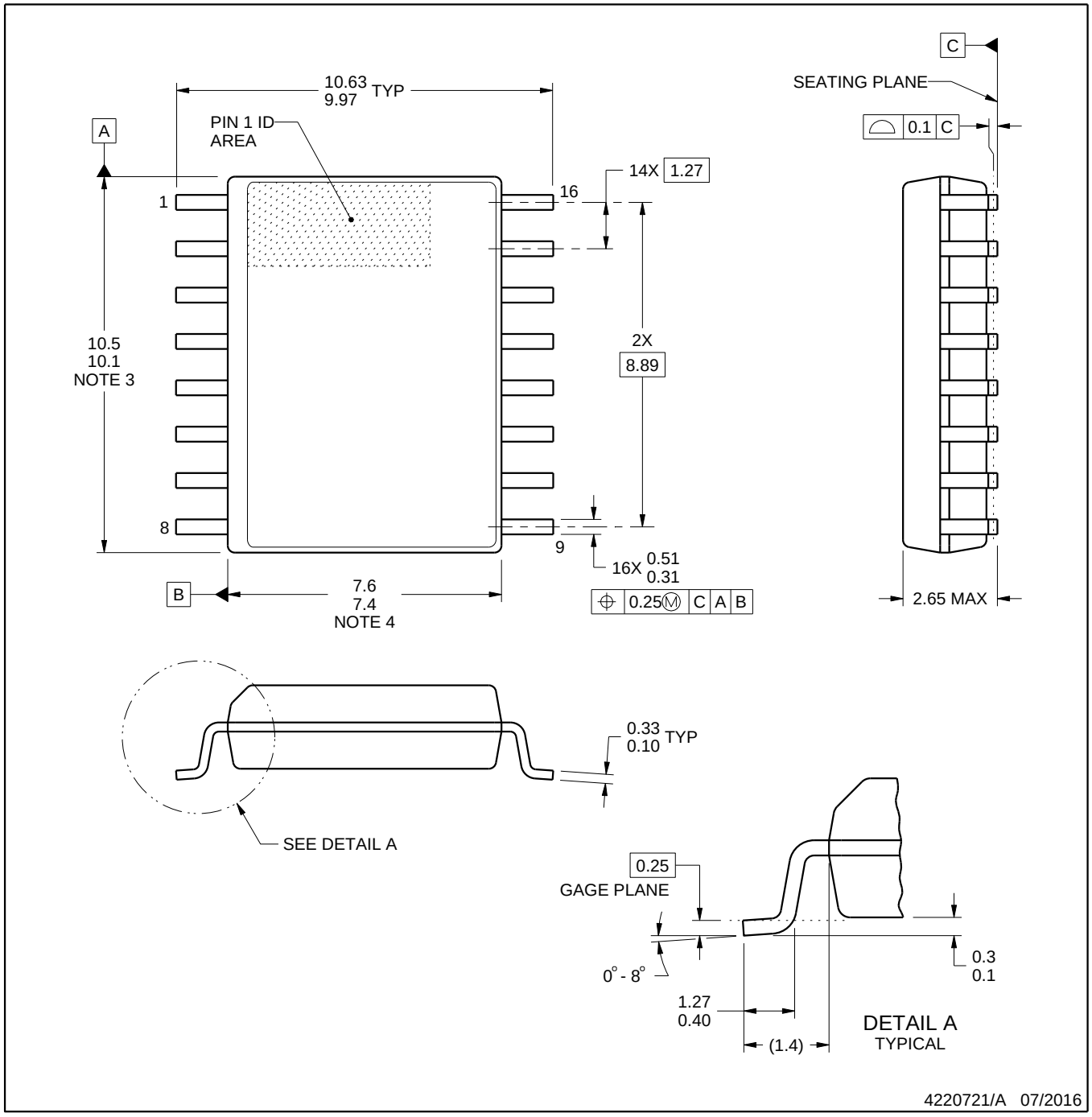


PACKAGE OUTLINE

DW0016A

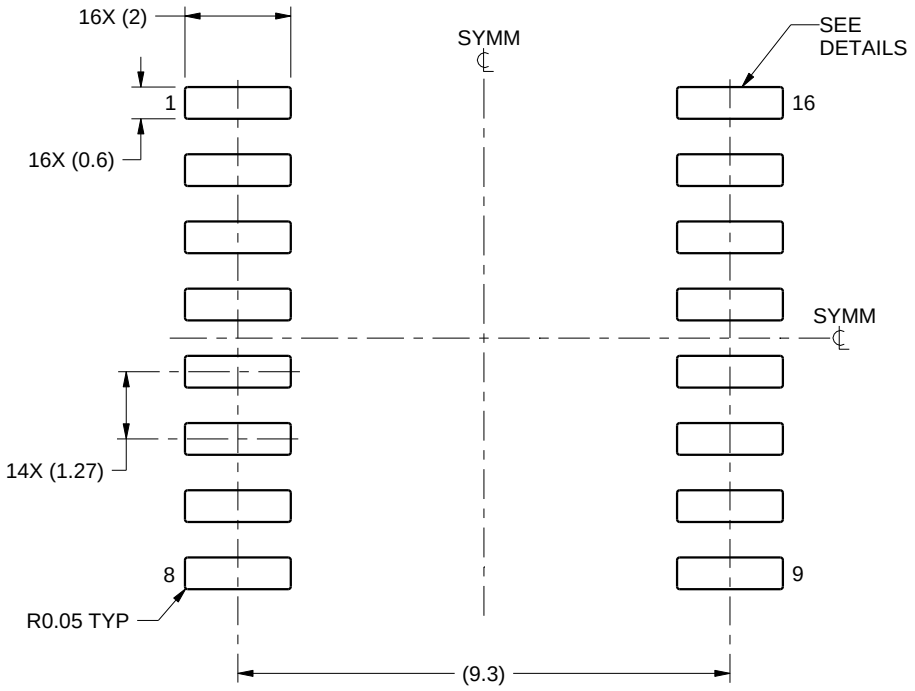
SOIC - 2.65 mm max height

SOIC

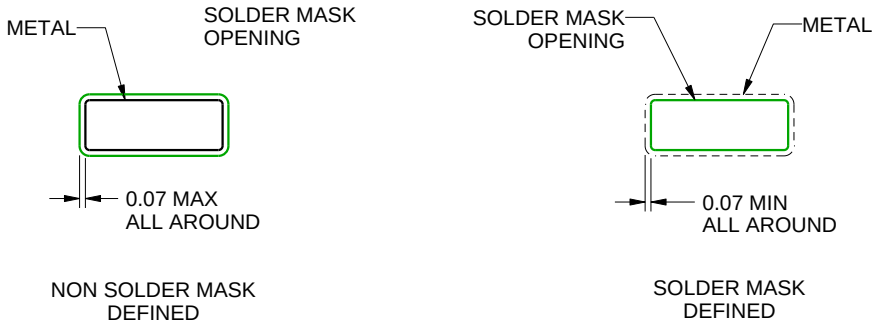


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

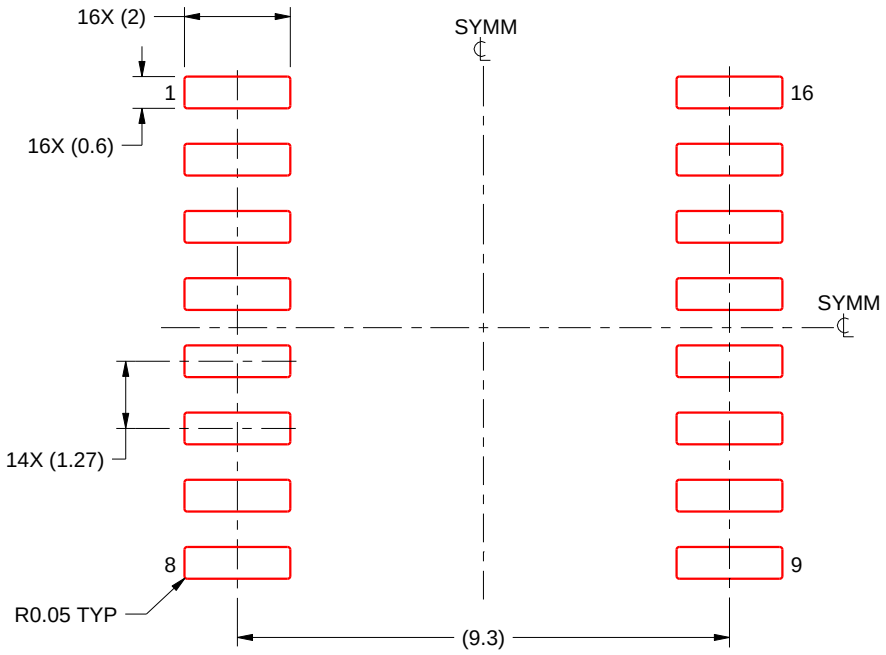


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

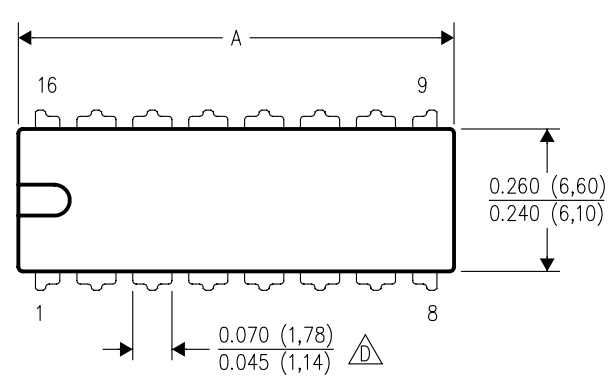
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

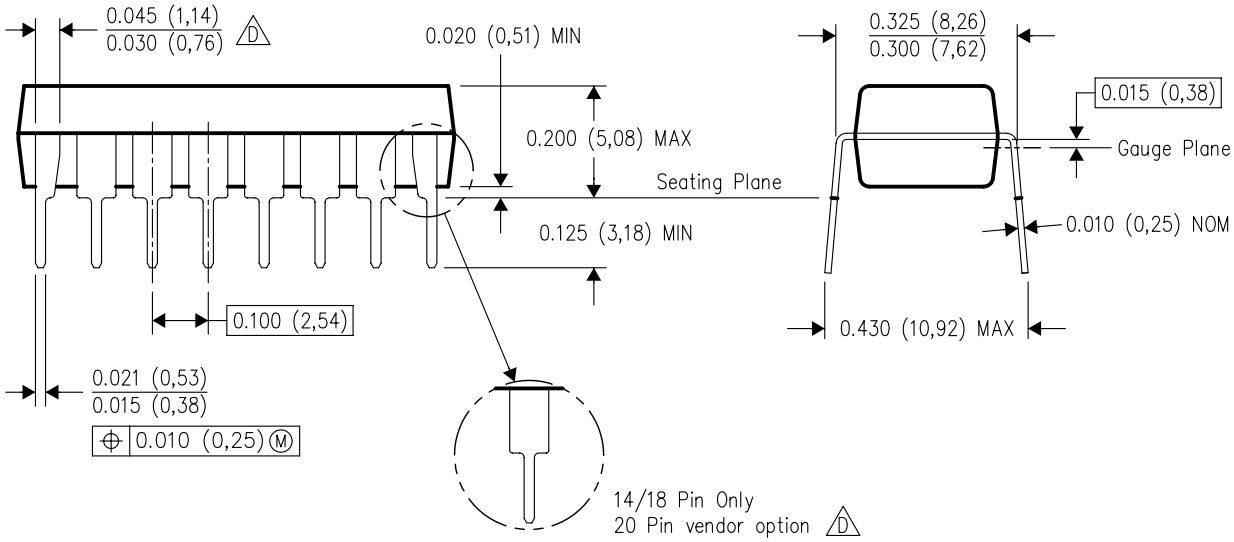
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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