



LM321 Low Power Single Operational Amplifier

1 Features

- ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$. Typical values unless specified.)
- Gain-Bandwidth Product 1 MHz
- Low Supply Current 430 μA
- Low Input Bias Current 45 nA
- Wide Supply Voltage Range 3 V to 32 V
- Stable With High Capacitive Loads
- Single Version of LM324

2 Applications

- Chargers
- Power Supplies
- Industrial: Controls, Instruments
- Desktops
- Communications Infrastructure

3 Description

The LM321 brings performance and economy to low power systems. With a high unity gain frequency and a specified 0.4-V/ μs slew rate, the quiescent current is only 430- μA /amplifier (5 V). The input common mode range includes ground and therefore the device is able to operate in single supply applications as well as in dual supply applications. It is also capable of comfortably driving large capacitive loads.

The LM321 is available in the SOT-23 package. Overall the LM321 is a low power, wide supply range performance operational amplifier that can be designed into a wide range of applications at an economical price without sacrificing valuable board space.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM321	SOT (5)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

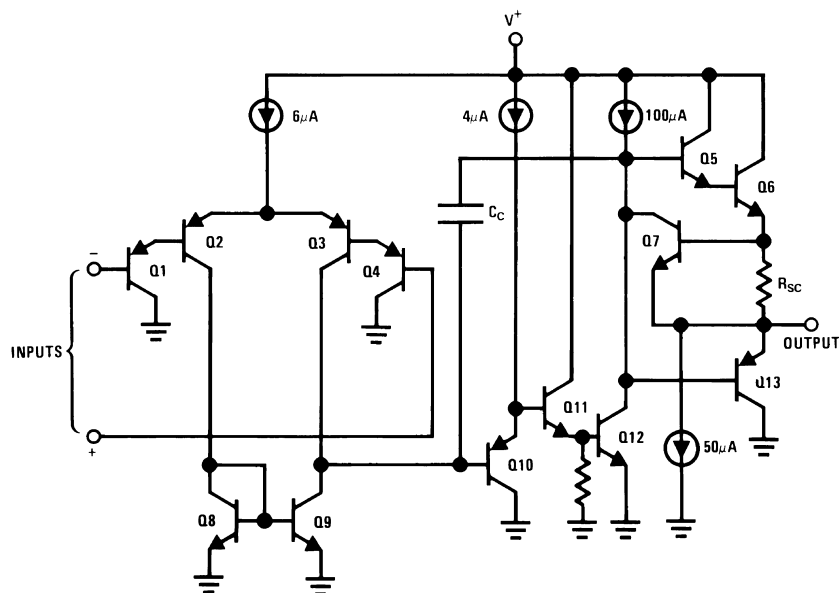


Table of Contents

1 Features	1	7.3 Feature Description	7
2 Applications	1	7.4 Device Functional Modes	8
3 Description	1	8 Application and Implementation	9
4 Revision History	2	8.1 Application Information	9
5 Pin Configuration and Functions	3	8.2 Typical Applications	10
6 Specifications	3	9 Power Supply Recommendations	13
6.1 Absolute Maximum Ratings	3	10 Layout	13
6.2 ESD Ratings	3	10.1 Layout Guidelines	13
6.3 Recommended Operating Conditions	4	10.2 Layout Example	14
6.4 Thermal Information	4	11 Device and Documentation Support	15
6.5 Electrical Characteristics	4	11.1 Trademarks	15
6.6 Typical Characteristics	6	11.2 Electrostatic Discharge Caution	15
7 Detailed Description	7	11.3 Glossary	15
7.1 Overview	7	12 Mechanical, Packaging, and Orderable Information	15
7.2 Functional Block Diagram	7		

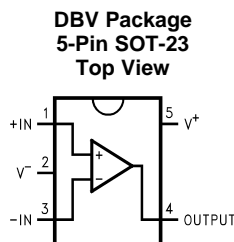
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2013) to Revision C	Page
<ul style="list-style-type: none"> Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 	1

Changes from Revision A (March 2013) to Revision B	Page
<ul style="list-style-type: none"> Changed layout of National Data Sheet to TI format 	13

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	1	I	Noninverting input
V–	2	—	Negative (lowest) power supply
–IN	3	I	Inverting input
OUTPUT	4	O	Output
V+	5	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings ⁽¹⁾

	MIN	MAX	UNIT
Differential Input Voltage	±Supply Voltage		
Input Current ($V_{IN} < -0.3$ V) ⁽²⁾		50	mA
Supply Voltage ($V^+ - V^-$)		32	V
Input Voltage	–0.3	32	V
Output Short Circuit to GND, $V^+ \leq 15$ V and $T_A = 25^\circ\text{C}$ ⁽³⁾	Continuous		
Junction Temperature ⁽⁴⁾		150	°C
Mounting Temperature: Lead temperature (Soldering, 10 sec)		260	°C
Mounting Temperature: Infrared (10 sec)		215	°C
Storage temperature, T_{stg}	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the operational amplifier to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.36 V (at 25°C).
- (3) Short circuits from the output V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground the maximum output current is approximately 40mA independent of the magnitude of V^+ . At values of supply voltage in excess of +15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.
- (4) The maximum power dissipation is a function of $T_J(\text{MAX})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $PD = (T_J(\text{MAX}) - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

	VALUE	UNIT
V_{ESD} Electrostatic discharge Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±300	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

LM321

SNOS935C – FEBRUARY 2001 – REVISED DECEMBER 2014

www.ti.com

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Temperature Range	-40	85	°C
Supply Voltage	3	30	V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LM321	UNIT
	DBV	
	5 PINS	
R _{θJA} Junction-to-ambient thermal resistance	265	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Unless otherwise specified, all limits specified for at T_A = 25°C; V⁺ = 5 V, V⁻ = 0 V, V_O = 1.4 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OS}	Input Offset Voltage			⁽¹⁾ 2	7	mV
		⁽¹⁾ , -40°C ≤ T _J ≤ 85°C			9	
I _{OS}	Input Offset Current			5	50	nA
		-40°C ≤ T _J ≤ 85°C			150	
I _B	Input Bias Current ⁽²⁾			45	250	nA
		-40°C ≤ T _J ≤ 85°C			500	
V _{CM}	Input Common-Mode Voltage Range	V ⁺ = 30 V ⁽³⁾ , for CMRR > = 50dB	0		V ⁺ - 1.5	V
		V ⁺ = 30 V ⁽³⁾ , for CMRR > = 50dB, -40°C ≤ T _J ≤ 85°C			V ⁺ - 2	
A _V	Large Signal Voltage Gain	(V ⁺ = 15 V, R _L = 2kΩ, V _O = 1.4 V to 11.4 V)	25	100		V/mV
		(V ⁺ = 15 V, R _L = 2kΩ, V _O = 1.4 V to 11.4 V), -40°C ≤ T _J ≤ 85°C	15			
PSRR	Power Supply Rejection Ratio	R _S ≤ 10kΩ, V ⁺ ≤ 5 V to 30 V	65	100		dB
CMRR	Common Mode Rejection Ratio	R _S ≤ 10kΩ	65	85		dB
V _O	Output Swing	V _{OH} V ⁺ = 30 V, R _L = 2kΩ, -40°C ≤ T _J ≤ 85°C	26			V
		V ⁺ = 30 V, R _L = 10kΩ, -40°C ≤ T _J ≤ 85°C	27	28		
		V _{OL} V ⁺ = 5 V, R _L = 10kΩ, -40°C ≤ T _J ≤ 85°C		5	20	mV
I _S	Supply Current, No Load	V ⁺ = 5 V		0.430	1.15	mA
		V ⁺ = 5 V, -40°C ≤ T _J ≤ 85°C		0.7	1.2	
		V ⁺ = 30 V		0.660	2.85	
		V ⁺ = 30 V, -40°C ≤ T _J ≤ 85°C		1.5	3	
I _{SOURCE}	Output Current Sourcing	V _{ID} = +1 V, V ⁺ = 15 V, V _O = 2 V	20	40		mA
		V _{ID} = +1 V, V ⁺ = 15 V, V _O = 2 V, -40°C ≤ T _J ≤ 85°C	10	20		
I _{SINK}	Output Current Sinking	V _{ID} = -1 V, V ⁺ = 15 V, V _O = 2 V	10	20		mA
		V _{ID} = -1 V, V ⁺ = 15 V, V _O = 2 V, -40°C ≤ T _J ≤ 85°C	5	8		
		V _{ID} = -1 V, V ⁺ = 15 V, V _O = 0.2 V	12	100		μA

(1) V_O ≅ 1.4 V, R_S = 0Ω with V⁺ from 5 V to 30 V; and over the full input common-mode range (0 V to V⁺ - 1.5 V) at 25°C.

(2) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

(3) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V (at 25°C). The upper end of the common-mode voltage range is V⁺ - 1.5 V at 25°C, but either or both inputs can go to +32 V without damage, independent of the magnitude of V⁺.

Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for at $T_A = 25^\circ\text{C}$; $V^+ = 5\text{ V}$, $V^- = 0\text{ V}$, $V_O = 1.4\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_O Output Short Circuit to Ground ⁽⁴⁾	$V^+ = 15\text{ V}$		40	85	mA
SR Slew Rate	$V^+ = 15\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_{IN} = 0.5\text{ to }3\text{ V}$, $C_L = 100\text{ pF}$, Unity Gain		0.4		V/ μs
GBW Gain Bandwidth Product	$V^+ = 30\text{ V}$, $f = 100\text{ kHz}$, $V_{IN} = 10\text{ mV}$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		1		MHz
ϕ_m Phase Margin			60		degrees
THD Total Harmonic Distortion	$f = 1\text{ kHz}$, $A_V = 20\text{ dB}$, $R_L = 2\text{ k}\Omega$, $V_O = 2V_{PP}$, $C_L = 100\text{ pF}$, $V^+ = 30\text{ V}$		0.015%		
e_n Equivalent Input Noise Voltage	$f = 1\text{ kHz}$, $R_S = 100\Omega$, $V^+ = 30\text{ V}$		40		nV/ $\sqrt{\text{Hz}}$

- (4) Short circuits from the output V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground the maximum output current is approximately 40mA independent of the magnitude of V^+ . At values of supply voltage in excess of +15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

6.6 Typical Characteristics

Unless otherwise specified, $V_S = 5\text{ V}$, single supply, $T_A = 25^\circ\text{C}$.

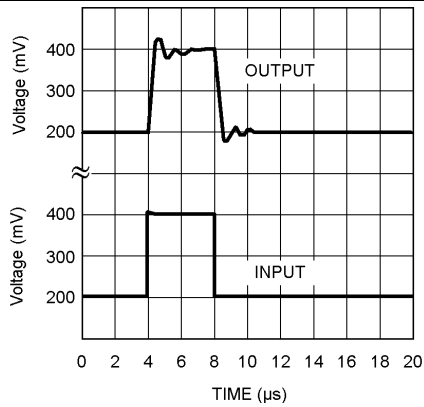


Figure 1. Small Signal Pulse Response

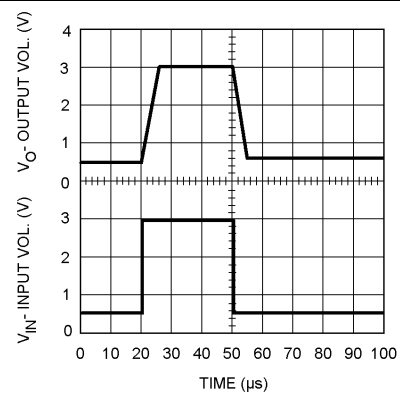


Figure 2. Large Signal Pulse Response

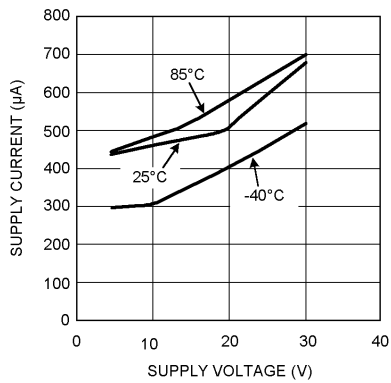


Figure 3. Supply Current vs. Supply Voltage

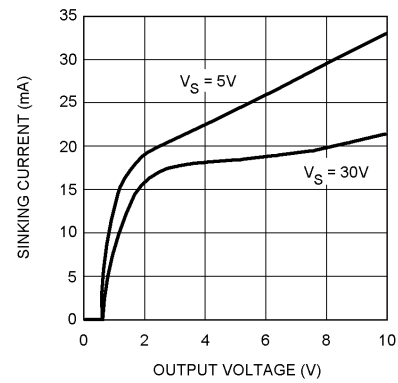


Figure 4. Sinking Current vs. Output Voltage

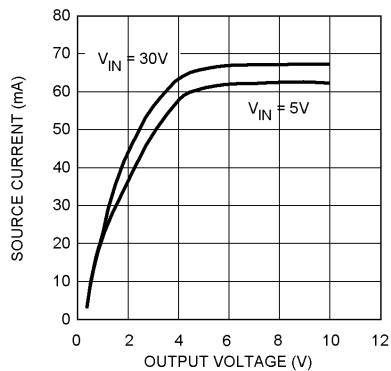


Figure 5. Source Current vs. Output Voltage

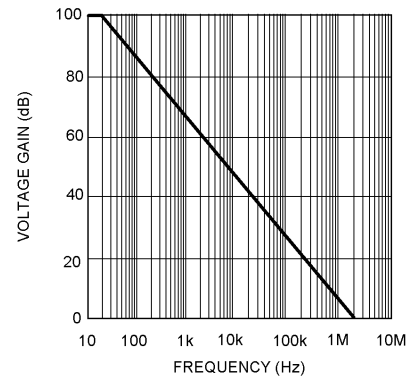


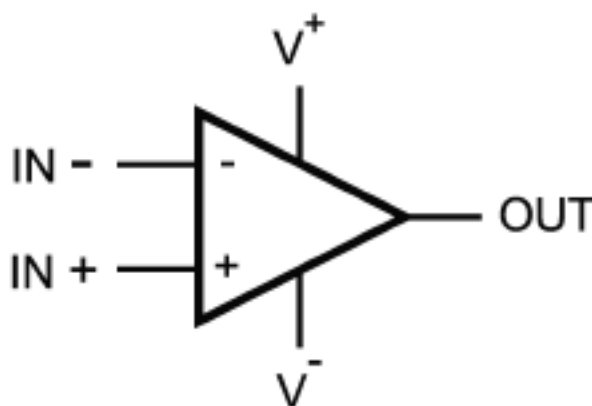
Figure 6. Open Loop Frequency Response

7 Detailed Description

7.1 Overview

The LM321 operational amplifier can operate with a single or dual power supply voltage, has true-differential inputs, and remains in the linear mode with an input common-mode voltage of 0 VDC. This amplifier operates over a wide range of power supply voltages, with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 3 V. Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 VDC (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

7.2 Functional Block Diagram



7.3 Feature Description

To reduce the power supply drain, the amplifier has a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on chip vertical PNP transistor for output current sinking applications.

For AC applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and to reduce distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if large load capacitance must be driven by the amplifier.

The bias network of the LM321 establishes a supply current which is independent of the magnitude of the power supply voltage over the range of from $3 V_{DC}$ to $30 V_{DC}$.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures than a standard IC operational amplifier.

7.4 Device Functional Modes

7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the LM321 series extends from 300 mV below ground to 32 V for normal operation. The typical performance in this range is summarized in [Table 1](#):

Table 1. Typical Performance Range (Vs = 5 V)

PARAMETER	MIN	TYP	MAX	UNIT
Input voltage range	–0.3		32	V
Offset voltage		2	7	mV
Offset voltage drift ($T_A = -40^{\circ}\text{C}$ to 85°C)			9	$\mu\text{V}/^{\circ}\text{C}$
CMRR	65	85		dB
PSRR	65	100		dB
Gain bandwidth product (GBP)		1		MHz
Slew rate		0.4		V/ μs
Phase margin		60		°
Equivalent input noise voltage		40		nV/ $\sqrt{\text{Hz}}$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM321 operational amplifier can operate with a single or dual power supply voltage, has true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. This amplifier operates over a wide range of power supply voltages, with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 3 V.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V⁺ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifier has a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For AC applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and to reduce distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if large load capacitance must be driven by the amplifier.

The bias network of the LM321 establishes a supply current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures than a standard IC operational amplifier.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard operational amplifier circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of V⁺/2) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

8.2 Typical Applications

8.2.1 Noninverting DC Gain (0-V Input = 0-V Output)

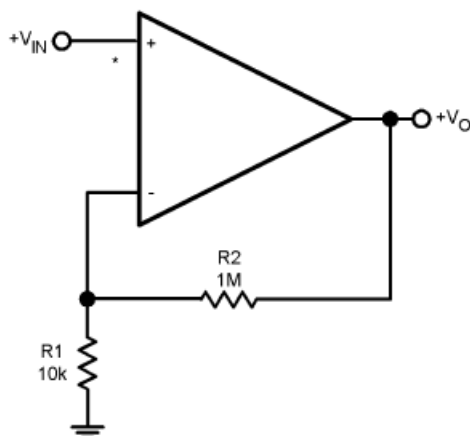


Figure 7. Non-Inverting DC Gain Schematic (0-V Input = 0-V Output)

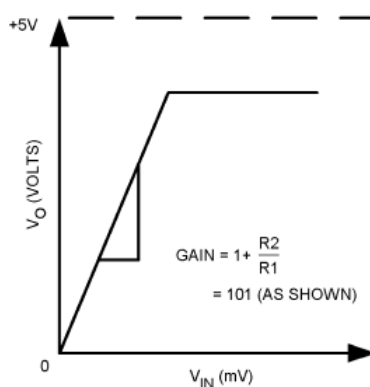
8.2.1.1 Design Requirements

- Supply voltage (up to 32 V)
- Phase margin: 60°

8.2.1.2 Detailed Design Procedure

- Connect 1-M Ω feedback resistor between the output and the inverting terminal of the amplifier.
- Connect 10-k Ω resistor between the inverting terminal and ground. Place the resistor as close to the inverting pin as possible.
- Connect power supply and input voltages.

8.2.1.3 Application Curve



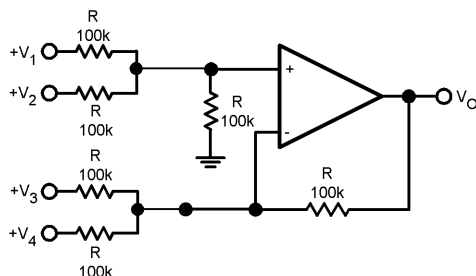
* R not needed due to temperature independent

Figure 8. Gain of the Noninverting Amplifier

Typical Applications (continued)

8.2.2 DC Summing Amplifier ($V_{IN's} \geq 0 V_{DC}$ and $V_O \geq V_{DC}$)

The summing amplifier, a special case of the inverting amplifier, is shown in Figure 7. The circuit gives an inverted output which is equal to the weighted algebraic sum of all four inputs. The gain of any input of this circuit is equal to the ratio of the appropriate input resistor to the feedback resistor. The advantage of this circuit is that there is no interaction between inputs and operations such as summing and weighted averaging are implemented very easily.



Where: $V_O = V_1 + V_2 - V_3 - V_4$, $(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0 V_{DC}$

Figure 9. DC Summing Amplifier Schematic
($V_{IN's} \geq 0 V_{DC}$ and $V_O \geq V_{DC}$)

8.2.3 Amplitude Modulator Circuit

The modulator circuit is shown in Figure 10. PWM signal is used to switch the MOSFET. When the MOSFET is on, the circuit acts as an inverting amplifier with gain 1. When The MOSFET is off, the inverting and non-inverting signals cancel each other out. Therefore, the output switches from $-V_{IN}$ to GND at the carrier frequency.

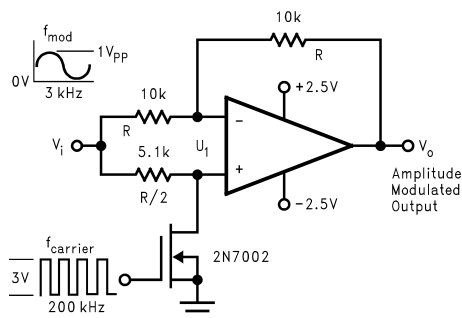
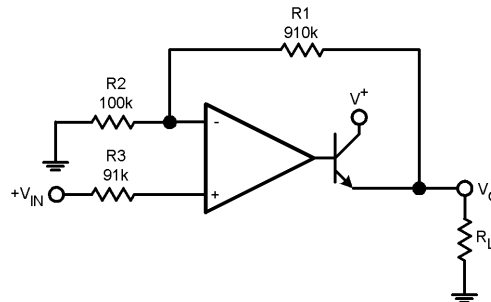


Figure 10. Amplitude Modulator Circuit Schematic

Typical Applications (continued)

8.2.4 Power Amplifier

Power amplifier application circuit is shown in [Figure 11](#). Voltage gain is set by R1 and R2. The output of the amplifier is connected to the base of BJT which amplifies the current. Current gain is set by β , current gain of a BJT. The resulting output provides high power to the load. Differential voltage supplies are necessary.



$$V_0 = 0 \text{ V}_{DC} \text{ for } V_{IN} = 0 \text{ V}_{DC}, A_V = 10$$

Figure 11. Power Amplifier Schematic

8.2.5 LED Driver

LM321 operating as an LED driver is shown in [Figure 12](#). The output of the amplifier sets the current through the diode. The voltage across the LED is assumed constant.

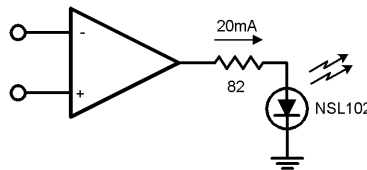


Figure 12. LED Driver Schematic

8.2.6 Fixed Current Sources

Operational amplifier can be used to provide fixed current source to multiple loads. The output voltage of the amplifier is connected to bases of bipolar transistors. The feedback is provided from the drain of a BJT to the inverting terminal of the amplifier. Currents in the second and later BJTs are set by the ratio of R1 and R2.

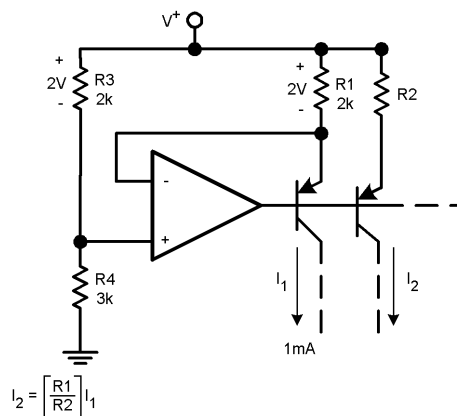


Figure 13. Fixed Current Sources Schematic

Typical Applications (continued)

8.2.7 Lamp Driver

Similar to the LED driver, LM321 can be used as a lamp driver. The output of the amplifier is to be connected to the base of a bipolar transistor which will drive $\beta \times$ output current of the amplifier through the lamp.

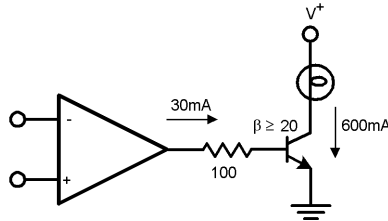


Figure 14. Lamp Driver Schematic

9 Power Supply Recommendations

The LM321 is specified for operation up to 32 V; many specifications apply from -40°C to 85°C . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in [Typical Characteristics](#). Place 0.1- μF bypass capacitors close to the power-supply terminals to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Layout](#).

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from $V+$ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, [SLOA089](#).
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [Figure 15](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

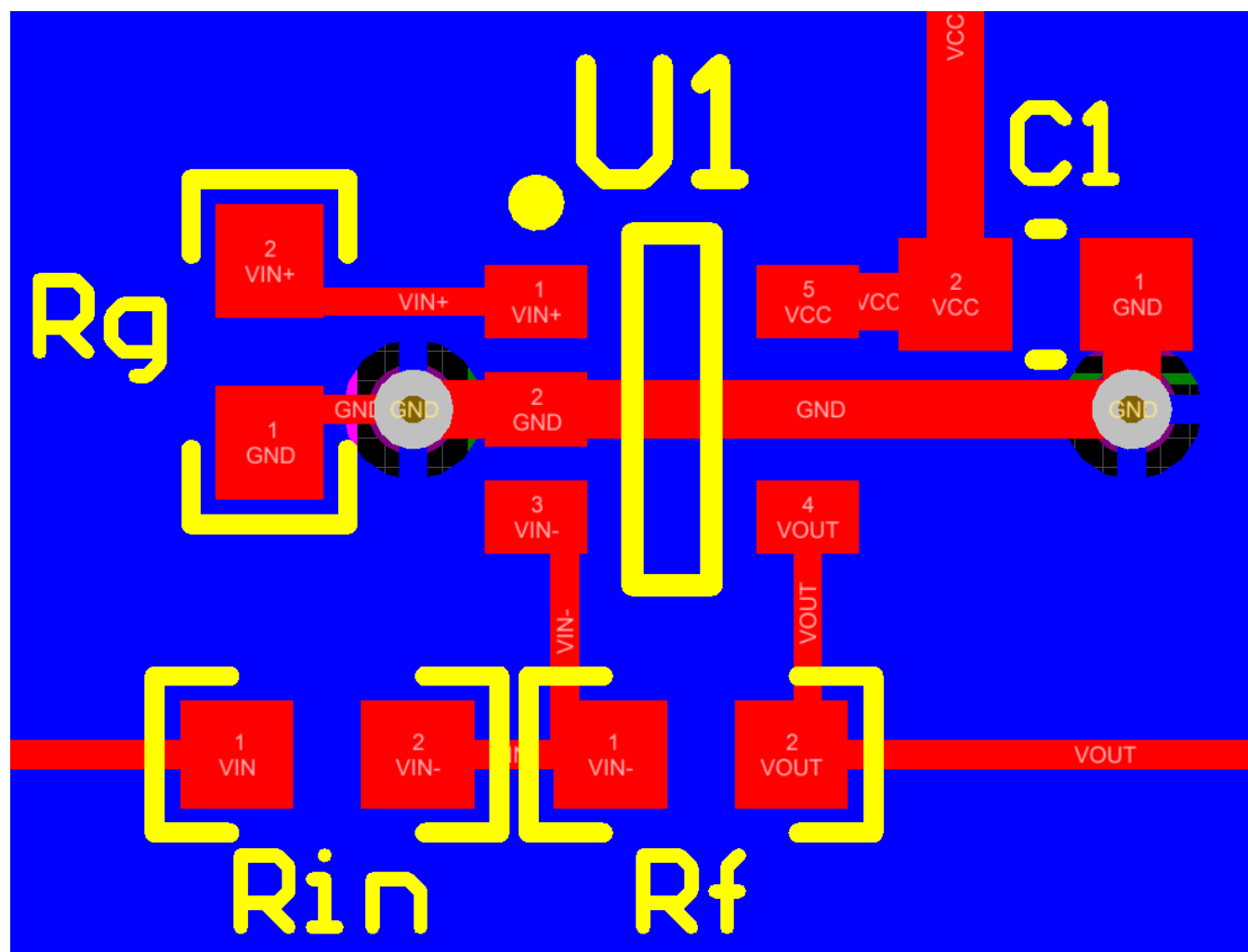


Figure 15. PCB Layout Example

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM321MF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A63A	
LM321MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A63A	Samples
LM321MFX	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A63A	
LM321MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A63A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and



www.ti.com

PACKAGE OPTION ADDENDUM

2-Aug-2015

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM321MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM321MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM321MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM321MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

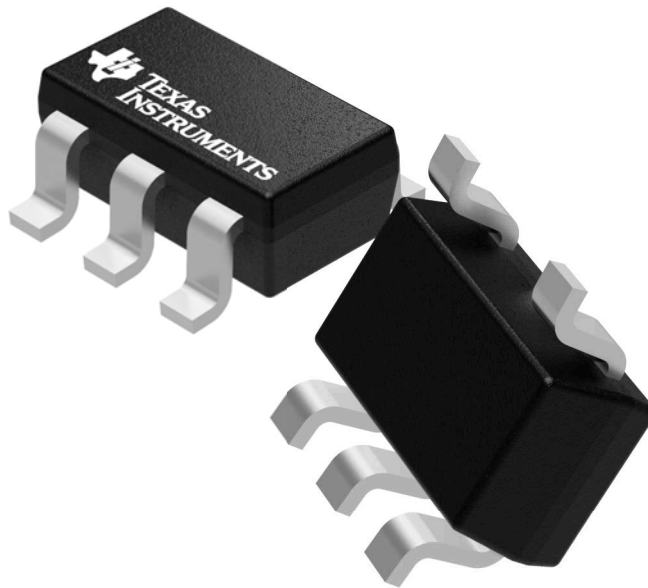
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM321MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM321MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM321MFX	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM321MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DBV 5

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073253/P

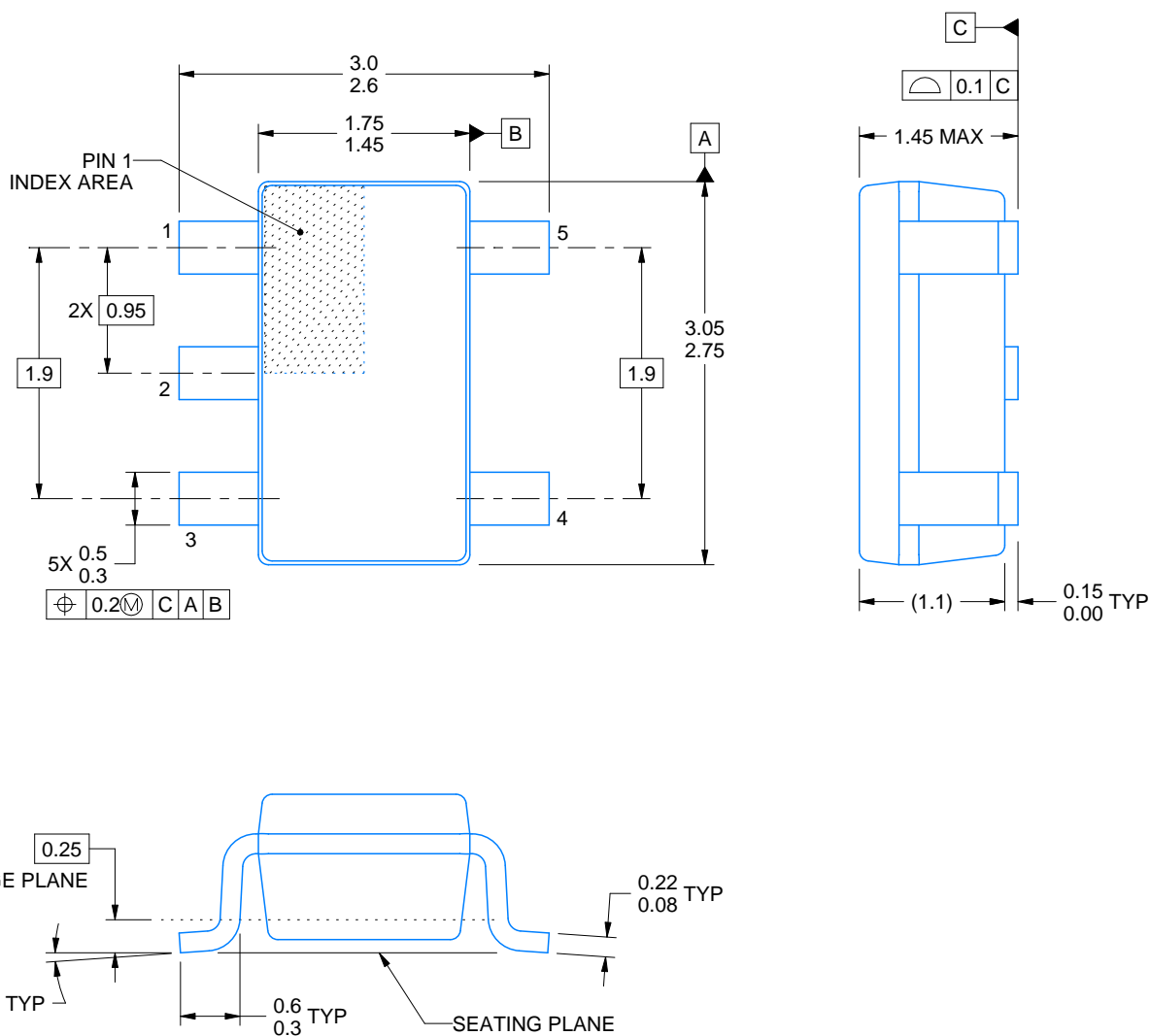


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

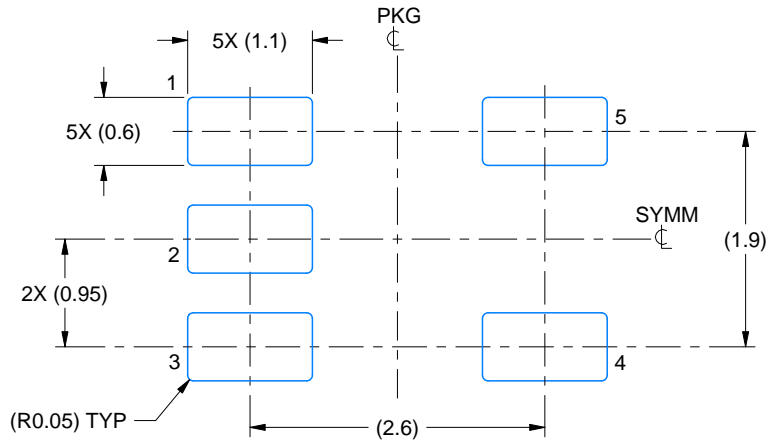
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

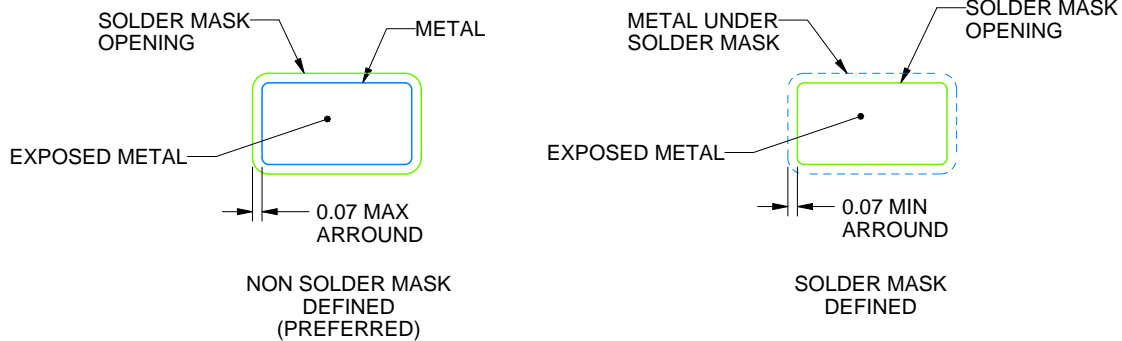
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

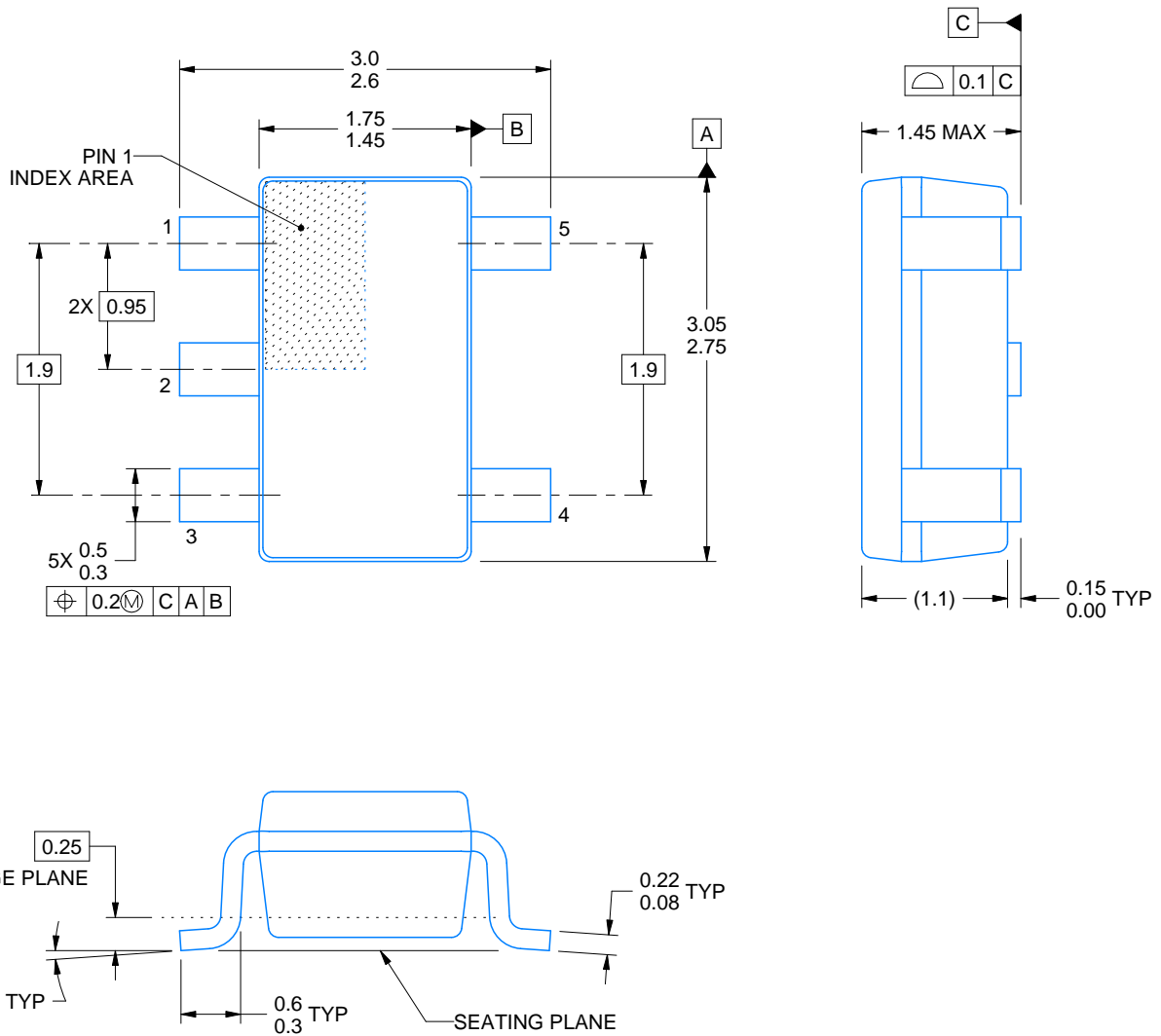


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

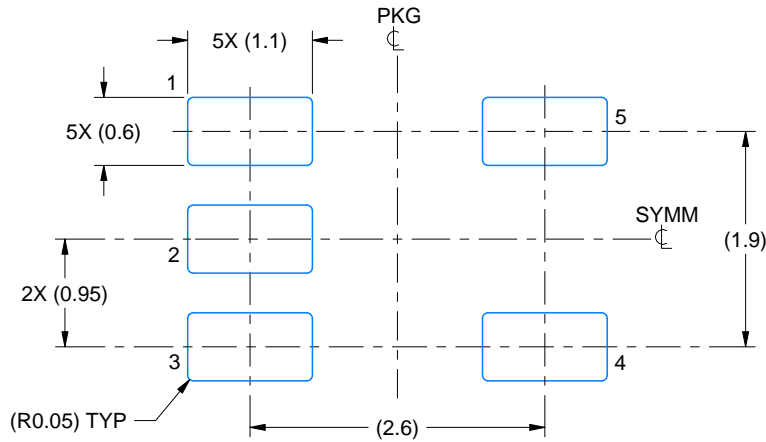
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

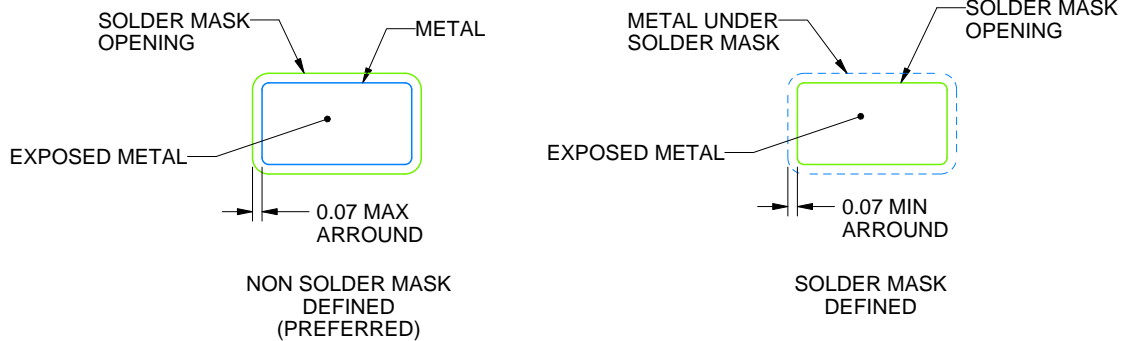
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

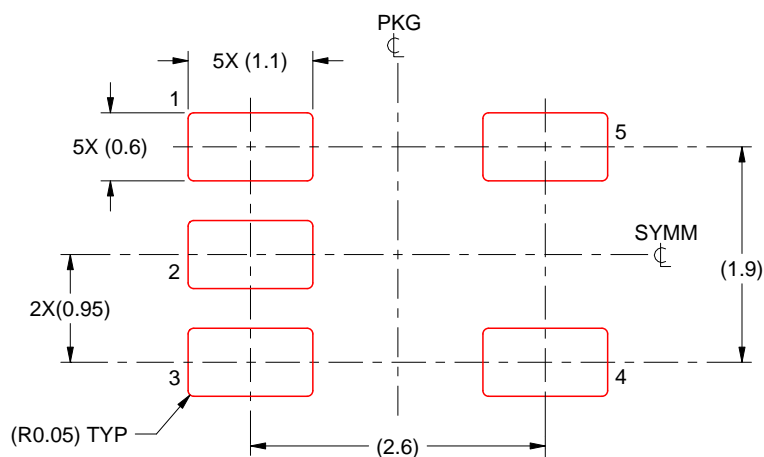
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Texas Instruments:

[LM3211MTX-ADJ/NOPB](#) [LM3215TL/NOPB](#) [LM3215TLX/NOPB](#) [LM321MF](#) [LM321MF/NOPB](#) [LM321MFX](#)
[LM321MFX/NOPB](#) [LM3215TLE-45/NOPB](#) [LM3215TLX-45/NOPB](#)