

# CDCLVC11xx 3.3-V and 2.5-V LVCMOS High-Performance Clock Buffer Family

## 1 Features

- High-Performance 1:2, 1:3, 1:4, 1:6, 1:8, 1:10, 1:12 LVCMOS Clock Buffer Family
- Very Low Pin-to-Pin Skew < 50 ps
- Very Low Additive Jitter < 100 fs
- Supply Voltage: 3.3 V or 2.5 V
- $f_{max} = 250$  MHz for 3.3 V  
 $f_{max} = 180$  MHz for 2.5 V
- Operating Temperature Range:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Available in 8-, 14-, 16-, 20-, 24-Pin TSSOP Package (All Pin-Compatible)

## 2 Applications

General-Purpose Communication, Industrial, and Consumer Applications

## 3 Description

The CDCLVC11xx is a modular, high-performance, low-skew, general-purpose clock buffer family from Texas Instruments.

The entire family is designed with a modular approach in mind. It is intended to round up TI's series of LVCMOS clock generators.

Seven different fan-out variations, 1:2 to 1:12, are available. All of the devices are pin-compatible to each other for easy handling.

All family members share the same high performing characteristics such as low additive jitter, low skew, and wide operating temperature range.

The CDCLVC11xx supports an asynchronous output enable control (1G) which switches the outputs into a low state when 1G is low.

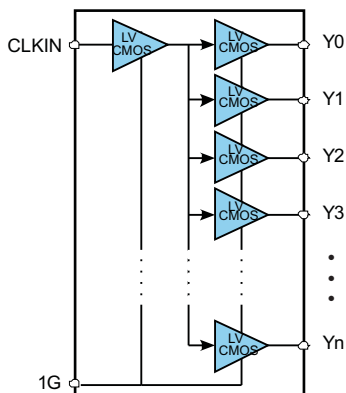
The CDCLVC11xx family operates in a 2.5-V and 3.3-V environment and are characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE    | BODY SIZE (NOM)   |
|-------------|------------|-------------------|
| CDCLVC1102  | TSSOP (8)  | 3.00 mm × 4.40 mm |
| CDCLVC1103  |            |                   |
| CDCLVC1104  |            |                   |
| CDCLVC1106  | TSSOP (14) | 5.00 mm × 4.40 mm |
| CDCLVC1108  | TSSOP (16) |                   |
| CDCLVC1110  | TSSOP (20) | 6.50 mm × 4.40 mm |
| CDCLVC1112  | TSSOP (24) | 7.80 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Functional Block Diagram



|       |    |             |    |     |
|-------|----|-------------|----|-----|
| CLKIN | 1  |             | 24 | Y1  |
| 1G    | 2  | CDCLVC 1102 | 23 | Y3  |
| Y0    | 3  | CDCLVC 1103 | 22 | VDD |
| GND   | 4  | CDCLVC 1104 | 21 | Y2  |
| VDD   | 5  |             | 20 | GND |
| Y4    | 6  | CDCLVC 1106 | 19 | Y5  |
| GND   | 7  |             | 18 | VDD |
| Y6    | 8  | CDCLVC 1108 | 17 | Y7  |
| VDD   | 9  |             | 16 | Y8  |
| Y9    | 10 | CDCLVC 1110 | 15 | GND |
| GND   | 11 |             | 14 | Y10 |
| Y11   | 12 | CDCLVC 1112 | 13 | VDD |



## Table of Contents

|  |           |  |           |
|--|-----------|--|-----------|
| <b>1 Features</b> .....                          | <b>1</b>  | 8.4 Device Functional Modes.....                                 | <b>10</b> |
| <b>2 Applications</b> .....                      | <b>1</b>  | <b>9 Application and Implementation</b> .....                    | <b>11</b> |
| <b>3 Description</b> .....                       | <b>1</b>  | 9.1 Application Information.....                                 | <b>11</b> |
| <b>4 Revision History</b> .....                  | <b>2</b>  | 9.2 Typical Application .....                                    | <b>11</b> |
| <b>5 Pin Configuration and Functions</b> .....   | <b>3</b>  | <b>10 Power Supply Recommendations</b> .....                     | <b>12</b> |
| <b>6 Specifications</b> .....                    | <b>5</b>  | 10.1 Power Considerations .....                                  | <b>13</b> |
| 6.1 Absolute Maximum Ratings .....               | <b>5</b>  | <b>11 Layout</b> .....   | <b>14</b> |
| 6.2 ESD Ratings.....                             | <b>5</b>  | 11.1 Layout Guidelines .....                                     | <b>14</b> |
| 6.3 Recommended Operating Conditions.....        | <b>5</b>  | 11.2 Layout Example .....  | <b>14</b> |
| 6.4 Thermal Information .....                    | <b>6</b>  | <b>12 Device and Documentation Support</b> .....                 | <b>15</b> |
| 6.5 Electrical Characteristics.....              | <b>6</b>  | 12.1 Related Links .....   | <b>15</b> |
| 6.6 Switching Characteristics .....              | <b>7</b>  | 12.2 Receiving Notification of Documentation Updates .....       | <b>15</b> |
| 6.7 Typical Characteristics .....                | <b>7</b>  | 12.3 Community Resources.....                                    | <b>15</b> |
| <b>7 Parameter Measurement Information</b> ..... | <b>8</b>  | 12.4 Trademarks .....  | <b>15</b> |
| <b>8 Detailed Description</b> .....              | <b>10</b> | 12.5 Electrostatic Discharge Caution.....                        | <b>15</b> |
| 8.1 Overview .....                               | <b>10</b> | 12.6 Glossary .....  | <b>15</b> |
| 8.2 Functional Block Diagram .....               | <b>10</b> | <b>13 Mechanical, Packaging, and Orderable Information</b> ..... | <b>15</b> |
| 8.3 Feature Description.....                     | <b>10</b> |  |           |

## 4 Revision History

| Changes from Revision A (October 2014) to Revision B   | Page      |
|--|-----------|
| • Changed Packaging name from <i>TTSOP</i> to <i>TSSOP</i> in <i>Device Information Table</i> .....          | <b>1</b>  |
| • Changed CDCLVC1110 Y8 pin number from: 10 to: 12 .....   | <b>3</b>  |
| • Changed CDCLVC1110 Y9 pin number from: — to: 10.....   | <b>3</b>  |
| • Moved $T_{stg}$ from <i>ESD Ratings</i> to <i>Absolute Maximum Ratings</i> .....                           | <b>5</b>  |
| • Added <i>Receiving Notification of Documentation Updates</i> and <i>Community Resources</i> sections ..... | <b>15</b> |

| Changes from Original (May 2010) to Revision A   | Page     |
|--|----------|
| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | <b>1</b> |

## 5 Pin Configuration and Functions

**PW Package**  
**8-, 14-, 16-, 20, 24-Pin TSSOP**  
**Top View**

|       |   |   |     |
|-------|---|---|-----|
| CLKIN | 1 | 8 | Y 1 |
| 1G    | 2 | 7 | NC  |
| Y 0   | 3 | 6 | VDD |
| GND   | 4 | 5 | NC  |

|       |   |   |     |
|-------|---|---|-----|
| CLKIN | 1 | 8 | Y 1 |
| 1G    | 2 | 7 | NC  |
| Y 0   | 3 | 6 | VDD |
| GND   | 4 | 5 | Y 2 |

|       |   |   |     |
|-------|---|---|-----|
| CLKIN | 1 | 8 | Y 1 |
| 1G    | 2 | 7 | Y 3 |
| Y 0   | 3 | 6 | VDD |
| GND   | 4 | 5 | Y 2 |

|       |   |    |     |
|-------|---|----|-----|
| CLKIN | 1 | 14 | Y 1 |
| 1G    | 2 | 13 | Y 3 |
| Y 0   | 3 | 12 | VDD |
| GND   | 4 | 11 | Y 2 |
| VDD   | 5 | 10 | GND |
| Y 4   | 6 | 9  | Y 5 |
| GND   | 7 | 8  | VDD |

|       |   |    |     |
|-------|---|----|-----|
| CLKIN | 1 | 16 | Y 1 |
| 1G    | 2 | 15 | Y 3 |
| Y 0   | 3 | 14 | VDD |
| GND   | 4 | 13 | Y 2 |
| VDD   | 5 | 12 | GND |
| Y 4   | 6 | 11 | Y 5 |
| GND   | 7 | 10 | VDD |
| Y 6   | 8 | 9  | Y 7 |

|       |    |    |     |
|-------|----|----|-----|
| CLKIN | 1  | 20 | Y 1 |
| 1G    | 2  | 19 | Y 3 |
| Y 0   | 3  | 18 | VDD |
| GND   | 4  | 17 | Y 2 |
| VDD   | 5  | 16 | GND |
| Y 4   | 6  | 15 | Y 5 |
| GND   | 7  | 14 | VDD |
| Y 6   | 8  | 13 | Y 7 |
| VDD   | 9  | 12 | Y 8 |
| Y 9   | 10 | 11 | GND |

|       |    |    |      |
|-------|----|----|------|
| CLKIN | 1  | 24 | Y 1  |
| 1G    | 2  | 23 | Y 3  |
| Y 0   | 3  | 22 | VDD  |
| GND   | 4  | 21 | Y 2  |
| VDD   | 5  | 20 | GND  |
| Y 4   | 6  | 19 | Y 5  |
| GND   | 7  | 18 | VDD  |
| Y 6   | 8  | 17 | Y 7  |
| VDD   | 9  | 16 | Y 8  |
| Y 9   | 10 | 15 | GND  |
| GND   | 11 | 14 | Y 10 |
| Y 11  | 12 | 13 | VDD  |

**Pin Functions**

| PIN                 |             |             |             |             |             |             |             | TYPE   | DESCRIPTION   |
|---------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|--------|---|
| NAME                | CDCLVC 1102 | CDCLVC 1103 | CDCLVC 1104 | CDCLVC 1106 | CDCLVC 1108 | CDCLVC 1110 | CDCLVC 1112 |        |   |
| LVCMOS CLOCK INPUT  |             |             |             |             |             |             |             |        |   |
| CLKIN               | 1           | 1           | 1           | 1           | 1           | 1           | 1           | Input  | Input Pin   |
| CLOCK OUTPUT ENABLE |             |             |             |             |             |             |             |        |   |
| 1G                  | 2           | 2           | 2           | 2           | 2           | 2           | 2           | Input  | Output Enable                                       |
| LVCMOS CLOCK OUTPUT |             |             |             |             |             |             |             |        |   |
| Y0                  | 3           | 3           | 3           | 3           | 3           | 3           | 3           | Output | LVCMOS output. Unused outputs can be left floating. |
| Y1                  | 8           | 8           | 8           | 14          | 16          | 20          | 24          |        |   |
| Y2                  | —           | 5           | 5           | 11          | 13          | 17          | 21          |        |   |
| Y3                  | —           | —           | 7           | 13          | 15          | 19          | 23          |        |   |
| Y4                  | —           | —           | —           | 6           | 6           | 6           | 6           |        |   |
| Y5                  | —           | —           | —           | 9           | 11          | 15          | 19          |        |   |
| Y6                  | —           | —           | —           | —           | 8           | 8           | 8           |        |   |
| Y7                  | —           | —           | —           | —           | 9           | 13          | 17          |        |   |
| Y8                  | —           | —           | —           | —           | —           | 12          | 16          |        |   |
| Y9                  | —           | —           | —           | —           | —           | 10          | 10          |        |   |
| Y10                 | —           | —           | —           | —           | —           | —           | 14          |        |   |
| Y11                 | —           | —           | —           | —           | —           | —           | 12          |        |   |
| SUPPLY VOLTAGE      |             |             |             |             |             |             |             |        |   |
| V <sub>DD</sub>     | 6           | 6           | 6           | 5           | 5           | 5           | 5           | Power  | 2.5-V or device supply                              |
|                     |             |             |             |             |             | 9           |             |        |   |
|                     |             |             |             | 9           | 13          |             |             |        |   |
|                     |             |             |             | 8           | 10          | 14          | 18          |        |   |
|                     |             |             |             | 12          | 14          | 18          | 22          |        |   |
| GROUND              |             |             |             |             |             |             |             |        |   |

Pin Functions (continued)

| NAME | PIN            |                |                |                |                |                |                | TYPE | DESCRIPTION   |
|------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|------|---------------|
|      | CDCLVC<br>1102 | CDCLVC<br>1103 | CDCLVC<br>1104 | CDCLVC<br>1106 | CDCLVC<br>1108 | CDCLVC<br>1110 | CDCLVC<br>1112 |      |               |
| GND  | 4              | 4              | 4              | 4              | 4              | 4              | 4              | GND  | Device ground |
|      |                |                |                |                |                |                | 7              |      |               |
|      |                |                |                | 7              | 7              | 11             | 11             |      |               |
|      |                |                |                |                |                |                | 15             |      |               |
|      |                |                |                | 10             | 12             | 16             | 20             |      |               |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                  |                               | MIN  | MAX                   | UNIT |
|------------------|-------------------------------|------|-----------------------|------|
| V <sub>DD</sub>  | Supply voltage                | −0.5 | 4.6                   | V    |
| V <sub>IN</sub>  | Input voltage <sup>(2)</sup>  | −0.5 | V <sub>DD</sub> + 0.5 | V    |
| V <sub>O</sub>   | Output voltage <sup>(2)</sup> | −0.5 | V <sub>DD</sub> + 0.5 | V    |
| I <sub>IN</sub>  | Input current                 | −20  | 20                    | mA   |
| I <sub>O</sub>   | Continuous output current     | −50  | 50                    | mA   |
| T <sub>J</sub>   | Maximum junction temperature  |      | 125                   | °C   |
| T <sub>stg</sub> | Storage temperature           | −65  | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This value is limited to 4.6 V maximum.

### 6.2 ESD Ratings

|                    |                         | VALUE  | UNIT  |
|--------------------|-------------------------|--|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±4000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1500 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                                 |                                | MIN                              | NOM                      | MAX                      | UNIT |
|---------------------------------|--------------------------------|----------------------------------|--------------------------|--------------------------|------|
| V <sub>DD</sub>                 | Supply voltage                 | 3.3-V supply                     | 3.0                      | 3.3                      | 3.6  |
|                                 |                                | 2.5-V supply                     | 2.3                      | 2.5                      | 2.7  |
| V <sub>IL</sub>                 | Low-level input voltage        | V <sub>DD</sub> = 3.0 V to 3.6 V |                          | V <sub>DD</sub> /2 − 600 | mV   |
|                                 |                                | V <sub>DD</sub> = 2.3 V to 2.7 V |                          | V <sub>DD</sub> /2 − 400 |      |
| V <sub>IH</sub>                 | High-level input voltage       | V <sub>DD</sub> = 3.0 V to 3.6 V | V <sub>DD</sub> /2 + 600 |                          | mV   |
|                                 |                                | V <sub>DD</sub> = 2.3 V to 2.7 V | V <sub>DD</sub> /2 + 400 |                          |      |
| V <sub>th</sub>                 | Input threshold voltage        | V <sub>DD</sub> = 2.3 V to 3.6 V | V <sub>DD</sub> /2       |                          | mV   |
| t <sub>r</sub> / t <sub>f</sub> | Input slew rate                |                                  | 1                        | 4                        | V/ns |
| t <sub>w</sub>                  | Minimum pulse width at CLKIN   | V <sub>DD</sub> = 3.0 V to 3.6 V | 1.8                      |                          | ns   |
|                                 |                                | V <sub>DD</sub> = 2.3 V to 2.7 V | 2.75                     |                          |      |
| f <sub>CLK</sub>                | LVCMOS clock Input Frequency   | V <sub>DD</sub> = 3.0 V to 3.6 V | DC                       | 250                      | MHz  |
|                                 |                                | V <sub>DD</sub> = 2.3 V to 2.7 V | DC                       | 180                      |      |
| T <sub>A</sub>                  | Operating free-air temperature | −40                              |                          | 85                       | °C   |

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |   | CDCLVC1102<br>CDCLVC1103<br>CDCLVC1104 | CDCLVC1106 | CDCLVC1108 | CDCLVC11010 | CDCLVC1112 | UNIT |
|-------------------------------|---|--|------------|------------|-------------|------------|------|
|                               |   | PW (TSSOP)                             |            |            |             |            |      |
|                               |   | 8 PINS                                 | 14 PINS    | 16 PINS    | 20 PINS     | 24 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance <sup>(2)</sup>   | 149.4                                  | 112.6      | 108.4      | 83.0        | 87.9       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case(top) thermal resistance <sup>(3)</sup> | 69.4                                   | 48.0       | 33.6       | 32.3        | 26.5       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## 6.5 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER   |   | TEST CONDITIONS  | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|---|---|--|-----|--------------------|-----|------|
| OVERALL PARAMETERS FOR ALL VERSIONS                   |   |  |     |                    |     |      |
| I <sub>DD</sub>                                       | Static device current <sup>(2)</sup>                    | 1G = V <sub>DD</sub> ; CLKIN = 0 V or V <sub>DD</sub> ; I <sub>O</sub> = 0 mA; V <sub>DD</sub> = 3.6 V |     | 6                  | 10  | mA   |
|   |   | 1G = V <sub>DD</sub> ; CLKIN = 0 V or V <sub>DD</sub> ; I <sub>O</sub> = 0 mA; V <sub>DD</sub> = 2.7 V |     | 3                  | 6   |      |
| I <sub>PD</sub>                                       | Power-down current                                      | 1G = 0 V; CLKIN = 0 V or V <sub>DD</sub> ; I <sub>O</sub> = 0 mA; V <sub>DD</sub> = 3.6 V or 2.7 V     |     |                    | 60  | μA   |
| C <sub>PD</sub>                                       | Power dissipation capacitance per output <sup>(3)</sup> | V <sub>DD</sub> = 3.3 V; f = 10 MHz  |     | 6                  |     | pF   |
|   |   | V <sub>DD</sub> = 2.5 V; f = 10 MHz  |     | 4.5                |     |      |
| I <sub>I</sub>  | Input leakage current at 1G                             | V <sub>I</sub> = 0 V or V <sub>DD</sub> ; V <sub>DD</sub> = 3.6 V or 2.7 V                             |     | 8                  | 8   | μA   |
|   | Input leakage current at CLKIN                          |  |     | 25                 | 25  |      |
| R <sub>OUT</sub>                                      | Output impedance  | V <sub>DD</sub> = 3.3 V  |     | 45                 |     | Ω    |
|   |   | V <sub>DD</sub> = 2.5 V  |     | 60                 |     |      |
| f <sub>OUT</sub>                                      | Output frequency  | V <sub>DD</sub> = 3 V to 3.6 V   |     | DC                 | 250 | MHz  |
|   |   | V <sub>DD</sub> = 2.3 V to 2.7 V   |     | DC                 | 180 |      |
| OUTPUT PARAMETERS FOR V <sub>DD</sub> = 3.3 V ± 0.3 V |   |  |     |                    |     |      |
| V <sub>OH</sub>                                       | High-level output voltage                               | V <sub>DD</sub> = 3 V, I <sub>OH</sub> = −0.1 mA   |     | 2.9                |     | V    |
|   |   | V <sub>DD</sub> = 3 V, I <sub>OH</sub> = −8 mA   |     | 2.5                |     |      |
|   |   | V <sub>DD</sub> = 3 V, I <sub>OH</sub> = −12 mA  |     | 2.2                |     |      |
| V <sub>OL</sub>                                       | Low-level output voltage                                | V <sub>DD</sub> = 3 V, I <sub>OL</sub> = 0.1 mA  |     |                    | 0.1 | V    |
|   |   | V <sub>DD</sub> = 3 V, I <sub>OL</sub> = 8 mA  |     |                    | 0.5 |      |
|   |   | V <sub>DD</sub> = 3 V, I <sub>OL</sub> = 12 mA   |     |                    | 0.8 |      |
| OUTPUT PARAMETERS FOR V <sub>DD</sub> = 2.5 V ± 0.2 V |   |  |     |                    |     |      |
| V <sub>OH</sub>                                       | High-level output voltage                               | V <sub>DD</sub> = 2.3 V, I <sub>OH</sub> = −0.1 mA   |     | 2.2                |     | V    |
|   |   | V <sub>DD</sub> = 2.3 V, I <sub>OH</sub> = −8 mA   |     | 1.7                |     |      |
| V <sub>OL</sub>                                       | Low-level output voltage                                | V <sub>DD</sub> = 2.3 V, I <sub>OL</sub> = 0.1 mA  |     |                    | 0.1 | V    |
|   |   | V <sub>DD</sub> = 2.3 V, I <sub>OL</sub> = 8 mA  |     |                    | 0.5 |      |

- (1) All typical values are at respective nominal V<sub>DD</sub>. For switching characteristics, outputs are terminated to 50 Ω to V<sub>DD</sub>/2 (see [Figure 3](#)).
- (2) For dynamic I<sub>DD</sub> over frequency see and [Figure 1](#).
- (3) This is the formula for the power dissipation calculation (see and the [Power Considerations](#) section).
- $$P_{\text{tot}} = P_{\text{stat}} + P_{\text{dyn}} + P_{\text{Cload}} \text{ [W]}$$
- $$P_{\text{stat}} = V_{\text{DD}} \times I_{\text{DD}} \text{ [W]}$$
- $$P_{\text{dyn}} = C_{\text{PD}} \times V_{\text{DD}}^2 \times f \text{ [W]}$$
- $$P_{\text{Cload}} = C_{\text{load}} \times V_{\text{DD}}^2 \times f \times n \text{ [W]}$$
- n = Number of switching output pins

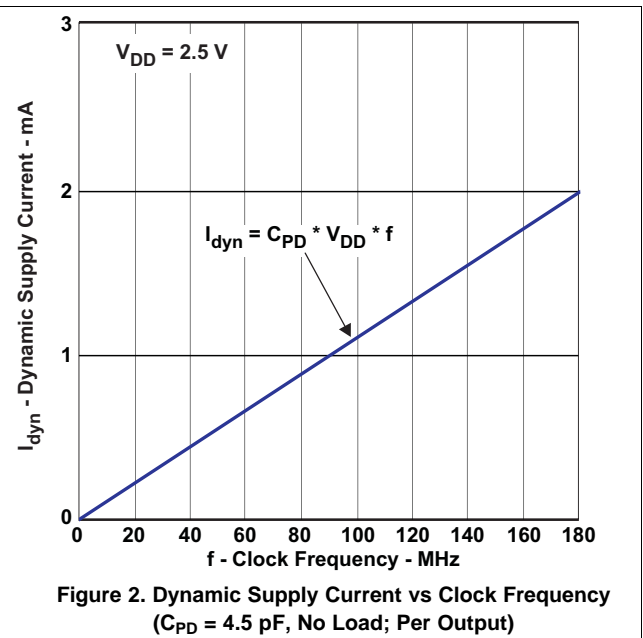
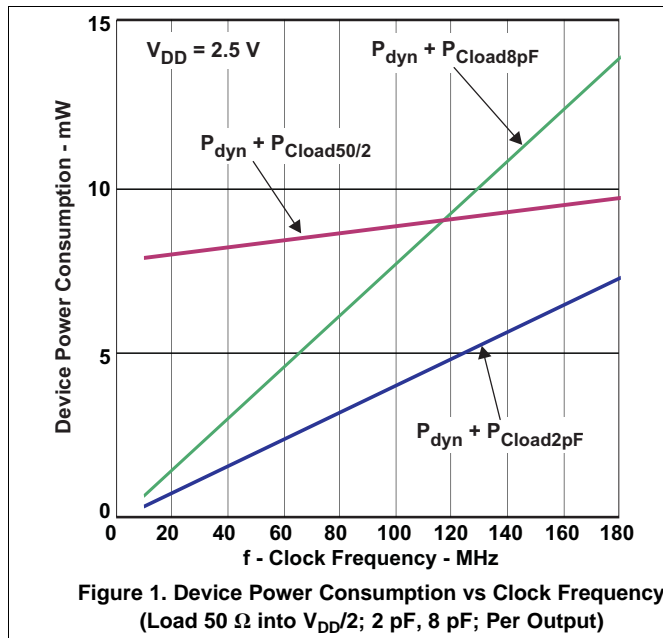
## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

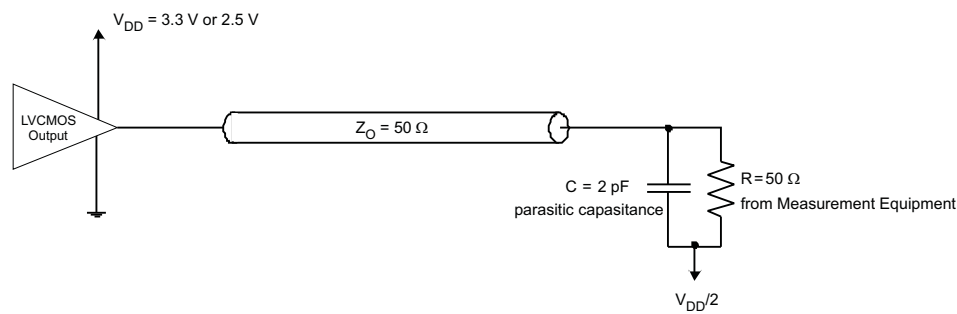
| PARAMETER  | TEST CONDITIONS                                | MIN | TYP | MAX | UNIT |
|--|--|-----|-----|-----|------|
| <b>OUTPUT PARAMETERS FOR <math>V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}</math></b> |  |     |     |     |      |
| $t_{PLH}$ , $t_{PHL}$ Propagation delay  | CLKIN to Yn                                    | 0.8 |     | 2.0 | ns   |
| $t_{sk(o)}$ Output skew  | Equal load of each output                      |     |     | 50  | ps   |
| $t_r/t_f$ Rise and fall time   | 20%–80% ( $V_{OH} - V_{OL}$ )                  | 0.3 |     | 0.8 | ns   |
| $t_{DIS}$ Output disable time  | 1G to Yn                                       |     |     | 6   | ns   |
| $t_{EN}$ Output enable time  | 1G to Yn                                       |     |     | 6   | ns   |
| $t_{sk(p)}$ Pulse skew ;<br>$t_{PLH(Yn)} - t_{PHL(Yn)}$ <sup>(1)</sup>           | To be measured with input duty cycle of 50%    |     |     | 180 | ps   |
| $t_{sk(pp)}$ Part-to-part skew   | Under equal operating conditions for two parts |     |     | 0.5 | ns   |
| $t_{jitter}$ Additive jitter rms <sup>(2)</sup>                                  | 12 kHz to 20 MHz, $f_{OUT} = 250\text{ MHz}$   |     |     | 100 | fs   |
| <b>OUTPUT PARAMETERS FOR <math>V_{DD} = 2.5\text{ V} \pm 0.2\text{ V}</math></b> |  |     |     |     |      |
| $t_{PLH}$ , $t_{PHL}$ Propagation delay  | CLKIN to Yn                                    | 1   |     | 2.6 | ns   |
| $t_{sk(o)}$ Output skew  | Equal load of each output                      |     |     | 50  | ps   |
| $t_r/t_f$ Rise and fall time   | 20%–80% reference point                        | 0.3 |     | 1.2 | ns   |
| $t_{DIS}$ Output disable time  | 1G to Yn                                       |     |     | 10  | ns   |
| $t_{EN}$ Output enable time  | 1G to Yn                                       |     |     | 10  | ns   |
| $t_{sk(p)}$ Pulse skew ;<br>$t_{PLH(Yn)} - t_{PHL(Yn)}$ <sup>(1)</sup>           | To be measured with input duty cycle of 50%    |     |     | 220 | ps   |
| $t_{sk(pp)}$ Part-to-part skew   | Under equal operating conditions for two parts |     |     | 1.2 | ns   |
| $t_{jitter}$ Additive jitter rms <sup>(2)</sup>                                  | 12 kHz to 20 MHz, $f_{OUT} = 180\text{ MHz}$   |     |     | 350 | fs   |

- (1)  $t_{sk(p)}$  depends on output rise- and fall-time ( $t_r/t_f$ ). The output duty-cycle can be calculated:  $odc = (t_{w(OUT)} \pm t_{sk(p)})/t_{period}$ ;  $t_{w(OUT)}$  is pulse-width of output waveform and  $t_{period}$  is  $1/f_{OUT}$ .  
(2) Parameter is specified by characterization. Not tested in production.

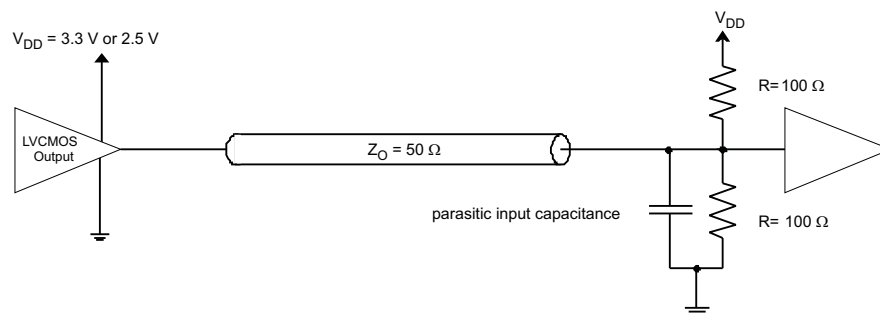
## 6.7 Typical Characteristics



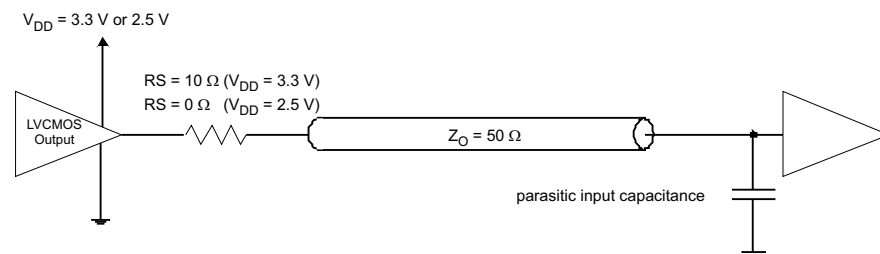
## 7 Parameter Measurement Information



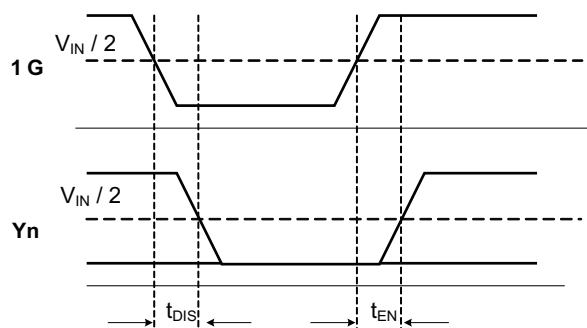
### Figure 3. Test Load Circuit



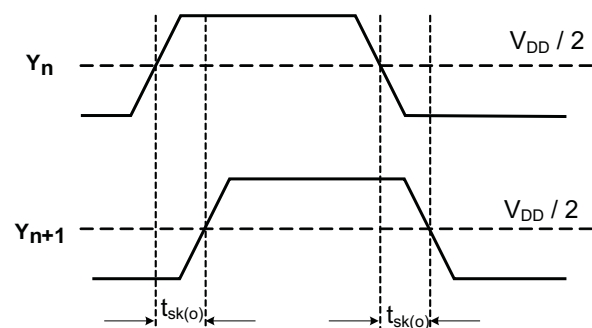
#### Figure 4. Application Load With 50-Ω Line Termination



### Figure 5. Application Load With Series Line Termination



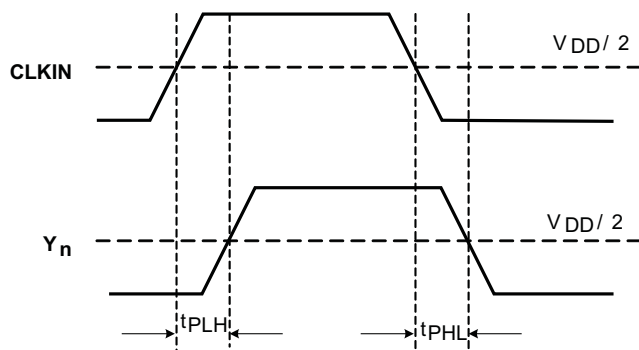
**Figure 6.  $t_{DIS}$  and  $t_{EN}$  for Disable Low**



**Figure 7. Output Skew  $t_{sk(o)}$**

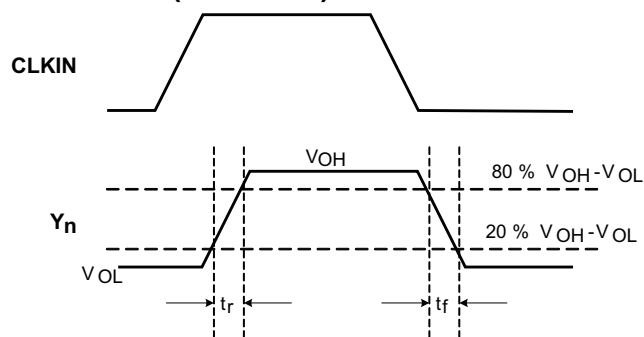


### Parameter Measurement Information (continued)



Note:  $t_{sk(p)} = |t_{PLH} - t_{PHL}|$

**Figure 8. Pulse Skew  $t_{sk(p)}$  and Propagation Delay  $t_{PLH}/t_{PHL}$**



**Figure 9. Rise/Fall Times  $t_r/t_f$**

## 8 Detailed Description

### 8.1 Overview

The CDCLVC11xx family of devices is a low-jitter and low-skew LVCMOS fan-out buffer solution. For best signal integrity, it is important to match the characteristic impedance of the CDCLVC11xx's output driver with that of the transmission line. [Figure 5](#) and [Figure 6](#) show the proper configuration per configuration for both  $V_{DD} = 3.3\text{ V}$  and  $V_{DD} = 2.5\text{ V}$ . TI recommends placing the series resistor close to the driver to minimize signal reflection.

### 8.2 Functional Block Diagram

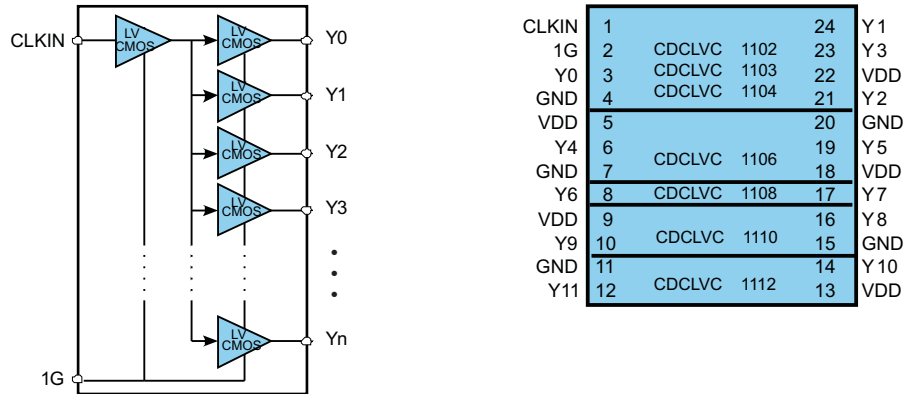


Table 1. Output Logic Table

| INPUTS |    | OUTPUTS |
|--------|----|---------|
| CLKIN  | 1G | Yn      |
| X      | L  | L       |
| L      | H  | L       |
| H      | H  | H       |

### 8.3 Feature Description

The outputs of the CDCLVC11xx can be disabled by driving the asynchronous output enable pin (1G) low. Unused output can be left floating to reduce overall system component cost. All supply and ground pins must be connected to  $V_{DD}$  and GND, respectively.

### 8.4 Device Functional Modes

The CDCLVC11xx operates from supplies between 2.5 V and 3.3 V.

## 9 Application and Implementation

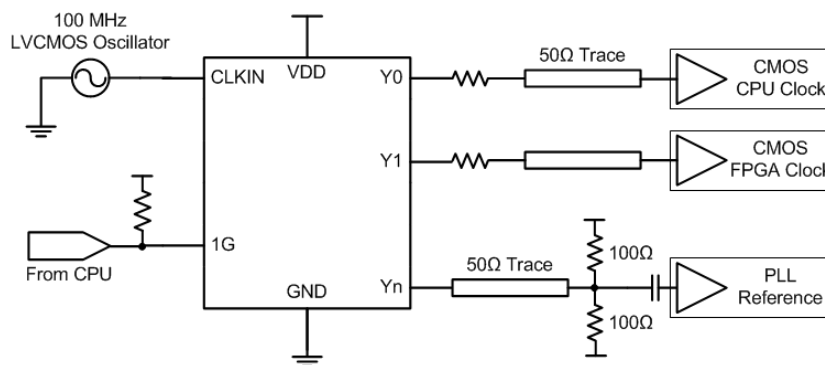
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The CDCLVC11xx family is a low additive jitter LVCMOS buffer solution that can operate up to 250 MHz at and 180 MHz at  $V_{DD} = 2.5$  V. Low output skew as well as the ability for asynchronous output enable is featured to simultaneously enable or disable buffered clock outputs as necessary in the application.

### 9.2 Typical Application



**Figure 10. Example System Configuration**

#### 9.2.1 Design Requirements

The CDCLVC11xx shown in [Figure 10](#) is configured to fan out a 100-MHz signal from a local LVCMOS oscillator. The CPU is configured to control the output state through 1G.

The configuration example is driving three LVCMOS receivers in a backplane application with the following properties:

- The CPU clock can accept a full swing DC-coupled LVCMOS signal. A series resistor is placed near the CDCLVC11xx to closely match the characteristic impedance of the trace to minimize reflections.
- The FPGA clock is similarly DC-coupled with an appropriate series resistor placed near the CDCLVC11xx.
- The PLL in this example can accept a lower amplitude signal, so a Thevenin's equivalent termination is used. The PLL receiver features internal biasing, so AC coupling can be used when common-mode voltage is mismatched.

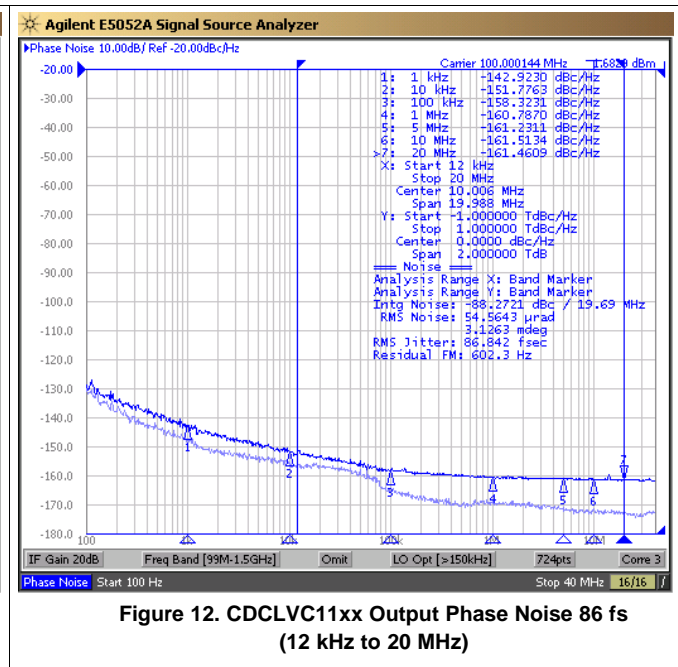
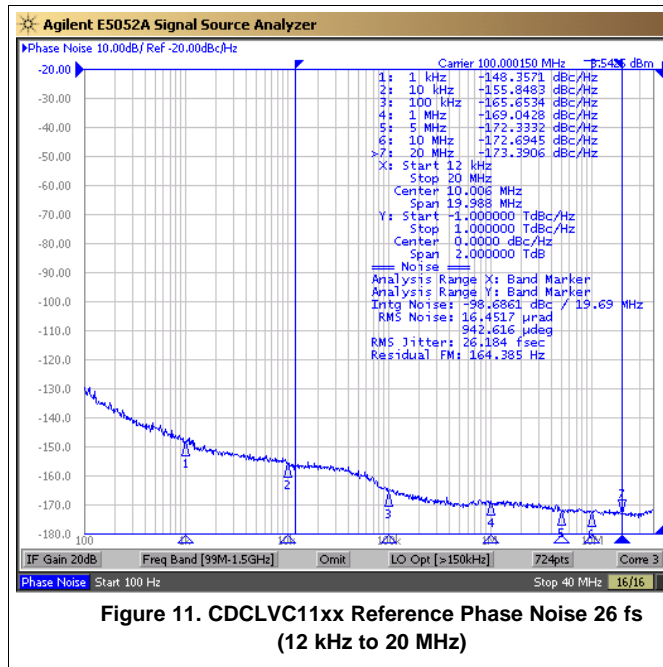
#### 9.2.2 Detailed Design Procedure

Refer to [Figure 5](#) and the [Electrical Characteristics](#) table to determine the appropriate series resistance needed for matching the output impedance of the CDCLVC11xx to that of the characteristic impedance of the transmission line.

Unused outputs can be left floating. See the [Power Supply Recommendations](#) section for recommended filtering techniques.

## Typical Application (continued)

### 9.2.3 Application Curves



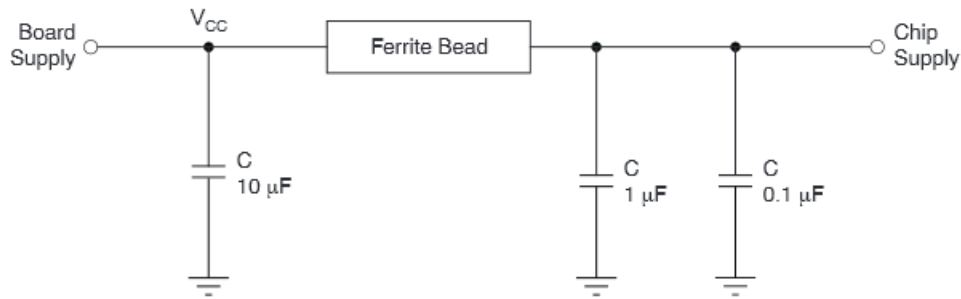
The low additive jitter of the CDCLVC11xx can be shown in the previous application example. The low-noise 100-MHz XO with 26-fs RMS jitter drives the CDCLVC11xx, resulting in 86-fs RMS jitter when integrated from 12 kHz to 20 MHz. The resultant additive jitter is a low 82-fs RMS for this configuration.

## 10 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when the jitter and phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guards the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply terminals and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1  $\mu$ F) bypass capacitors, as there are supply terminals in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 13 shows this recommended power supply decoupling method.



**Figure 13. Power Supply Decoupling**

## 10.1 Power Considerations

The following power consideration refers to the device-consumed power consumption only. The device power consumption is the sum of static power and dynamic power. The dynamic power usage consists of two components:

- Power used by the device as it switches states.
- Power required to charge any output load.

The output load can be capacitive only or capacitive and resistive. The following formula and the power graphs in and Figure 1 can be used to obtain the power consumption of the device:

$$P_{dev} = P_{stat} + n (P_{dyn} + P_{Cload})$$

$$P_{stat} = V_{DD} \times I_{DD}$$

$$P_{dyn} + P_{Cload} = \text{see and Figure 1}$$

where:

$V_{DD}$  = Supply voltage ( or 2.5 V)

$I_{DD}$  = Static device current (typical 6 mA for  $V_{DD} = 3.3$  V; typical 3 mA for  $V_{DD} = 2.5$  V)

$n$  = Number of switching output pins

Example for device power consumption for CDCLVC1104: four outputs are switching,  $f = 120$  MHz,  $V_{DD} = 3.3$  V, and  $C_{load} = 2$  pF per output:

$$P_{dev} = P_{stat} + n (P_{dyn} + P_{Cload}) = 19.8 \text{ mW} + 40 \text{ mW} = 59.8 \text{ mW}$$

$$P_{stat} = V_{DD} \times I_{DD} = 6 \text{ mA} \times 3.3 \text{ V} = 19.8 \text{ mW}$$

$$n (P_{dyn} + P_{Cload}) = 4 \times 10 \text{ mW} = 40 \text{ mW}$$

### NOTE

For dimensioning the power supply, the total power consumption must be considered. The total power consumption is the sum of the device power consumption and the power consumption of the load.

## 11 Layout

### 11.1 Layout Guidelines

Figure 14 shows a conceptual layout detailing recommended placement of power supply bypass capacitors. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

### 11.2 Layout Example

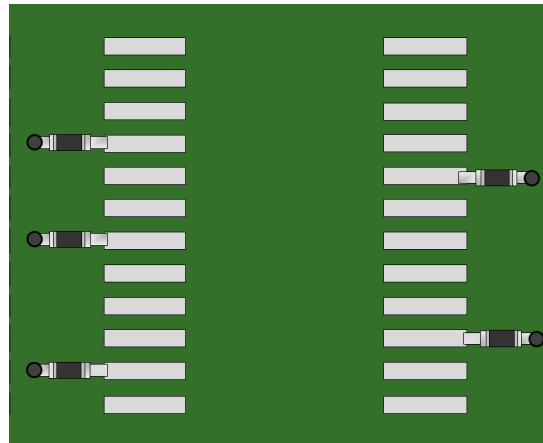


Figure 14. PCB Conceptual Layout

## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS      | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| CDCLVC1102 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CDCLVC1103 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CDCLVC1104 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CDCLVC1106 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CDCLVC1108 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CDCLVC1110 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CDCLVC1112 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CDCLVC1102PW     | ACTIVE        | TSSOP        | PW                 | 8    | 150            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C9C2                    | <a href="#">Samples</a> |
| CDCLVC1102PWR    | ACTIVE        | TSSOP        | PW                 | 8    | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C9C2                    | <a href="#">Samples</a> |
| CDCLVC1103PW     | ACTIVE        | TSSOP        | PW                 | 8    | 150            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C9C3                    | <a href="#">Samples</a> |
| CDCLVC1103PWR    | ACTIVE        | TSSOP        | PW                 | 8    | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C9C3                    | <a href="#">Samples</a> |
| CDCLVC1104PW     | ACTIVE        | TSSOP        | PW                 | 8    | 150            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C9C4                    | <a href="#">Samples</a> |
| CDCLVC1104PWR    | ACTIVE        | TSSOP        | PW                 | 8    | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C9C4                    | <a href="#">Samples</a> |
| CDCLVC1106PW     | ACTIVE        | TSSOP        | PW                 | 14   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C9C6                    | <a href="#">Samples</a> |
| CDCLVC1106PWR    | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C9C6                    | <a href="#">Samples</a> |
| CDCLVC1108PW     | ACTIVE        | TSSOP        | PW                 | 16   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C9C8                    | <a href="#">Samples</a> |
| CDCLVC1108PWR    | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C9C8                    | <a href="#">Samples</a> |
| CDCLVC1110PW     | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C9CA                    | <a href="#">Samples</a> |
| CDCLVC1110PWR    | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C9CA                    | <a href="#">Samples</a> |
| CDCLVC1112PW     | ACTIVE        | TSSOP        | PW                 | 24   | 60             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C9CC                    | <a href="#">Samples</a> |
| CDCLVC1112PWR    | ACTIVE        | TSSOP        | PW                 | 24   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C9CC                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.



<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDCLVC1102PWR | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CDCLVC1103PWR | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CDCLVC1104PWR | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CDCLVC1106PWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CDCLVC1108PWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CDCLVC1110PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| CDCLVC1112PWR | TSSOP        | PW              | 24   | 2000 | 330.0              | 16.4               | 6.95    | 8.3     | 1.6     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CDCLVC1102PWR | TSSOP        | PW              | 8    | 2000 | 367.0       | 367.0      | 35.0        |
| CDCLVC1103PWR | TSSOP        | PW              | 8    | 2000 | 367.0       | 367.0      | 35.0        |
| CDCLVC1104PWR | TSSOP        | PW              | 8    | 2000 | 367.0       | 367.0      | 35.0        |
| CDCLVC1106PWR | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| CDCLVC1108PWR | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |
| CDCLVC1110PWR | TSSOP        | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| CDCLVC1112PWR | TSSOP        | PW              | 24   | 2000 | 367.0       | 367.0      | 38.0        |

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

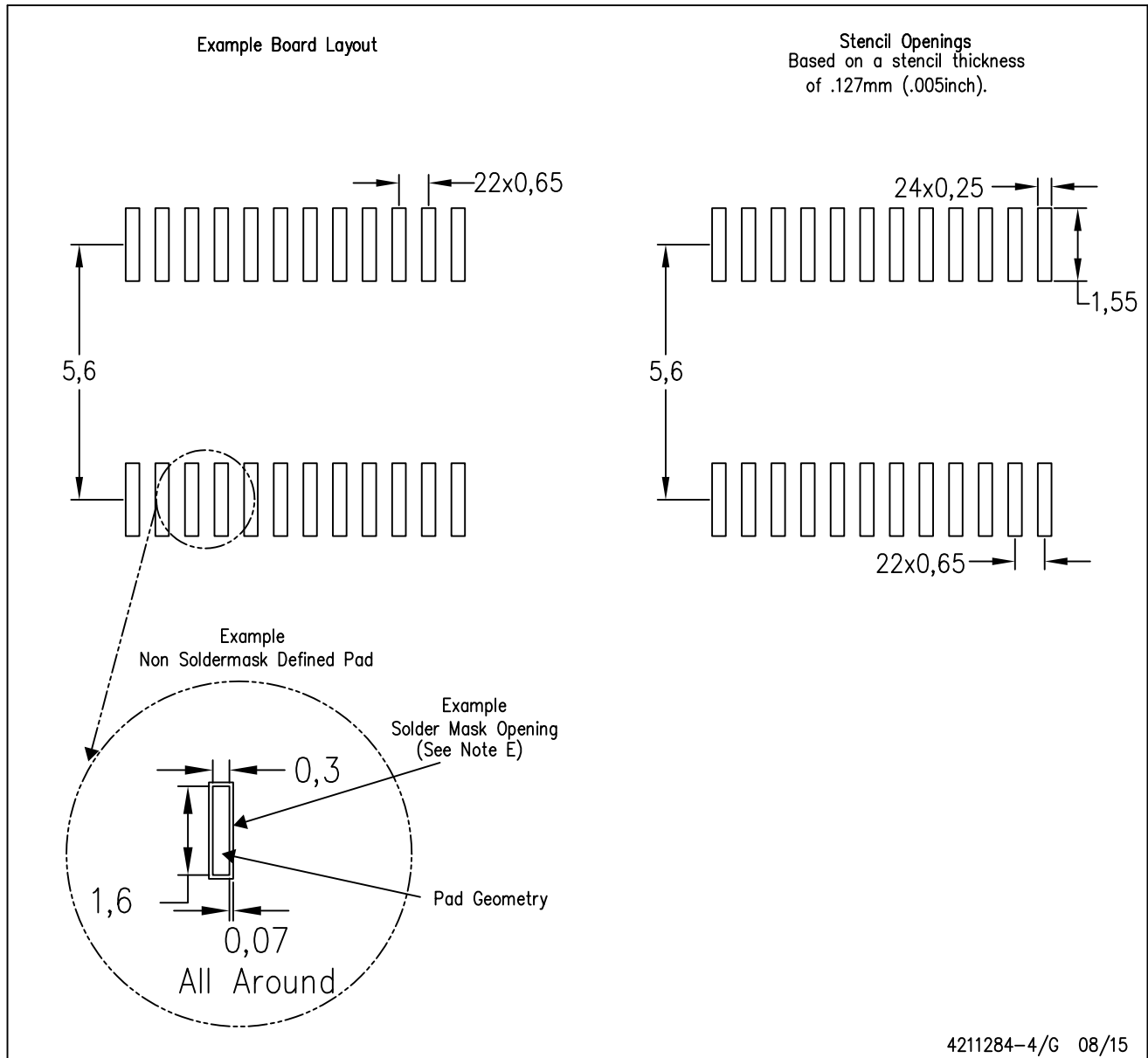


4040064-6/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

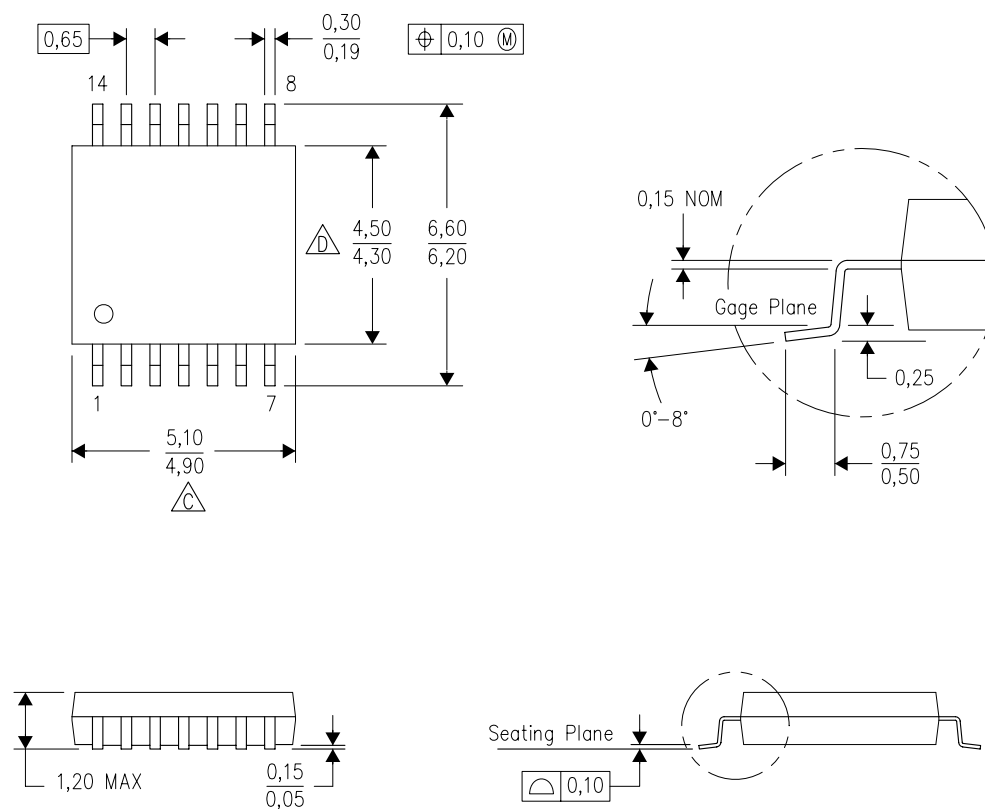


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA



PW (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



4040064-3/G 02/11

NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
-  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
-  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

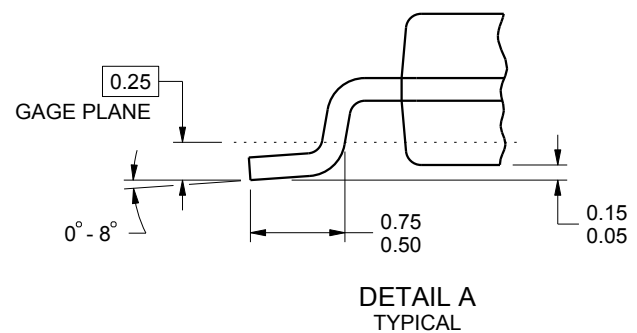
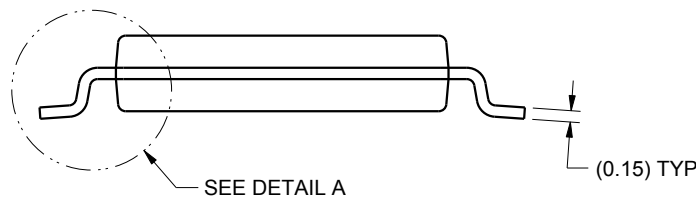
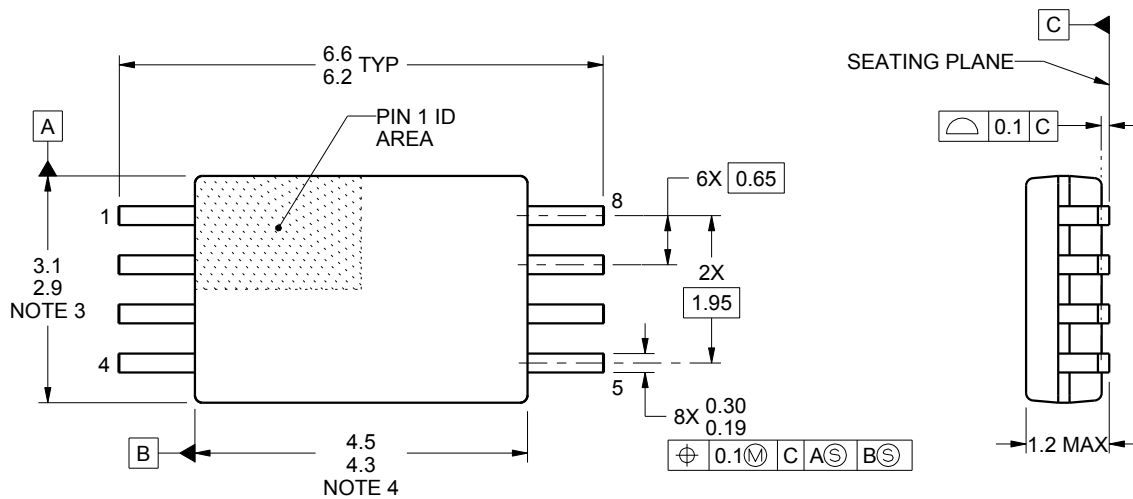
PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Texas Instruments:](#)

[CDCLVC1106PW](#) [CDCLVC1106PWR](#)