



## CD4049UB and CD4050B CMOS Hex Inverting Buffer and Converter

### 1 Features

- CD4049UB Inverting
- CD4050B Noninverting
- High Sink Current for Driving 2 TTL Loads
- High-to-Low Level Logic Conversion
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current of 1  $\mu$ A at 18 V Over Full Package Temperature Range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V Parametric Ratings

### 2 Applications

- CMOS to DTL or TTL Hex Converters
- CMOS Current *Sink* or *Source* Drivers
- CMOS High-to-Low Logic Level Converters

### 3 Description

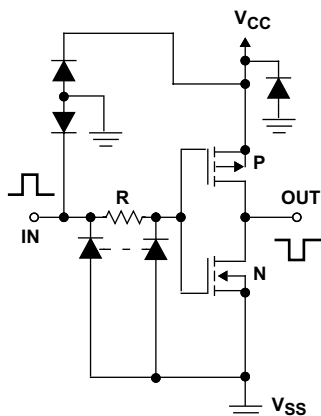
The CD4049UB and CD4050B devices are inverting and noninverting hex buffers, and feature logic-level conversion using only one supply voltage ( $V_{CC}$ ). The input-signal high level ( $V_{IH}$ ) can exceed the  $V_{CC}$  supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL or TTL converters and can drive directly two DTL or TTL loads. ( $V_{CC} = 5$  V,  $V_{OL} \leq 0.4$  V, and  $I_{OL} \geq 3.3$  mA.)

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CD4049UBE, CD4050BE	PDIP (16)	3.90 mm × 19.30 mm
CD4049UBD, CD4050BD	SOIC (16)	9.90 mm × 3.91 mm
CD4049UBDW, CD4050BDW	SOIC (16)	10.30 mm × 7.50 mm
CD4049UBNS, CD4050BNS	SO (16)	19.30 mm × 6.35 mm
CD4049UBPW, CD4050BPW	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

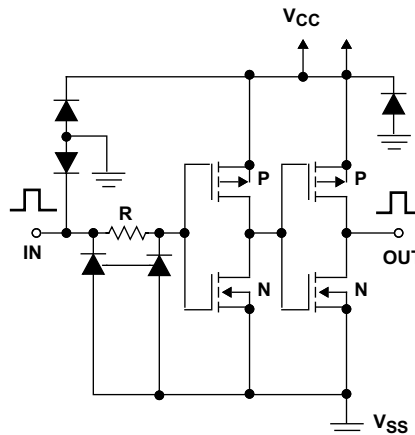
**Schematic Diagram of CD4049UB**



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1 of 6 Identical Units

**Schematic Diagram of CD4050B**



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1 of 6 Identical Units



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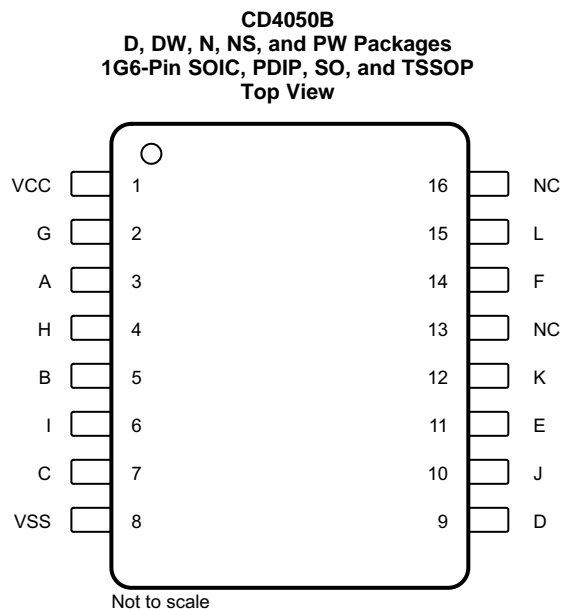
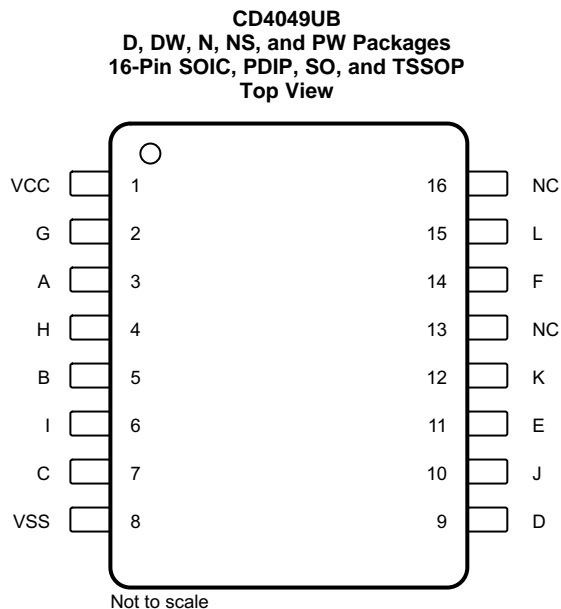
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (May 2004) to Revision J	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....	<b>1</b>
• Deleted <i>Ordering Information</i> table; see POA at the end of the data sheet.....	<b>1</b>
• Changed Storage temperature minimum value from 65 to –65 .....	<b>4</b>
• Changed $R_{\theta JA}$ values for the CD4049UB device: D (SOIC) from 73 to 81.6, DW (SOIC) from 57 to 81.6, E (PDIP) from 67 to 49.5, NS (SO) from 64 to 84.3, and PW (TSSOP) from 108 to 108.9 .....	<b>5</b>
• Changed $R_{\theta JA}$ values for the CD4050B device: D (SOIC) from 73 to 81.6, DW (SOIC) from 57 to 81.2, E (PDIP) from 67 to 49.7, NS (SO) from 64 to 83.8, and PW (TSSOP) from 108 to 108.4 .....	<b>5</b>

## 5 Pin Configuration and Functions



**Pin Functions: CD4049UB**

PIN		I/O	DESCRIPTION
NAME	NO.		
A	3	I	Input 1
B	5	I	Input 2
C	7	I	Input 3
D	9	I	Input 4
E	11	I	Input 5
F	14	I	Input 6
G	2	O	Inverting output 1. $G = \overline{A}$
H	4	O	Inverting output 2. $H = \overline{B}$
I	6	O	Inverting output 3. $I = \overline{C}$
J	10	O	Inverting output 4. $J = \overline{D}$
K	12	O	Inverting output 5. $K = \overline{E}$
L	15	O	Inverting output 6. $L = \overline{F}$
NC	13, 16	—	No connection
VCC	1	—	Power pin
VSS	8	—	Negative supply

**Pin Functions: CD4050B**

PIN		I/O	DESCRIPTION
NAME	NO.		
A	3	I	Input 1
B	5	I	Input 2
C	7	I	Input 3
D	9	I	Input 4
E	11	I	Input 5
F	14	I	Input 6
G	2	O	Inverting output 1. G = A
H	4	O	Inverting output 2. H = B
I	6	O	Inverting output 3. I = C
J	10	O	Inverting output 4. J = D
K	12	O	Inverting output 5. K = E
L	15	O	Inverting output 6. L = F
NC	13, 16	—	No connection
VCC	1	—	Power pin
VSS	8	—	Negative supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	VCC to VSS	−0.5	20	V
DC input current, $I_{IK}$	Any one input		±10	mA
Lead temperature (soldering, 10 s)	SOIC, lead tips only		265	°C
Junction temperature, $T_J$			150	°C
Storage temperature, $T_{stg}$		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	3	18	V
$T_A$	Operating temperature	−55	125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	CD4049UB					CD4050B					UNIT
	D (SOIC)	DW (SOIC)	E (PDIP)	NS (SO)	PW (TSSOP)	D (SOIC)	DW (SOIC)	E (PDIP)	NS (SO)	PW (TSSOP)	
	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance <sup>(2)</sup>	81.6	81.6	49.5	84.3	108.9	81.6	81.2	49.7	83.8	108.4	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	41.5	44.5	36.8	43	43.7	41.5	44.1	37	42.5	43.2	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	39	46.3	29.4	44.6	54	39	45.9	29.6	44.1	53.5	°C/W
$\psi_{JT}$ Junction-to-top characterization parameter	10.7	16.5	21.7	12.8	4.6	10.7	16.1	21.9	12.5	4.5	°C/W
$\psi_{JB}$ Junction-to-board characterization parameter	38.7	45.8	29.3	44.3	53.4	38.7	45.4	29.5	43.8	52.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.

## 6.5 Electrical Characteristics: DC

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{DD(Max)}$ Quiescent device current		$V_{IN} = 0$ or $5\text{ V}$ , $V_{CC} = 5\text{ V}$	$T_A = -55\text{ °C}$			1	$\mu\text{A}$
			$T_A = -40\text{ °C}$			1	
			$T_A = 25\text{ °C}$		0.02	1	
			$T_A = 85\text{ °C}$			30	
			$T_A = 125\text{ °C}$			30	
		$V_{IN} = 0$ or $10\text{ V}$ , $V_{CC} = 10\text{ V}$	$T_A = -55\text{ °C}$			2	
			$T_A = -40\text{ °C}$			2	
			$T_A = 25\text{ °C}$		0.02	2	
			$T_A = 85\text{ °C}$			60	
			$T_A = 125\text{ °C}$			60	
		$V_{IN} = 0$ or $15\text{ V}$ , $V_{CC} = 4\text{ V}$	$T_A = -55\text{ °C}$			4	
			$T_A = -40\text{ °C}$			4	
			$T_A = 25\text{ °C}$		0.02	4	
			$T_A = 85\text{ °C}$			120	
			$T_A = 125\text{ °C}$			120	
		$V_{IN} = 0$ or $20\text{ V}$ , $V_{CC} = 20\text{ V}$	$T_A = -55\text{ °C}$			20	
			$T_A = -40\text{ °C}$			20	
			$T_A = 25\text{ °C}$		0.04	20	
			$T_A = 85\text{ °C}$			600	
			$T_A = 125\text{ °C}$			600	

**Electrical Characteristics: DC (continued)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{OL}(\text{Min})$	Output low (sink) current	$V_{OUT} = 0.4 \text{ V}$ , $V_{IN} = 0 \text{ or } 5 \text{ V}$ , $V_{CC} = 4.5 \text{ V}$	$T_A = -55^\circ\text{C}$			3.3	mA
			$T_A = -40^\circ\text{C}$			3.1	
			$T_A = 25^\circ\text{C}$	2.6	5.2		
			$T_A = 85^\circ\text{C}$			2.1	
			$T_A = 125^\circ\text{C}$			1.8	
	$V_{OUT} = 0.4 \text{ V}$ , $V_{IN} = 0 \text{ or } 5 \text{ V}$ , $V_{CC} = 5 \text{ V}$		$T_A = -55^\circ\text{C}$			4	
			$T_A = -40^\circ\text{C}$			3.8	
			$T_A = 25^\circ\text{C}$	3.2	6.4		
			$T_A = 85^\circ\text{C}$			2.9	
			$T_A = 125^\circ\text{C}$			2.4	
	$V_{OUT} = 0.5 \text{ V}$ , $V_{IN} = 0 \text{ or } 10 \text{ V}$ , $V_{CC} = 10 \text{ V}$		$T_A = -55^\circ\text{C}$			10	
			$T_A = -40^\circ\text{C}$			9.6	
			$T_A = 25^\circ\text{C}$	8	16		
			$T_A = 85^\circ\text{C}$			6.6	
			$T_A = 125^\circ\text{C}$			5.6	
	$V_{OUT} = 1.5 \text{ V}$ , $V_{IN} = 0 \text{ or } 15 \text{ V}$ , $V_{CC} = 15 \text{ V}$		$T_A = -55^\circ\text{C}$			26	
			$T_A = -40^\circ\text{C}$			25	
			$T_A = 25^\circ\text{C}$	24	48		
			$T_A = 85^\circ\text{C}$			20	
			$T_A = 125^\circ\text{C}$			18	
$I_{OH}(\text{Min})$	Output high (source) current	$V_{OUT} = 4.6 \text{ V}$ , $V_{IN} = 0 \text{ or } 5 \text{ V}$ , $V_{CC} = 5 \text{ V}$	$T_A = -55^\circ\text{C}$			-0.81	mA
			$T_A = -40^\circ\text{C}$			-0.73	
			$T_A = 25^\circ\text{C}$	-0.65	-1.2		
			$T_A = 85^\circ\text{C}$			-0.58	
			$T_A = 125^\circ\text{C}$			-0.48	
	$V_{OUT} = 2.5 \text{ V}$ , $V_{IN} = 0 \text{ or } 5 \text{ V}$ , $V_{CC} = 5 \text{ V}$		$T_A = -55^\circ\text{C}$			-2.6	
			$T_A = -40^\circ\text{C}$			-2.4	
			$T_A = 25^\circ\text{C}$	-2.1	-3.9		
			$T_A = 85^\circ\text{C}$			-1.9	
			$T_A = 125^\circ\text{C}$			-1.55	
	$V_{OUT} = 9.5 \text{ V}$ , $V_{IN} = 0 \text{ or } 10 \text{ V}$ , $V_{CC} = 10 \text{ V}$		$T_A = -55^\circ\text{C}$			-2	
			$T_A = -40^\circ\text{C}$			-1.8	
			$T_A = 25^\circ\text{C}$	-1.65	-3		
			$T_A = 85^\circ\text{C}$			-1.35	
			$T_A = 125^\circ\text{C}$			-1.18	
	$V_{OUT} = 1.3 \text{ V}$ , $V_{IN} = 0 \text{ or } 15 \text{ V}$ , $V_{CC} = 15 \text{ V}$		$T_A = -55^\circ\text{C}$			-5.2	
			$T_A = -40^\circ\text{C}$			-4.8	
			$T_A = 25^\circ\text{C}$	-4.3	-8		
			$T_A = 85^\circ\text{C}$			-3.5	
			$T_A = 125^\circ\text{C}$			-3.1	

**Electrical Characteristics: DC (continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OL}(\text{Max})$ Out voltage low level	$V_{IN} = 0 \text{ or } 5 \text{ V}, V_{CC} = 5 \text{ V}$	$T_A = -55^\circ\text{C}$			0.05	V
		$T_A = -40^\circ\text{C}$			0.05	
		$T_A = 25^\circ\text{C}$		0	0.05	
		$T_A = 85^\circ\text{C}$			0.05	
		$T_A = 125^\circ\text{C}$			0.05	
	$V_{IN} = 0 \text{ or } 10 \text{ V}, V_{CC} = 10 \text{ V}$	$T_A = -55^\circ\text{C}$			0.05	
		$T_A = -40^\circ\text{C}$			0.05	
		$T_A = 25^\circ\text{C}$		0	0.05	
		$T_A = 85^\circ\text{C}$			0.05	
		$T_A = 125^\circ\text{C}$			0.05	
	$V_{IN} = 0 \text{ or } 15 \text{ V}, V_{CC} = 15 \text{ V}$	$T_A = -55^\circ\text{C}$			0.05	
		$T_A = -40^\circ\text{C}$			0.05	
		$T_A = 25^\circ\text{C}$		0	0.05	
		$T_A = 85^\circ\text{C}$			0.05	
		$T_A = 125^\circ\text{C}$			0.05	
$V_{OH}(\text{Min})$ Output voltage high level	$V_{IN} = 0 \text{ or } 5 \text{ V}, V_{CC} = 5 \text{ V}$	$T_A = -55^\circ\text{C}$			4.95	V
		$T_A = -40^\circ\text{C}$			4.95	
		$T_A = 25^\circ\text{C}$	4.95	5		
		$T_A = 85^\circ\text{C}$			4.95	
		$T_A = 125^\circ\text{C}$			4.95	
	$V_{IN} = 0 \text{ or } 10 \text{ V}, V_{CC} = 10 \text{ V}$	$T_A = -55^\circ\text{C}$			9.95	
		$T_A = -40^\circ\text{C}$			9.95	
		$T_A = 25^\circ\text{C}$	9.95	10		
		$T_A = 85^\circ\text{C}$			9.95	
		$T_A = 125^\circ\text{C}$			9.95	
	$V_{IN} = 0 \text{ or } 15 \text{ V}, V_{CC} = 15 \text{ V}$	$T_A = -55^\circ\text{C}$			14.95	
		$T_A = -40^\circ\text{C}$			14.95	
		$T_A = 25^\circ\text{C}$	14.95	15		
		$T_A = 85^\circ\text{C}$			14.95	
		$T_A = 125^\circ\text{C}$			14.95	
$V_{IL}(\text{Max})$	Input low voltage (CD4049UB)	$V_{OUT} = 4.5 \text{ V}, V_{CC} = 5 \text{ V}, \text{ Full temperature range}$			1	V
		$V_{OUT} = 9 \text{ V}, V_{CC} = 10 \text{ V}, \text{ Full temperature range}$			2	
		$V_{OUT} = 13.5 \text{ V}, V_{CC} = 15 \text{ V}, \text{ Full temperature range}$			2.5	
	Input low voltage (CD4050B)	$V_{OUT} = 0.5 \text{ V}, V_{CC} = 5 \text{ V}, \text{ Full temperature range}$			1.5	
		$V_{OUT} = 1 \text{ V}, V_{CC} = 10 \text{ V}, \text{ Full temperature range}$			3	
		$V_{OUT} = 1.5 \text{ V}, V_{CC} = 15 \text{ V}, \text{ Full temperature range}$			4	

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**Electrical Characteristics: DC (continued)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IH}(\text{Min})$	Input high voltage (CD4049UB)	$V_{OUT} = 0.5 \text{ V}$ , $V_{CC} = 5 \text{ V}$	$T_A = -55^\circ\text{C}$			4	V
			$T_A = -40^\circ\text{C}$			4	
			$T_A = 25^\circ\text{C}$	4			
			$T_A = 85^\circ\text{C}$			4	
			$T_A = 125^\circ\text{C}$			4	
		$V_{OUT} = 1 \text{ V}$ , $V_{CC} = 10 \text{ V}$	$T_A = -55^\circ\text{C}$			8	
			$T_A = -40^\circ\text{C}$			8	
			$T_A = 25^\circ\text{C}$	8			
			$T_A = 85^\circ\text{C}$			8	
			$T_A = 125^\circ\text{C}$			8	
		$V_{OUT} = 1.5 \text{ V}$ , $V_{CC} = 15 \text{ V}$	$T_A = -55^\circ\text{C}$			12.5	
			$T_A = -40^\circ\text{C}$			12.5	
			$T_A = 25^\circ\text{C}$	12.5			
			$T_A = 85^\circ\text{C}$			12.5	
			$T_A = 125^\circ\text{C}$			12.5	
$V_{IH}$	Input high voltage (CD4050B)	$V_{OUT} = 4.5 \text{ V}$ , $V_{CC} = 5 \text{ V}$	$T_A = -55^\circ\text{C}$			3.5	V
			$T_A = -40^\circ\text{C}$			3.5	
			$T_A = 25^\circ\text{C}$	3.5			
			$T_A = 85^\circ\text{C}$			3.5	
			$T_A = 125^\circ\text{C}$			3.5	
		$V_{OUT} = 9 \text{ V}$ , $V_{CC} = 10 \text{ V}$	$T_A = -55^\circ\text{C}$			7	
			$T_A = -40^\circ\text{C}$			7	
			$T_A = 25^\circ\text{C}$	7			
			$T_A = 85^\circ\text{C}$			7	
			$T_A = 125^\circ\text{C}$			7	
		$V_{OUT} = 13.5 \text{ V}$ , $V_{CC} = 15 \text{ V}$	$T_A = -55^\circ\text{C}$			11	
			$T_A = -40^\circ\text{C}$			11	
			$T_A = 25^\circ\text{C}$	11			
			$T_A = 85^\circ\text{C}$			11	
			$T_A = 125^\circ\text{C}$			11	
$I_{IN}(\text{Max})$	Input current	$V_{IN} = 0 \text{ or } 18 \text{ V}$ , $V_{CC} = 18 \text{ V}$	$T_A = -55^\circ\text{C}$			$\pm 0.1$	$\mu\text{A}$
			$T_A = -40^\circ\text{C}$			$\pm 0.1$	
			$T_A = 25^\circ\text{C}$	$\pm 10^{-5}$		$\pm 0.1$	
			$T_A = 85^\circ\text{C}$			$\pm 1$	
			$T_A = 125^\circ\text{C}$			$\pm 1$	



## 6.6 Electrical Characteristics: AC

$T_A = 25^\circ\text{C}$ , Input  $t_r$  and  $t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time Low to high (CD4049UB)	$V_{IN} = 5\text{ V}$ , $V_{CC} = 5\text{ V}$		60	120	ns
		$V_{IN} = 10\text{ V}$ , $V_{CC} = 10\text{ V}$		32	65	
		$V_{IN} = 10\text{ V}$ , $V_{CC} = 5\text{ V}$		45	90	
		$V_{IN} = 15\text{ V}$ , $V_{CC} = 15\text{ V}$		25	50	
		$V_{IN} = 15\text{ V}$ , $V_{CC} = 5\text{ V}$		45	90	
	Propagation delay time Low to high (CD4050B)	$V_{IN} = 5\text{ V}$ , $V_{CC} = 5\text{ V}$		70	140	ns
		$V_{IN} = 10\text{ V}$ , $V_{CC} = 10\text{ V}$		40	80	
		$V_{IN} = 10\text{ V}$ , $V_{CC} = 5\text{ V}$		45	90	
		$V_{IN} = 15\text{ V}$ , $V_{CC} = 15\text{ V}$		30	60	
		$V_{IN} = 15\text{ V}$ , $V_{CC} = 5\text{ V}$		40	80	
$t_{PHL}$	Propagation delay time High to low (CD4049UB)	$V_{IN} = 5\text{ V}$ , $V_{CC} = 5\text{ V}$		32	65	ns
		$V_{IN} = 10\text{ V}$ , $V_{CC} = 10\text{ V}$		20	40	
		$V_{IN} = 10\text{ V}$ , $V_{CC} = 5\text{ V}$		15	30	
		$V_{IN} = 15\text{ V}$ , $V_{CC} = 15\text{ V}$		15	30	
		$V_{IN} = 15\text{ V}$ , $V_{CC} = 5\text{ V}$		10	20	
	Propagation delay time High to low (CD4050B)	$V_{IN} = 5\text{ V}$ , $V_{CC} = 5\text{ V}$		55	110	ns
		$V_{IN} = 10\text{ V}$ , $V_{CC} = 10\text{ V}$		22	55	
		$V_{IN} = 10\text{ V}$ , $V_{CC} = 5\text{ V}$		50	100	
		$V_{IN} = 15\text{ V}$ , $V_{CC} = 15\text{ V}$		15	30	
		$V_{IN} = 15\text{ V}$ , $V_{CC} = 5\text{ V}$		50	100	
$t_{TLH}$	Transition time Low to high	$V_{IN} = 5\text{ V}$ , $V_{CC} = 5\text{ V}$		80	160	ns
		$V_{IN} = 10\text{ V}$ , $V_{CC} = 10\text{ V}$		40	80	
		$V_{IN} = 15\text{ V}$ , $V_{CC} = 15\text{ V}$		30	60	
$t_{THL}$	Transition time High to low	$V_{IN} = 5\text{ V}$ , $V_{CC} = 5\text{ V}$		30	60	ns
		$V_{IN} = 10\text{ V}$ , $V_{CC} = 10\text{ V}$		20	40	
		$V_{IN} = 15\text{ V}$ , $V_{CC} = 15\text{ V}$		15	30	
$C_{IN}$	Input capacitance (CD4049UB)			15	22.5	pF
	Input capacitance (CD4050B)			5	7.5	pF

## 6.7 Typical Characteristics

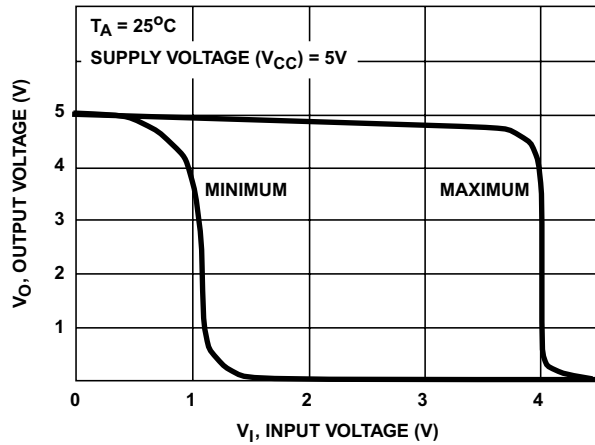


Figure 1. Minimum and Maximum Voltage Transfer Characteristics for CD4049UB

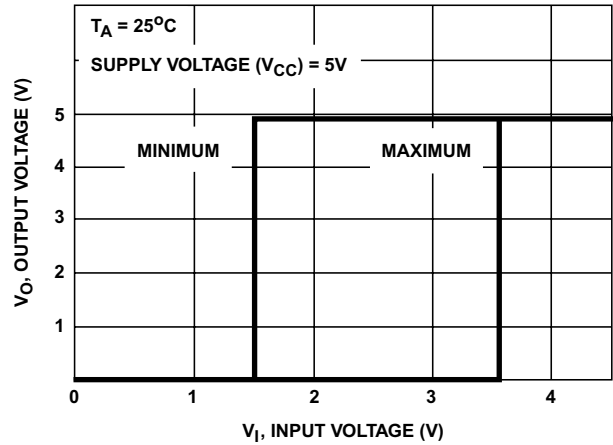


Figure 2. Minimum and Maximum Voltage Transfer Characteristics for CD4050B

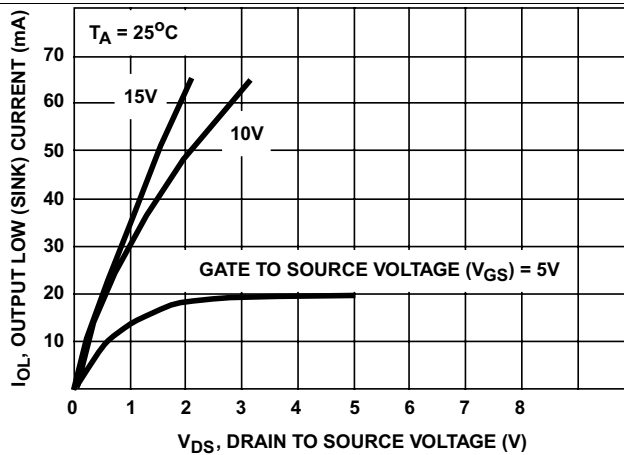


Figure 3. Typical Output Low (Sink) Current Characteristics

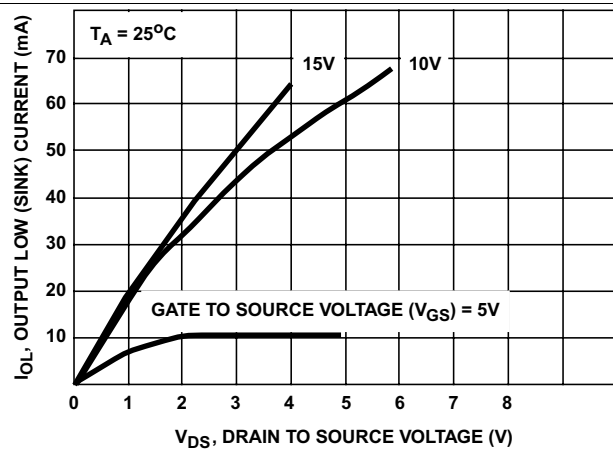


Figure 4. Minimum Output Low (Sink) Current Drain Characteristics

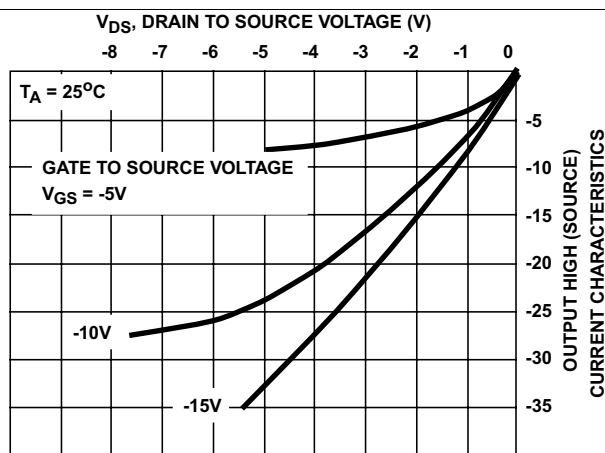


Figure 5. Typical Output High (Source) Current Characteristics

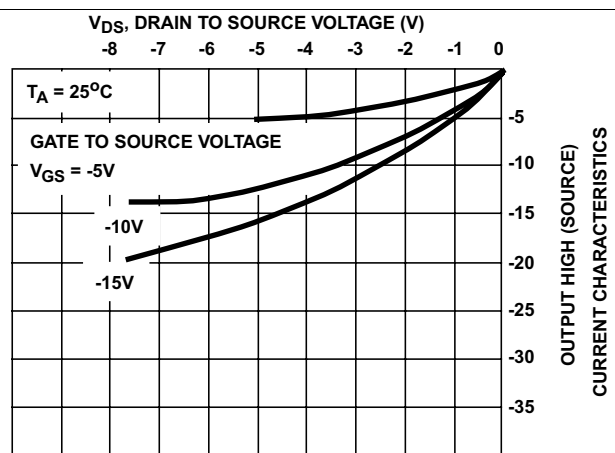


Figure 6. Minimum Output High (Source) Current Characteristics

## Typical Characteristics (continued)

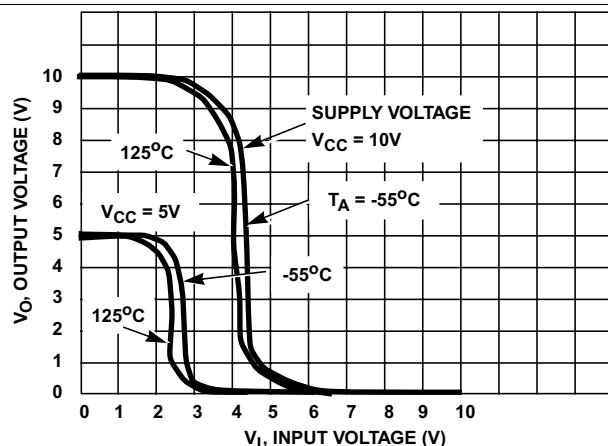


Figure 7. Typical Voltage Transfer Characteristics as a Function of Temperature for CD4049UB

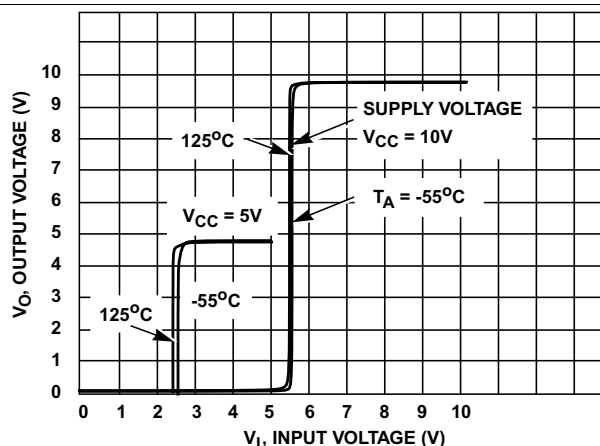


Figure 8. Typical Voltage Transfer Characteristics as a Function of Temperature for CD4050B

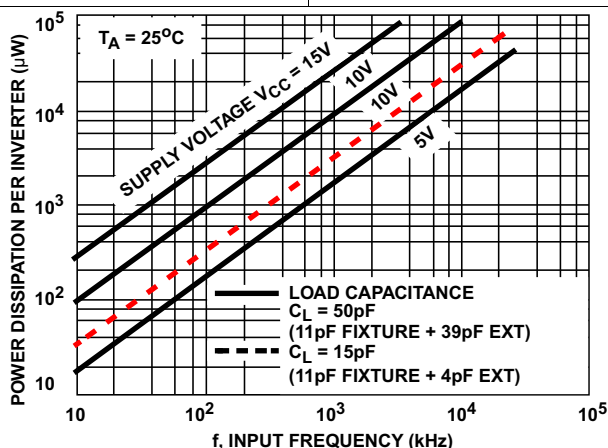


Figure 9. Typical Power Dissipation versus Frequency Characteristics

## 7 Parameter Measurement Information

### 7.1 Test Circuits

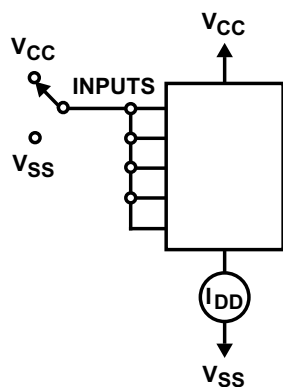
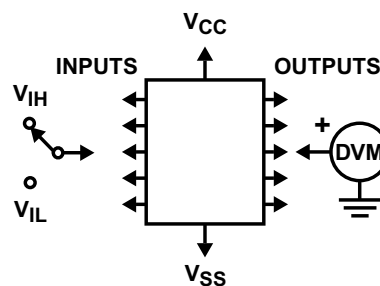


Figure 10. Quiescent Device Current Test Circuit

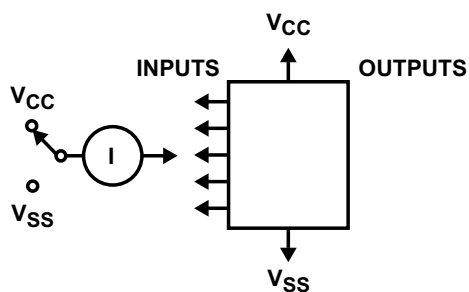


Test any one input with other inputs at V<sub>CC</sub> or V<sub>SS</sub>.

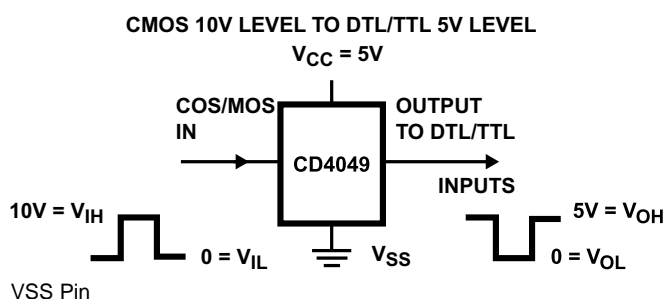
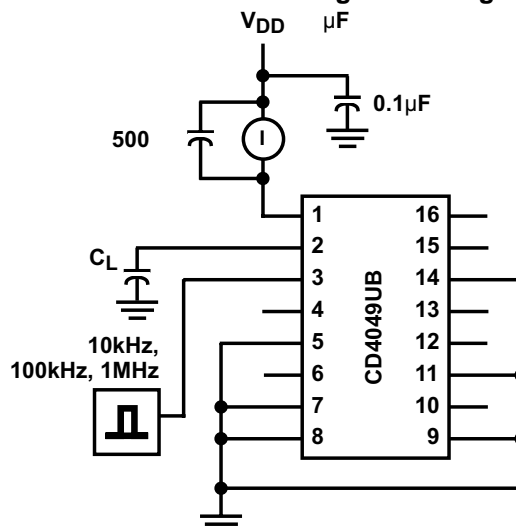
Figure 11. Input Voltage Test Circuit

**CD4049UB, CD4050B**

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[www.ti.com](http://www.ti.com)
**Test Circuits (continued)**


Measure inputs sequentially, to both VCC and VSS connect all unused inputs to either VCC or VSS.

**Figure 12. Input Current Test Circuit**

**Figure 13. Logic Level Conversion Application**


$C_L$  includes fixture capacitance.

**Figure 14. Dynamic Power Dissipation Test Circuits**

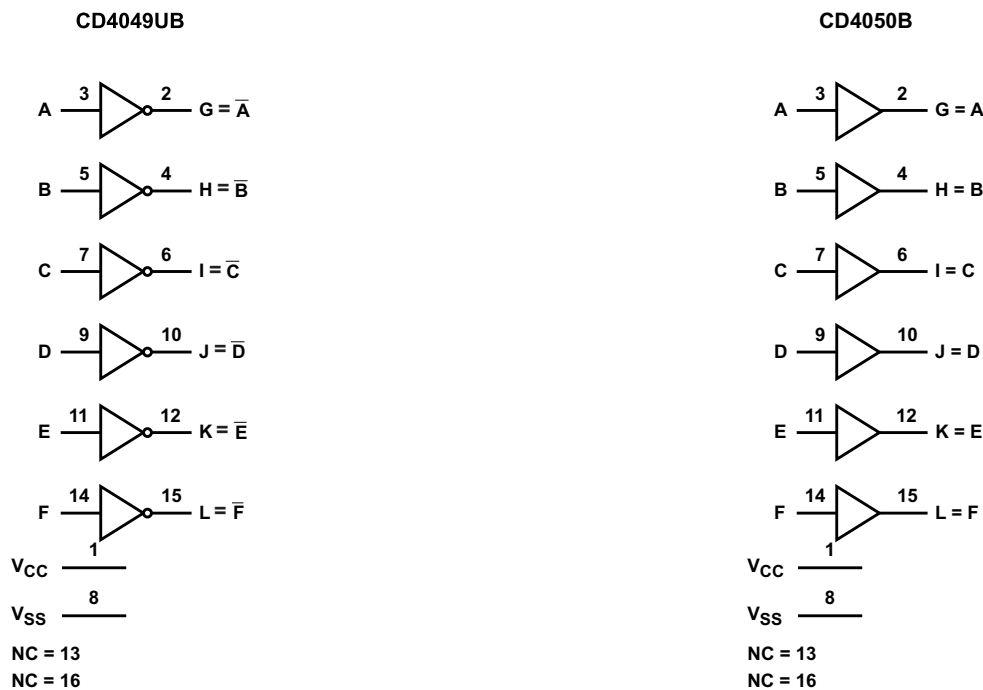
## 8 Detailed Description

### 8.1 Overview

The CD4049UB device is an inverting hex buffer; the CD4050B device is a noninverting hex buffer. These devices do logic-level conversions and have a high sink current that can drive two TTL loads. These devices also have low input current of 1  $\mu\text{A}$  across the full temperature range at 18 V.

The CD4049UB and CD4050B devices are designated as replacements for CD4009UB and CD4010B devices, respectively. Because the CD4049UB and CD4050B require only one power supply, they are preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Pin 16 (NC) is not connected internally on the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. TI recommends the CD4069UB hex inverter is recommended for applications not requiring high sink-current or voltage conversion.

### 8.2 Functional Block Diagram



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### 8.3 Feature Description

CD4049UB and CD4050B have standardized symmetrical output characteristics and a wide operating voltage from 3 V to 18 V with quiescent current tested at 20 V. These devices have transition times of  $t_{\text{TLH}} = 40$  ns and  $t_{\text{THL}} = 20$  ns (typical) at 10 V. The operating temperature is from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

## 8.4 Device Functional Modes

[Table 1](#) shows the functional modes for CD4049UB. [Table 2](#) shows the functional modes for CD4050B.

**Table 1. Function Table for CD4049UB**

INPUT A, B, C, D, E, F	OUTPUT G, H, I, J, K, L
H	L
L	H

**Table 2. Function Table for CD4050B**

INPUT A, B, C, D, E, F	OUTPUT G, H, I, J, K, L
H	H
L	L

## 9 Application and Implementation

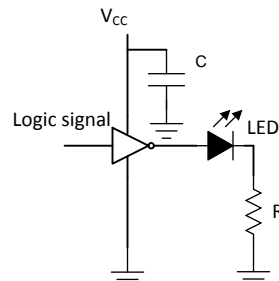
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The CD4049UB and CD4050B devices have low input currents of 1  $\mu$ A at 18 V over full package-temperature range and 100 nA at 18 V, 25°C. These devices have a wide operating voltage from 3 V to 18 V and used in high-voltage applications.

### 9.2 Typical Application



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**Figure 15. CD4049UB Application**

#### 9.2.1 Design Requirements

The CD4049UB device is the industry's highest logic inverter operating at 18 V under recommended conditions. These devices have high sink current capabilities.

#### 9.2.2 Detailed Design Procedure

The recommended input conditions for [Figure 15](#) includes rise time and fall time specifications (see  $\Delta t/\Delta V$  in [Recommended Operating Conditions](#)) and specified high and low levels (see  $V_{IH}$  and  $V_{IL}$  in [Recommended Operating Conditions](#)). Inputs are not overvoltage tolerant and must be below  $V_{CC}$  level because of the presence of input clamp diodes to  $V_{CC}$ .

The recommended output condition for the CD4049UB application includes specific load currents. Load currents must be limited so as to not exceed the total power (continuous current through  $V_{CC}$  or GND) for the device. These limits are in the [Absolute Maximum Ratings](#). Outputs must not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 9.2.3 Application Curves

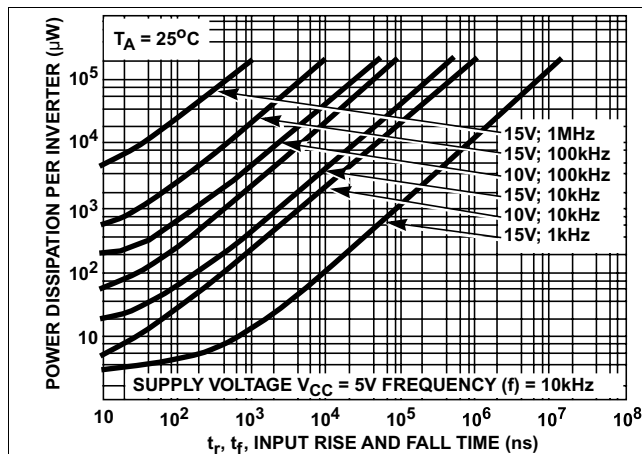


Figure 16. Typical Power Dissipation vs Input Rise and Fall Times Per Inverter for CD4049UB

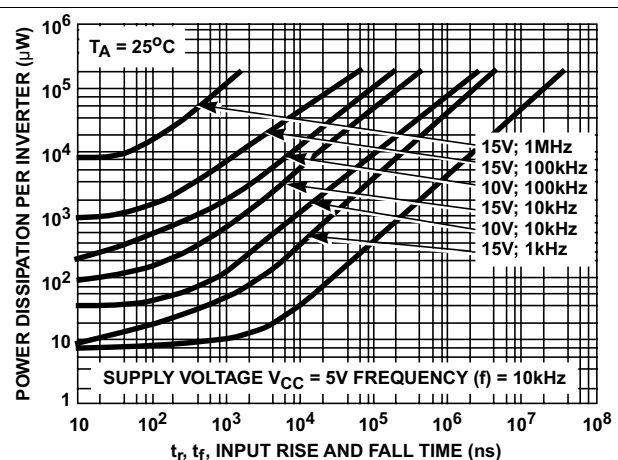


Figure 17. Typical Power Dissipation vs Input Rise and Fall Times Per Buffer for CD4050B

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating in [Recommended Operating Conditions](#).

Each VCC pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor. If there are multiple VCC pins, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float.

In many cases, digital logic device functions or parts of these functions are unused (for example, when only two inputs of a triple-input and gate are used, or only 3 of the 4 buffer gates are used). Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. This rule must be observed under all circumstances specified in the next paragraph.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. See [Implications of Slow or Floating CMOS Inputs](#) for more information on the effects of floating inputs. The logic level must apply to any particular unused input depending on the function of the device. Generally, they are tied to GND or VCC (whichever is convenient).

### 11.2 Layout Example

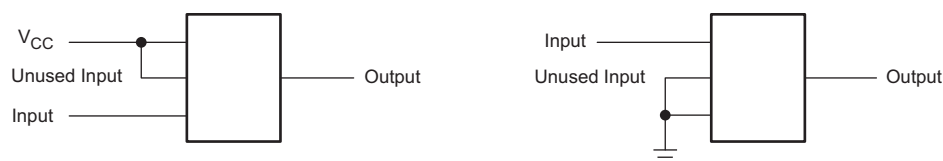


Figure 18. Layout Diagram



## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#) (SCBA004)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 3. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD4049UB	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
CD4050B	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4049UBD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM	<a href="#">Samples</a>
CD4049UBDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM	<a href="#">Samples</a>
CD4049UBDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM	<a href="#">Samples</a>
CD4049UBDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM	<a href="#">Samples</a>
CD4049UBDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM	<a href="#">Samples</a>
CD4049UBDT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM	<a href="#">Samples</a>
CD4049UBDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM	<a href="#">Samples</a>
CD4049UBDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UBM	<a href="#">Samples</a>
CD4049UBE	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4049UBE	<a href="#">Samples</a>
CD4049UBEE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4049UBE	<a href="#">Samples</a>
CD4049UBF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4049UBF	<a href="#">Samples</a>
CD4049UBF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4049UBF3A	<a href="#">Samples</a>
CD4049UBNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4049UB	<a href="#">Samples</a>
CD4049UBPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM049UB	<a href="#">Samples</a>
CD4049UBPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM049UB	<a href="#">Samples</a>
CD4050BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4050BM	<a href="#">Samples</a>
CD4050BDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4050BM	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4050BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4050BM	<a href="#">Samples</a>
CD4050BDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4050BM	<a href="#">Samples</a>
CD4050BDT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4050BM	<a href="#">Samples</a>
CD4050BDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4050BM	<a href="#">Samples</a>
CD4050BDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4050BM	<a href="#">Samples</a>
CD4050BE	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4050BE	<a href="#">Samples</a>
CD4050BEE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4050BE	<a href="#">Samples</a>
CD4050BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4050BF	<a href="#">Samples</a>
CD4050BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4050BF3A	<a href="#">Samples</a>
CD4050BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4050B	<a href="#">Samples</a>
CD4050BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM050B	<a href="#">Samples</a>
CD4050BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM050B	<a href="#">Samples</a>
JM38510/05553BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 05553BEA	<a href="#">Samples</a>
JM38510/05554BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 05554BEA	<a href="#">Samples</a>
M38510/05553BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 05553BEA	<a href="#">Samples</a>
M38510/05554BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 05554BEA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

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**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD4049UB, CD4049UB-MIL, CD4050B, CD4050B-MIL :**

● Catalog: [CD4049UB](#), [CD4050B](#)

● Military: [CD4049UB-MIL](#), [CD4050B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4049UBDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4049UBPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4050BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4050BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
CD4050BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS

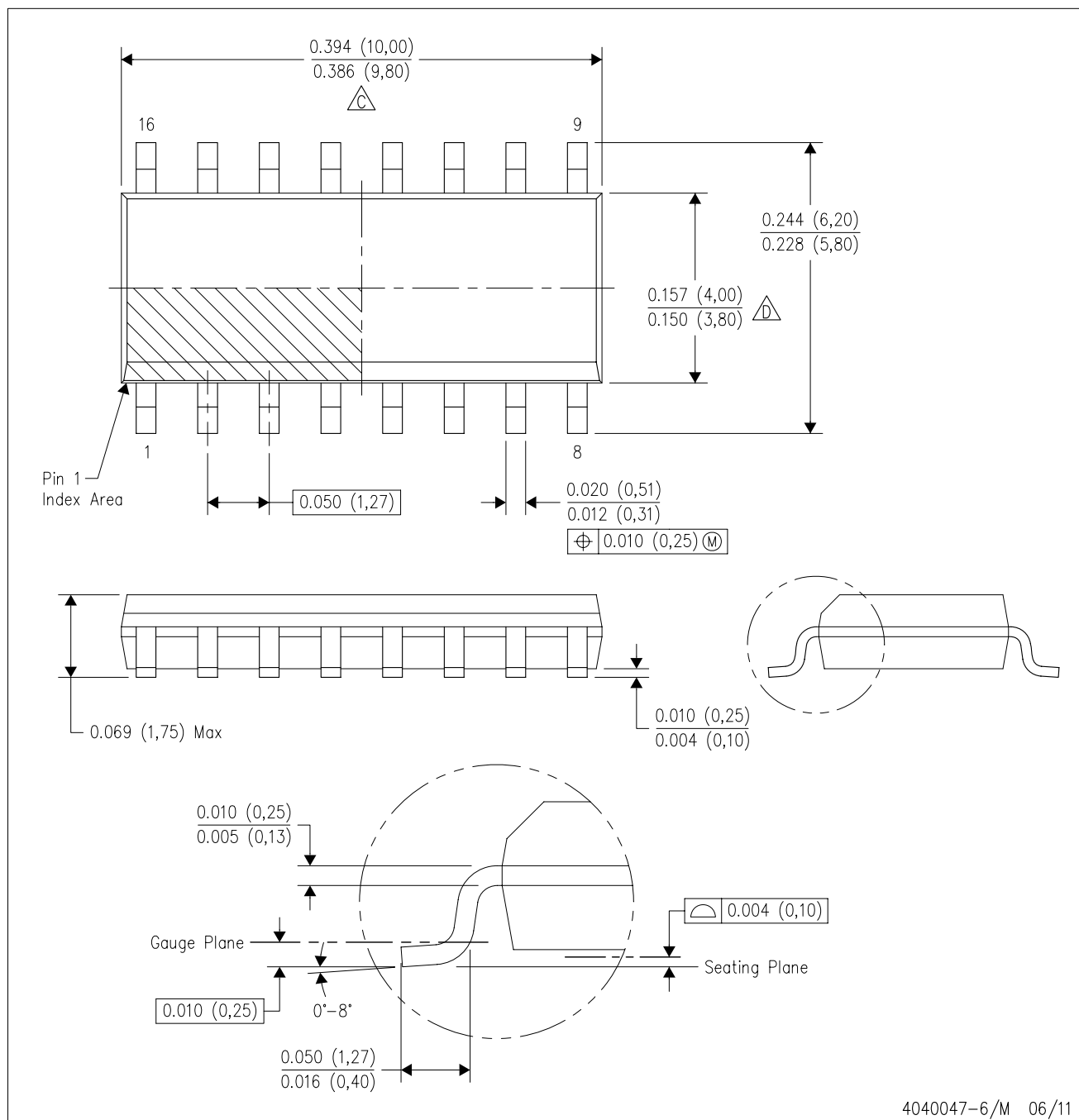


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4049UBDR	SOIC	D	16	2500	333.2	345.9	28.6
CD4049UBPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4050BDR	SOIC	D	16	2500	333.2	345.9	28.6
CD4050BDWR	SOIC	DW	16	2000	367.0	367.0	38.0
CD4050BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

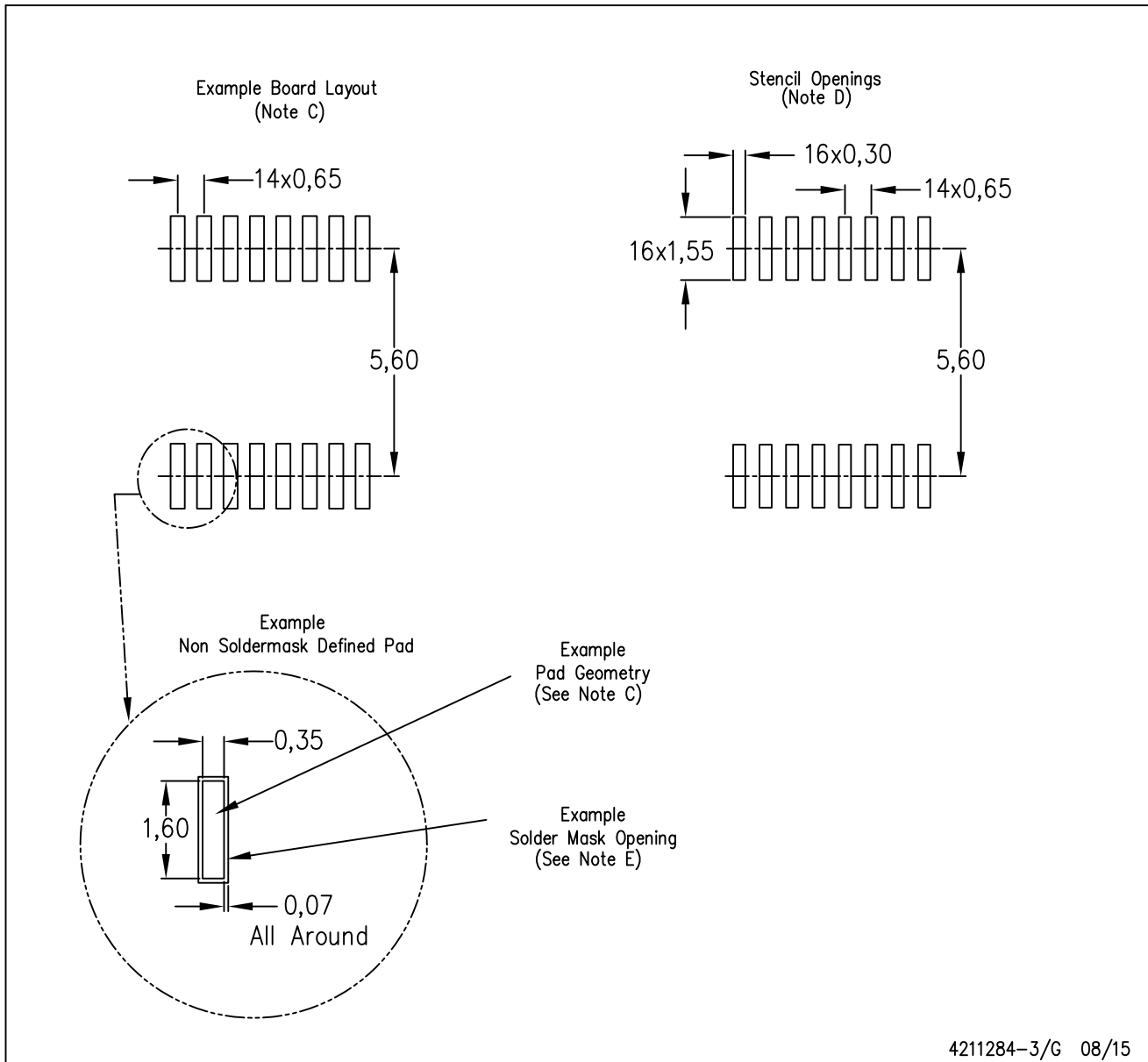


4040064-4/G 02/11

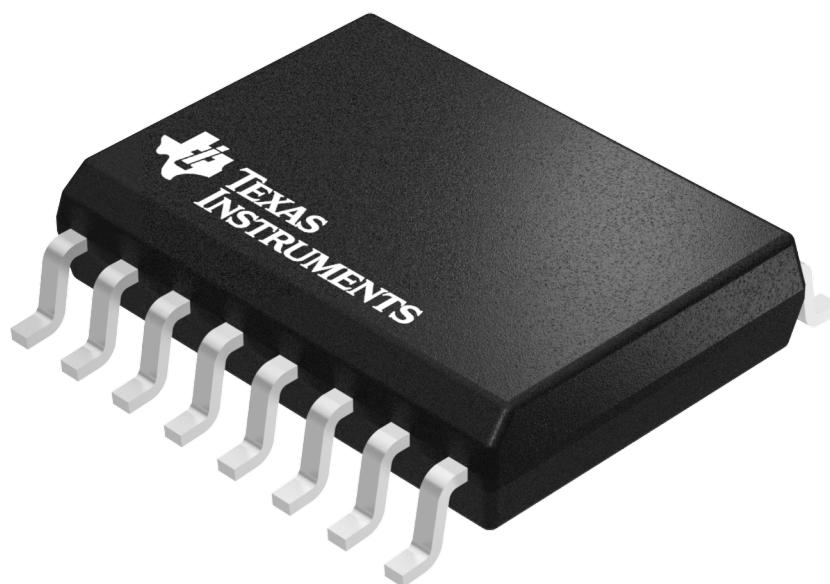
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



DW0016A

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

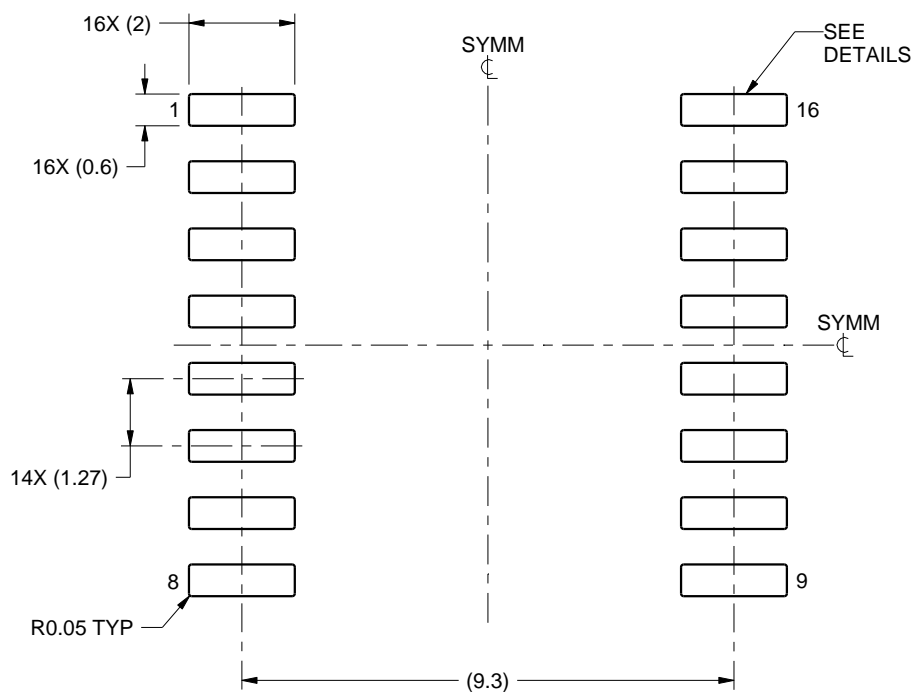
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

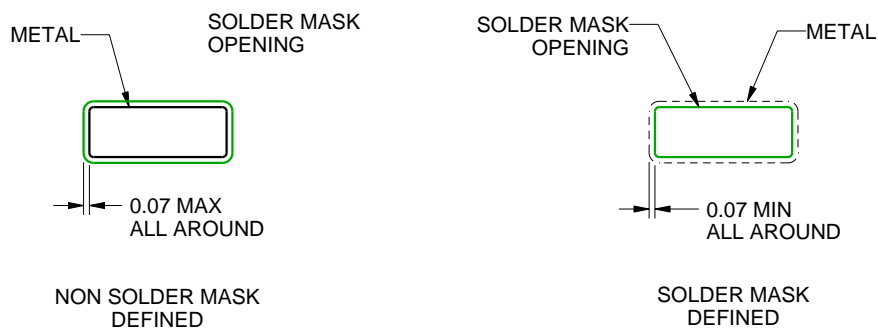
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

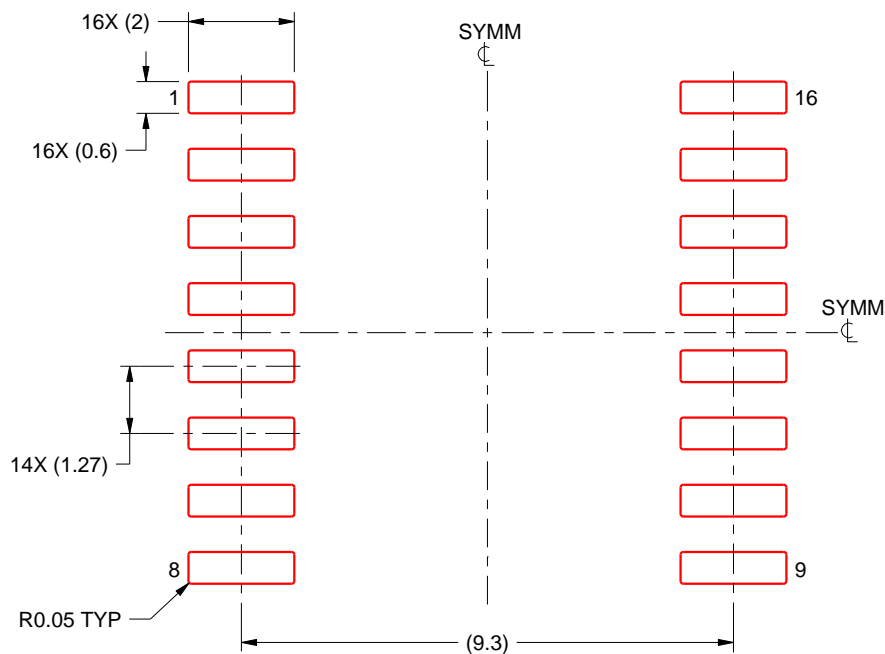


# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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