ICS-52000

Low-Noise Microphone with TDM Digital Output

GENERAL DESCRIPTION

The ICS-52000 is a digital TDM output bottom port microphone. The complete ICS-52000 solution consists of a MEMS sensor, signal conditioning, an analog-to-digital converter, decimation and anti-aliasing filters, power management, and an industry standard 24-bit TDM interface. The TDM interface allows an array of up to 16 of the ICS-52000 microphones to connect directly to digital processors, such as DSPs and microcontrollers, without the need for an audio codec in the system. All microphones in an array sample their acoustic signals synchronously, enabling precise array processing.

The ICS-52000 has a high SNR of 65 dBA and a wideband frequency response. The sensitivity tolerance of the ICS-52000 is ±1 dB, which enables high-performance microphone arrays without the need for system calibration.

The ICS-52000 is available in a small 4 mm × 3 mm × 1 mm surface-mount package.

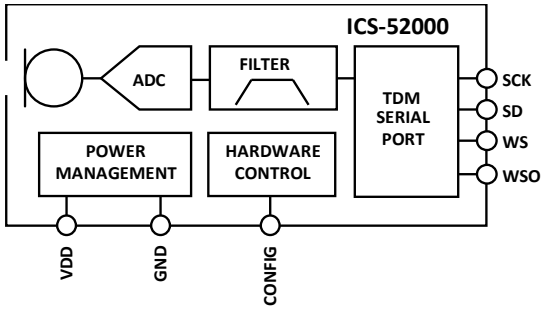
APPLICATIONS

- Speech Recognition Arrays
- Smart Televisions
- Teleconferencing Systems
- Gaming Consoles
- Security Systems
- Microphone Arrays

FEATURES

- Digital TDM Interface with High Precision 24-bit Data
- Supports TDM arrays of up to 16 synchronously-sampled channels
- High 65 dBA SNR
- −26 dB FS Sensitivity
- ±1 dB Sensitivity Tolerance
- Wide Frequency Response from 50 Hz to 20 kHz
- Low Current Consumption: 1.0 mA
- High Power Supply Rejection: −89 dB FS
- 117 dB SPL Acoustic Overload Point
- Small 4 mm × 3 mm × 1 mm Surface-Mount Package
- Compatible with Sn/Pb and Pb-Free Solder Processes
- RoHS/WEEE Compliant

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART	TEMP RANGE	PACKAGING
ICS-52000	−40°C to +85°C	13” Tape & Reel
EV_ICS-52000-FX	—	

InvenSense Inc.
1745 Technology Drive, San Jose, CA 95110 U.S.A
+1(408) 988–7339
www.invensense.com

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SPECIFICATIONS

TABLE 1. ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_{DD} = 1.8 to 3.3V, f_{SCK} = 3.072 MHz, C_{LOAD} = 30 pF unless otherwise noted. Typical specifications are not guaranteed.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PERFORMANCE							
Directionality				Omni			
Sensitivity		1 kHz, 94 dB SPL	−27	−26	−25	dB FS	
Signal-to-Noise Ratio (SNR)				65		dBA	
Equivalent Input Noise (EIN)				29		dBA SPL	
Dynamic Range		Derived from EIN and acoustic overload point		88		dB	
Total Harmonic Distortion (THD)		105 dB SPL		0.3	1	%	
Power-Supply Rejection (PSR)		217 Hz, 100 mVp-p square wave superimposed on VDD = 1.8 V (A-weighted)		−89		dB FS	
Power-Supply Rejection – Swept Sine		1 kHz sine wave		−98		dB FS	
Acoustic Overload Point		10% THD		117		dB SPL	
Noise Floor		20 Hz to 20 kHz, A-weighted, rms		−91		dB FS	
POWER SUPPLY							
Supply Voltage (V_{DD})			1.62		3.63	V	
Supply Current (I_S)	V_{DD} = 1.8V	Normal Mode		1.0	1.4	mA	
		Standby		5	20	µA	
	V_{DD} = 3.3V	Normal Mode		1.1	1.5	mA	
		Standby		7	24	µA	
DIGITAL FILTER							
Group Delay		Acoustic input to digital output – includes filter and TDM serial output		$2/f_S$		sec	
Pass Band Ripple					±0.3	dB	
Stop Band Attenuation				58		dB	
Pass Band		fs = 48 kHz		20		kHz	

TABLE 2. TDM DIGITAL INPUT/OUTPUT

–40°C < T_A < +85°C, 1.8 V < VDD < 3.3 V, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	MAX	UNITS	NOTES
DIGITAL INPUT					
Voltage Input Low (V_{IL})		0	0.25 × V_{DD}	V	
Voltage Input High (V_{IH})		0.7 × V_{DD}	V_{DD}	V	
SD DIGITAL OUTPUT					
Voltage Output Low (V_{OL})		0	0.25 × V_{DD}	V	
Voltage Output High (V_{OH})		0.7 × V_{DD}	V_{DD}	V	
Maximum Load	CLK = 24.576 MHz		150	pF	

TABLE 3. SERIAL DATA PORT TIMING SPECIFICATION

–40°C < TA < +85°C, 1.8 V < VDD < 3.3 V, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	MAX	UNITS	NOTES
SCK duty cycle		48	52	%	
SCK period (t_{SCP})		37		ns	
SCK frequency (f_{SCK})		0.460	27.034	MHz	
WS setup (t_{WSS})		0		ns	
WS hold (t_{WSH})		10		ns	
WS frequency (f_S)		7.19	52.8	kHz	
SD data valid (t_{SDV})	From SCK rising to valid SD data		18	ns	
SD data disable (t_{SDD})	From SCK rising to SD output tristated		18	ns	
WSO valid (t_{WSOV})	15 pF trace load		18	ns	
WSO disable (t_{WSOD})	15 pF trace load		18	ns	

TIMING DIAGRAM

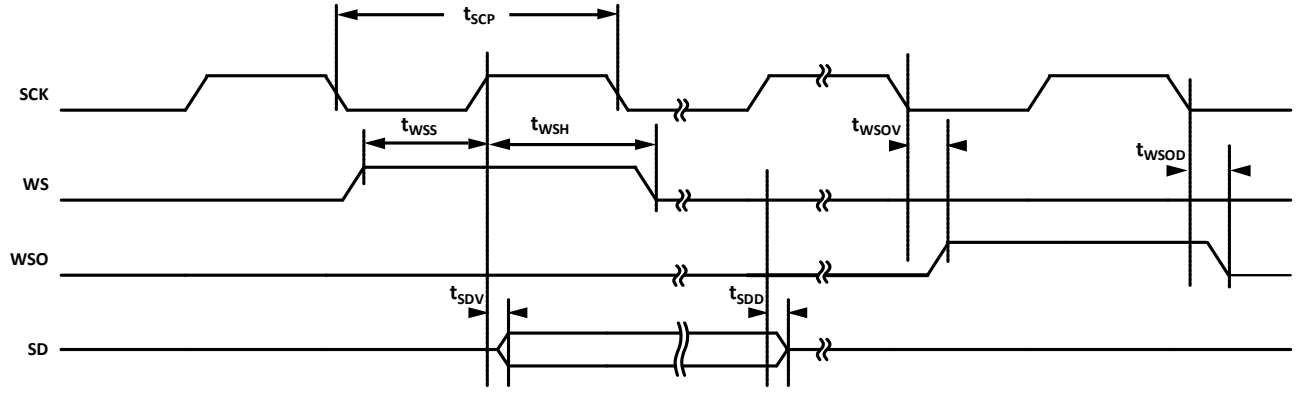

Figure 1. Serial Data Port Timing

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ABSOLUTE MAXIMUM RATINGS

Stress above those listed as Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

TABLE 4. ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING
Supply Voltage (V_{DD})		−0.3V to +3.63V
Digital Pin Input Voltage		−0.3V to V_{DD} + 0.3V or 3.63V, whichever is less
Sound Pressure Level		160 dB
Mechanical Shock		10,000 *g*
Vibration		Per MIL-STD-883 Method 2007, Test Condition B
Temperature Range	Biased	−40°C to +85°C
	Storage	−55°C to +150°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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SOLDERING PROFILE

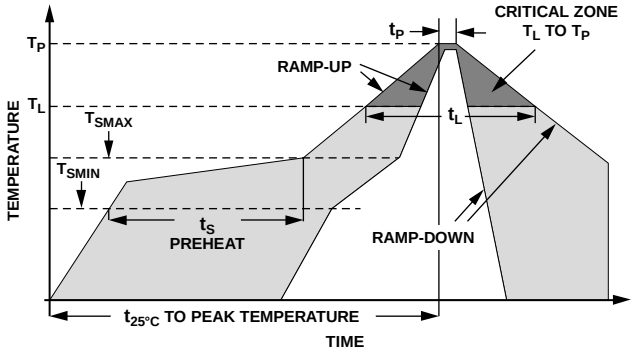

Figure 2. Recommended Soldering Profile Limits

TABLE 5. RECOMMENDED SOLDERING PROFILE

PROFILE FEATURE		Sn63/Pb37	Pb-Free
Average Ramp Rate (T_L to T_P)		1.25°C/sec max	1.25°C/sec max
Preheat	Minimum Temperature (T_{SMIN})	100°C	100°C
	Minimum Temperature (T_{SMIN})	150°C	200°C
	Time (T_{SMIN} to T_{SMAX}), t_S	60 sec to 75 sec	60 sec to 75 sec
Ramp-Up Rate (T_{SMAX} to T_L)		1.25°C/sec	1.25°C/sec
Time Maintained Above Liquidous (t_L)		45 sec to 75 sec	~50 sec
Liquidous Temperature (T_L)		183°C	217°C
Peak Temperature (T_P)		215°C ±3°C/−3°C	260°C +0°C/−5°C
Time Within +5°C of Actual Peak Temperature (t_P)		20 sec to 30 sec	20 sec to 30 sec
Ramp-Down Rate		3°C/sec max	3°C/sec max
Time +25°C ($t_{25°C}$) to Peak Temperature		5 min max	5 min max

**The reflow profile in Table 5 is recommended for board manufacturing with InvenSense MEMS microphones. All microphones are also compatible with the J-STD-020 profile.*

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

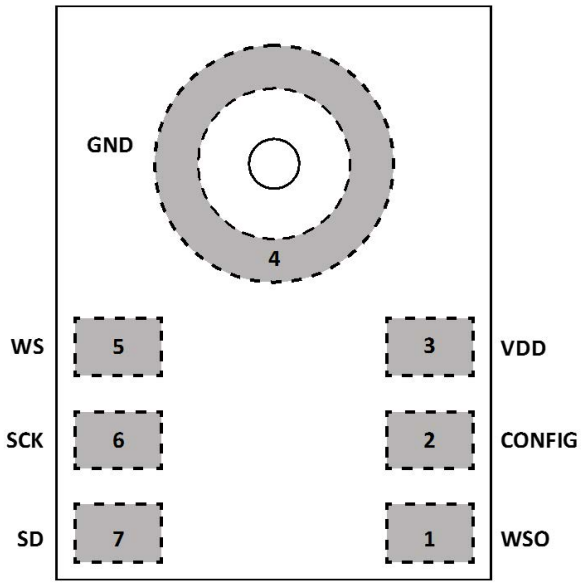

Figure 3. Pin Configuration (Top View, Terminal Side Down)

TABLE 6. PIN FUNCTION DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1	WSO	Output	WS output, connect to WS of the next ICS-52000 in the daisy-chain.
2	CONFIG	Input	Pull to VDD. The state of this pin is used at power-up.
3	VDD	Power	Power, 1.62V to 3.63V. This pin should be decoupled to GND with a 0.1 µF capacitor.
4	GND	Ground	Ground. Connect to ground on the PCB.
5	WS	Input	Serial Data-Word Select for TDM Interface
6	SCK	Input	Serial Data Clock for TDM Interface
7	SD	Output	Serial Data Output for TDM Interface. This pin tri-states when not actively driving the appropriate output channel. The SD trace should have a 100 kΩ pulldown resistor to discharge the line during the time that all microphones on the bus have tri-stated their outputs.

TYPICAL PERFORMANCE CHARACTERISTICS

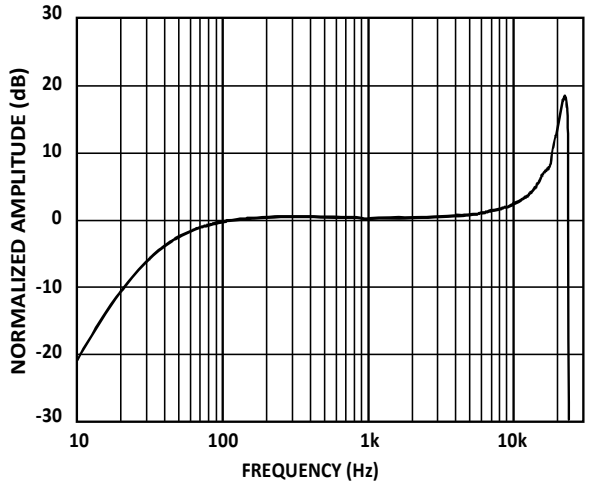

Figure 4. Typical Frequency Response (Measured)

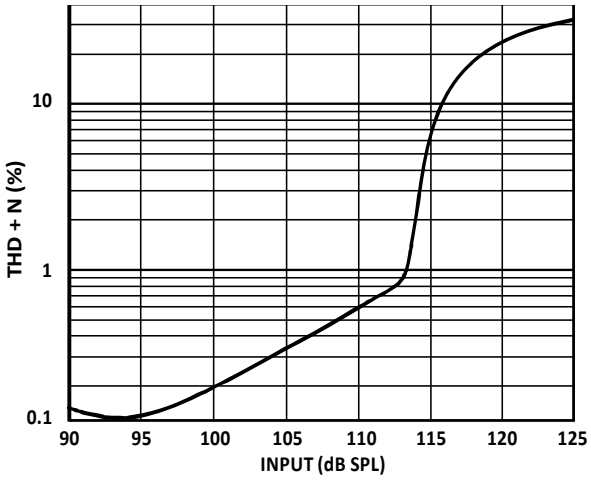

Figure 5. Total Harmonic Distortion + Noise (THD+N) vs. Input SPL

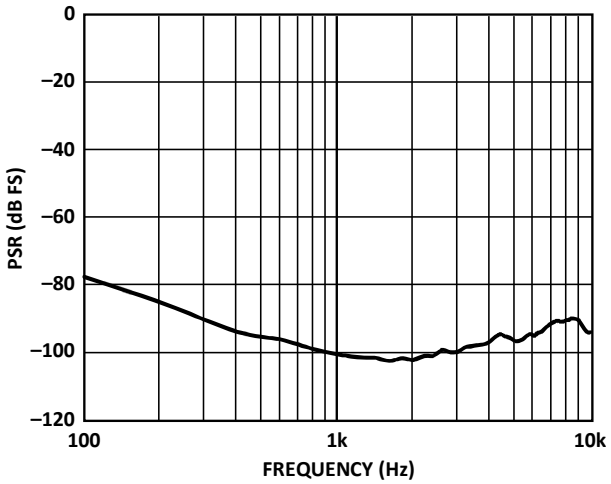

Figure 6. PSR vs. Frequency, 100 mV p-p Swept Sine Wave

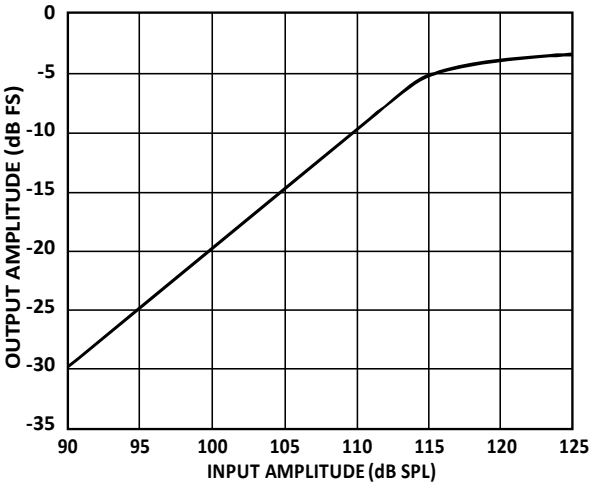

Figure 7. Linearity

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THEORY OF OPERATION

STARTUP AND POWER MANAGEMENT

The ICS-52000 has two power states: normal operation, and standby mode.

Startup

At startup of the ICS-52000, the start of the frame sync (WS) signal should be delayed from the start of the serial clock (SCK) by at least 10 ms. This enables the microphone's internal circuits to completely initialize before starting the synchronization sequence with other microphones in the TDM array. This delay can be implemented either by enabling the WS output on the clock master at least 10 ms after the SCK is enabled, or by externally controlling the signals given to the ICS-52000s.

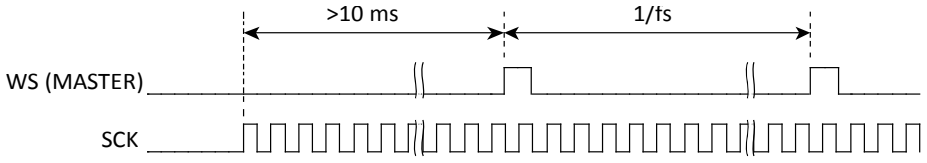

Figure 8. Clock Startup Sequence

The ICS-52000 will begin to output non-zero data 4462 SCK clock cycles (1.5 ms with f_{SCK} = 3.072 MHz) after initial power-up. The data is valid to use after the initial 262,144 SCK cycles (85 ms with f_{SCK} = 3.072 MHz). This startup time is applicable any time it is entering normal operation mode, coming either from power-down or out of standby.

Table 7 shows the startup time for different sampling rates.

Table 7. Startup time

f_S (WS frequency)	Time to non-zero data output	Startup time to valid data
48 kHz	1.5 ms	85 ms
24 kHz	3.0 ms	171 ms
16 kHz	4.5 ms	256 ms
8 kHz	9.0 ms	512 ms

Normal Operation

The part is in normal operation mode when SCK and WS are active. Clocks should not be supplied to the microphones until they are settled and stable.

Standby Mode

The microphone enters standby mode when the frequency of SCK falls below about 1 kHz. It is recommended to enter standby mode by stopping both the SCK and WS clock signals and pulling those signals to ground to avoid drawing current through the WS pin's internal pull-down resistor. The timing for exiting standby mode is the same as normal startup.

Do not supply active clocks (WS and SCK) to the ICS-52000 while there is no power supplied to VDD, doing this continuously turns on ESD protection diodes, which may affect long-term reliability of the microphone.

Soft Unmute

The ICS-52000 has a soft unmute feature to prevent pops on power-up. From the time that the ICS-52000 starts to output data, the volume will ramp up to the full-scale output level over 256 WS clock cycles. With a 48 kHz sampling rate, this unmute sequence will take about 5.3 ms.

SYNCHRONIZING MICROPHONES

ICS-52000 microphones are synchronized by the WS signal, so audio captured from multiple microphones sharing the same clock will be sampled synchronously.

TDM DATA INTERFACE

The slave serial data port's format is TDM, 24-bit, twos complement and up to 16 ICS-52000 microphones can be daisy-chained together on a single data bus. There must be 64, 128, 256 or 512 SCK cycles in each WS frame. Each microphone will output 24-bit data in subsequent 32-bit slots. Tie the SD pins of all ICS-52000 microphones driving the data bus together as shown in Figure 9. The ICS-52000 will always be a slave on the TDM bus.

The word select/word clock signals of the microphones in the system will be daisy-chained so that the clock master drives WS of the first ICS-52000, whose WSO will drive WS of the second ICS-52000, and so on; the last ICS-52000 in the chain can leave WSO disconnected. See Figure 9 for an illustration of these connections. The ICS-52000's WS clock input is sampled on the rising edge of SCK and the falling edge of WS can come anywhere before the start of the next frame. The ICS-52000 connected directly to the system's clock master will output its data in the first TDM slot, the next microphone in the chain will output its data in the second TDM slot, and so on.

The frequency of SCK will depend on the number of microphones in the system. The SCK frequency should be $n \times 32 \times f_S$, where n is a power of two (2, 4, 8, or 16) equal to or greater than the number of ICS-52000s on the bus. Table 8 shows the recommended SCK frequency for a chain of ICS-52000 microphones.

Table 8. SCK Frequency

Number of ICS-52000 Microphones	SCK Frequency, based on WS frequency (f_S)
1-2	$64 \times f_S$
3-4	$128 \times f_S$
5-8	$256 \times f_S$
9-16	$512 \times f_S$

Figure 10 shows the format of an n-channel TDM data stream. Figure 11 zooms in on a single TDM data slot as output from a single ICS-52000 microphone.

Data Output Format

The output data word length is 24 bits/channel. The data word format is 2's complement, MSB-first.

The serial TDM data output bits are triggered on SCK's rising edge. The receiver (DSP, codec, microcontroller) should sample that data bit on the next SCK rising edge. This is illustrated in Figure 11; SCK rising edge A triggers the SD output bit and the receiver should sample the data at its input on SCK rising edge B. The data is formatted in this way to support the internal propagation delay of the microphone data at high SCK frequencies.

The output data pin (SD) is tri-stated when it is not actively driving TDM output data. SD will immediately tri-state after the LSB is output so that another microphone can drive the common data line.

The SD trace should have a pull-down resistor to discharge the line during the time that all microphones on the bus have tri-stated their outputs. A 100 kΩ or smaller resistor is sufficient for this, as shown in Figure 9.

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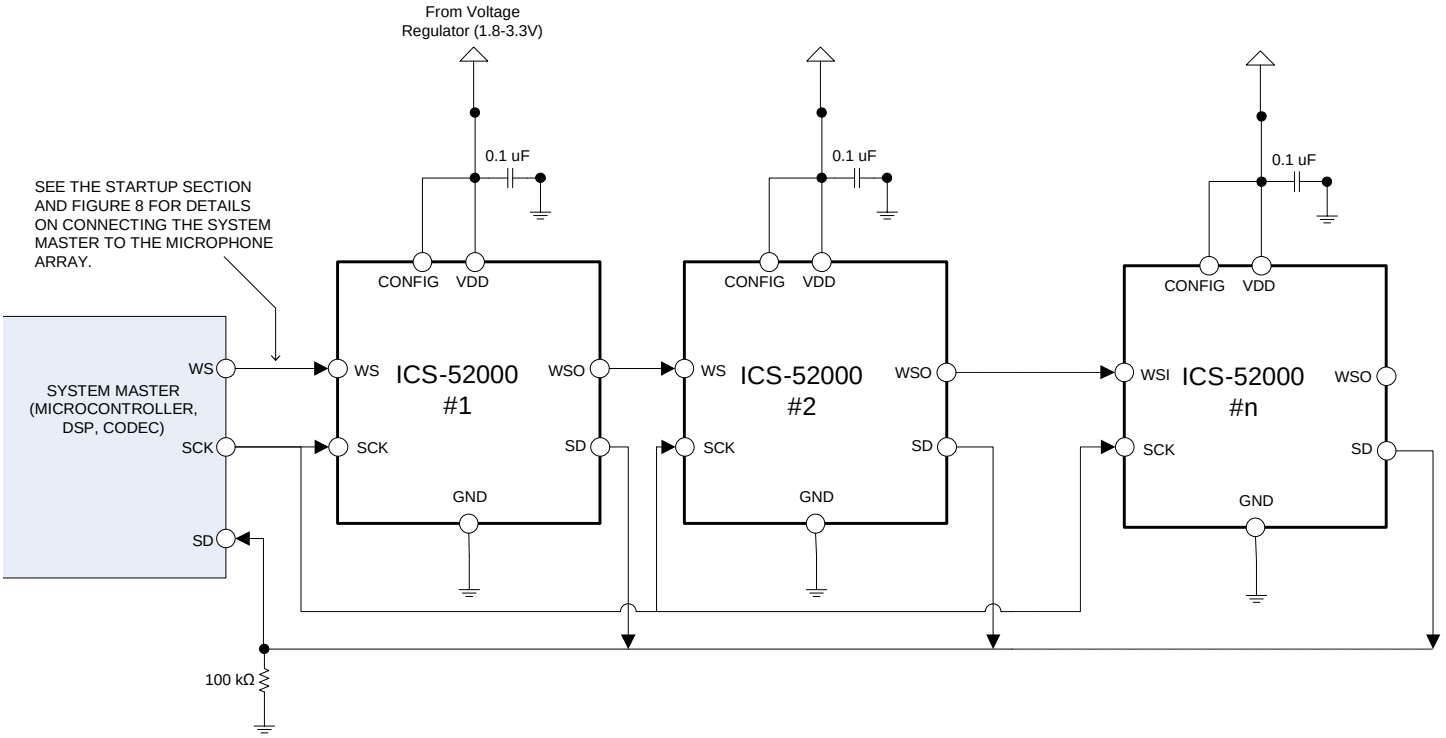

Figure 9. System Block Diagram

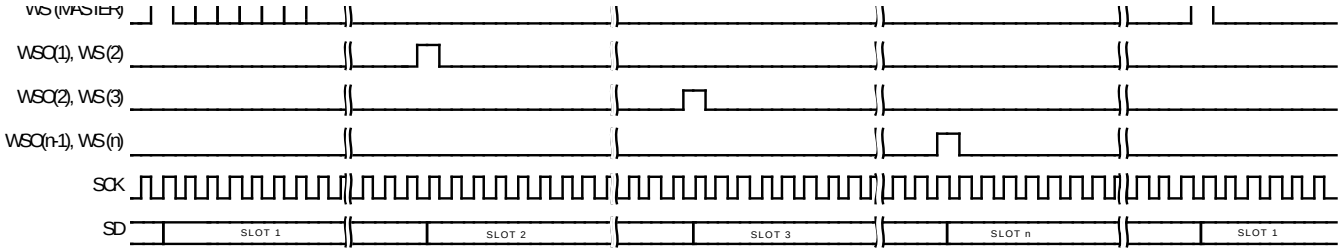

Figure 10. n-Channel Output TDM Timing Diagram

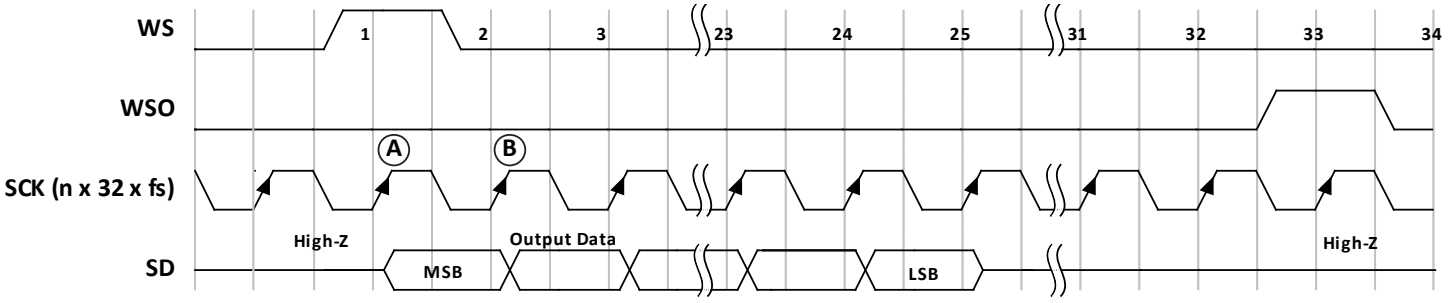

Figure 11. Single TDM Slot Timing Diagram

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DIGITAL MICROPHONE SENSITIVITY

The sensitivity of a digital output microphone is specified in units of dB FS (decibels relative to a full-scale digital output). A 0 dB FS sine wave is defined as a signal whose peak just touches the full-scale code of the digital word (see Figure 5). This measurement convention means that signals with a different crest factor may have an RMS level higher than 0 dB FS. For example, a full-scale square wave has an RMS level of 3 dB FS.

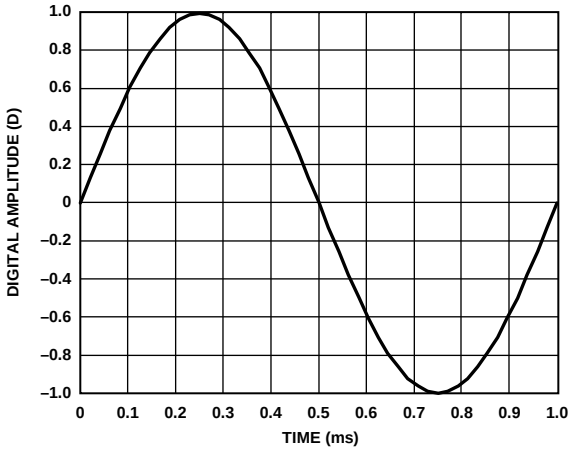

Figure 12. 1 kHz, 0 dB FS Sine Wave

The definition of a 0 dB FS signal must be understood when measuring the sensitivity of the ICS-52000. An acoustic input signal of a 1 kHz sine wave at 94 dB SPL applied to the ICS-52000 results in an output signal with a −26 dB FS level. This means that the output digital word peaks at −26 dB below the digital full-scale level. A common misunderstanding is that the output has an RMS level of −29 dB FS; however, this is not the case because of the definition of a 0 dB FS sine wave.

There is no commonly accepted unit of measurement to express the instantaneous level of a digital signal output from the microphone, as opposed to the RMS level of the signal. Some measurement systems express the instantaneous level of an individual sample in units of D, where 1.0 D is digital full scale (see Figure 12). In this case, a −26 dB FS sine wave has peaks at 0.05 D.

For more information about digital microphone sensitivity, see the AN-1112 Application Note, *Microphone Specifications Explained*.

DIGITAL FILTER CHARACTERISTICS

The ICS-52000 has an internal digital bandpass filter. A high-pass filter eliminates unwanted low frequency signals. A low-pass decimation filter scales the pass band with the sampling frequency and performs required out-of-band noise reduction.

High-Pass Filter

The ICS-52000 incorporates a high-pass filter to remove unwanted dc and very low frequency components. With f_S = 48 kHz, this high pass filter has a −3 dB corner frequency of 3.7 Hz. The cutoff frequency scales with changes in sampling rate.

This digital filter response is in addition to the acoustic high-pass response of the ICS-52000 that has a −3 dB corner of 50 Hz.

Low-Pass Decimation Filter

The analog-to-digital converter in the ICS-52000 is a single-bit, high order, sigma-delta (Σ-Δ) running at a high oversampling ratio. The noise shaping of the converter pushes the majority of the noise well above the audio band and gives the microphone a wide dynamic range. However, it does require a good quality low-pass decimation filter to eliminate the high frequency noise.

The pass band of the filter extends to 0.417 × f_S and, in that band, has only 0.04 dB of ripple. The high frequency cutoff of −3 dB occurs at 0.5 × f_S. A 48 kHz sampling rate results in a pass band of 20.3 kHz and a half amplitude corner at 24 kHz; the stop-band attenuation of the filter is 58 dB. Note that these filter specifications scale with sampling frequency.

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APPLICATIONS INFORMATION

SD OUTPUT DRIVE STRENGTH

The SD data output pin must drive a load that includes the PCB trace and the tri-stated inputs of the other ICS-52000 SD pins connected to that same trace. The tri-stated load capacitance of the ICS-52000 SD pin is about 6 pF. The ICS-52000 is designed to drive a load of 150 pF. If 16 ICS-52000 microphones are connected to a common 30" SD trace on a typical PCB, the driver will meet the timing specs with a 24.576 MHz SCK and 2 ns propagation delay.

Design Recommendations

The SD output driver has an output impedance of about 25-35Ω. A source termination resistor placed close to each microphone's SD pin may help to reduce ringing and overshoot on the output signal. A 15-25Ω resistor will help to match the source impedance to a typical 50Ω transmission line.

The SD signal's propagation delay is a function of the PCB material and length of the trace. Arrays with a larger number of microphones will usually have a longer SD trace on the PCB. The worst-case timing conditions specified above (24.576 MHz SCK, 2 ns propagation delay) were calculated for a 16 microphone array with 2" spacing between each microphone and f_S = 48 kHz.

The propagation delay is minimized by reducing the distance between the SD source and the device receiving the data. This is done by placing the receiver in the layout in the middle of the SD trace, rather than at one of the extremes. That will cut the worst-case propagation delay in half, compared to if the receiver is placed at one end of a long SD trace.

If the distance between the microphone array and the receiver cannot be minimized, it may be useful to have a buffer between the two. Place the buffer at the point that minimizes the distance between it and the furthest microphones on the PCB trace. This single buffer could drive the remaining distance between it and the data receiver. The buffer's propagation delay may be a critical spec, especially with higher clock rates.

POWER SUPPLY DECOUPLING

For best performance and to avoid potential parasitic artifacts, placing a 0.1 µF ceramic type X7R or better capacitor between Pin 3 (VDD) and ground is strongly recommended. The capacitor should be placed as close to Pin 3 as possible.

The connections to each side of the capacitor should be as short as possible, and the trace should stay on a single layer with no vias. For maximum effectiveness, locate the capacitor equidistant from the power and ground pins or, when equidistant placement is not possible, slightly closer to the power pin. Thermal connections to the ground planes should be made on the far side of the capacitor, as shown in Figure 13.

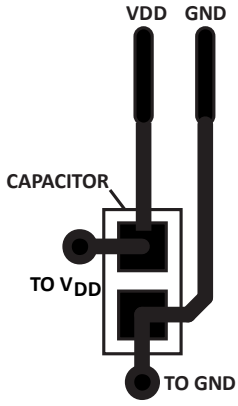

Figure 13. Recommended Power Supply Bypass Capacitor Layout

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SUPPORTING DOCUMENTS

For additional information, see the following documents.

EVALUATION BOARD USER GUIDE

AN-000001, *Bottom-Port I²S/TDM Output MEMS Microphone Evaluation Board*
AN-000099, *Synchronous Sampling with an Array of ICS-52000 TDM Microphones*

APPLICATION NOTES

AN-100, *MEMS Microphone Handling and Assembly Guide*
AN-1003, *Recommendations for Mounting and Connecting the InvenSense Bottom-Ported MEMS Microphones*
AN-1112, *Microphone Specifications Explained*
AN-1124, *Recommendations for Sealing InvenSense Bottom-Port MEMS Microphones from Dust and Liquid Ingress*
AN-1140, *Microphone Array Beamforming*

PCB DESIGN AND LAND PATTERN LAYOUT

The recommended PCB land pattern for the ICS-52000 should be laid out to a 1:1 ratio to the solder pads on the microphone package, as shown in Figure 14. Take care to avoid applying solder paste to the sound hole in the PCB. A suggested solder paste stencil pattern layout is shown in Figure 15. The diameter of the sound hole in the PCB should be larger than the diameter of the sound port of the microphone. A minimum diameter of 0.5 mm is recommended.

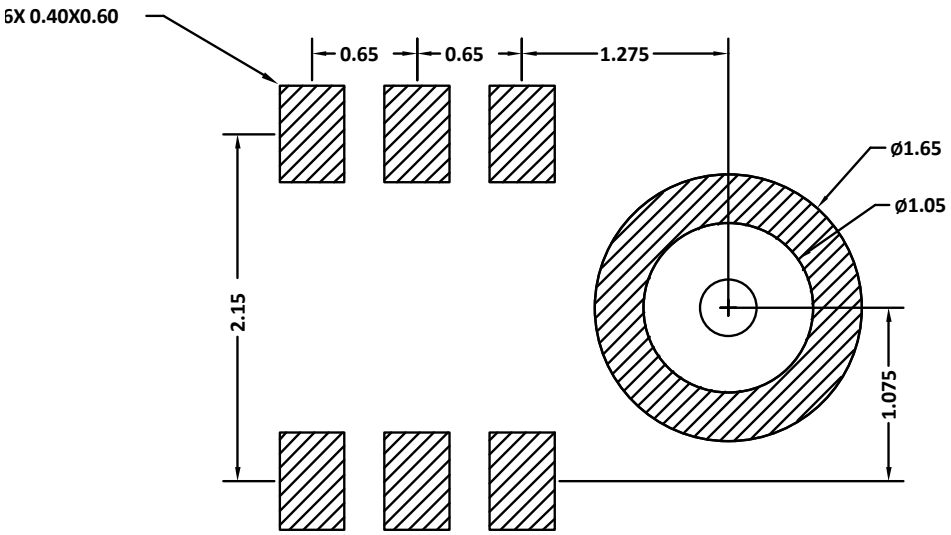

Figure 14. PCB Land Pattern Layout

Dimensions shown in millimeters

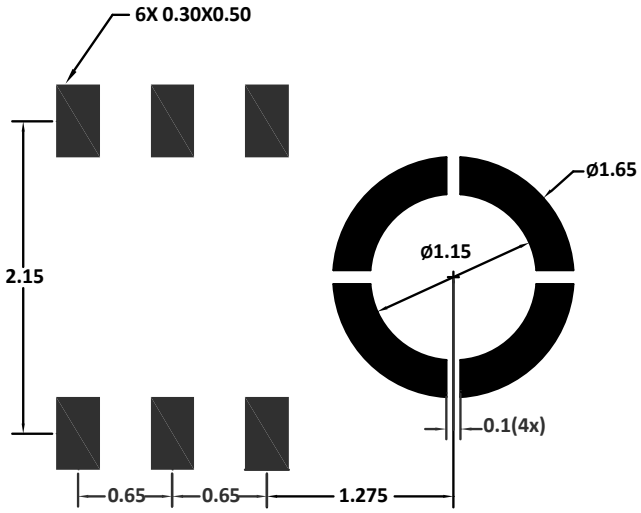

Figure 15. Suggested Solder Paste Stencil Pattern Layout

Dimensions shown in millimeters

PCB MATERIAL AND THICKNESS

The performance of the ICS-52000 is not affected by PCB thickness. The ICS-52000 can be mounted on either a rigid or flexible PCB. A flexible PCB with the microphone can be attached directly to the device housing with an adhesive layer. This mounting method offers a reliable seal around the sound port while providing the shortest acoustic path for good sound quality.

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HANDLING INSTRUCTIONS

PICK AND PLACE EQUIPMENT

The MEMS microphone can be handled using standard pick-and-place and chip shooting equipment. Take care to avoid damage to the MEMS microphone structure as follows:

- Use a standard pickup tool to handle the microphone. Because the microphone hole is on the bottom of the package, the pickup tool can make contact with any part of the lid surface.
- Do not pick up the microphone with a vacuum tool that makes contact with the bottom side of the microphone. Do not pull air out of or blow air into the microphone port.
- Do not use excessive force to place the microphone on the PCB.

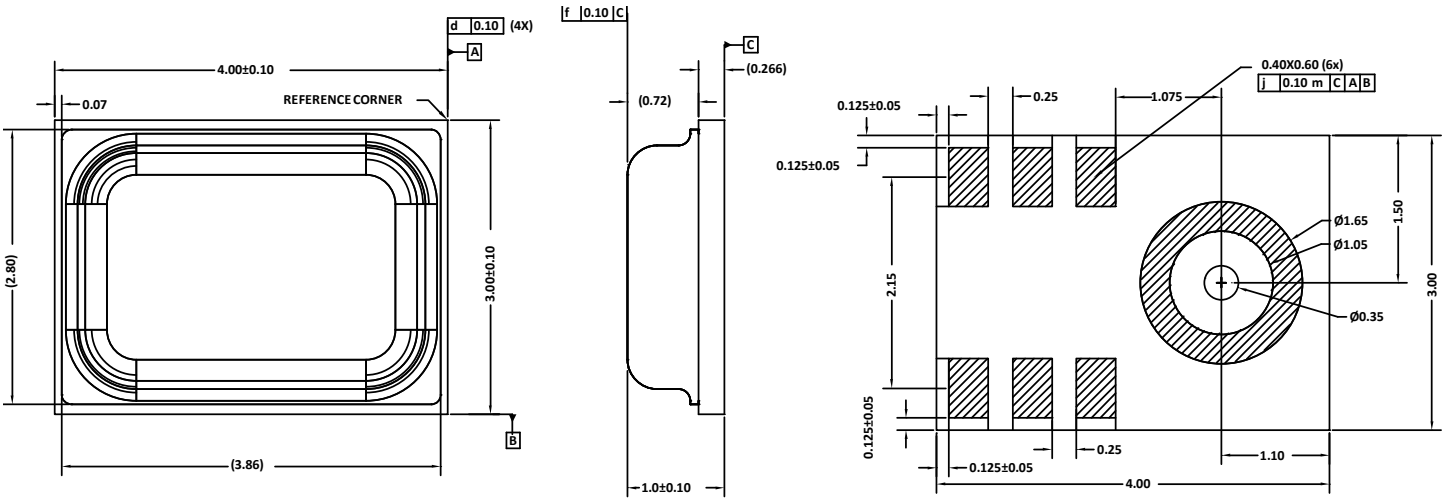
REFLOW SOLDER

For best results, the soldering profile must be in accordance with the recommendations of the manufacturer of the solder paste used to attach the MEMS microphone to the PCB. It is recommended that the solder reflow profile not exceed the limit conditions specified in Figure 2 and Table 5.

BOARD WASH

When washing the PCB, ensure that water does not make contact with the microphone port. Do not use blow-off procedures or ultrasonic cleaning.

OUTLINE DIMENSIONS



TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

Figure 16. 7-Terminal Chip Array Small Outline No Lead Cavity
4.00 × 3.00 × 1.00 mm Body
Dimensions shown in millimeters

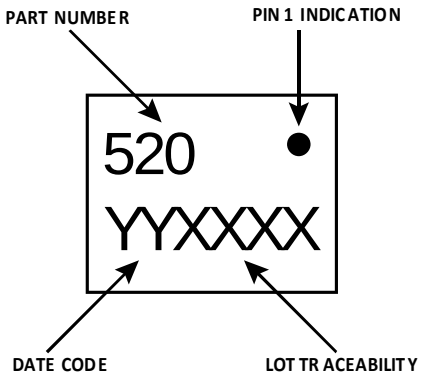


Figure 17. Package Marking Specification (Top View)

ORDERING GUIDE

PART	TEMP RANGE	PACKAGE	QUANTITY	PACKAGING
ICS-52000	−40°C to +85°C	7-Terminal LGA_CAV	5,000	13” Tape and Reel
EV_ICS-52000-FX		Flex Evaluation Board		

REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
8/26/2016	1.0	Initial Version
9/14/2016	1.1	Fixed typo on Table 8
1/4/2017	1.2	Updated boilerplate text to reflect Production status.
4/14/2017	1.3	Updated Table 3, Figure 1, Startup and TDM Data Interface Sections

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