

## N-Channel Power MOSFET

600V, 2A, 4.4Ω

### FEATURES

- Advanced planar process
- 100% avalanche tested
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

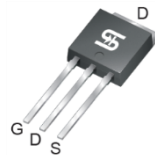
### APPLICATION

- Power Supply
- Lighting

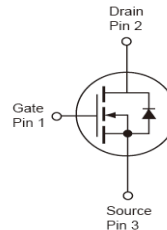
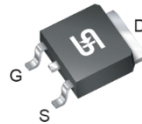
KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
$V_{DS}$	600	V
$R_{DS(on)}$ (max)	4.4	Ω
$Q_g$	9.4	nC



TO-251(IPAK)



TO-252(DPAK)



Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	±30	V
Continuous Drain Current <sup>(Note 1)</sup>	$I_D$	$T_C = 25^\circ\text{C}$	2
		$T_C = 100^\circ\text{C}$	1.35
Pulsed Drain Current <sup>(Note 2)</sup>	$I_{DM}$	8	A
Single Pulsed Avalanche Energy <sup>(Note 3)</sup>	$E_{AS}$	55	mJ
Single Pulsed Avalanche Current <sup>(Note 3)</sup>	$I_{AS}$	2	A
Repetitive Avalanche Energy <sup>(Note 2)</sup>	$E_{AR}$	4.4	mJ
Peak Diode Recovery $dv/dt$ <sup>(Note 4)</sup>	$dv/dt$	4.5	V/ns
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_{DTOT}$	44	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +150	°C

<b>THERMAL PERFORMANCE</b>			
<b>PARAMETER</b>	<b>SYMBOL</b>	<b>LIMIT</b>	<b>UNIT</b>
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.87	$^{\circ}\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	110	$^{\circ}\text{C/W}$

**Notes:**  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\theta JA}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.  $R_{\theta JA}$  shown below for single device operation on FR-4 PCB in still air

<b>ELECTRICAL SPECIFICATIONS</b> ( $T_A = 25^{\circ}\text{C}$ unless otherwise noted)						
<b>PARAMETER</b>	<b>CONDITIONS</b>	<b>SYMBOL</b>	<b>MIN</b>	<b>TYP</b>	<b>MAX</b>	<b>UNIT</b>
<b>Static</b> (Note 5)						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	$BV_{DSS}$	600	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	2.5	3.6	4.5	V
Gate Body Leakage	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	$I_{GSS}$	--	--	$\pm 100$	nA
Zero Gate Voltage Drain Current	$V_{DS} = 600\text{V}, V_{GS} = 0\text{V}$	$I_{DSS}$	--	--	10	$\mu\text{A}$
Drain-Source On-State Resistance	$V_{GS} = 10\text{V}, I_D = 1\text{A}$	$R_{DS(ON)}$	--	3.9	4.4	$\Omega$
Forward Transfer Conductance	$V_{DS} = 40\text{V}, I_D = 1\text{A}$	$g_{fs}$	--	1.5	--	S
<b>Dynamic</b> (Note 6)						
Total Gate Charge	$V_{DS} = 480\text{V}, I_D = 2\text{A},$ $V_{GS} = 10\text{V}$	$Q_g$	--	9.4	--	nC
Gate-Source Charge		$Q_{gs}$	--	2.2	--	
Gate-Drain Charge		$Q_{gd}$	--	4.7	--	
Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$	$C_{iss}$	--	249	--	pF
Output Capacitance		$C_{oss}$	--	30.7	--	
Reverse Transfer Capacitance		$C_{rss}$	--	5	--	
Gate Resistance	$F = 1\text{MHz}, \text{open drain}$	$R_g$	--	8.5	--	$\Omega$
<b>Switching</b> (Note 7)						
Turn-On Delay Time	$V_{GS} = 10\text{V}, I_D = 2\text{A},$ $V_{DD} = 300\text{V}, R_G = 25\Omega$	$t_{d(on)}$	--	9.1	--	ns
Turn-On Rise Time		$t_r$	--	9.8	--	
Turn-Off Delay Time		$t_{d(off)}$	--	17.4	--	
Turn-Off Fall Time		$t_f$	--	12.4	--	

<b>ELECTRICAL SPECIFICATIONS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise noted)						
<b>PARAMETER</b>	<b>CONDITIONS</b>	<b>SYMBOL</b>	<b>MIN</b>	<b>TYP</b>	<b>MAX</b>	<b>UNIT</b>
<b>Source-Drain Diode</b> (Note 5)						
Diode Forward Voltage	$I_S = 2\text{A}, V_{GS} = 0\text{V}$	$V_{SD}$	--	0.9	1.4	V
Reverse Recovery Time	$V_{GS} = 0\text{V}, I_S = 2\text{A},$ $dI_F/dt = 100\text{A}/\mu\text{s}$	$t_{rr}$	--	490	--	ns
Reverse Recovery Charge		$Q_{rr}$	--	0.8	--	$\mu\text{C}$
Source Current	Integral reverse diode in the MOSFET	$I_S$	--	--	2	A
Source Current (Pulse)		$I_{SM}$	--	--	8	A

**Notes:**

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3.  $L = 25\text{mH}, I_{AS} = 2\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$ .  
100% Eas Test Condition:  $L = 25\text{mH}, I_{AS} = 1\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
4.  $I_{SD} \leq 2\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$ .
5. Pulse test:  $PW \leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
6. For DESIGN AID ONLY, not subject to production testing.
7. Switching time is essentially independent of operating temperature.

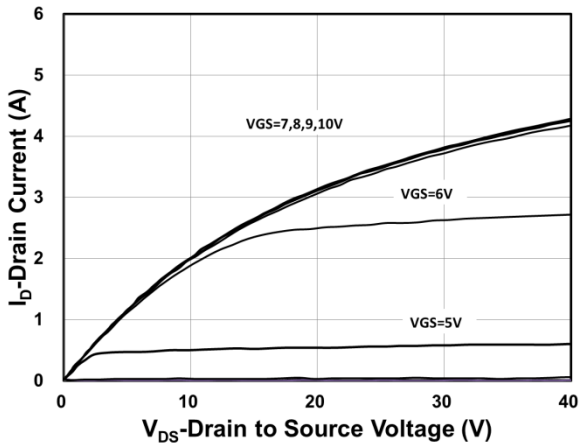
**ORDERING INFORMATION**

<b>PART NO.</b>	<b>PACKAGE</b>	<b>PACKING</b>
TSM2NB60CH C5G	TO-251 (IPAK)	75pcs / Tube
TSM2NB60CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

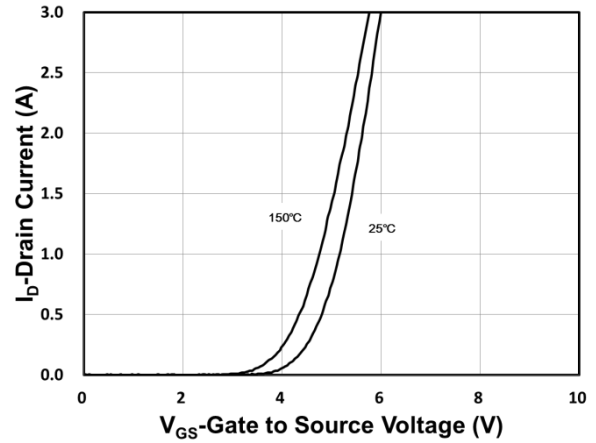
**CHARACTERISTICS CURVES**

( $T_C = 25^\circ\text{C}$  unless otherwise noted)

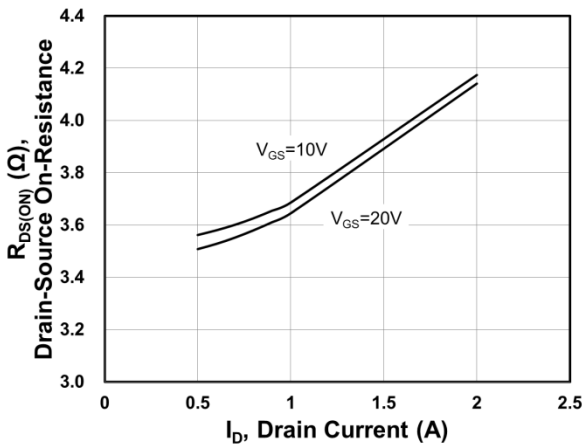
**Output Characteristics**



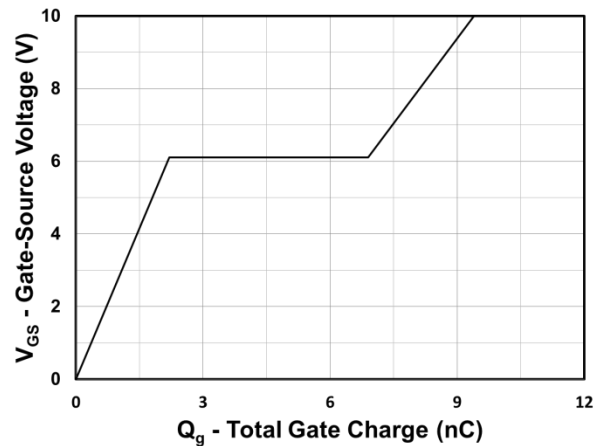
**Transfer Characteristics**



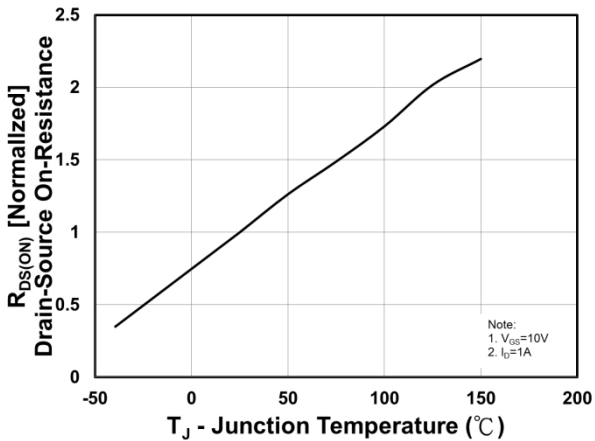
**On-Resistance vs. Drain Current**



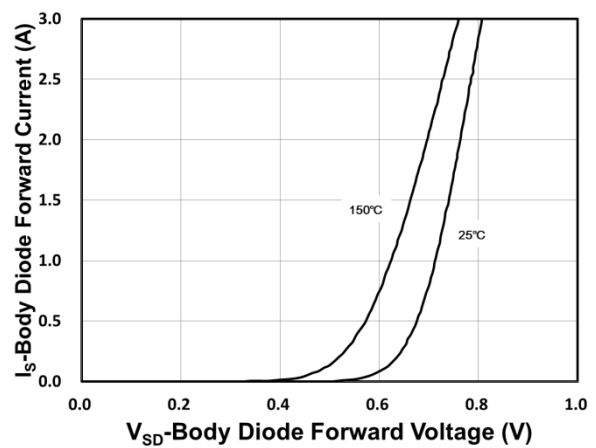
**Gate-Source Voltage vs. Gate Charge**



**On-Resistance vs. Junction Temperature**



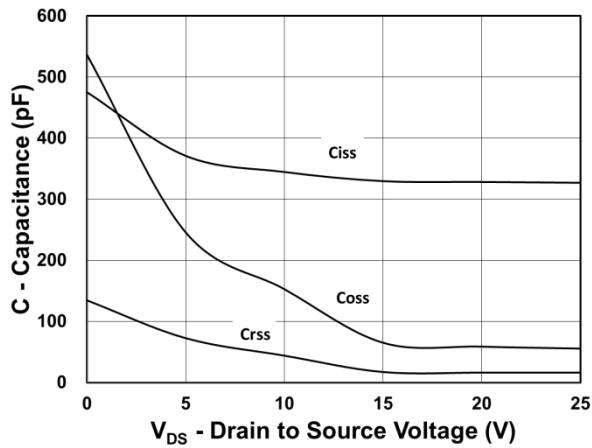
**Source-Drain Diode Forward Current vs. Voltage**



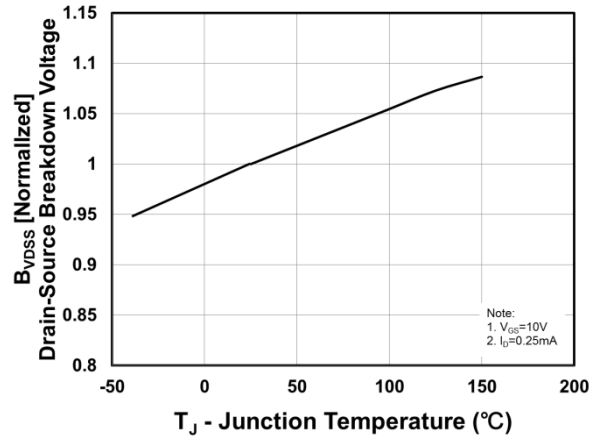
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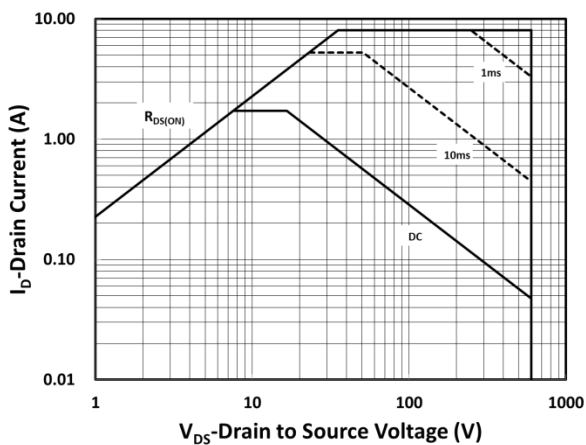
**Capacitance vs. Drain-Source Voltage**



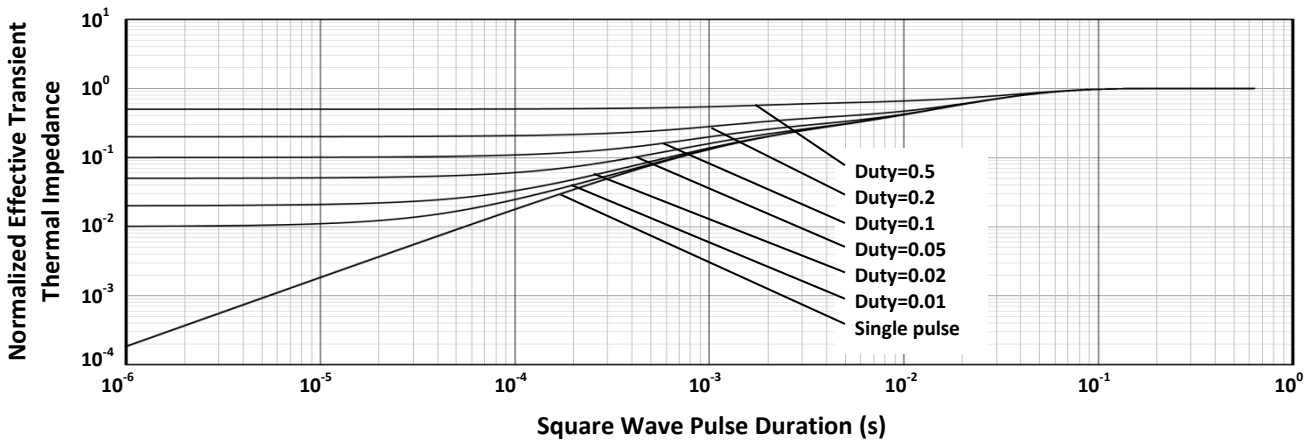
**$BV_{DSS}$  vs. Junction Temperature**



**Maximum Safe Operating Area**

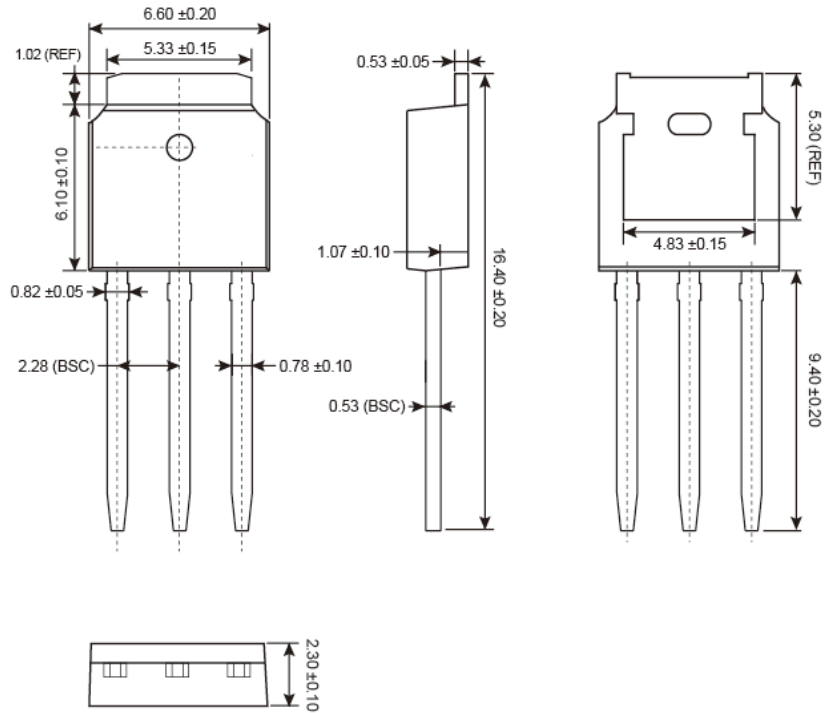


**Normalized Thermal Transient Impedance, Junction-to-Case**

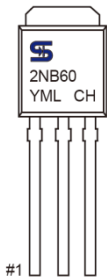


**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)

**TO-251(IPAK)**



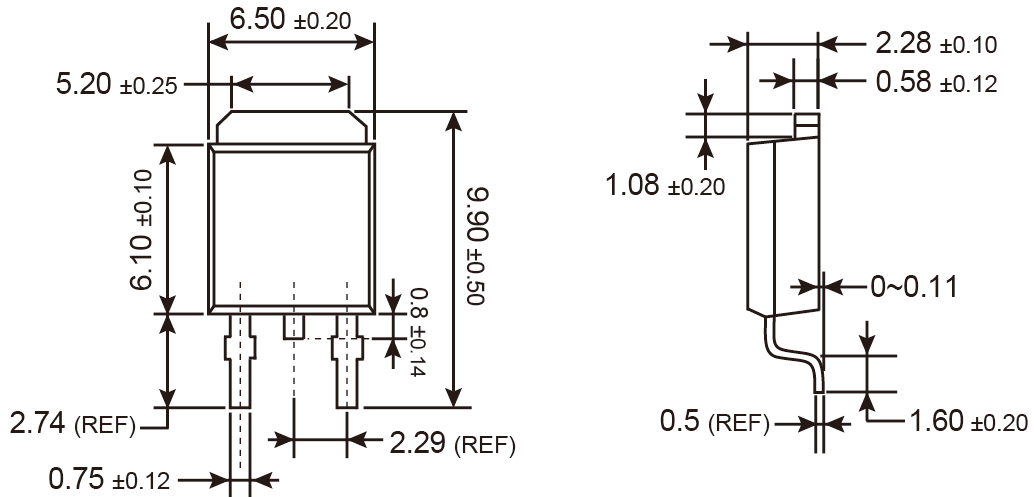
**MARKING DIAGRAM**



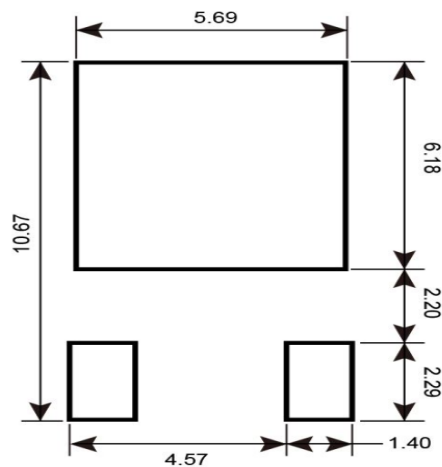
- Y** = Year Code
- M** = Month Code for Halogen Free Product
  - O** =Jan    **P** =Feb    **Q** =Mar    **R** =Apr
  - S** =May    **T** =Jun    **U** =Jul    **V** =Aug
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- L** = Lot Code (1~9, A~Z)

**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)

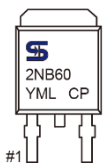
**TO-252(DPAK)**



**SUGGESTED PAD LAYOUT** (Unit: Millimeters)



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