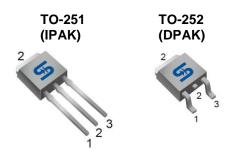


Pb-Free ROHS COMPLIANT

TSM2N60E

 $600V,\,2A,\,4\Omega$ N-Channel Power MOSFET



Pin Definition: 1. Gate 2. Drain 3. Source

Key Parameter Performance

Parameter	Value	Unit
V _{DS}	600	V
R _{DS(on)} (max)	4	Ω
Qg (typ)	9.5	nC
		•

Features

- 100% Avalanche Tested
- G-S ESD Protection Diode Embedded

Ordering Information

Ordering code	Package	Packing		
TSM2N60ECH C5G	TO-251	75pcs / Tube		
TSM2N60ECP ROG	TO-252	2.5kpcs / 13" Reel		

Note: Halogen-free according to IEC 61249-2-21 definition

Block Diagram

N-Channel MOSFET with ESD Protection

Absolute Maximum Ratings (T_c = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	600	V	
Gate-Source Voltage		V _{GS}	±30	V	
Continuous Drain Current (Note 1) $Tc = 25^{\circ}C$ $Tc = 100^{\circ}C$	Note 1) Tc = 25°C	- I _D	2	А	
	Tc = 100°C		1.43	А	
Pulsed Drain Current (Note 2)		I _{DM}	8	А	
Repetitive Avalanche Curre	ent ^(Note 1)	I _{AR}	2	А	
Repetitive Avalanche Ener	gy ^(Note 1)	E _{AR}	5.2	А	
Single Pulse Avalanche Er	nergy ^(Note 3)	E _{AS}	66	mJ	
Total Dower Discipation	T _C = 25°C	P	±30 2 1.43 8 2 5.2	W	
Total Power Dissipation	Derate above T _C = 25°C		W/°C		
Peak Diode Recovery dV/c	It (Note 4)	dV/dt	4.5	V/ns	
Operating Junction Tempe	rature	TJ	-55 to +150	°C	
Storage Temperature Rang	je	T _{STG}	-55 to +150	°C	

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	R _{eJC}	2.4	°C/W
Thermal Resistance - Junction to Ambient	R _{eja}	110	°C/W





TSM2N60E 600V, 2A, 4Ω

N-Channel Power MOSFET

Electrical Specifications ($T_c = 25^{\circ}C$ unless otherwise noted)

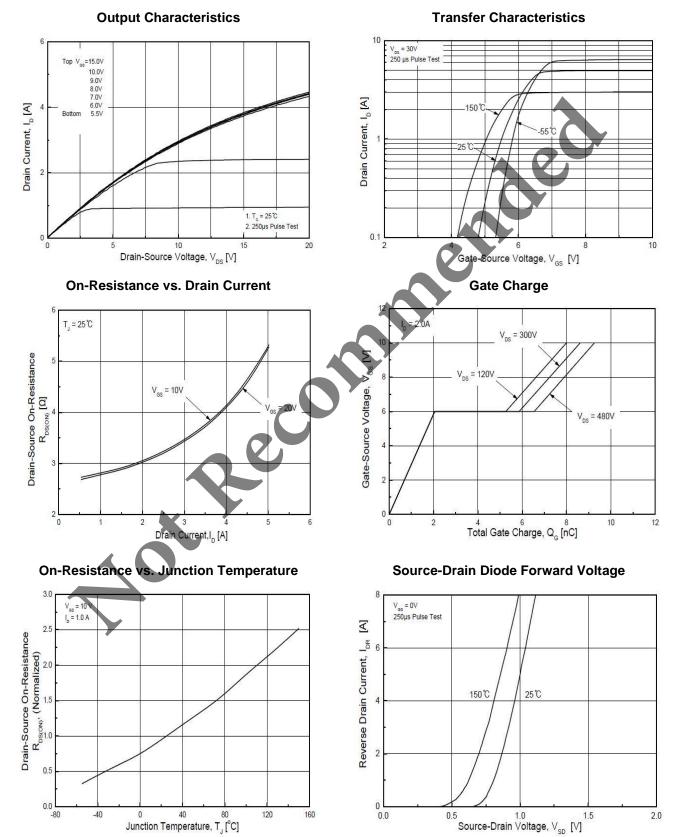
Parameter	Conditions	Symbol	Min	Тур	Max	Unit
Static (Note 5)		L	1	1		
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250 \mu A$	BV _{DSS}	600			V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 1A$	R _{DS(ON)}		3.2	4	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	V _{GS(TH)}	3		5	V
	$V_{DS} = 600V, V_{GS} = 0V$	I _{DSS}			1	μA
Zero Gate Voltage Drain Current	V _{DS} = 480V, T _J = 125°C				10	
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I _{GSS}		7 -7	±100	μA
Forward Transconductance	$V_{DS} = 30V, I_{D} = 1A$	g _{fs}		3		S
Dynamic (Note 6)				7		
Total Gate Charge		Q _g		9.5		
Gate-Source Charge	$V_{DS} = 480V, I_D = 2A,$	Q _{gs}	Y	2.1		nC
Gate-Drain Charge	– V _{GS} = 10V	Q _{gd}		3.9		
Input Capacitance		C _{iss}		362		pF
Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$	C _{oss}		40		
Reverse Transfer Capacitance	- f = 1MHz	C _{rss}		7.2		
Switching (Note 7)		L	•	•		1
Turn-On Delay Time		t _{d(on)}		21		
Turn-On Rise Time	$V_{DD} = 300V, V_{GS} = 10V,$	t _r		22		
Turn-Off Delay Time	$R_{\rm G} = 25\Omega, I_{\rm D} = 2A$	t _{d(off)}		41		ns
Turn-Off Fall Time		t _f		21		1
Source-Drain Diode Ratings and	Characteristic (Note 5)	I	ı.			
Maximum Continuous Drain-Source		ls			2	Α
Maximum Pulse Drain-Source Diod	e Forward Current	I _{SM}			8	Α
Diode-Source Forward Voltage	$V_{GS} = 0V, I_S = 2A$	V _{SD}			1.5	V
Reverse Recovery Time	$V_{GS} = 0V, I_{S} = 2A$	t _{rr}		238		ns
Reverse Recovery Charge	dl _F /dt = 100A/µs	Q _{rr}		0.8		nC

Notes:

- 1. Current limited by package
- 2. Pulse width limited by the maximum junction temperature
- 3. $V_{DD} = 50V$, L= 30.5mH, $I_{AS} = 2A$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}C$
- 4. $I_{SD} \le 2A$, di/dt $\le 200A/\mu s$, $V_{DD} \le BV_{DS}$, Starting $T_J = 25^{\circ}C$
- 5. Pulse test: PW \leq 300µs, duty cycle \leq 2%
- 6. For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature. 7.



TSM2N60E 600V, 2A, 4Ω N-Channel Power MOSFET

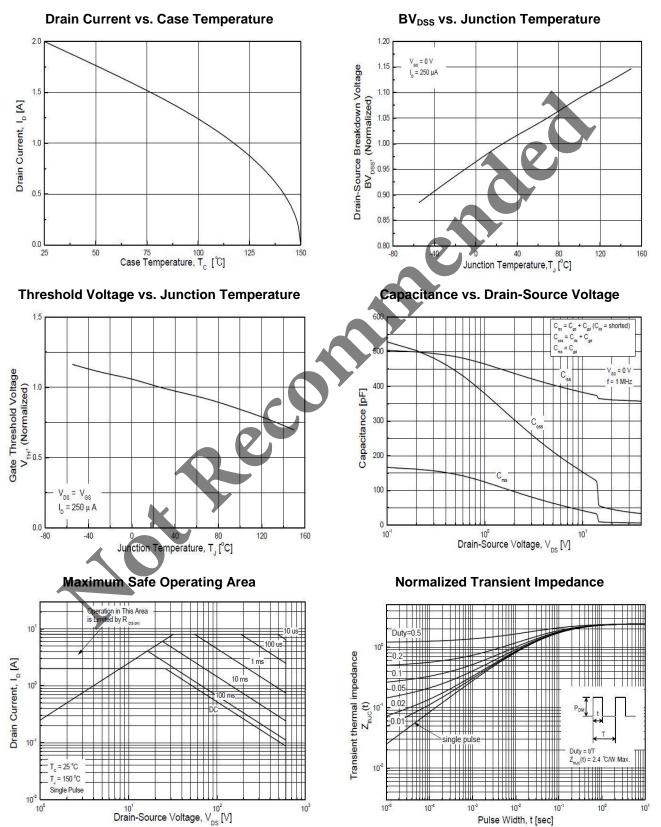


Electrical Characteristics Curves (T_C = 25°C, unless otherwise noted)



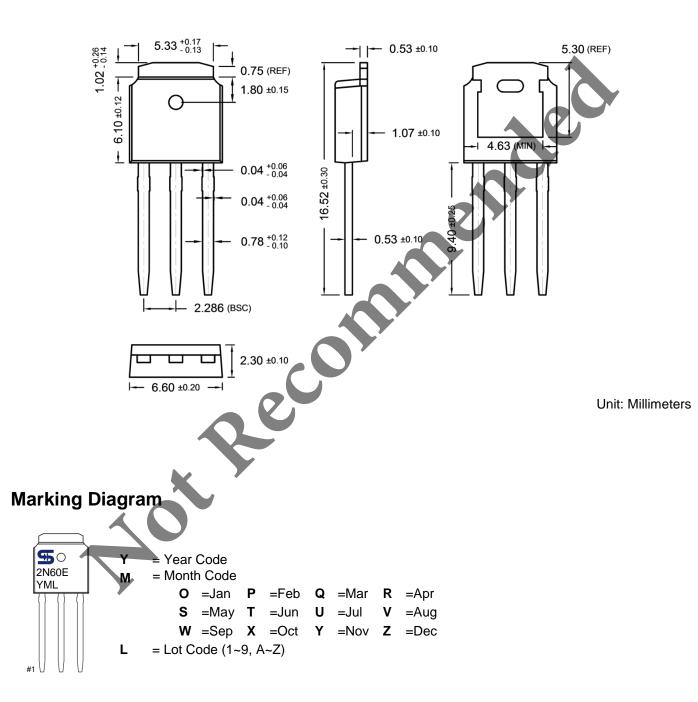
TSM2N60E 600V, 2A, 4Ω N-Channel Power MOSFET

Electrical Characteristics Curve ($T_c = 25^{\circ}C$, unless otherwise noted)





TSM2N60E 600V, 2A, 4Ω N-Channel Power MOSFET



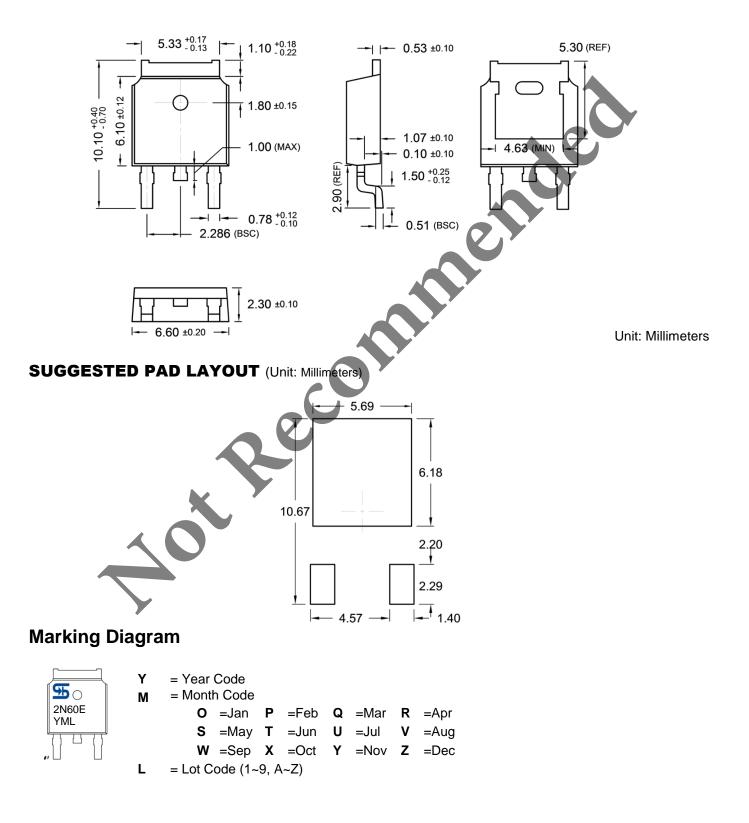
TO-251 Mechanical Drawing



COMPLIAN

TSM2N60E 600V, 2A, 4Ω N-Channel Power MOSFET

TO-252 Mechanical Drawing









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