Bi-directional TVS Diode Array

FEATURES

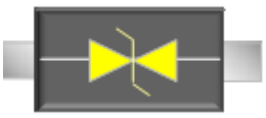
- Meet IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- Meet IEC61000-4-4 (EFT) rating. 40A (5/50ns)
- Protects one Bi-directional I/O line
- Moisture sensitivity level: level 1, per J-STD-020
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC

KEY PARAMETERS		
PARAMETER	**VALUE**	**UNIT**
P_{PPM}	500	W
I_{PP}	5	A
V_{RWM}	24	V
V_C at I_{PP}= 5 A	40	V
Package	SOD-323	

APPLICATIONS

- Cell Phone Handsets and Accessories
- Notebooks, Desktops, and Servers
- Keypads, Side Keys
- Portable Instrumentation
- Microprocessor Based Equipment
- Peripherals

Pb-Free RoHS COMPLIANT



MECHANICAL DATA

- Case: SOD-323
- Molding compound meets UL 94 V-0 flammability rating
- Terminal: Matte tin plated leads, solderable per J-STD-002
- Meet JESD 201 class 1A whisker test
- Weight: 4.85 mg (approximately)
- Marking code on the device: 2H

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)			
PARAMETER	**SYMBOL**	**TESDC24V**	**UNIT**
Rated random recurring peak Impulse power dissipation (tp=8/20μs waveform)	P_{PPM}	500	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	± 15 ± 8	KV
Junction temperature range	T_J	-55 to +150	°C
Storage temperature range	T_{STG}	-55 to +150	°C

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Reverse breakdown voltage (1)	I_R = 1 mA	$V_{(BR)}$	26.7	-	-	V
Rated working standoff voltage		V_{WM}	-	-	24	V
Reverse current (1)	V_R= 24 V	I_R	-	-	1	μA
Clamping voltage (2)	I_{PP} = 5 A	V_C	-	-	40	V
Clamping voltage (2)	I_{PP} = 17 A	V_C	-	-	52	V
Junction capacitance	1 MHz, V_R=0V	C_J	-	50	-	pF

Notes:

1. Pulse test with PW=30 ms
2. tp=8/20μs waveform

ORDERING INFORMATION		
ORDERING CODE	**PACKAGE**	**PACKING**
TESDC24V RR	SOD-323	3K / 7" Reel
TESDC24V RRG	SOD-323	3K / 7" Reel

Note: “G” means green compound (halogen)

CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig. 1 Non-Repetitive Peak Pulse Power vs. Pulse Time

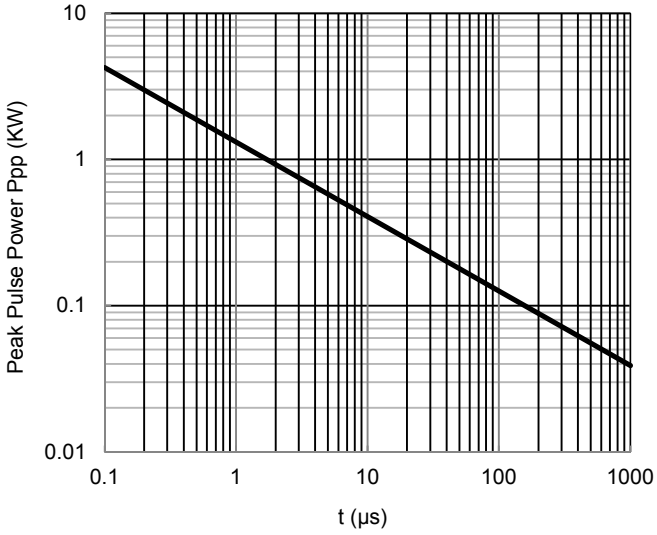


Fig. 2 8/20μs pulse waveform according to IEC 61000-4-5

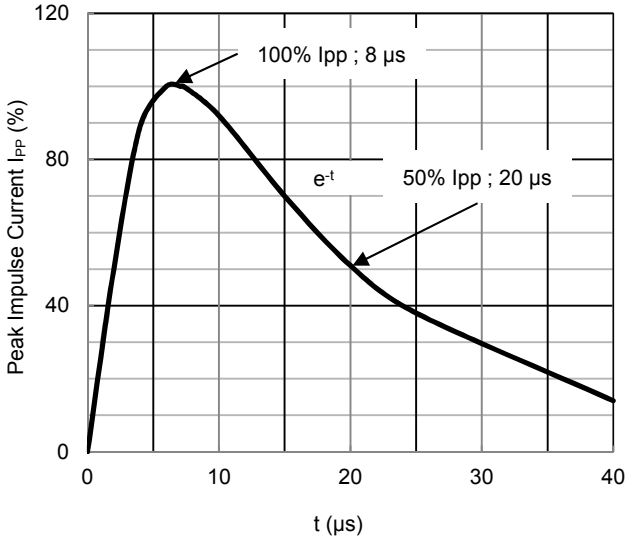


Fig. 3 Admissible Power Dissipation Curve

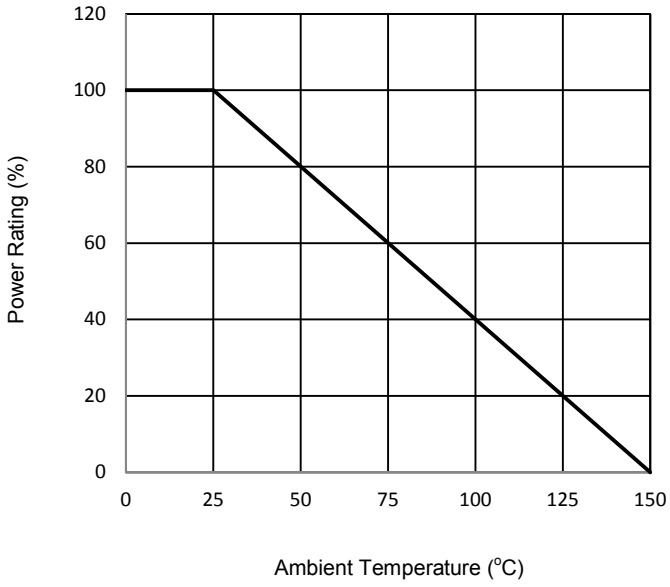
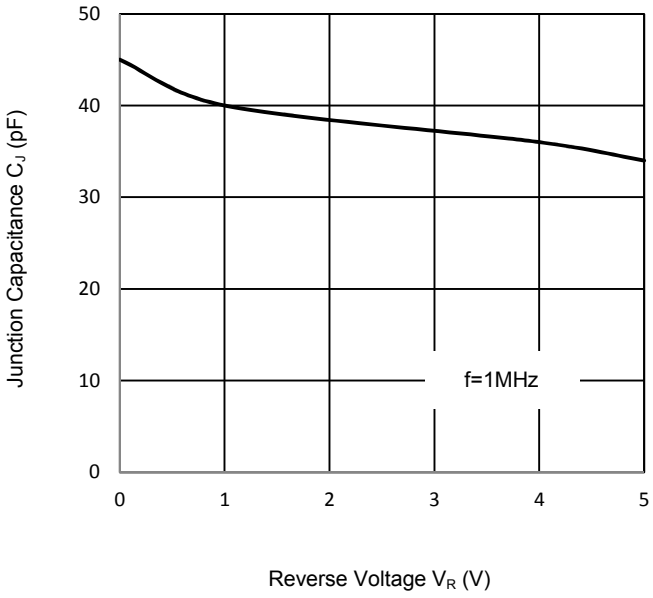


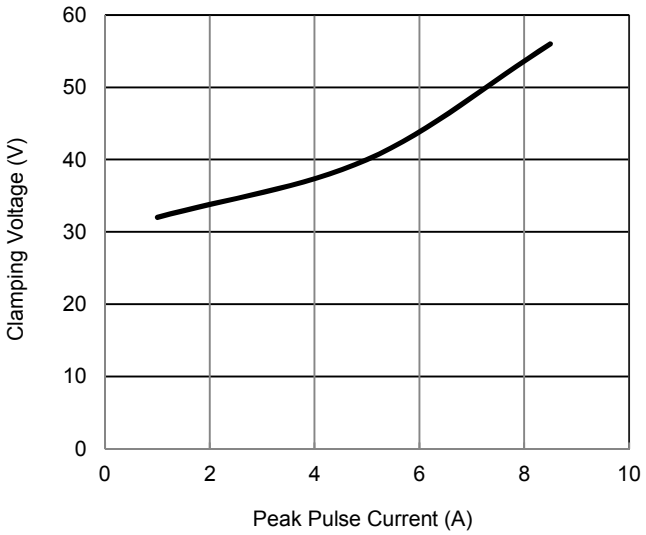
Fig. 4 Typical Junction Capacitance



CHARACTERISTICS CURVES

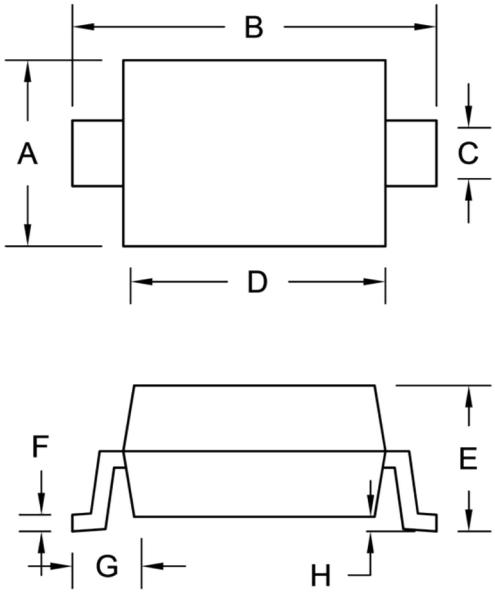
(T_A = 25°C unless otherwise noted)

Fig. 5 Clamping Voltage vs. Peak Pulse Current



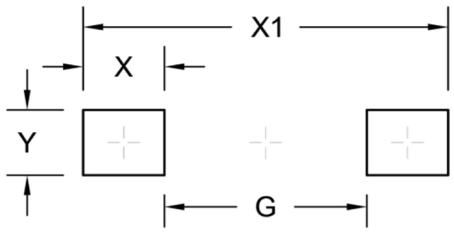
PACKAGE OUTLINE DIMENSION

SOD-323



DIM.	Unit (mm)		Unit (inch)	
	Min.	Max.	Min.	Max.
A	1.150	1.400	0.045	0.055
B	2.300	2.700	0.091	0.106
C	0.250	0.450	0.010	0.018
D	1.600	1.800	0.063	0.071
E	0.800	1.000	0.031	0.039
F	0.050	0.177	0.002	0.007
G	0.475 (Ref.)		0.019 (Ref.)	
H	-	0.100	-	0.004

SUGGEST PAD LAYOUT



Symbol	Unit (mm)	Unit (inch)
G	1.52	0.060
X	0.61	0.024
X1	2.74	0.108
Y	0.49	0.019

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.

APPLICATION INFROMATION

- Designed to protect one data, I/O, or power supply line
- Designed to protect sensitive electronics from damage or latch-up due to ESD
- Designed to replace multilayer varistors (MLVs) in portable applications
- Offers superior electrical characteristics such as lower clamping voltage and no device degradation when compared to MLVs
- The combination of small size and high ESD surge capability makes them ideal for use in portable applications

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

- Good circuit board layout is critical for the suppression of ESD induced transients
- Place the ESD Protection Diode near the input terminals or connectors to restrict transient coupling
- Minimize the path length between the ESD Protection Diode and the protected line
- Minimize all conductive loops including power and ground loops
- The ESD transient return path to ground should be kept as short as possible
- Never run critical signals near board edges
- Use ground planes whenever possible

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