Small Signal Product

Low Capacitance ESD Protection Array

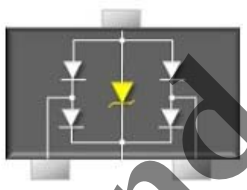
FEATURES

- Meet IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- Meet IEC61000-4-4 (EFT) rating. 40A (5/50ns)
- Meet IEC61000-4-5 (Lightning) rating. 12A (8/20μs)
- Protects two directional I/O lines
- Working voltage: 5V
- Low leakage current
- Pb free version and RoHS compliant
- Packing code with suffix "G" means green compound (halogen-free)

Pb-Free

SOT-23

RoHS COMPLIANT



MECHANICAL DATA

- Case: SOT-23 small outline plastic package
- Terminal: Matte tin plated, lead free., solderable per MIL-STD-202, Method 208 guaranteed
- High temperature soldering guaranteed : 260°C/10s
- Weight: 8 ± 0.5 mg
- Marking code : Y D05

APPLICATIONS

- USB Power & Data Line Protection
- Ethernet 10BaseT
- T1/E1 Secondary IC Side Protection
- ISDN S/T Interface
- WAN/LAN Equipment

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)			
PARAMETER	SYMBOL	VALUE	UNIT
Peak Pulse Power (tp=8/20μs waveform)	P_{PP}	350	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	± 15 ± 8	KV
Junction and Storage Temperature Range	T_J , T_{STG}	-55 to +150	°C

PARAMETER		SYMBOL	MIN	MAX	UNIT
Reverse Stand-Off Voltage		V_{RWM}	-	5	V
Reverse Breakdown Voltage	I_R = 1 mA	$V_{(BR)}$	6	-	V
Reverse Leakage Current	V_R = 5 V	I_R	-	1	μA
Clamping Voltage	I_{PP} = 1 A	V_C	-	9.8	V
	I_{PP} = 5 A		-	12	
Junction Capacitance	V_R = 0 V , f = 1.0 MHz	C_J	1		pF

RATINGS AND CHARACTERISTICS CURVES

(T_A=25°C unless otherwise noted)

Fig. 1 Admissible Power Dissipation Curve

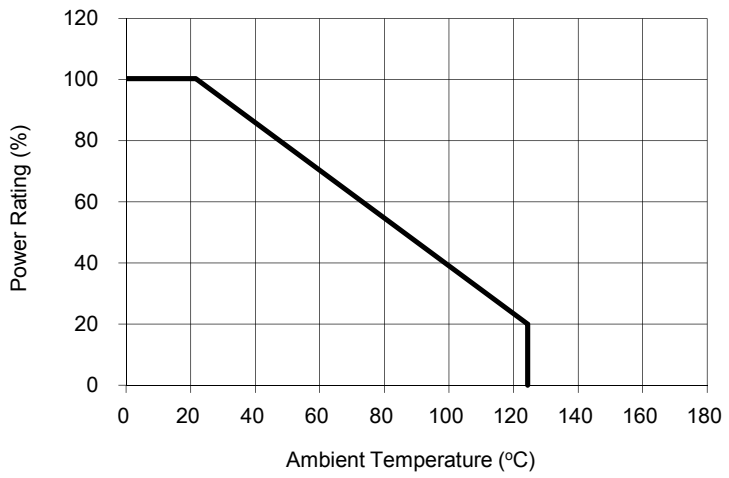


Fig. 2 Pulse Waveform

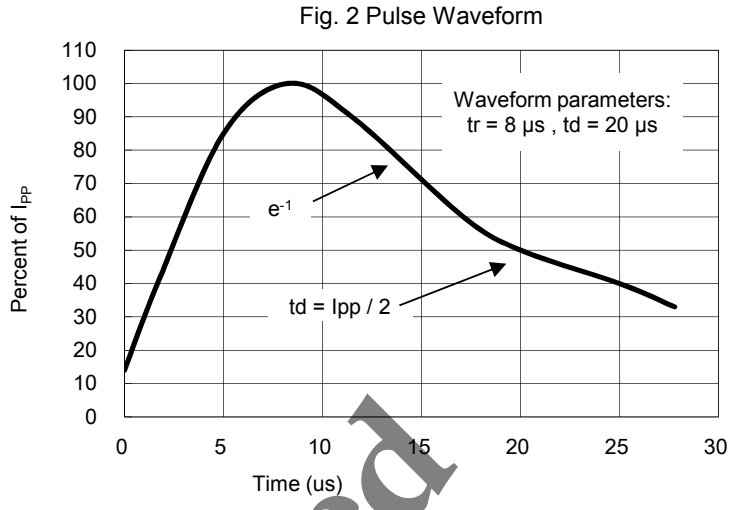


Fig. 3 Clamping Voltage VS. Peak Pulse Current

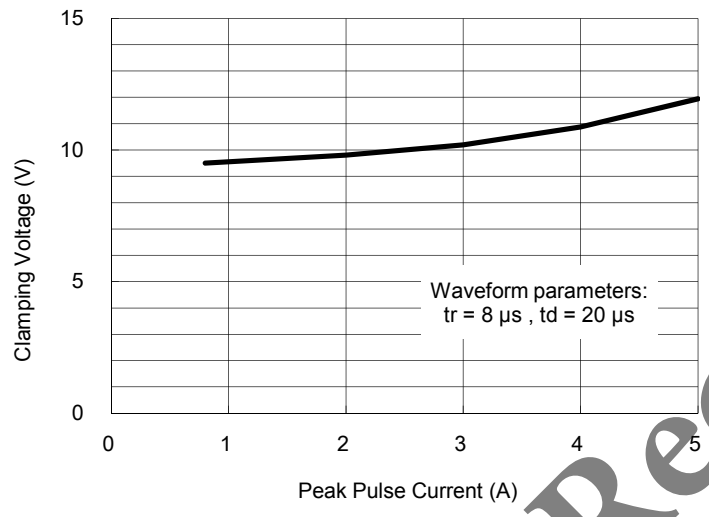
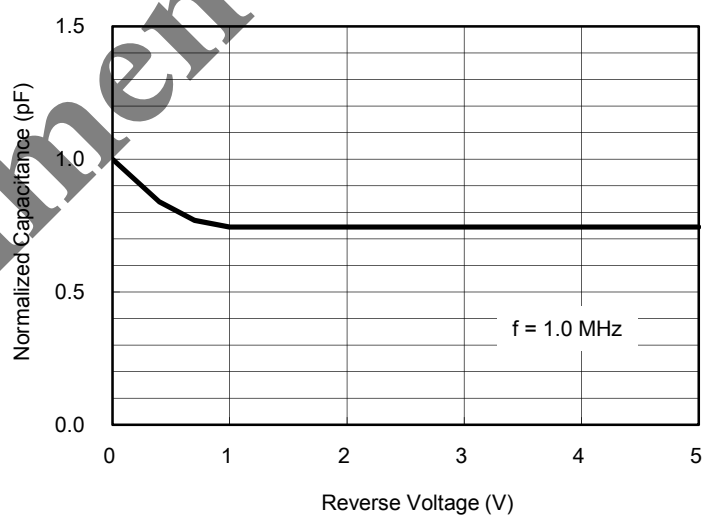


Fig. 4 Typical Junction Capacitance



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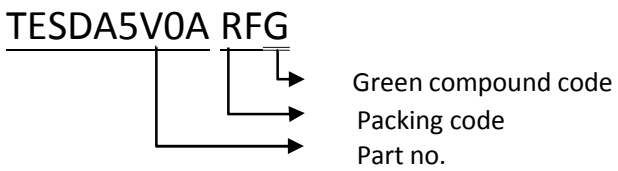
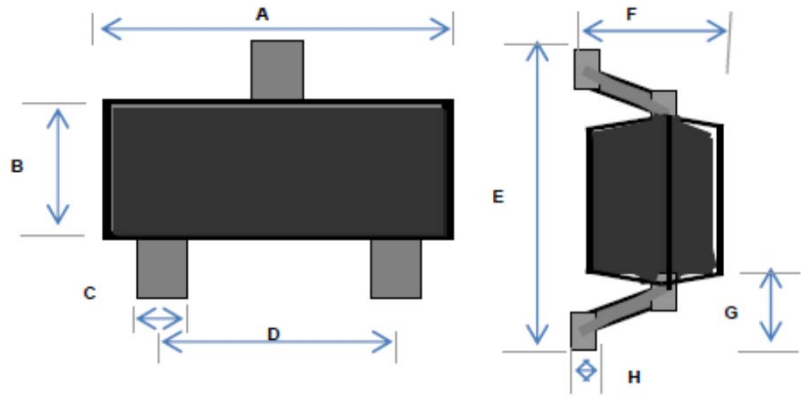
ORDER INFORMATION (EXAMPLE)



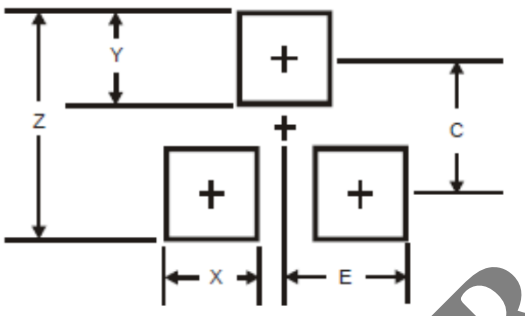
PACKAGE OUTLINE DIMENSIONS

SOT-23



DIM.	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	2.70	3.10	0.106	0.122
B	1.10	1.50	0.043	0.059
C	0.30	0.51	0.012	0.020
D	1.78	2.04	0.070	0.080
E	2.10	2.64	0.083	0.104
F	0.89	1.30	0.035	0.051
G	0.55 REF		0.022 REF	
H	0.10 REF		0.004 REF	

SUGGEST PAD LAYOUT



DIM.	Unit (mm)	Unit (inch)
	Typ.	Typ.
Z	2.8	0.110
X	0.7	0.028
Y	0.9	0.035
C	1.9	0.075
E	1.0	0.039

Note: 1. The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.

APPLICATIONS INFORMATION

◇ Designed for the bi-directional protection of 2 lines form the damage caused by Electro Static Discharge (ESD) and surge pulses

◇ Be used on lines where the signal polarities are above and below ground

◇ Provides a surge capability of 350 Watts peak Ppp per line for an 8/20 ms waveform

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

◇ Place the ESD Protection array as close to the input terminal or connector as possible

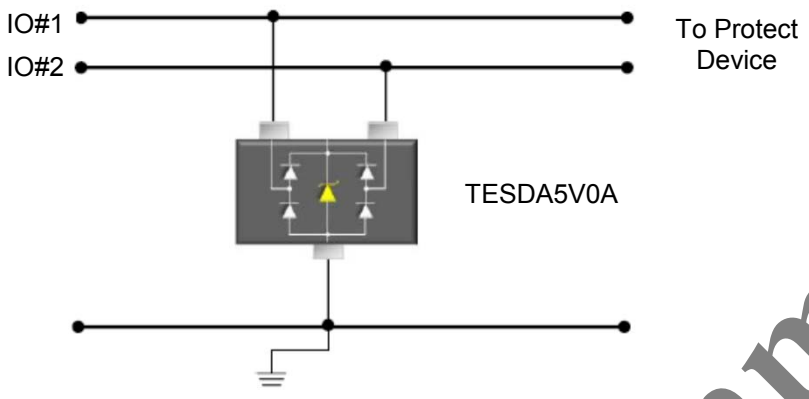
◇ Keep parallel signal paths to a minimum

◇ Minimize all printed-circuit board conductive loops including power and group loops

◇ Advoid using shared transient return paths to a common ground point

◇ Ground planes should be used. For multilayer printed-circuit boards, use ground vias

◇ Below picture is the typical application for bi-directional protection of two lines



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