

High Voltage EL Lamp Driver IC

Features

- ▶ 1.8 to 3.5V operating supply voltage
- ▶ DC to AC conversion
- ▶ Output voltage regulation
- ▶ Adjustable output lamp frequency
- ▶ Adjustable converter frequency
- ▶ Enable/disable function

Applications

- ▶ Pagers
- ▶ Portable Transceiver
- ▶ Cellular phones
- ▶ Remote control units
- ▶ Calculators

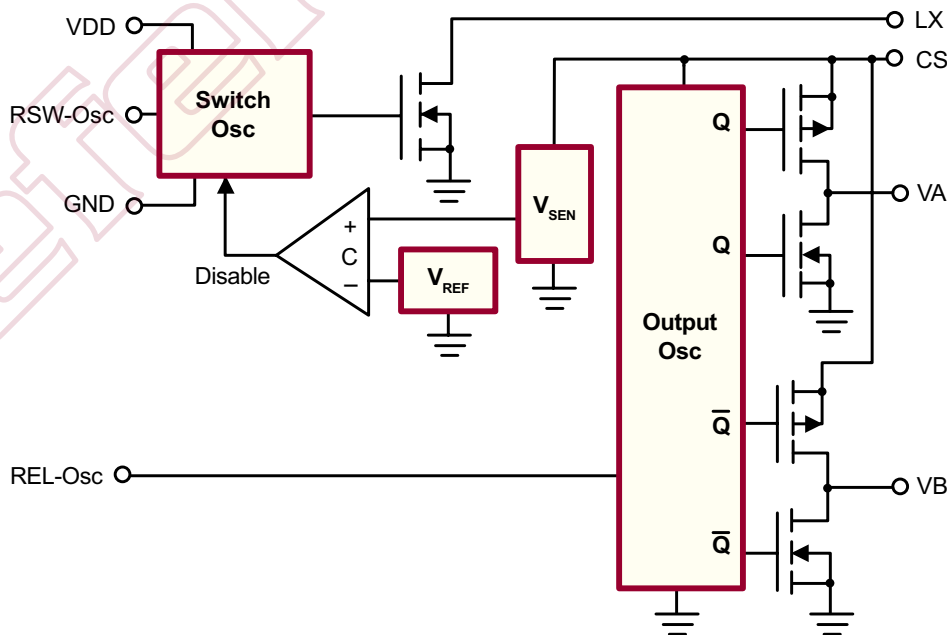
General Description

The Supertex HV826 is a high voltage driver designed for driving EL lamps. The input supply voltage range is from 1.8V to 3.5V. The device uses a single inductor and a minimum number of passive components. The nominal regulated output voltage that is applied to the EL lamp is $\pm 80V$. The chip can be enabled/disabled by connecting the resistor on the RSW-Osc pin to VDD/GND.

The HV826 has two internal oscillators, a switching MOSFET, and a high voltage EL lamp driver. The frequency for the switching MOSFET is set by an external resistor connected between the RSW-Osc pin and the VDD supply pin. The EL lamp driver frequency is set by an external resistor connected between REL-Osc pin and the VDD pin. An external inductor is connected between the LX pin and VDD pin. A $0.01-0.1\mu F$ capacitor is connected between the CS pin and GND. The EL lamp is connected between the VA pin and the VB pin.

The switching MOSFET charges the external inductor and discharges it into the capacitor at the CS pin. The voltage at CS will start to increase. Once the voltage at CS reaches a nominal value of 80V, the switching MOSFET is turned OFF to conserve power. The output pins VA and VB are configured as an H bridge and are switching in opposite states to achieve 160V peak-to-peak across the EL lamp.

HV826 Block Diagram



Ordering Information

Device	Package Options	
	8-Lead SOIC 4.90x3.90mm body 1.75mm height (max) 1.27mm pitch	8-Lead MSOP 3.00x3.00mm body 1.10mm height (max) 0.65mm pitch
HV826	HV826LG-G	HV826MG-G

-G indicates package is RoHS compliant ("Green")



Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{DD}	-0.5V to +4.5V
Output voltage, V_{CS}	-0.5V to +100V
Operating temperature range	-25°C to +85°C
Storage temperature range	-65°C to +150°C
8-Lead SOIC power dissipation	400mW
8-Lead MSOP power dissipation	300mW

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device GND.

Electrical Characteristics

DC Characteristics (Over recommended operating conditions unless otherwise specified - $T_A = 25^\circ\text{C}$)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$R_{DS(ON)}$	On-resistance of switching transistor	-	-	6.0	Ω	$I = 100\text{mA}$
I_{IN}	V_{DD} supply current (including inductor current)	-	35	45	mA	$V_{IN} = 1.5\text{V}$. See Fig.1
I_{DDQ}	Quiescent V_{DD} supply current	-	-	100	nA	RSW-Osc = low
V_{CS}	Output voltage on CS	75	80	85	V	$V_{DD} = 1.8 - 3.5\text{V}$
V_{A-B}	Differential output voltage across lamp	150	160	170	V	$V_{DD} = 1.8 - 3.5\text{V}$
f_{EL}	V_{A-B} output drive frequency	300	375	450	Hz	$V_{IN} = 1.5\text{V}$. See Fig.1
f_{SW}	Switching transistor frequency	-	80	-	kHz	$V_{IN} = 1.5\text{V}$. See Fig.1
D	Switching transistor duty cycle	-	88	-	%	See Fig.1

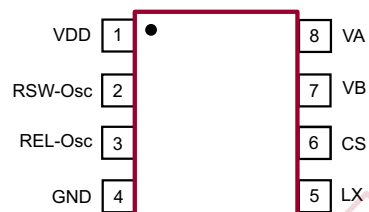
Recommended Operating Conditions

V_{DD}	Supply voltage	1.8	-	3.5	V	---
f_{EL}	V_{A-B} output drive frequency	60	-	1000	Hz	---
T_A	Operating temperature	-25	-	+85	$^\circ\text{C}$	---

Enable/Disable Function Table

EN-L	Logic input low voltage	0	-	0.5	V	$V_{DD} = 1.8 - 3.5\text{V}$
EN-H	Logic input high voltage	$V_{DD}-0.5$	-	V_{DD}	V	$V_{DD} = 1.8 - 3.5\text{V}$

Pin Configuration



8-Lead SOIC (LG) / 8-Lead MSOP (MG)
(top view)

Product Marking



Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC (LG)

Top Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

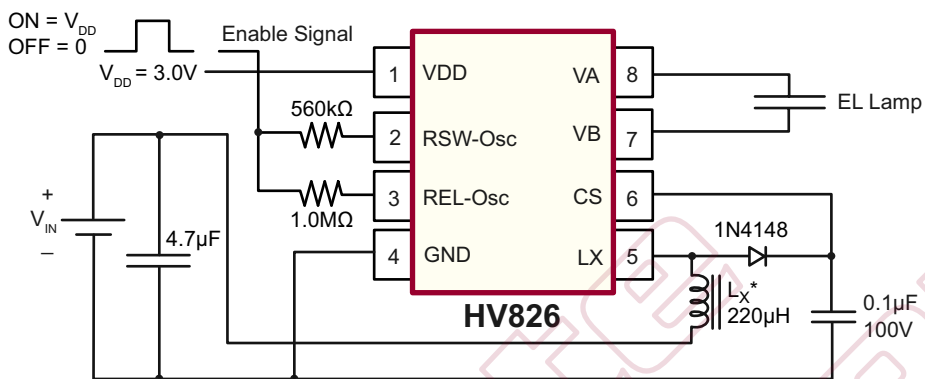
Bottom Marking



Package may or may not include the following marks: Si or

8-Lead MSOP (MG)

Fig.1: Typical Application



Typical Performance

Lamp Size	V _{IN}	I _{IN}	V _{CS}	f _{EL}	Brightness
1.6in ²	1.5V	35mA	66V	345Hz	5.00ft-Im

Notes:

* Murata part # LQH4N221K04 (DC resistance < 14.5Ω)

Typical Performance Curves for Fig.1 (1.6in² Lamp)

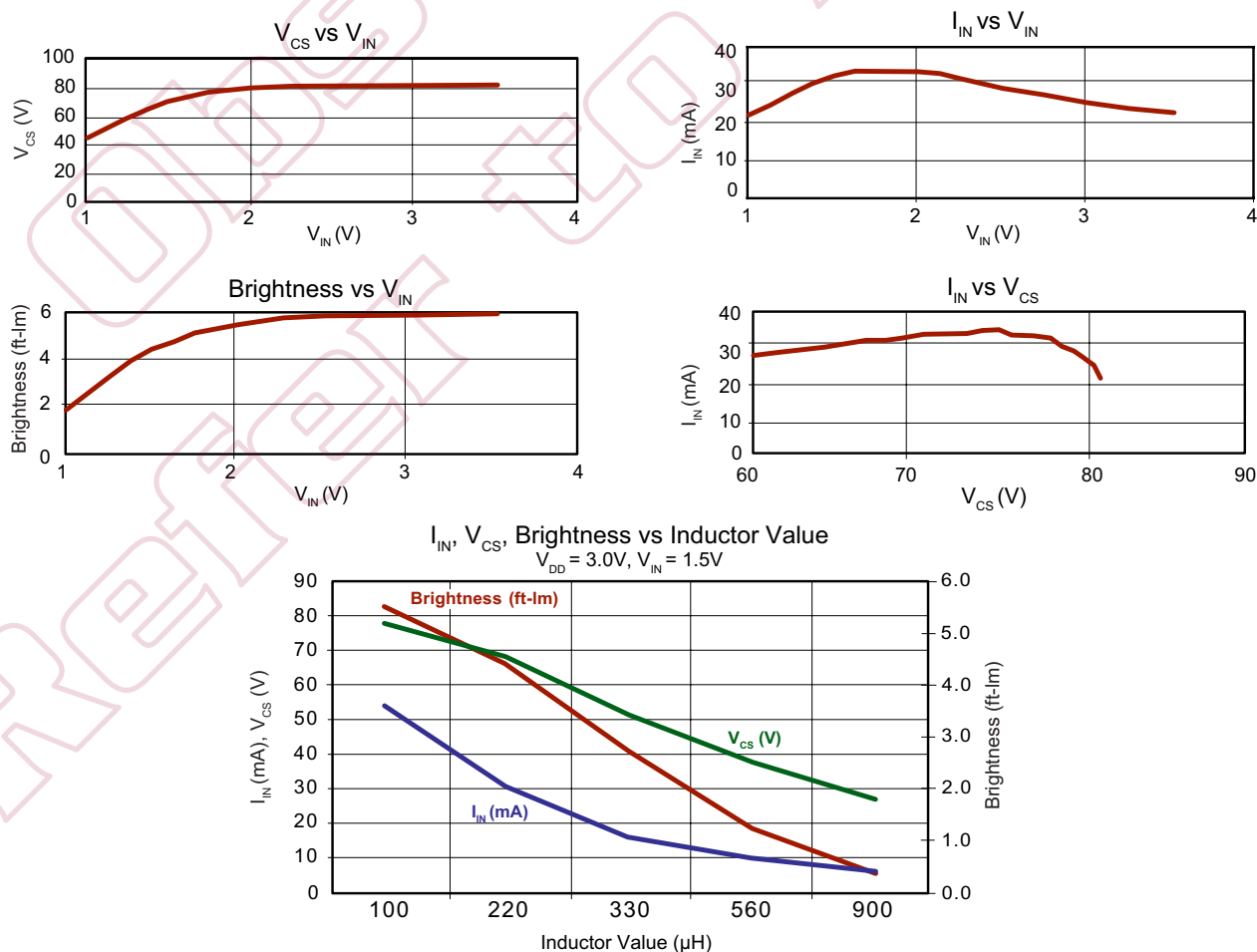
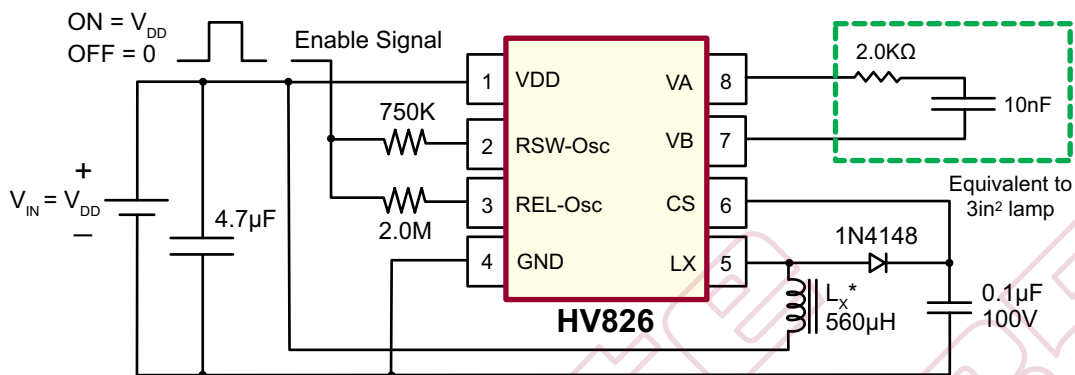


Fig.2: Typical Application ($V_{IN} = 3.0V = V_{DD}$)



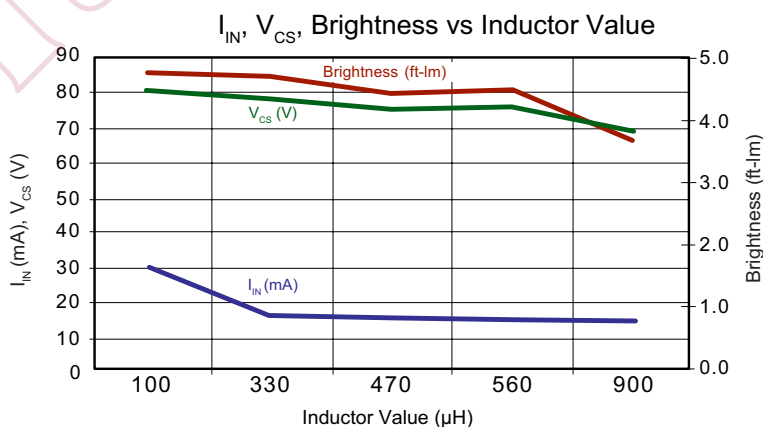
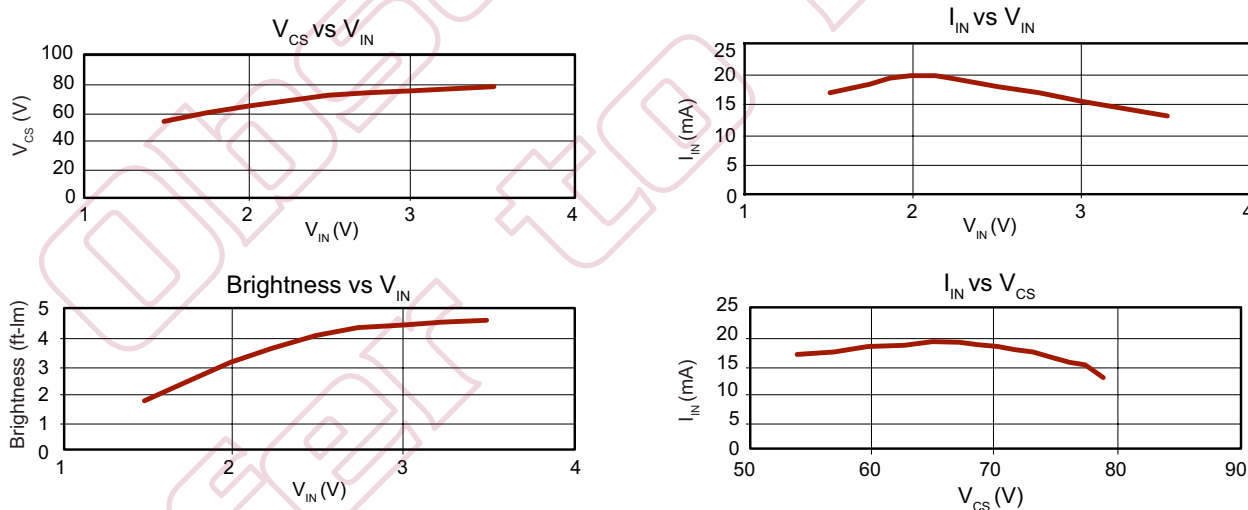
Typical Performance

Lamp Size	V_{IN}	I_{DD}	V_{CS}	f_{EL}	Brightness
3.0in ²	3.0V	23mA	80V	195Hz	4.0ft-lm

Notes:

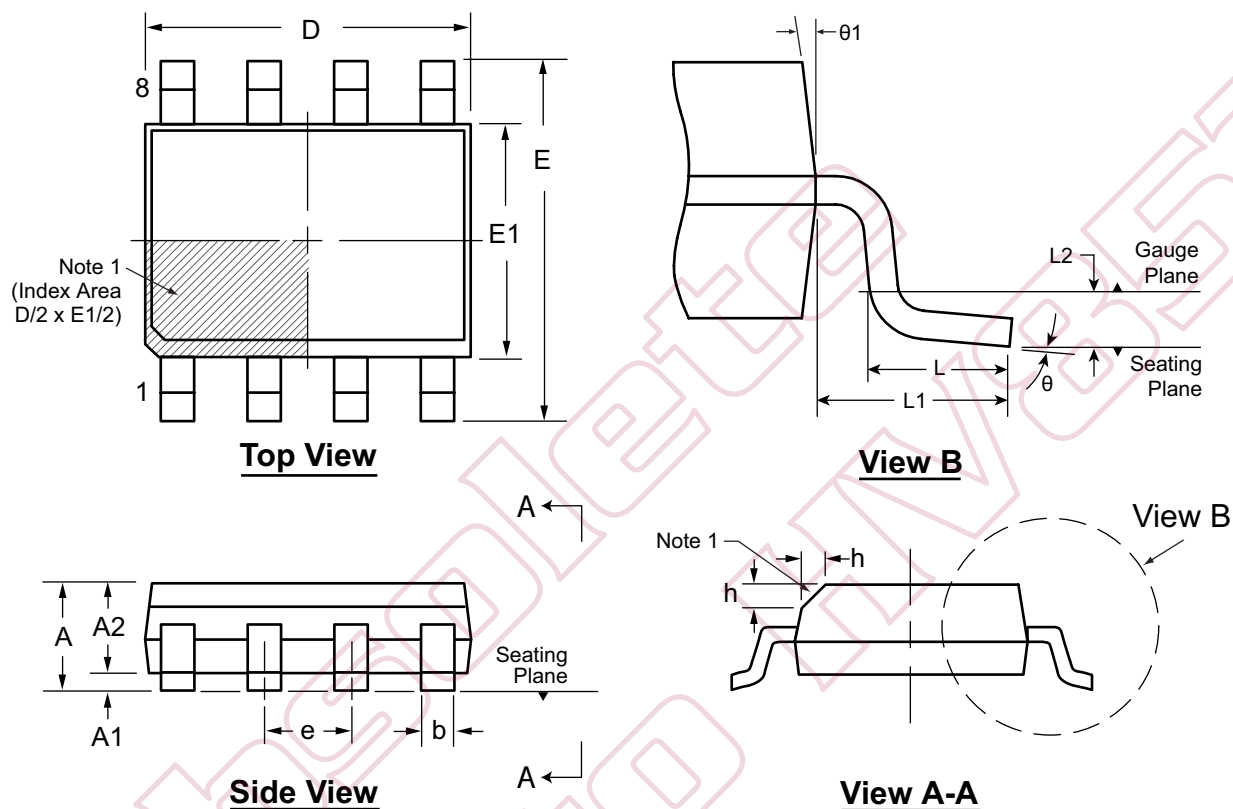
* Murata part # LQH4N561K04

Typical Performance Curves for Fig.2 (3.0in² Lamp)



8-Lead SOIC (Narrow Body) Package Outline (LG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:
 1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

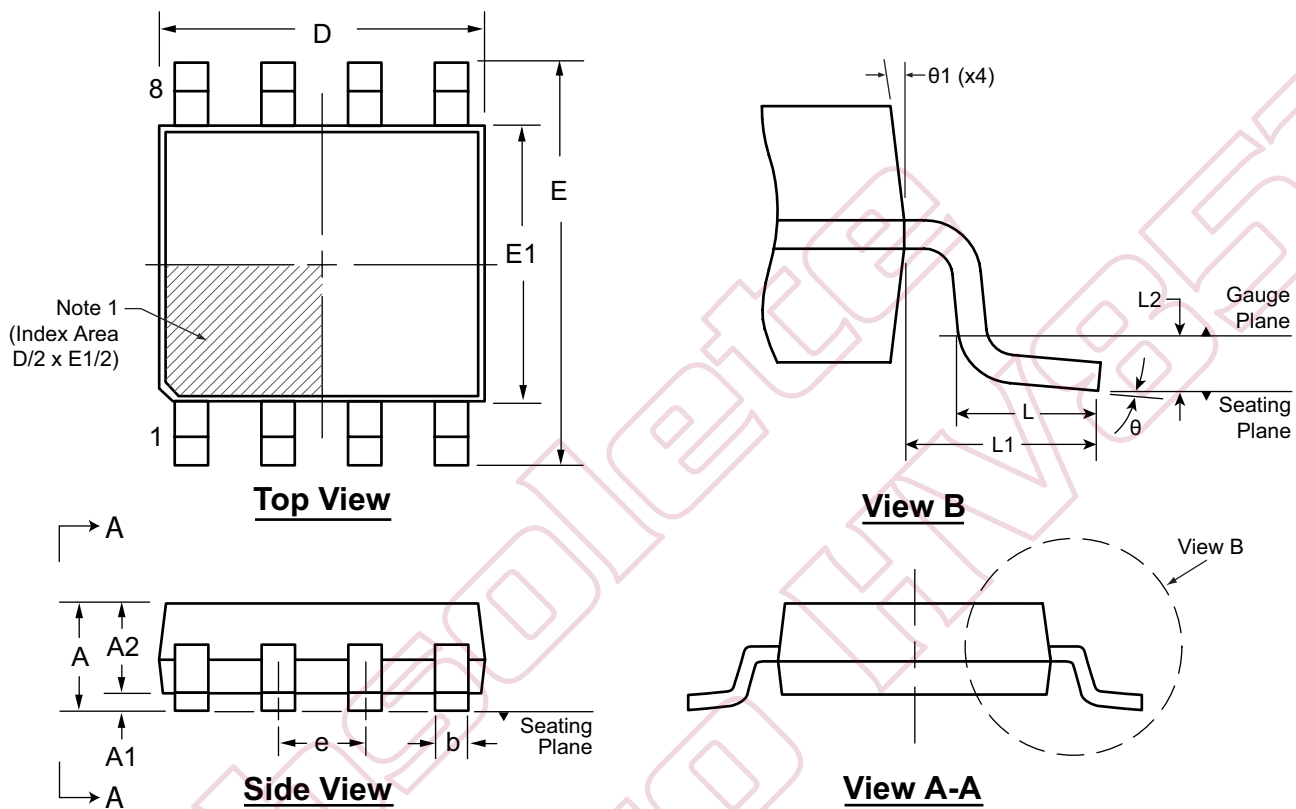
* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

Supertex Doc. #: DSPD-8SOLGTG, Version I041309.

8-Lead MSOP Package Outline (MG)

3.00x3.00mm body, 1.10mm height (max), 0.65mm pitch



Note:
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	E	E1	e	L	L1	L2	θ	θ1	
Dimension (mm)	MIN	0.75*	0.00	0.75	0.22	2.80*	4.65*	2.80*	0.65 BSC	0.40	0.95 REF	0.25 BSC	0°	5°
	NOM	-	-	0.85	-	3.00	4.90	3.00		0.60		0.25	-	-
	MAX	1.10	0.15	0.95	0.38	3.20*	5.15*	3.20*		0.80		0.25	8°	15°

JEDEC Registration MO-187, Variation AA, Issue E, Dec. 2004.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

Supertex Doc. #: DSPD-8MSOPMG, Version H041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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