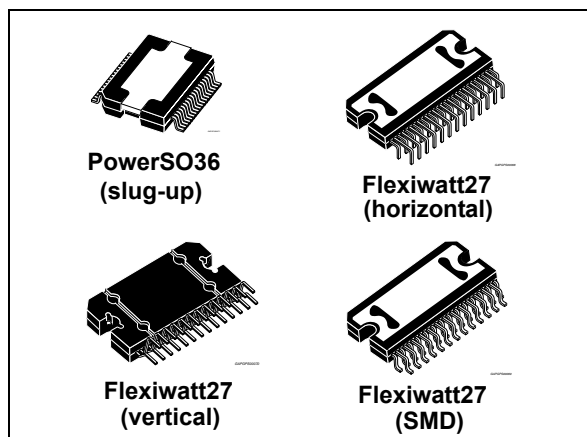


## Digital input quad power amplifier with built-in diagnostics features

Datasheet - production data



- Two I<sup>2</sup>C bus addresses and 8-ch TDM mode (only in PowerSO package)
- Optional non I<sup>2</sup>C bus mode
- Offset detector (play or mute mode)
- Clipping detector (selectable level) and diagnostics pin
- CMOS compatible enable pin (3.3/5 V)
- Full fault protection
- Four independent short circuit protections
- Linear thermal protection (four thermal warnings)
- ESD protection

### Features

- Integrated 110 dB D/A conversion
- I<sup>2</sup>S digital input (3.3/1.8 V) with TDM option
- Selectable input sampling frequency: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- MOSFET power outputs
- High output power capability 4x28 W/ 4 Ω @ 14.4 V, 1 kHz, 10 % THD
- Max. output power 4x72 W/2 Ω
- Full I<sup>2</sup>C bus driving (3.3/5 V):
  - Independent front/rear soft play/ mute
  - Selectable gain (four levels) for very low noise line-out function
  - I<sup>2</sup>C bus digital diagnostics (including DC and AC load detection)

### Description

The TDA7801 is a new BCD technology quad bridge amplifier for car audio applications.

Thanks to the BCD6 technology it is possible to integrate a high performance D/A converter together with powerful MOSFET outputs.

The possibility of having the D/A conversion on board allows the performance to reach an outstanding 115 dB S/N ratio with more than 105 dB of dynamic range.

This device is equipped with a full diagnostics array that communicates the status of each speaker through the I<sup>2</sup>C bus. The possibility to control the configuration and behavior of the device by means of the I<sup>2</sup>C bus makes TDA7801 a very flexible machine.

**Table 1. Device summary**

Order code	Package	Packing
TDA7801PD	PowerSO36 (slug-up)	Tube
TDA7801PDTR	PowerSO36 (slug-up)	Tape and reel
TDA7801	Flexiwatt27 (vertical)	Tube
TDA7801H	Flexiwatt27 (horizontal)	Tube
TDA7801SM	Flexiwatt27 (SMD)	Tube

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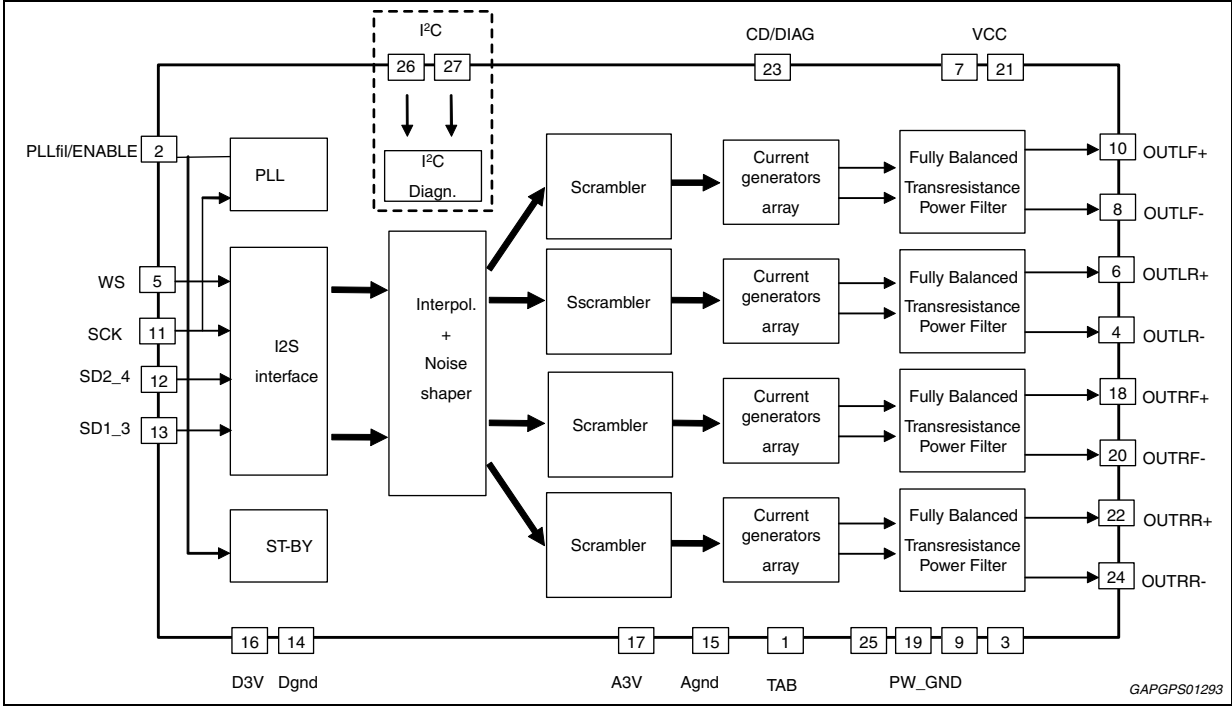
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# 1 Block diagram and pins description

## 1.1 Block diagram

Figure 1. Block diagram (Flexiwatt27)



## 2 Application diagrams

Figure 2. I<sup>2</sup>C bus mode application diagram (TDA7801/H/SM)

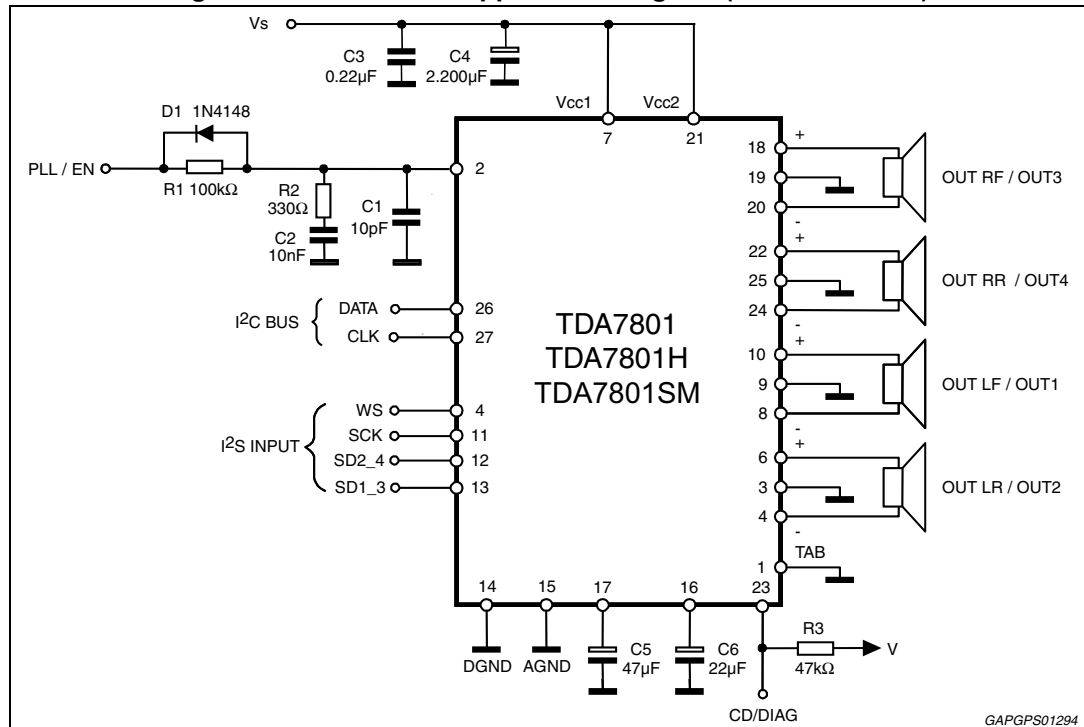


Figure 3. I<sup>2</sup>C bus mode application diagram (TDA7801PD)

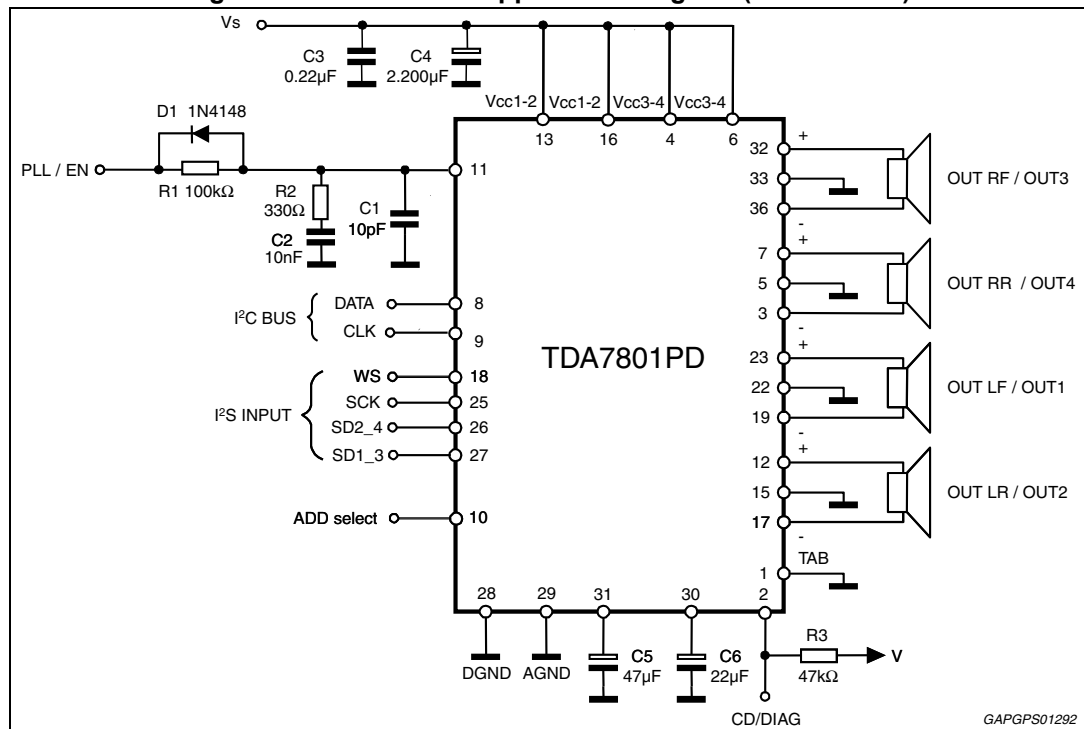


Figure 4. Legacy mode application diagram (TDA7801/H/SM)

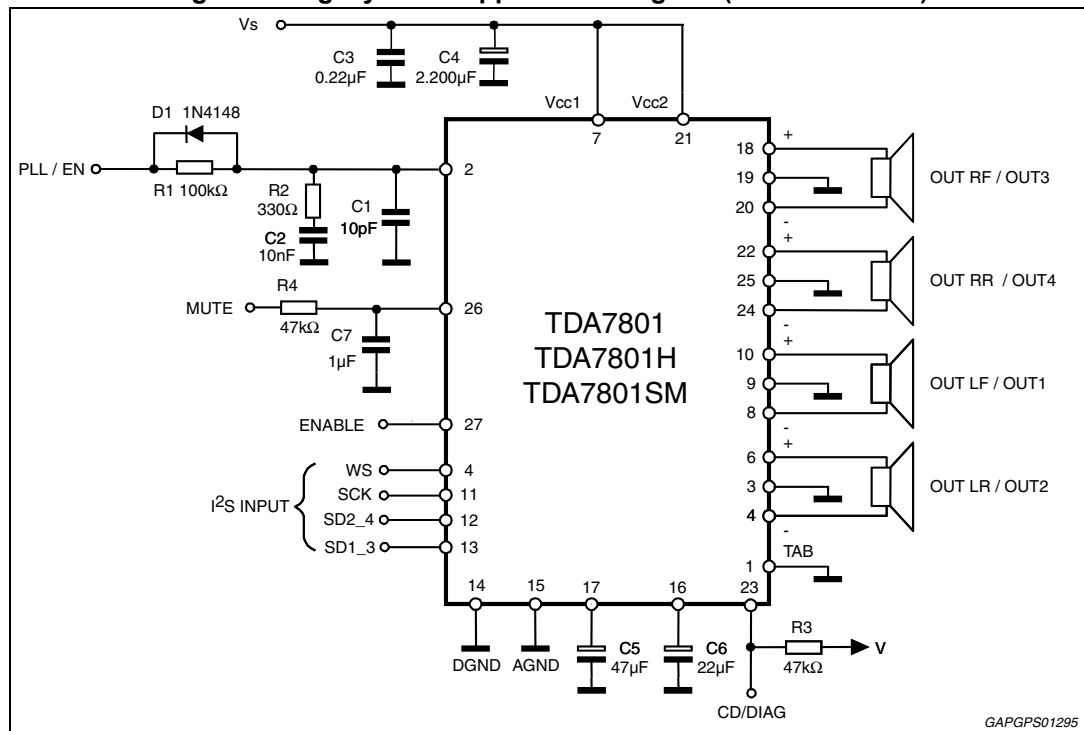
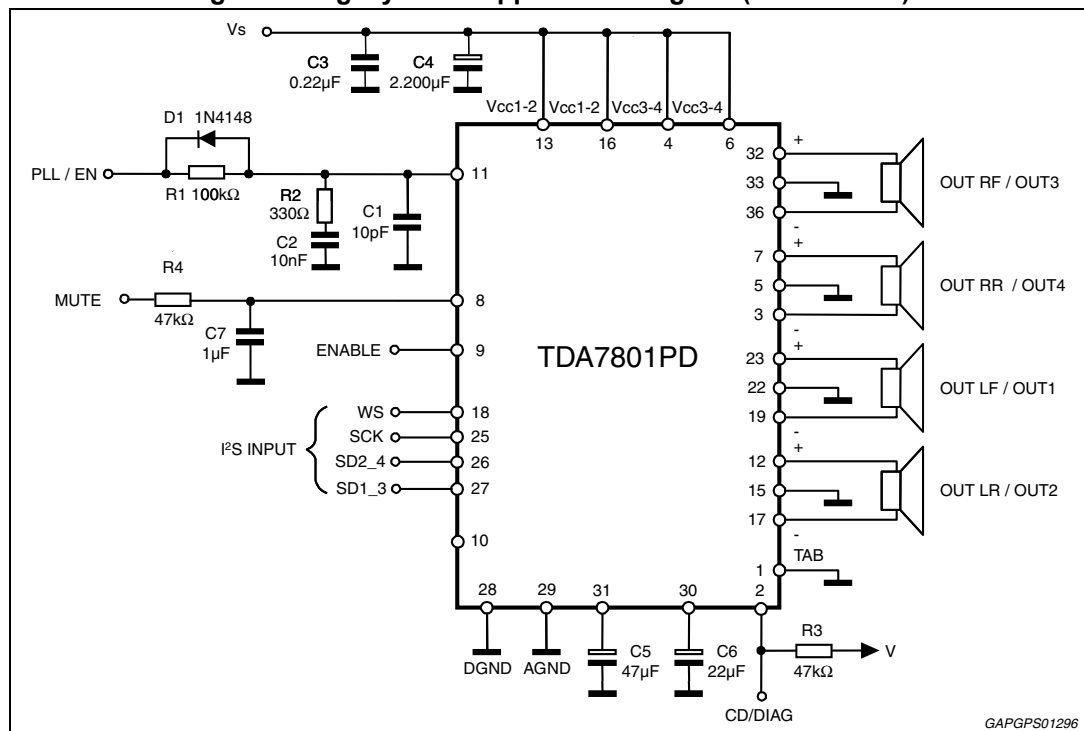


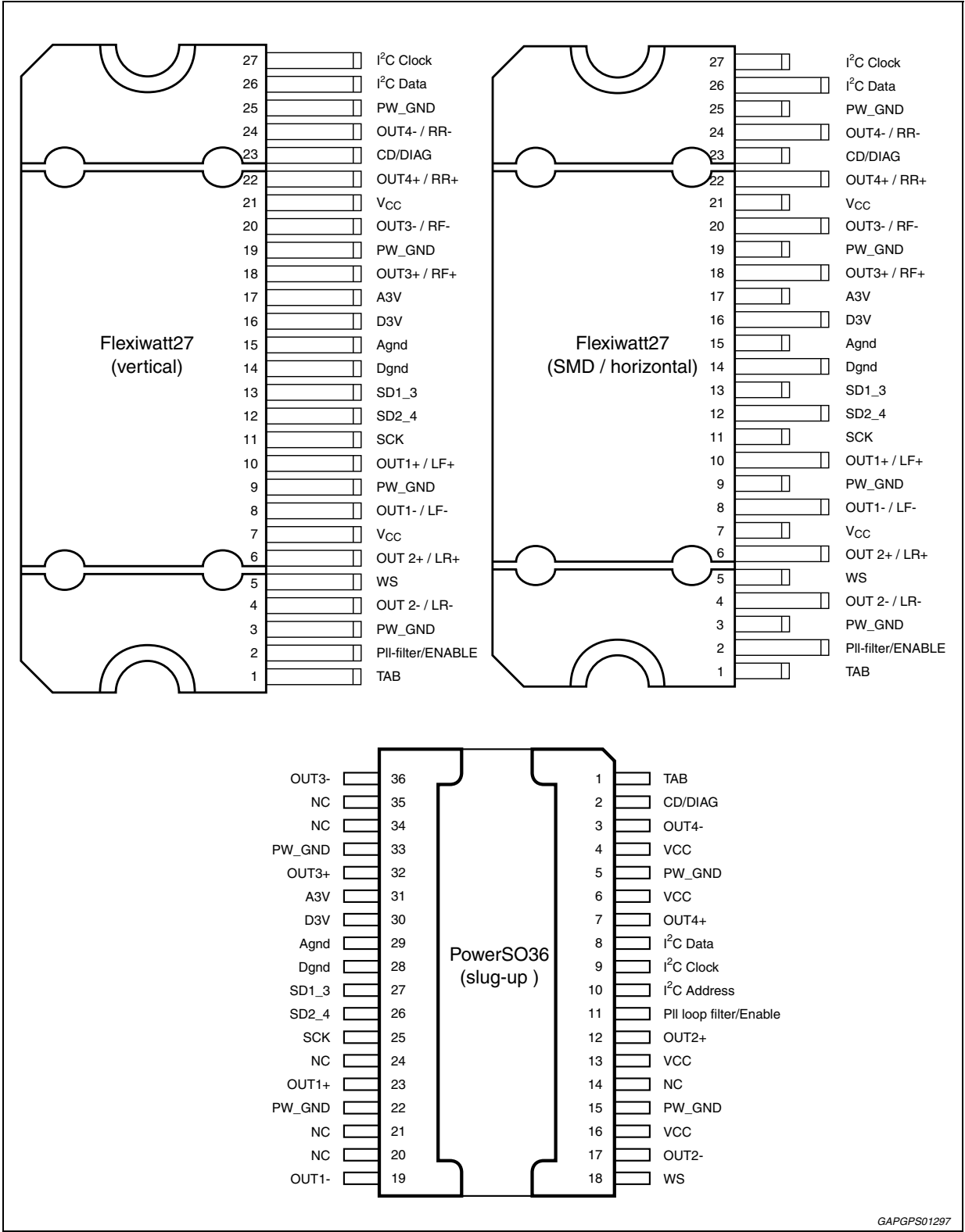
Figure 5. Legacy mode application diagram (TDA7801PD)





2.1 Pin description

Figure 6. Pin connection diagrams



GAPGPS01297

**Table 2. Flexiwatt27 (vertical/SMD/horizontal) pin description**

N°	Pin	Function
1	TAB	TAB connection (GND)
2	PII-filter / ENABLE	PII loop filter / ENABLE
3	PW_GND	Power ground channel 2
4	OUT 2- / LR-	Channel 2 (Left Rear) negative output
5	WS	Word select (I <sup>2</sup> S bus, logic input)
6	OUT 2+ / LR+	Channel 2 (Left Rear) positive output
7	Vcc	Channel 1 and 2 positive supply
8	OUT 1- / LF-	Channel 1 (Left Front) negative output
9	PW_GND	Power ground channel 1
10	OUT 1+ / LF+	Channel 1 (Left Front) positive output
11	SCK	Serial clock (I <sup>2</sup> S bus, logic input)
12	SD2_4	Serial data channels 2 and 4 (I <sup>2</sup> S bus, logic input)
13	SD1_3	Serial data channels 1 and 3 (I <sup>2</sup> S bus, logic input)
14	Dgnd	Digital ground
15	Agnd	Analog ground
16	D3V	Digital 3.3 V supply filter
17	A3V	Analog 3.3 V supply filter
18	OUT3+ / RF+	Channel 3 (right front) positive output
19	PW_GND	Power ground channel 3
20	OUT3- / RF-	Channel 3 (right front) negative output
21	Vcc	Channels 3 and 4 positive supply
22	OUT4+ / RR+	Channel 4 (right rear) positive output
23	CD/DIAG	Clip detector and diagnostic output: – Overcurrent protection intervention – Thermal warning – POR – (Open drain output)
24	OUT4- / RR-	Channel 4 (right rear) negative output
25	PW_GND	Power ground channel 4
26	I <sup>2</sup> C Data	I <sup>2</sup> C data/legacy mode mute
27	I <sup>2</sup> C Clock	I <sup>2</sup> C clock/enable legacy mode

Table 3. PowerSO36 pin description

N°	Pin	Function
1	TAB	TAB connection (GND)
2	CD/DIAG	Clip detector and diagnostic output: Overcurrent protection intervention Thermal warning Offset detection POR (Open drain output)
3	OUT4-	Channel 4 (right rear) negative output
4	VCC	Channels 3-4 positive supply
5	PW_GND	Power ground channel 4
6	VCC	Channels 3-4 positive supply
7	OUT4+	Channel 4 (right rear) positive output
8	I2C Data	I <sup>2</sup> C Data / legacy mode mute
9	I2C Clock	I <sup>2</sup> C Clock / enable legacy mode
10	I2C Address	I <sup>2</sup> C Address
11	PII loop filter/Enable	PII loop filter / Enable
12	OUT2+	Channel 2 (left rear) positive output
13	VCC	Channel 1-2 positive supply
14	NC	Not connected
15	PW_GND	Power ground channel 2
16	VCC	Channel 1-2 positive supply
17	OUT2-	Channel 2 (left rear) negative output
18	WS	Word Select (I <sup>2</sup> S bus, logic input)
19	OUT1-	Channel 1 (left front) negative output
20	NC	Not connected
21	NC	Not connected
22	PW_GND	Power ground channel 1
23	OUT1+	Channel 1 (left front) positive output
24	NC	Not connected
25	SCK	Serial clock (I <sup>2</sup> S bus, logic input)
26	SD2_4	Serial data channels 2 and 4 (I <sup>2</sup> S bus, logic input)
27	SD1_3	Serial data channels 1 and 3 (I <sup>2</sup> S bus, logic input)
28	Dgnd	Digital ground
29	Agnd	Analog ground
30	D3V	Digital 3.3 V supply filter
31	A3V	Analog 3.3 V supply filter
32	OUT3+	Channel 3 (right front) positive output
33	PW_GND	Power ground channel 3
34	NC	Not connected
35	NC	Not connected
36	OUT3-	Channel 3 (right front) negative output

## 3 Electrical specifications

### 3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{op}$	Operating supply voltage	18	V
$V_S$	DC supply voltage	28	V
$V_{peak1}$	Peak supply voltage (for $t = 50$ ms)	50	V
$V_{peak2}$	Peak supply voltage (for $t = 500$ ms)	34	V
$V_{i2cdata}$	I <sup>2</sup> C bus data pin voltage / legacy mode mute	20	V
$V_{i2ck}$	I <sup>2</sup> C bus clock pin voltage / enable legacy mode	50	V
$V_{i2s}$	I <sup>2</sup> S bus pins voltage	3.6	V
$I_O$	Output peak current (not repetitive $t = 100$ $\mu$ s)	8	A
$I_O$	Output peak current (repetitive $f > 10$ Hz)	6	A
$P_{tot}$	Power dissipation $T_{case} = 70$ °C	85	W
$F_s$ max	Maximum input sample rate	200	kHz
$T_{amb}$	Operative temperature range <sup>(1)</sup>	-40 to 105	°C
$T_{stg}, T_j$	Storage and junction temperature	-55 to 150	°C
$C_{max}$	Maximum capacitor vs. ground connected to the output	10	nF

1. A suitable heatsink/dissipation system should be used to keep  $T_j$  inside the specific limits.

### 3.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	PowerSO36	Flexiwatt 27	Unit
$R_{th j-case}$	Thermal resistance junction-to-case Max	1	1	°C/W

### 3.3 Electrical characteristics

Refer to the test circuit,  $V_S = 14.4\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $f = 1\text{ kHz}$ ;  $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified.

**Table 6. Electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_S$	Supply voltage range	-	8	-	18	V
$I_d$	Total quiescent drain current in amplifier mode	enable on amplifier mode muted	150	260	350	mA
$I_t$	Total quiescent drain current in tristate mode	enable on tristate mode	30	45	60	mA
$P_O$	Output power	$R_L = 4\ \Omega$ ; max power	41	45	-	W
		THD = 10 %	25	28	-	W
		THD = 1 %	20	22	-	W
		$R_L = 2\ \Omega$ ; max power	70	78	-	W
		$R_L = 2\ \Omega$ ; THD 10%	43	49	-	W
		$R_L = 2\ \Omega$ ; THD 1%	34	38	-	W
THD	Total harmonic distortion	$P_O = 1\text{ W to }10\text{ W}$ , $f=1\text{ kHz}$ , $G_{V1}$	-	0.03	0.05	%
		$P_O = 1\text{ W to }10\text{ W}$ , $f=10\text{ kHz}$ , $G_{V1}$	-	0.2	0.5	%
		$R_L = 100\ \Omega$ , input=-10 dBFS, $f=1\text{ kHz}$ , $G_{V1,2,3,4}$	-	0.01	0.02	%
$C_T$	Cross talk	$f = 1\text{ kHz to }10\text{ kHz}$	60	80	-	dB
$G_{V1}$	Voltage gain 1	Output voltage @ -10 dBFS	14.9	-	16.9	dB (Vp)
$G_{V2}$	Voltage gain 2		9.45	-	11.45	dB (Vp)
$G_{V3}$	Voltage gain 3		6.9	-	8.9	dB (Vp)
$G_{V4}$	Voltage gain 4		1.45	-	3.45	dB (Vp)
$F_{SV1}$	Full scale voltage $G_{V1}$	Output voltage @ 0 dBFS $V_S=18\text{ V}$ ; $R_L = 100\ \Omega$	12.7	-	-	Vrms
$F_{SV2}$	Full scale voltage $G_{V2}$	Output voltage @ 0 dBFS	6.65	-	8.35	Vrms
$F_{SV3}$	Full scale voltage $G_{V3}$		4.9	-	6.2	Vrms
$F_{SV4}$	Full scale voltage $G_{V4}$		2.65	-	3.35	Vrms
DG	Delta voltage gain 20 Hz – 20 kHz	$P_O = 1\text{ W}$	-0.5	-	0.5	dB
DR	Dynamic range $G_V = G_{V1}$ $G_V = G_{V2}$ $G_V = G_{V3}$ $G_V = G_{V4}$	Bw=20 Hz to 20 kHz, un weighted	105	110	-	dB
			100	105		
			100	105		
			98	103		

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$E_{IN}$	Output noise voltage $G_V = G_{V1}$ $G_V = G_{V2}$ $G_V = G_{V3}$ $G_V = G_{V4}$	Bw = 20 Hz to 20 kHz, unweighted	-	25 25 19 19	35 35 26 26	$\mu V$
SNR	Signal to noise ratio $G_V = G_{V1}$ $G_V = G_{V2}$ $G_V = G_{V3}$ $G_V = G_{V4}$	Bw = 20 Hz to 20 kHz, unweighted	111 105 105 100	115 109 109 104	-	dB
$G_B$	Gain balance		-1	-	+1	dB
SVR	Supply voltage rejection	$f = 1$ kHz; $V_r = 1$ Vpk;	50	70	-	dB
$I_{SB}$	Stand-by current	$V_{pin\ ENABLE} = 0V$	-	-	10	$\mu A$
$A_M$	Mute attenuation	-	80	-	-	dB
$V_{OS}$	Offset voltage	Mute & Play	-50	-	50	mV
$V_{AM}$	Supply automute range	Above this voltage the device is in play	7.8	-	-	V
		Below this voltage the device is in mute	-	-	6.8	V
$V_{POWONRESET}$	Supply voltage of power-on reset	-	-	4.5	5	V
$V_{OVERVOLTAGE}$	Over voltage shut-down	-	18	-	24	V
$CD_{LK}$	Clip det high Leakage current	CD off	-	0	5	$\mu A$
$CD_{SAT}$	Clip det sat. voltage	CD on; $I_{CD} = 1$ mA	-	150	300	mV
$CD1_{THD}$	Clip det THD level 1 %	-	-	1	2	%
$CD2_{THD}$	Clip det THD level 5 %	-	3	5	7	%
$CD3_{THD}$	Clip det THD level 10 %	-	7	10	13	%
$T_{mute}$	Mute and unmute commutation time	Programmable by I <sup>2</sup> C bus register IB1(6:4) $F_s = 44.1$ kHz	-	1.45	-	ms
			-	5.8	-	
			-	11.6	-	
			-	23.2	-	
			-	34.8	-	
			-	69.6	-	
			-	140	-	
			-	278	-	
$N_{GL}$	Noise gating input level	Under this level the device is in mute	-	-102	-	dB

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$N_{GT}$	Noise gating time	$F_s = 44100$ Hz	-	92	-	ms
$E_{IN2}$	Output noise voltage GV=GV1 GV=GV2 GV=GV3 GV=GV4	Bw=20 Hz to 20 kHz, unweighted, noise gating off, No input signal	-	44.2 42 31.2 21	88 84 63 42	$\mu V$
<b>Turn on diagnostics speaker mode</b>						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	-	-	-	1	V
$P_{Vs}$	Short to $V_s$ det. (above this limit, the output is considered in short circuit to $V_s$ )	-	$V_s - 1$	-	-	V
Pnop	Normal operation thresholds. (Within these limits, the output is considered without faults).	-	2	-	$V_s - 2$	V
Lsc	Shorted load det.	-	-	-	0.5	$\Omega$
Lop	Normal load det.	-	1.65	-	25	$\Omega$
Lnop	Open load det.	-	75	-	-	$\Omega$
Td	Max diagnostic time	Input sampling frequency $F_s = 44100$ Hz	-	-	190	ms
<b>Turn on diagnostics booster mode</b>						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	-	-	-	1	V
Pvs	Short to $V_s$ det. (above this limit, the output is considered in short circuit to $V_s$ )	-	$V_s - 1$	-	-	V
Pnop	Normal operation thresholds. (Within these limits, the output is considered without faults).	-	2	-	$V_s - 2$	V
Lsc	Shorted load det.	-	-	-	15	$\Omega$
Lop	Normal load det.	-	0.065	-	1	k $\Omega$
Lnop	Open load det.	-	3.5	-	-	k $\Omega$
<b>AC-diagnostic</b>						
$I_{ACTRESH}$	AC diagnostic current threshold	IB4 – D6= '0'	250	375	500	mA
		IB4 – D6= '1'	125	187	250	mA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Permanent diagnostics						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	-	-	-	1	V
Pvs	Short to $V_s$ det. (above this limit, the Output is considered in short circuit to $V_s$ )	-	$V_s - 1$	-	-	V
Pnop	Normal operation thresholds. (Within these limits, the output is considered without faults)	-	2	-	$V_s - 2$	V
L <sub>SC</sub>	Shorted load det.	Speaker mode	-	-	0.5	Ω
		Booster mode	-	-	15	Ω
Lop	Normal load det.	Speaker mode	1.65	-	-	Ω
		Booster mode	0.065	-	-	kΩ
V <sub>O</sub>	Offset detection	Absolute value	1.5	-	2.5	V
T <sub>ph</sub>	Thermal protection junction temperature	Gain attenuation of 60 dB	-	175	-	°C
T <sub>pl</sub>		Gain attenuation of 0.5 dB	-	165	-	°C
T <sub>w1</sub>	Thermal warning junction temperature	-	-	Tpl-10	-	°C
T <sub>w2</sub>		-	-	Tpl-27	-	°C
T <sub>w3</sub>		-	-	Tpl-45	-	°C
T <sub>w4</sub>		-	-	Tpl-62	-	°C
Legacy mode						
V <sub>LM_MUTE</sub>	Legacy mode mute threshold	Gain Attenuation of 80 dB	-	-	1.2	V
		Gain Attenuation of 0.1 dB	2.6	-	-	V
V <sub>LM_ON</sub>	Legacy mode threshold	Device in legacy mode	Vs-2	-	Vs	V
I <sub>LKG_MUTE</sub>	Mute pin leakage	-	-5	-	+5	μA
I <sup>2</sup> C Bus interface						
f <sub>SCL</sub>	Clock frequency	-	-	-	400	kHz
V <sub>IL</sub>	Input low voltage	-	-	-	1.5	V
V <sub>IH</sub>	Input high voltage	-	2.3	-	-	V
PII-filter /ENABLE pin						
V <sub>ILENB</sub>	Input low voltage	-	-	-	1.5	V
V <sub>IHENB</sub>	Input high voltage	-	2.3	-	-	V
I <sub>ILENB</sub> <sup>(1)</sup>	Logic '0' output current	V <sub>IN</sub> = 0.45 V	-	-	2	mA
I <sub>IHENB</sub>	Logic '1' input current	V <sub>IN</sub> = 2.3 V (IB0 D4=0)	-	-	2	μA



Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>I<sup>2</sup>S pin</b>						
V <sub>IL-I2S</sub>	Input low voltage	-	-	-	0.8	V
V <sub>IH-I2S</sub>	Input high voltage	-	1.3	-	-	V
I <sub>IH</sub>	Input high current except WS pin	V <sub>I</sub> = 3.3 V	-	-	5	μA
I <sub>IL</sub>	Input low current	V <sub>I</sub> = 0 V	-	-	5	μA
I <sub>IH_WS</sub>	Input high current for WS	V <sub>I</sub> = 3.3 V	-	70	150	μA

1. This has to be considered the maximum current value for a short time and not the standby current.

### 3.4 Electrical characteristics typical curves

Figure 7. Quiescent current vs. supply voltage      Figure 8. Output power vs. supply voltage (4 Ω)

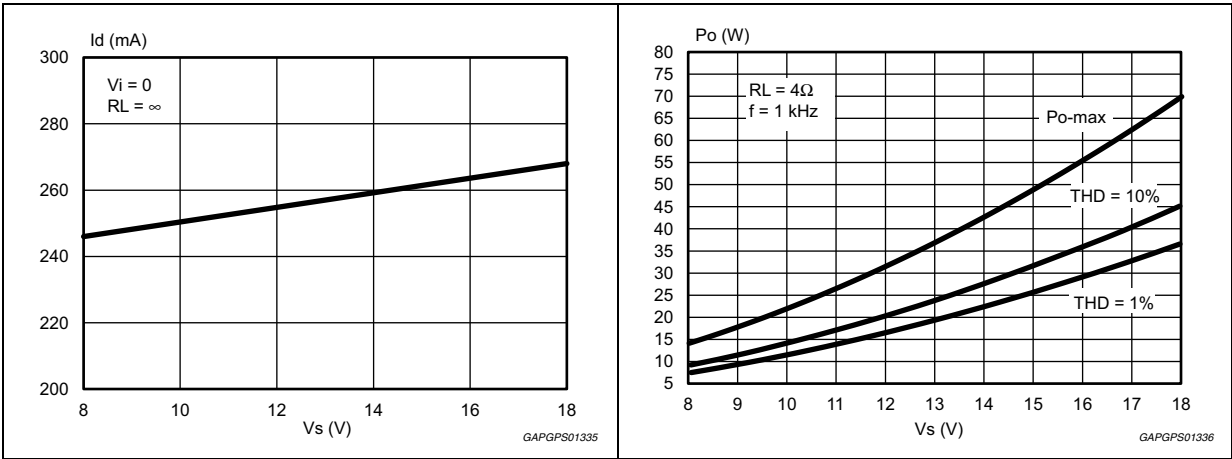


Figure 9. Output power vs. supply voltage (2 Ω)      Figure 10. Distortion vs. output power (4 Ω)

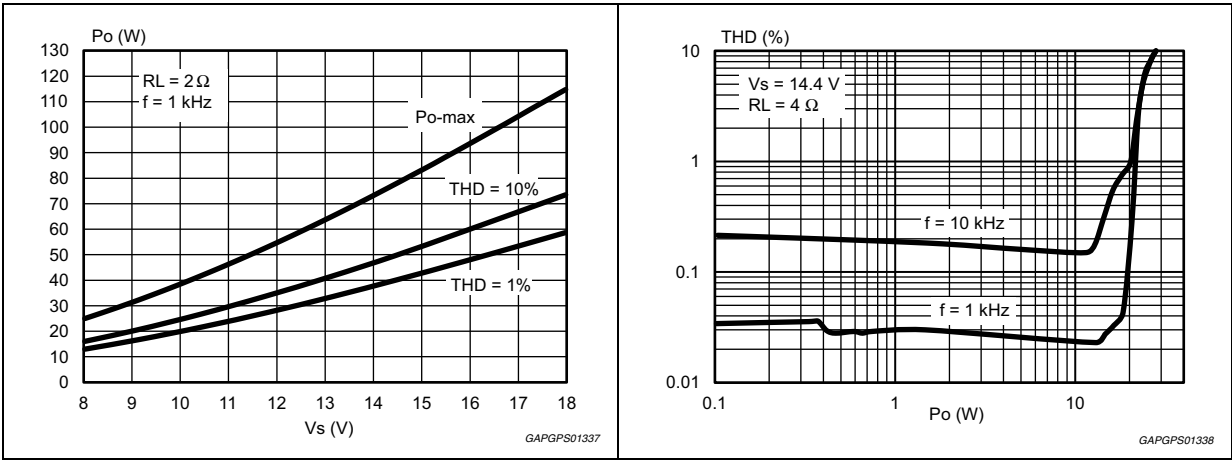


Figure 11. Distortion vs. output power (2  $\Omega$ )

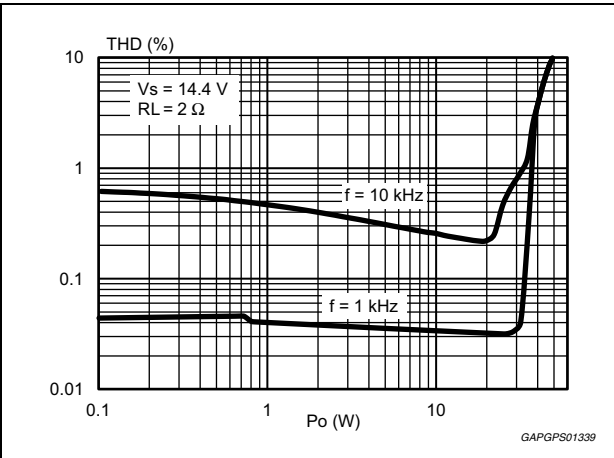


Figure 12. Distortion vs. frequency (4  $\Omega$ )

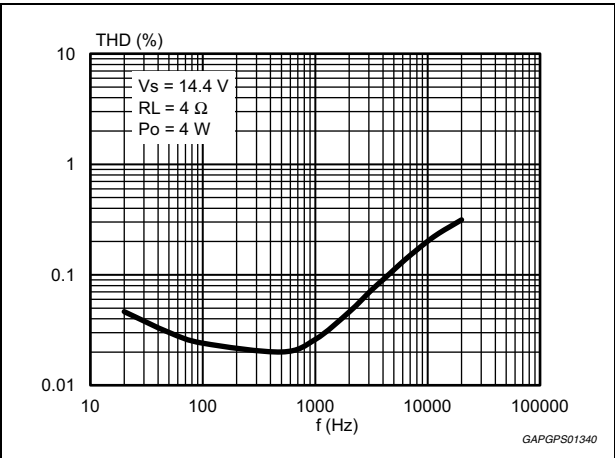


Figure 13. Distortion vs. frequency (2  $\Omega$ )

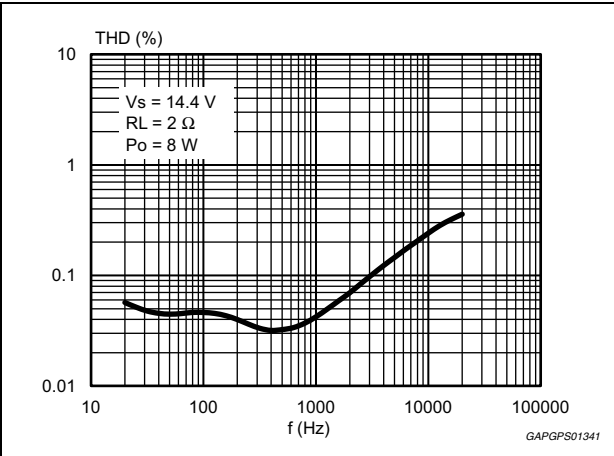


Figure 14. Vo vs. Vin (Gv1-2-3-4 settings)

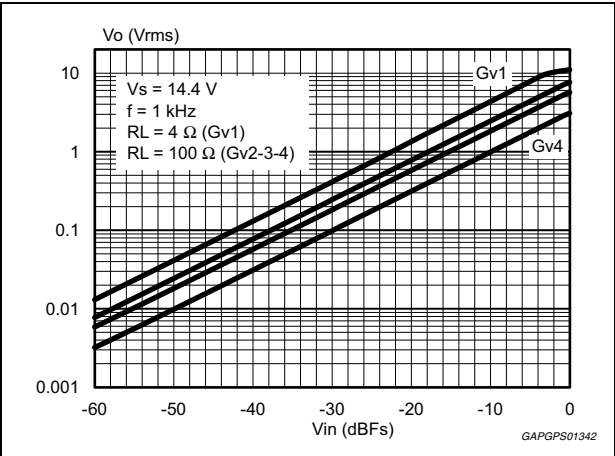


Figure 15. Vo vs. Vin (Gv1-2-3-4 settings + 6 dB dig. gain)

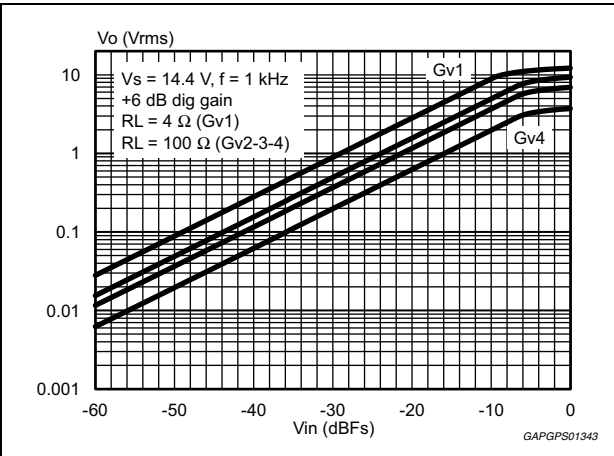


Figure 16. Distortion vs. output voltage (LD-Gv2)

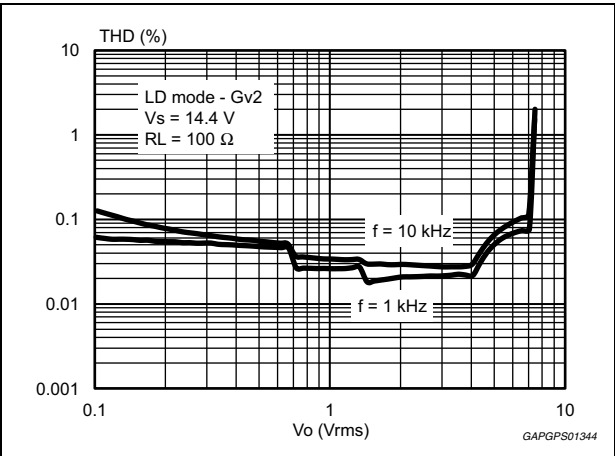


Figure 17. Distortion vs. output voltage (LD-Gv3)

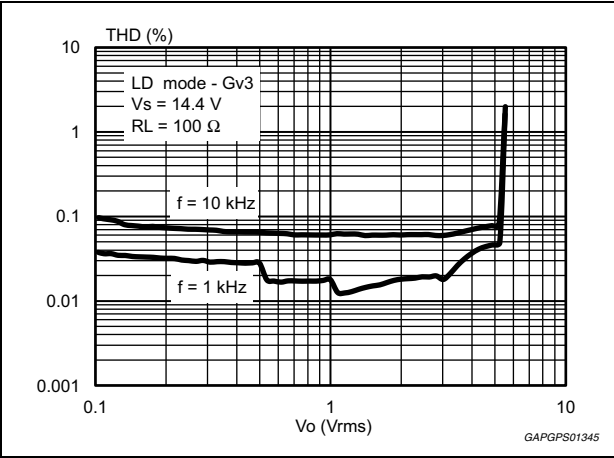


Figure 18. Distortion vs. output voltage (LD-Gv4)

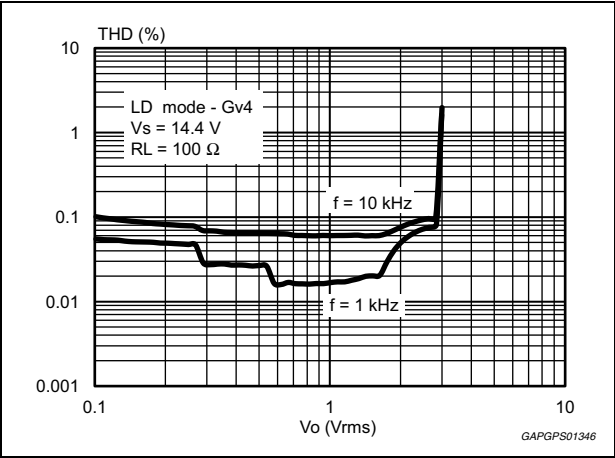


Figure 19. Output attenuation vs. Vs

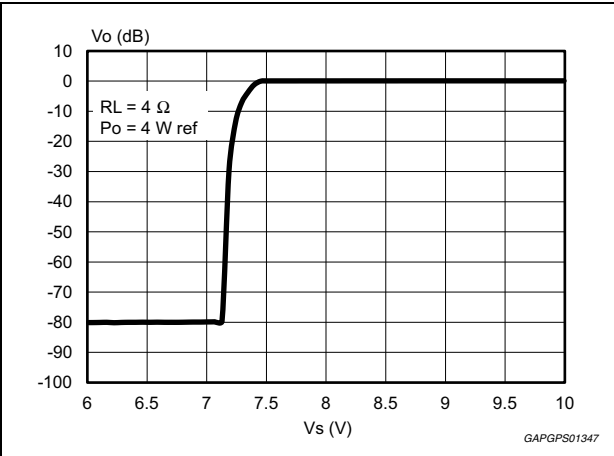


Figure 20. Crosstalk vs. frequency

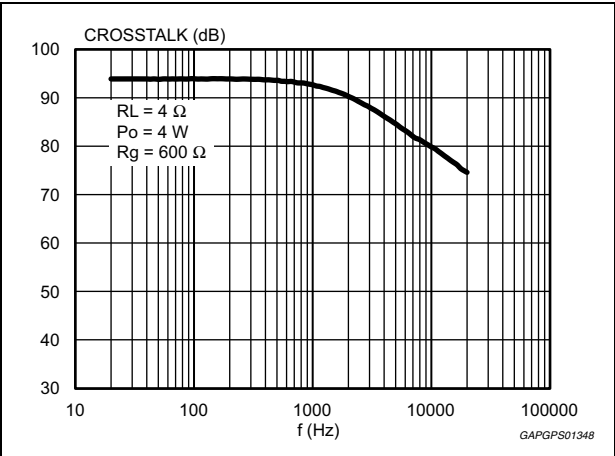


Figure 21. Supply voltage rejection vs. frequency

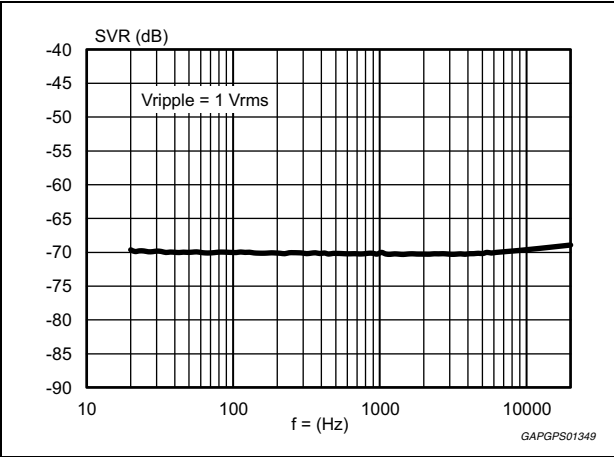
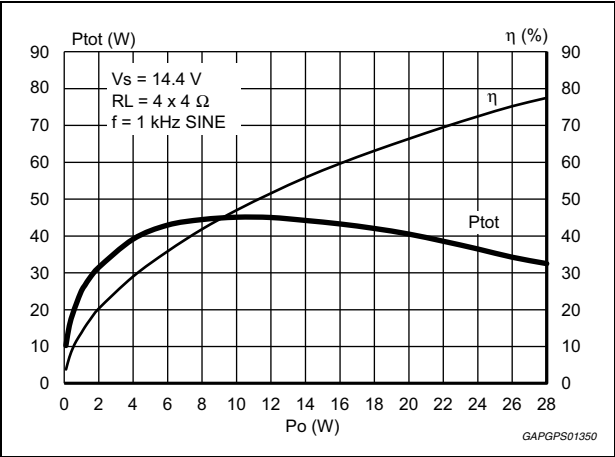
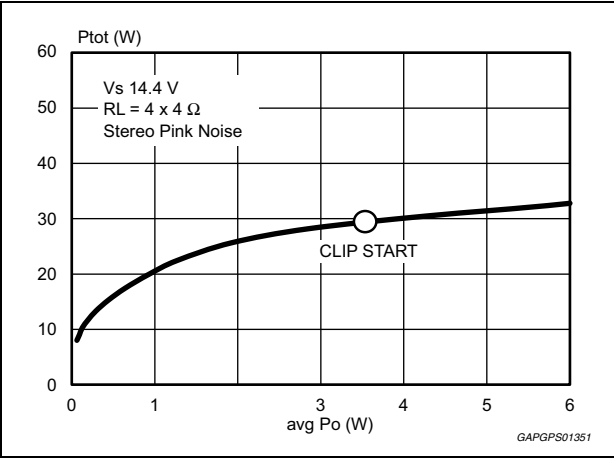


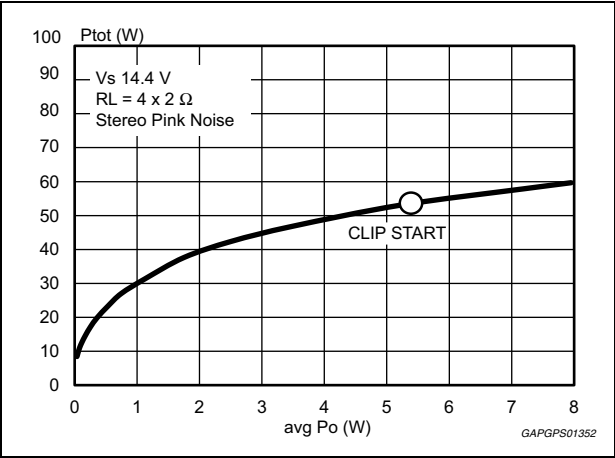
Figure 22. Total power dissipation & efficiency vs. Po (4 Ω)



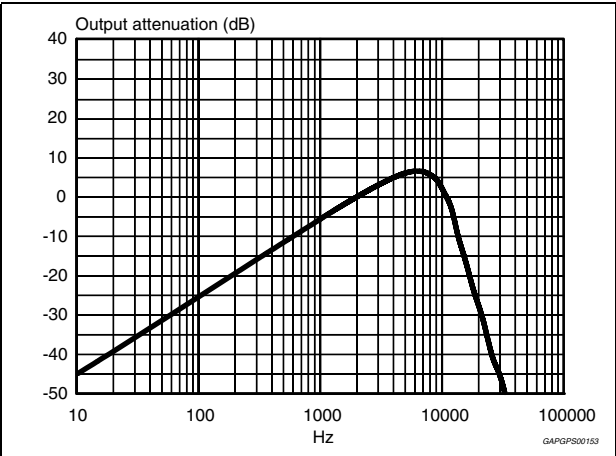
**Figure 23. Power dissipation vs. average Po (audio program simulation, 4 Ω)**



**Figure 24. Power dissipation vs. average Po (audio program simulation, 2 Ω)**



**Figure 25. ITU R-ARM frequency response, weighting filter for transient pop**



## 4 Operation mode

The device has three main operation modes:

- Standby mode
- Tristate mode
- Amplifier mode

### 4.1 Standby mode

When the ENABLE pin is low the device is in standby-mode. The current consumption is  $I_{SB}$ .

### 4.2 Tristate mode

When the ENABLE pin is high and the bit D7 of register DB0 is low the device is in tristate-mode. In that state the amplifier outputs are "high impedance", the I<sup>2</sup>C bus is ready to receive command.

### 4.3 Amplifier mode

When the ENABLE pin is high and the bit D7 of register DB0 is high the device is in amplifier-mode ready to play. To move the device in that state it is enough to write '1' on bit D7 of register IB1 from tristate-mode. Note that the device starts with all channels muted by default (see I<sup>2</sup>C registers description, [Section 9](#)).

## 5 "PLL-filter /enable" pin description

### 5.1 Functionality

The pin 2 has the functions to:

- ENABLE
- PLL filter

When the pin 2 is set to logic level low the TDA7801 is in standby-mode and the current consumption is ISB. The device is waked-up and put in tristate-mode setting the same pin to logic level high. In tristate-mode the TDA7801 is ready to receive I<sup>2</sup>C bus instructions. The device is set in amplifier-mode writing '1' on bit D7 of byte IB1.

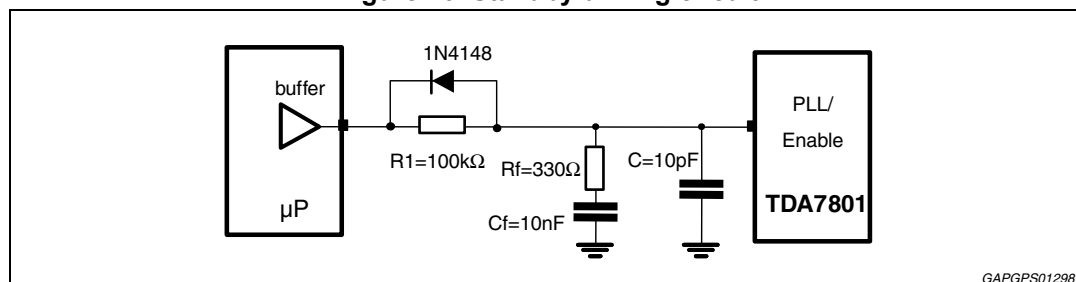
In amplifier-mode the PIN2 works as PLL filter pin. The TDA7801 will place this pin to have a precise voltage value.

During the transition from amplifier-mode to standby-mode, the device will try to force the Pin2 level sourcing a current  $I_{ILENB}$ .

### 5.2 Driving

In [Figure 26](#) an applicative schematic to drive the Pin 2 is reported. In the schematic, it is supposed that the TDA7801 is interfaced with a  $\mu P$ .

Figure 26. Standby driving circuit



The  $R_f$  and  $C_f$  components are respectively resistance and capacitance of the PLL filter. The resistance  $R_1$  and diode 1N4848 allows the Pin 2 to force to logic level low and the TDA7801 to force its voltage level in amplifier-mode. During the transition amplifier-mode/standby-mode the TDA7801 tries to forces the voltage on the PLL/Enable by sourcing a current flow. Since the PLL/ENABLE pin is forced at a voltage lower than  $V_{ILENB}$  in the above described conditions, the buffer input resistance should be chosen small enough to take this effect into account.

It's important to keep the PLL-Filter ground as close as possible to digital ground in the application board in order to minimize the PLL reference movement.

## 6 Functional description

### 6.1 Voltage supplies timing

TDA7801 internal voltage supplies rise time and fall time are determined by the two capacitors at pin 16 and 17, respectively digital supply pin (D3V3) and analog supply pin (A3V3). Capacitor on analog supply pin, (pin 17), and capacitor on digital supply, (pin 16), should respect the ratio 2:1. It is suggested to fix a minimum value of 22  $\mu\text{F}$  on digital supply pin and 47  $\mu\text{F}$  on analog supply pin, which correspond to a typical Turn-on time of 1.5 ms and a typical turn-off time of 8.5 ms.

### 6.2 Turn-on diagnostic description

Turn-on diagnostic is activated under I<sup>2</sup>C bus request. Detectable output faults are:

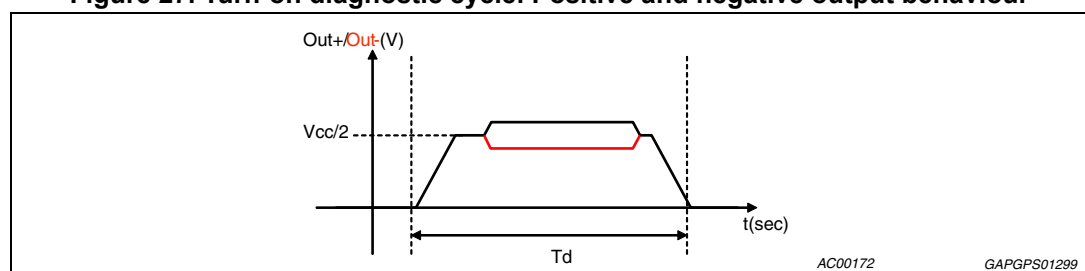
- Short to GND
- Short to  $V_s$
- Short across the speaker
- Open load

In the TDA7801 a new diagnostic that exploits the presence of D/A converters has been implemented. To verify if some of the above connections are in place, a subsonic (inaudible) voltage pulse is digitally and internally generated and converted (*Figure 27*). The amplitude of this pulse is stopped when the current flowing through the speaker is the same as the prefixed one corresponding to a specified load. The exact knowledge of the voltage drop across the load in any phase of the diagnostic time gives the possibility to know the connected load.

During the observation time, the measured load is compared with tabled values in order to determine the result.

The turn-on diagnostic status is internally stored until a successive diagnostic pulse is requested.

**Figure 27. Turn-on diagnostic cycle. Positive and negative output behaviour**



A turn-on diagnostic cycle is activated writing '1' on the D7 of byte IB0 only when the amplifier is in Tristate-mode. Note that the turn-on diagnostic state machine is sensible to the rise edge of this bit. To run another cycle of turn-on diagnostic it is necessary to:

1. wait that the previous cycle ends;
2. clear the D7-IB0 bit.
3. write '1' on D7-IB0 bit.

It is possible to run the turn-on diagnostic several times by simply resetting the D7-IB0 meanwhile the amplifier is in amplifier mode and writing back '1' on D7-IB0 when the amplifier is in tristate mode.

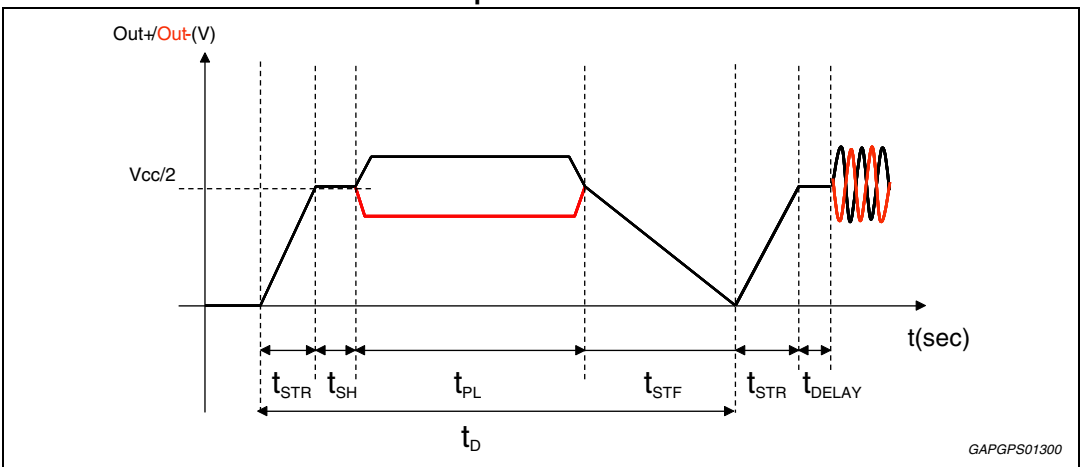
Between two diagnostic sequences it is necessary to reset the data register by an I<sup>2</sup>C reading instruction. Note that the reading instruction has been placed during the second diagnostic pulse.

The  $\mu$ P can program the TDA7801 in order to run a cycle of turn-on diagnostic and to move in amplifier-mode at the end of this cycle ([Figure 28](#)); the I<sup>2</sup>C bus instructions needed to program this sequence are:

11011000 -00100000-1XXXXXXX-1XXXXXXX

*Note:* The diagnostic enable bit (D7-IB0) has to be set before the amplifier mode bit (D7-IB1)

**Figure 28. Turn-on diag. cycle with transition in amp. mode. Positive and negative output behaviour**



**Table 7. Start-up diagnostic pulse typical timing**

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max	
$t_{STR}^{(1)}$	Start-up diagnostic rise	0.8	1.5	3	ms
$t_{SH}^{(2)}$	Short to Vcc/Gnd check		5		ms
$t_{PL}^{(2)}$	Plateau time		162		ms
$t_{STF}^{(1)}$	Start-up diagnostic fall	6	8.5	14	ms
$t_{DELAY}^{(2)}$	Delay time before play		5		ms
$t_D$	Diagnostic pulse		182	190	ms

1. These  $t_{STR}$  and  $t_{STF}$  values are relative to capacitors on A3V3 and D3V3 respectively equal to 47  $\mu$ F and 22  $\mu$ F. The  $t_{STR}$  and  $t_{STF}$  are proportional to capacitors value.

2. Values relative to  $f_s = 44100$ Hz.

The information related to the outputs status is read and memorized at the end of the voltage pulse top. The diagnostic cycle last no more than  $T_d$ . No audible noise is generated in the process. As for short to GND / Vs the fault-detection thresholds remain unchanged independently of the gain setting. They are as in [Figure 29](#).



**Figure 29. Short to GND and short to  $V_s$ , threshold description**

S.C. to GND	X	Normal Operation	X	S.C. to Vs	
0V	1.0V	2.0V	Vs-2.0V	Vs-1.0V	Vs

GAPGPS01301

Concerning short across the speaker / open speaker, the threshold varies from speaker mode to booster mode diagnostic setting, since different loads are expected (either normal speaker's impedance or high impedance). The speaker or booster mode is selected with bit D6-IB0 (channel 1 and 3) and bit D5-IB0 (channel 2 and 4). The values in case of speaker mode gain are as in [Figure 30](#).

**Figure 30. Short across the speaker and open load threshold description, in amplifier mode.**

S.C. across Load	X	Normal Load	X	Open Load	
0	0.5	1.65	25	75	infinite

GAPGPS01302

If the booster mode is selected, the same thresholds will change as in [Figure 31](#).

**Figure 31. Short across the speaker and open load threshold description, in line driver mode.**

S.C. across Load						X	Normal Load		X	Open Load	
0	15			65		1 k			3.5 k		infinite

GAPGPS01303

When the amplifier is biased and the diagnostic is still enabled the permanent diagnostic takes place. The previous turn-on state is kept until a short appears at the outputs because only in this case a new diagnostic cycle can start.

## 6.3 Permanent diagnostic

Detectable conventional faults are:

- Short to GND
- Short to  $V_s$
- Short across the speaker

The following additional features are provided:

- Output offset detection
- AC diagnostic

The TDA7801 diagnostic has 2 different cycles:

1. Restart cycle. It is a 1 ms pulse. During this period a check of the outputs is made.
2. Plateau cycle. It is a 100 ms pulse. During this period a check of the outputs is performed and the result of diagnostic analysis is communicated by means of I<sup>2</sup>C bus.

The TDA7801 has 2 different operating behaviors when a fault occurs:

1. Restart mode, (D6-IB0='0'). The diagnostic is not enabled. Each audio channel operates independently of each other. If any of the a.m. faults occurs, only the

channel(s) concerned are shut down. The diagnostic performs restart cycles every 1 ms until a fault condition is present. The amplifier restarts in play only once the overload is removed.

Diagnostic mode, (D6-IB0='1'). It is enabled via I<sup>2</sup>C bus and self activates if an output overload (so as to cause the intervention of the short-circuit protection) occurs to the speakers outputs. Once activated, the diagnostics procedure develops as below:

- The diagnostic performs 1 restart cycle in order to avoid momentary re-circulation spikes which could give erroneous diagnostic results. If normal situation (no overloads) is detected the channel returns active.
- Instead, if after 1 restart cycle an overload is detected then the diagnostic circuit performs a plateau cycle.
- After the plateau cycle, the fault audio channel generates restart cycles every 1 ms until a fault condition is present. The relevant data acquired during plateau cycle are stored and can be read by the microprocessor. A new plateau cycle can be activated by an I<sup>2</sup>C reading only if the fault condition persists. This is to ensure continuous diagnostics throughout the car-radio operating time.

The diagnostic performs another plateau cycle after each I<sup>2</sup>C bus registers read if the diagnostic bit is activated, (IB0-d7="1"). If I<sup>2</sup>C read is performed during the diagnostic permanent plateau cycle then, once the short is removed, the amplifier waits for another I<sup>2</sup>C read before starting to play again, in order to communicate the diagnostic plateau cycle results.

## 6.4 AC diagnostic

It is targeted at detecting accidental disconnection of tweeters in 2-way speaker and, more in general, presence of capacitive (AC) coupled loads. This diagnostic is based on the notion that the overall speaker's impedance (woofer + parallel tweeter) will tend to increase towards high frequencies if the tweeter gets disconnected, because the remaining speaker (woofer) would be out of its operating range (high impedance).

To determine the load impedance, a sinewave tone at a suitable ( $F > 10$  kHz or even ultrasonic) frequency should be fed to the output pins. Depending on the test's result the AC diagnostic is able to determine if the tweeter is connected or not. The tweeter is not connected if for four consecutive sine wave the current threshold on the load is not surpassed.

AC diagnostic is managed by I<sup>2</sup>C commands. The AC diagnostic is enabled by bit D7 of register IB4, while the bit D6 is used to choose the current level threshold. The result of AC test are stored in the data register DB4 (bits D7:D4) which are set to logic level '1' if a tweeter is detected on the correspondent channel.

Note, the results on D7:D4 are valid only if the bit D3 is zero; in order to avoid this condition the pulse generated has to respect the condition  $V_{out\_peak} < V_{battery-4V}$ .

## 6.5 Output DC offset detection

Any DC output offset exceeding  $\pm V_O$  are signalled out. This inconvenient might occur as a consequence of improper DC input signal. The offset detection is performed at the end of the digital chain by a low pass digital filter. The offset detection is permanent, and also works in play mode. The results of the DC offset detection are obtained from the right pin for each channel (see I<sup>2</sup>C table in [Section 9](#)); the bits are continuously refreshed.

## 6.6 Multiple faults

Faults can occur simultaneously. If this happens, faults are read out according to a "priority table" (see [Table 8](#)); this guarantees that the most dangerous fault is signalled. This is true only for the turn-on diagnostic but not in case of permanent diagnostic (only the faults causing protection intervention are recognized).

**Table 8. Multiple faults priority**

	<b>S. GND</b>	<b>S. Vs</b>	<b>S. Across L.</b>	<b>Open L.</b>
<b>S. GND</b>	S. GND	S. Vs + S. GND	S. GND	S. GND
<b>S. Vs</b>	/	S. Vs	S. Vs	S. Vs
<b>S. Across L.</b>	/	/	S. Across L.	N.A.
<b>Open L.</b>	/	/	/	Open Load <sup>(1)</sup>

1. Only in Startup Diagnostic

In permanent diagnostic mode the table is the same, with only a difference concerning open load, which is not among the recognizable faults. If an open load is present during the device's normal operation, it should be detected at a subsequent turn-on diagnostic cycle (i.e. at the successive car radio turn-on).

## 6.7 Faults availability

All the results coming from I<sup>2</sup>C bus, by read operations, are the consequence of measurements inside a defined period of time. If the fault is stable throughout the whole period, it will be sent out.

The turn-on diagnostic faults are reported on the byte DB 0-3 at the bits D 4-0. The faults are consistent when the bit D6 of DB0 is '1'. The byte DB 0-3 is reset when read.

During Amplifier-mode, when the bit D4 of byte DB 0-3 is '1' an overload on the correspondent channel has been detected and a 100 ms permanent diagnostic cycle has been done. The data on the bits D 4-0 reports the results of this diagnostic cycle. If the bits are all zero it means that an overload event has been detected, a 100ms cycle has been performed and the fault has not been detected or removed.

## 6.8 I<sup>2</sup>C programming/reading sequence

A correct turn on/off sequence respectful of the diagnostic timings and producing no audible noises could be as follows (after battery connection):

- Turn-on:** (Stand-by out + Dlag Enable) → 200 ms (min.) → Muting out
- Turn-off:** Muting in → 10 ms → (Diag disable + stand-by in)
- Car radio installation:** Dlag enable (write) → 200 ms → I<sup>2</sup>C read (repeat until all faults disappear).

## 6.9 Legacy mode

In case of applications without the I<sup>2</sup>C bus the TDA7801 could be turned on in legacy mode.

In order to put the device in legacy mode it is enough to tie the IC clock pin (PIN 27) at Vcc. In this mode the device is turned on, as usual, with the ENABLE pin (PIN 2). The I<sup>2</sup>C Data pin (PIN26) acts as analog mute. The device is set with all the instruction registers equal to zero.

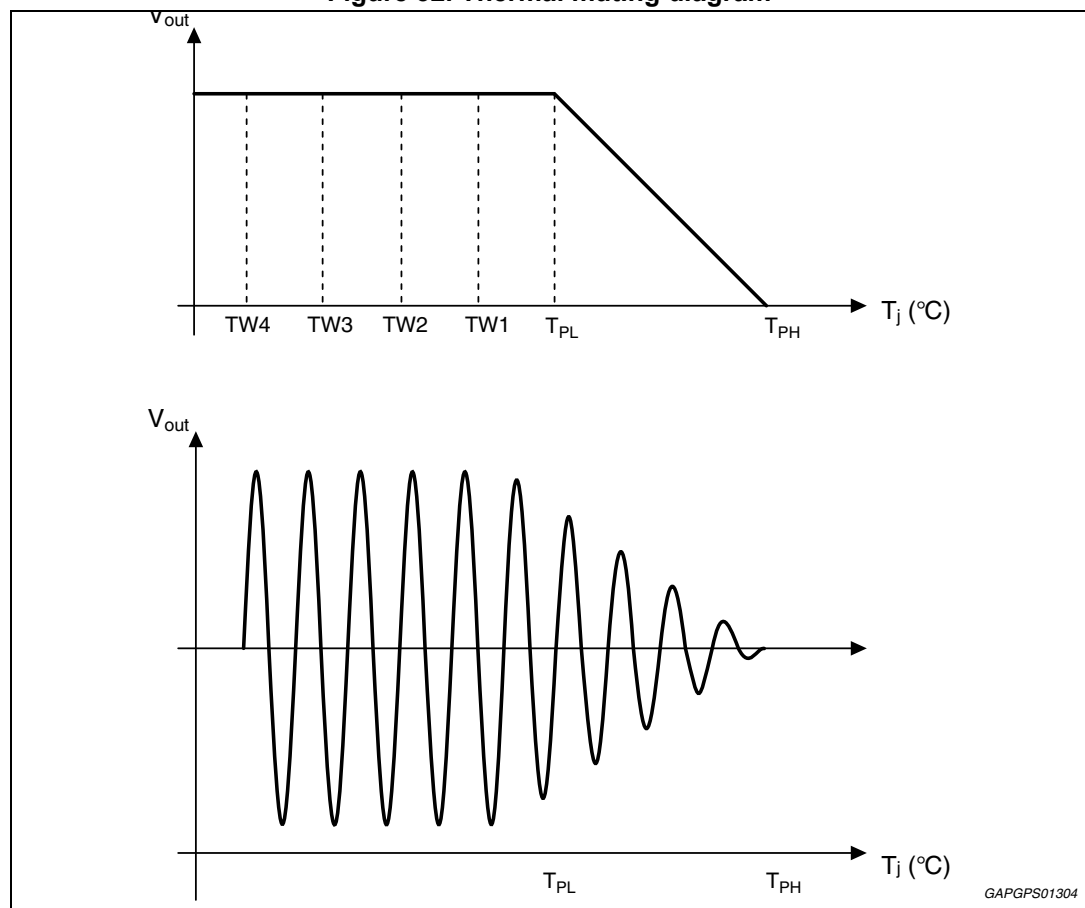
In legacy mode the I<sup>2</sup>S interface does not support the TDM format.

## 6.10 Thermal protection

The TDA7801 has four thermal warnings (Tw1, Tw2, Tw3, Tw4) at different temperatures which are stored on the I<sup>2</sup>C bus. Only one of the four thermal warnings could be sent to the DIAG pin. The selection is done by an I<sup>2</sup>C bus.

A mute function dependent on temperature is present in order to protect the junction by over-temperature with limited effects on the sound quality. For junction temperature over the thermal warning threshold  $T_{pl}$ , the device is gradually carried in mute. The mute level depends on the temperature: when the junction temperature reaches the  $T_{pl}$  threshold (refer to [Figure 32](#)), the output signal is attenuated of 0.5 dB, while when the junction temperature reaches  $T_{ph}$  the output attenuation is 60 dB. This attenuation is performed without output signal distortion.

Figure 32. Thermal muting diagram



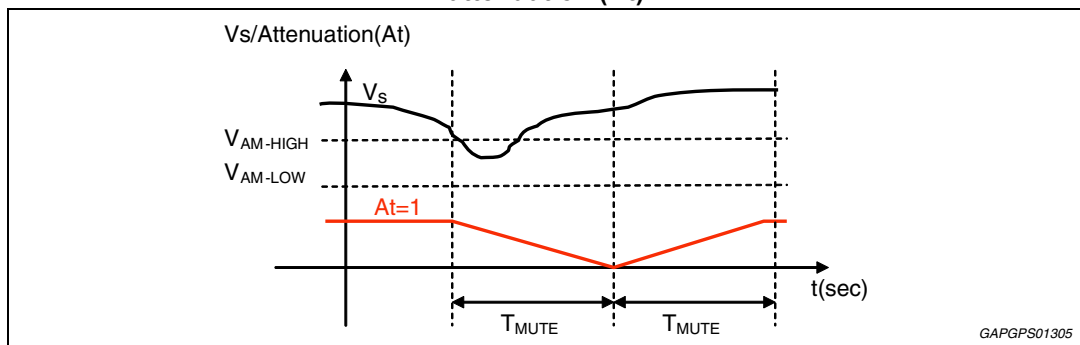
## 6.11 Under-voltage threshold

### 6.11.1 Supply voltage auto-mute threshold

The device in play-mode is put in mute when the supply voltage gets lower than the  $V_{AM}$  threshold.

When the supply voltage gets lower than the  $V_{AM}$  threshold the device is put in mute. The muting strategy in this case is reported in [Figure 33](#): once the supply voltage  $V_s$  becomes lower than  $V_{AM\_HIGH}$ , analog mute and digital mute are activated. The analog mute attenuation is proportional to the  $V_s$  voltage and becomes equal to AM when the  $V_s$  gets lower than  $V_{AM\_LOW}$ . Note that once the digital mute procedure is started, it cannot be stopped to move back the device in play, the procedure is going on until the attenuation level has reached AM. This mechanism avoids that a fast oscillation on  $V_s$  cause a similar oscillation on the output.

**Figure 33. Low voltage mute attenuation, supply voltage variation ( $V_s$ ); result digital attenuation ( $A_t$ )**



### 6.11.2 Digital mute disabling

The digital mute is disabled in the following conditions:

- when TW1 threshold is trespassed (to avoid simultaneous intervention of digital mute and thermal mute)
- when the bit IB3-D5 is set to '1'
- during the start-up diagnostic

When the digital mute is disabled, the analog mute is kept active.

### 6.11.3 Power-on reset threshold

When the ENABLE pin is low or the supply voltage value doesn't guarantee the integrity of the I<sup>2</sup>C bus registers ( $V_{POWERONRESET}$ ) the TDA7801 is put in tristate-mode and the registers are set to the initial state. The event is signalled by the low value of DIAG pin and the '0' value of bit D7 of byte DB0. The DIAG pin is set to high after a POR when the bit D7 of byte IB1 is set to '1' (amplifier mode on) if no other event on DIAG pin is present. The same I<sup>2</sup>C bus write operation automatically sets to '1' the bit D7 of byte DB0. When the device is programmed with the D7=1 of IB0 and D7=1 of byte IB1 the device turns-on after a diagnostic cycle and the DIAG pin stays low for the whole duration of the diagnostic cycle.

## 6.12 Fast mute features

The TDA7801 is put in mute by a fast-mute procedure by one of the following event:

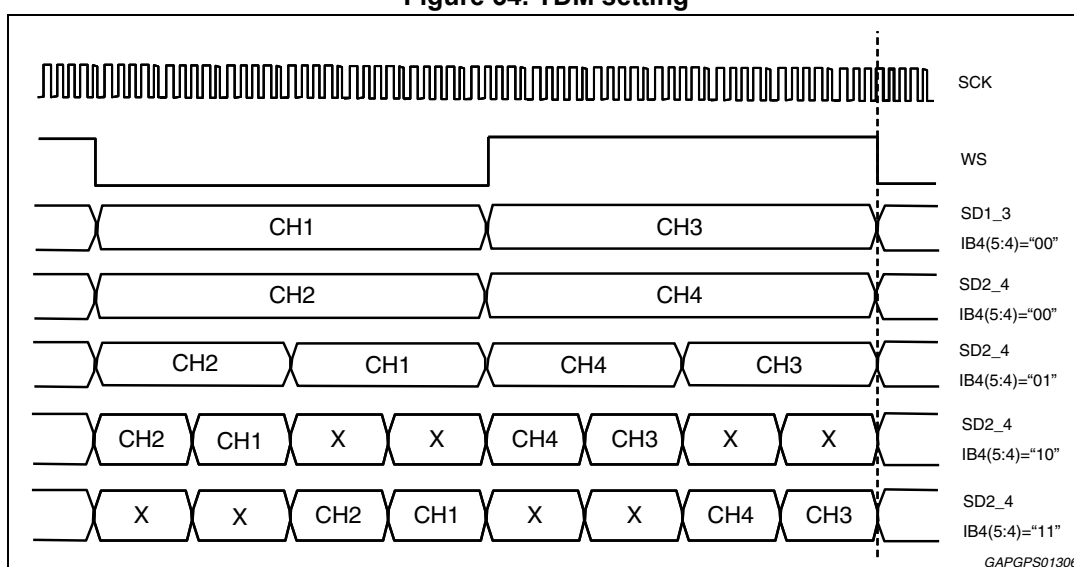
- the ENABLE pin is set to low
- the PLL loses the locking
- the  $V_S$  voltage level is under the auto-mute threshold.
- by an I<sup>2</sup>C programming

## 7 I<sup>2</sup>S bus interface

The TDA7801 accepts the I<sup>2</sup>S standard format that could be time division multiplexed (TDM), however the WS still needs a 50% duty-cycle to work correctly. The [Figure 34](#) shows the different I<sup>2</sup>C settings allowed for the I<sup>2</sup>S interface (2,4 or 8 channels transmission on a single serial data line (SD) can be selected). By I<sup>2</sup>C programming it is possible to choose between the following interface settings:

- channel 1 and channel 3 channel on SD1\_3 and channel 2 and channel 4 on SD2\_4
- all four channels on SD2\_4. SD1\_3 has not function.
- eight channels transferred on the SD2\_4 line. This setting is feasible in the PowerSO36 and Flexiwatt27 package.

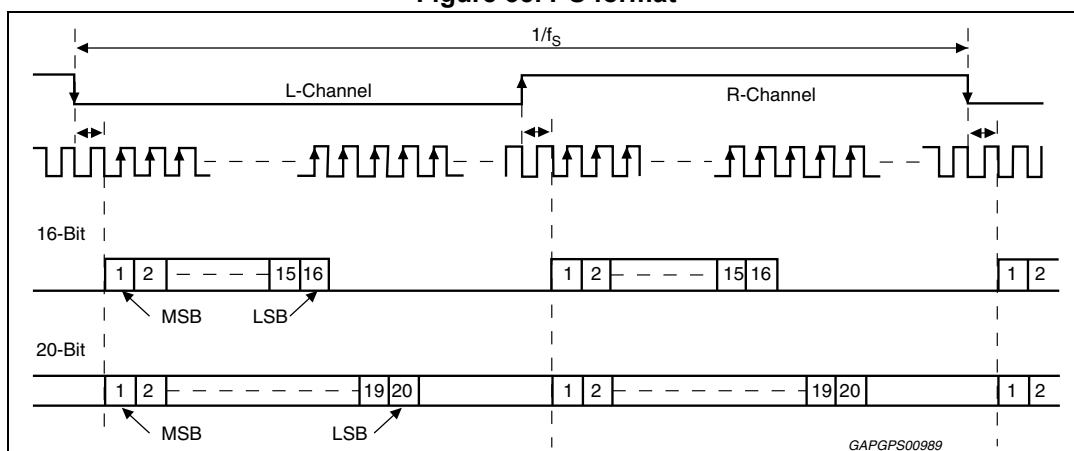
**Figure 34. TDM setting**



The TDA7801 accepts the I<sup>2</sup>S standard format with a bit clock (SCK) equal to 64 fs.

Note, TDM setting is guaranteed for a maximum  $F_s = 96$  kHz.

**Figure 35. I<sup>2</sup>S format**



## 7.1 Interface timings requirements

The data interface timings are described below. In the TDA7801 the TDM format as shown in [Figure 34](#), is an I<sup>2</sup>S extended: if the four channels option is set then the serial clock is multiplied by two while it will be multiplied by four when the eight channels option is set. This means that it is important to keep a duty-cycle of 50% for the Word Select signal and moreover, all the timings for serial clock and data don't change in every I<sup>2</sup>S configuration.

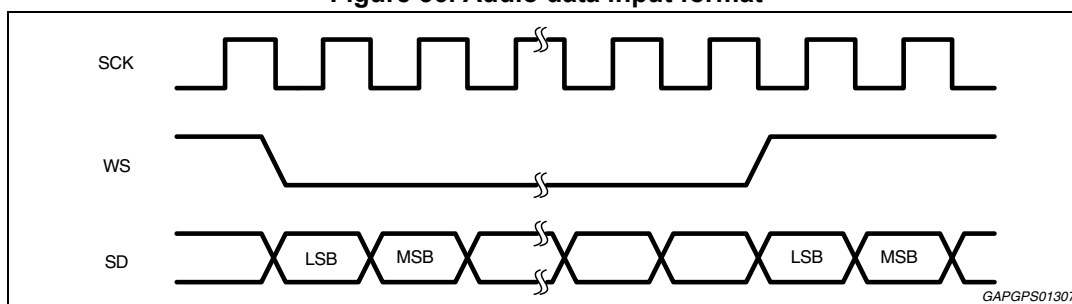
**Table 9. System clock frequencies for common audio sampling frequencies**

Frequency sampling ( $f_s$ )	System clock frequency ( $f_{SCK}$ ), (MHz)			
	I <sup>2</sup> S standard ( $f_s \times 64$ )	TDM 4ch ( $f_s \times 128$ )	TDM 8ch md1 ( $f_s \times 256$ )	TDM 8ch md2 ( $f_s \times 256$ )
44.1 (kHz)	2.82	5.64	11.29	11.29
48.0 (kHz)	3.07	6.14	12.29	12.29
96.0 (kHz)	6.14	12.29	24.58	24.58
192.0 (kHz)	12.29	24.58	N.A.	N.A.

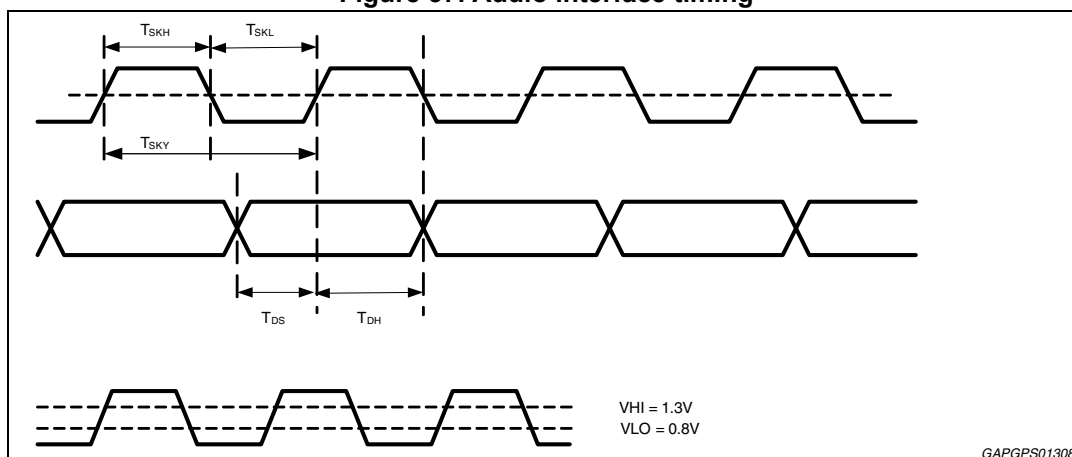
[Table 9](#) shows the values of system clock frequencies (serial clock SCK) for common audio sampling frequencies.

Figure 12 shows the detail of the audio input format as specified by the standard I<sup>2</sup>S specification. When more channels are sent the input format does not change and they follow the sequence as shown in [Figure 34](#).

**Figure 36. Audio data input format**



**Figure 37. Audio interface timing**





**Table 10. Example timing for  $t_{ck} = 1/f_{SCK}$ , where  $f_{SCK}$  is stated in the [Table 9](#)**

Parameter	MIN	TYP	MAX	Note
Clock period $T_{SKY}$	$0.9 \cdot T_{ck}$	$T_{ck}$	$1.1 \cdot T_{ck}$	
Clock HIGH $T_{SKH}$	$0.4 \cdot T_{ck}$			Measured from VHI to VHI
Clock LOW $T_{SKL}$	$0.4 \cdot T_{ck}$			Measured from VLO to VLO
Setup time SD to $f_{SCK}$ rising edge $T_{DS}$	$0.2 \cdot T_{ck}$			
Hold time SD from $f_{SCK}$ rising edge $T_{HD}$	$0.2 \cdot T_{ck}$		$0.8 \cdot T_{ck}^{(1)}$	
$f_{SCK}$ duty-cycle	40%		60%	
VHI	1.3			
VLO			0.8	

1. Measured from VLO to VHI.

## 7.2 Group delay

The group delay of the amplifier is basically due the FIR filter of the interpolator and it is given by:

$$t_{DELAY} = \frac{32}{f_s}, (f_s < 48 \text{ kHz})$$

## 8 I<sup>2</sup>C bus interface

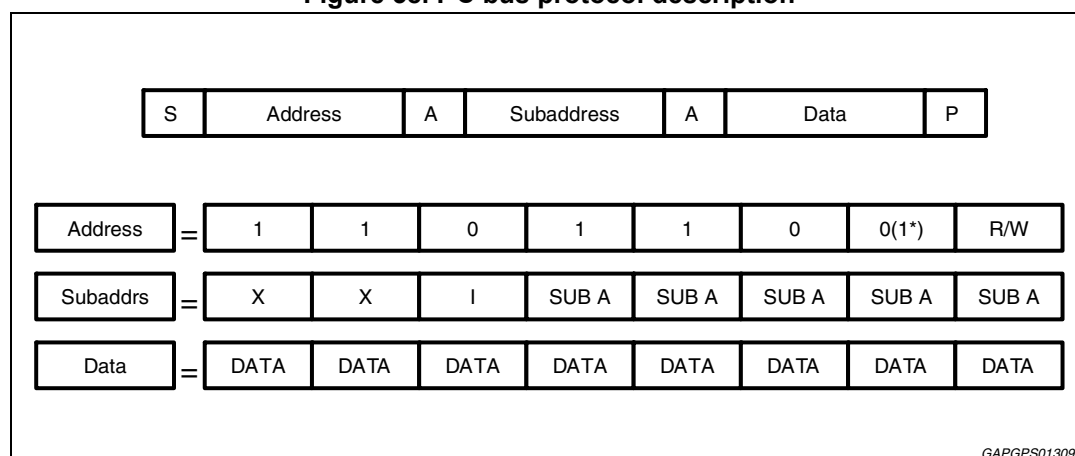
Data transmission from microprocessor to the TDA7801 and viceversa takes place through the 2 wires I<sup>2</sup>C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

When I<sup>2</sup>C bus is active any operating mode of the IC may be modified and the diagnostic may be controlled and results read back.

The protocol used for the bus is depicted in [Figure 38](#) and comprises:

- a start condition (S)
- a chip address byte (the LSB bit determines read/write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)

**Figure 38. I<sup>2</sup>C bus protocol description**



### Description:

S = Start

R/W = '0' => Receive-Mode (Chip could be programmed by  $\mu$ P)

I = Auto increment; when 1, the address is automatically increased for each byte transferred

X: not used

A = Acknowledge

P = Stop

MAX CLOCK SPEED 400kbit/sec

\* = available in PowerSO36

## 8.1 Writing procedure

There are two possible procedures:

1. without increment: the I bit is set to 0 and the register is addressed by the subaddress. Only this register is written by the data following the subaddress byte.
2. with increment: the I bit is set to 1 and the first register written is the one addressed by subaddress. Then all the registers starting from the one indicated by this address up to stop bit (or up to last register) are written.

## 8.2 Reading procedure

There are two possible procedures:

1. without increment: the I bit is set to 0 and the register is addressed by the subaddress sent in the previous write procedure. Only this register is read by the data following the address.
2. with increment: the I bit is set to 1 and the first register read is the one addressed by subaddress sent in the previous write procedure. Then all registers starting from the one indicated by this address up to stop bit (or up to last register) are read.

*Note:* the reading procedure reset the register that has been read.

## 8.3 Data validity

The data on the SDA line must be stable during the high period of the clock. The high and low state of the data line can only change when the clock signal on the SCL line is low.

## 8.4 Start and stop conditions

A start condition is a high to low transition of the SDA line while SCL is high.  
The stop condition is a low to high transition of the SDA line while SCL is high.

## 8.5 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

## 8.6 Acknowledge

The transmitter\* puts a resistive HIGH level on the SDA line during the acknowledge clock pulse. The receiver\*\* has to pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low using this clock pulse.

\* Transmitter

- = master (μP) when it writes an address to the TDA7801
- = slave (TDA7801) when the μP reads a data byte from TDA7801

\*\* Receiver

- = slave (TDA7801) when the μP writes an address to the TDA7801
- = master (μP) when it reads a data byte from TDA7801

## 9 I<sup>2</sup>C registers

### 9.1 IB0-Addr:"00000"

Table 11. IB0-Addr:"00000"

Bit	Instruction decoding bit
D7	0: diagnostic defeat 1: diagnostic enable
D6	0: Speaker mode diagnostic ch. 1 and 3 (FRONT) 1: Booster mode diagnostic ch. 1 and 3
D5	0: Speaker mode diagnostic ch. 2 and 4 (REAR) 1: Booster mode diagnostic ch. 2 and 4
D4	Gain channel 1 and 3 (FRONT) D4 D3
D3	00 GV1 01 GV2 10 GV3 11 GV4
D2	Gain channel 2 and 4 (REAR) D2 D1
D1	00 GV1 01 GV2 10 GV3 11 GV4
D0	0: No increase of digital gain 1: +6dB increase of digital gain

### 9.2 IB1-Addr:"00001"

Table 12. IB1-Addr:"00001"

Bit	Instruction decoding bit
D7	0: Amplifier mode off - Amplifier not working 1: Amplifier mode on - Amplifier working
D6	Mute Time Setting D6 D5 D4 mute timing(Fs=44.1kHz)
D5	000 1.45 ms 001 5.8 ms
D4	010 11.6 ms 011 23.2 ms 100 34.8 ms 101 69.6 ms 110 140 ms 111 278 ms
D3	0: Mute channel 1 and 3 (FRONT) 1: Unmute channel 1 and 3

**Table 12. IB1-Addr:"00001" (continued)**

Bit	Instruction decoding bit	
<b>D2</b>	0: Mute channel 2 and 4 (REAR) 1: Unmute channel 2 and 4	
<b>D1</b>	Sample Frequency Range <sup>(1)</sup> D1 D0	
<b>D0</b>	00	44.1/48 kHz
	01	44.1/48 kHz
	10	96 kHz
	11	192 kHz

1. When the amplifier is in Tristate Mode (IB0-D7=0 and IB1-D7=0), any accidental change of Frequency sample is ignored.

### 9.3 IB2-Addr:"00010"

**Table 13. IB3-Addr:"00010"**

Bit	Instruction decoding bit	
<b>D7</b>	0: no short fault information on diag. pin 1: short fault information on diag. pin	
<b>D6</b>	0: Offset information on diag pin 1: no offset information on diag pin	
<b>D5</b>	Temperature warning information on diag. pin D5 D4 D3	
<b>D4</b>	000	Tw1
	001	Tw2
<b>D3</b>	010	Tw3
	011	Tw4
	1xx	no thermal warning information on diag. pin
<b>D2</b>	Clip detection level D2 D1	
<b>D1</b>	00	1 %
	01	5 %
	10	10 %
	11	clip detection disabled
<b>D0</b>	0 (no selectable from user)	

## 9.4 IB3-Addr:"00011"

Table 14. IB3-Addr:"00011"

Bit	Instruction decoding bit
D7	0: Noise gating on 1: Noise gating off
D6	0 (not used)
D5	0: under-voltage digital mute on 1: under-voltage digital mute off
D4	Tristate channel 3 (right front) 0: ch.3 not in tristate 1: ch.3 in tristate
D3	Tristate channel 1 (left front) 0: ch.1 not in tristate 1: ch.1 in tristate
D2	Tristate channel 4 (right rear) 0: ch.4 not in tristate 1: ch.4 in tristate
D1	Tristate channel 2 (left rear) 0: ch.2 not in tristate 1: ch.2 in tristate
D0	0: Input high pass filter off 1: Input high pass filter on

## 9.5 IB4-Addr:"00100"

Table 15. IB4-Addr:"00100"

Bit	Instruction decoding bit
D7	AC diagnostic On (D7='1')
D6	AC diagnostic current threshold D6 = '0': high D6 = '1': low
D5	TDM 00 I2S standard
D4	01 I2S - 4 ch 10 I2S - 8 ch (first channels) 11 I2S - 8 ch (last channels)
D3	0 (not used)
D2	0 (not used)
D1	0 (not used)
D0	0 (not used)

## 9.6 DB0-Addr:"10000" - Channel 1 (left front)

**Table 16. DB0-Addr:"10000" - Channel 1 (left front)**

Bit	Instruction decoding bit
<b>D7</b>	Power on reset (POR) 0: After a POR the device is in tristate 1: The device has been put out of tristate at least one time after POR
<b>D6</b>	Start-up diagnostic status 0: Turn-On diag. cycle not activated or not terminated 1: Turn-On diag. cycle terminated
<b>D5</b>	Channel 1 offset detection 0: No output offset 1: Output offset detected
<b>D4</b>	Channel 1 <sup>(1)</sup> 0: Permanent diagnostic cycle not activated or not terminated 1: Permanent diagnostic cycle terminated
<b>D3</b>	Channel 1 0: Normal load 1: Short load
<b>D2</b>	Channel 1 0: No open load 1: Open load detection (only during turn-on diagnostic)
<b>D1</b>	Channel 1 0: No short to Vcc 1: Short to Vcc
<b>D0</b>	Channel 1 0: No short to GND 1: Short to GND

1. The permanent diagnostic cycle is activated after each register reading if the permanent diagnostic is still present, (IB0-d7="1").

## 9.7 DB1-Addr:"10001" - Channel 2 (left rear)

Table 17. DB1-Addr:"10001" - Channel 2 (left rear)

Bit	Instruction decoding bit
<b>D7</b>	TW1 active 0: TW1 threshold not trespassed 1: TW1 threshold tress-passed
<b>D6</b>	TW2 active 0: TW2 threshold not trespassed 1: TW2 threshold tress-passed
<b>D5</b>	Channel 2 offset detection 0: No output offset 1: Output offset detected
<b>D4</b>	Channel 2 <sup>(1)</sup> 0: permanent diag. cycle not activated or not terminated 1: Permanent diag. cycle terminated
<b>D3</b>	Channel 2 0: Normal load 1: Short load
<b>D2</b>	Channel 2 0: No open load 1: Open load detection (only during turn-on diagnostic)
<b>D1</b>	Channel 2 0: No short to Vcc 1: Short to Vcc
<b>D0</b>	Channel 2 0: No short to GND 1: Short to GND

1. The permanent diagnostic cycle is activated after each register reading if the permanent diagnostic is still present.



## 9.8 DB2-Addr:"10010"" - Channel 3 (right front)

Table 18. DB2-Addr:"10010"" - Channel 3 (right front)

Bit	Instruction decoding bit
<b>D7</b>	TW3 active 0: TW3 threshold not trespassed 1: TW3 threshold tress-passed
<b>D6</b>	TW4 active 0: TW4 threshold not trespassed 1: TW4 threshold tress-passed
<b>D5</b>	Channel 3 offset detection 0: No output offset 1: Output offset detected
<b>D4</b>	Channel 3 <sup>(1)</sup> 0: Permanent diag. cycle not activated or not terminated 1: Permanent diag. cycle terminated
<b>D3</b>	Channel 3 0: Normal load 1: Short load
<b>D2</b>	Channel 3 0: No open load 1: Open load detection (only during turn-on diagnostic)
<b>D1</b>	Channel 3 0: No short to Vcc 1: Short to Vcc
<b>D0</b>	Channel 3 0: No short to GND 1: Short to GND

1. The permanent diagnostic cycle is activated after each register reading if the permanent diagnostic is still present.

## 9.9 DB3-Addr:"10011" - Channel 4 (right rear)

Table 19. DB3-Addr:"10011" - Channel 4 (right rear)

Bit	Instruction decoding bit
<b>D7</b>	0: channel 2 and 4 in play (FRONT) 1: channel 2 and 4 in mute
<b>D6</b>	0: channel 1 and 3 in play (REAR) 1: channel 1 and 3 in mute
<b>D5</b>	Channel 4 offset detection 0: No output offset 1: Output offset detected
<b>D4</b>	Channel 4 <sup>(1)</sup> 0: permanent diag. cycle not activated or not terminated 1: Permanent diag. cycle terminated
<b>D3</b>	Channel 4 0: Normal load 1: Short load
<b>D2</b>	Channel 4 0: No open load 1: Open load detection (only during turn-on diagnostic)
<b>D1</b>	Channel 4 0: No short to Vcc 1: Short to Vcc
<b>D0</b>	Channel 4 0: No short to GND 1: Short to GND

1. The permanent diagnostic cycle is activated after each register reading if the permanent diagnostic is still present.

## 9.10 DB4-Addr:"10100"

Table 20. DB4-Addr:"10100"

Bit	Instruction decoding bit
<b>D7</b>	Ch1 tweeter present
<b>D6</b>	Ch2 tweeter present
<b>D5</b>	Ch3 tweeter present
<b>D4</b>	Ch4 tweeter present
<b>D3</b>	Signal to high
<b>D2</b>	0
<b>D1</b>	0
<b>D0</b>	0

## 10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

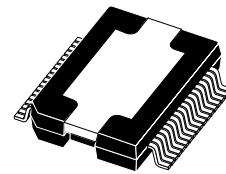
ECOPACK<sup>®</sup> is an ST trademark.

**Figure 39. PowerSO36 (slug-up) mechanical data and package dimensions**

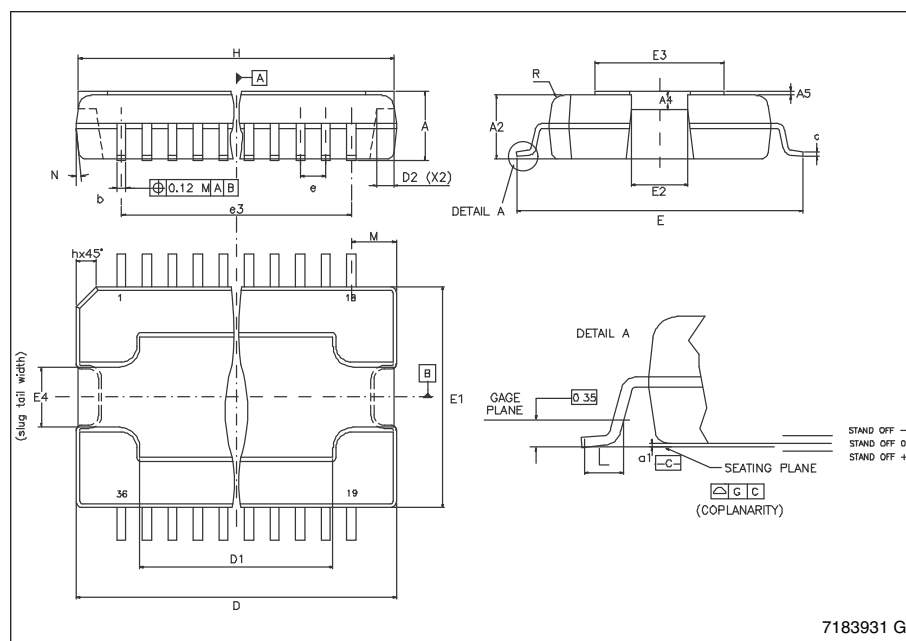
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.270	-	3.410	0.1287	-	0.1343
A2	3.100	-	3.180	0.1220	-	0.1252
A4	0.800	-	1.000	0.0315	-	0.0394
A5	-	0.200	-	-	0.0079	-
a1	0.030	-	-0.040	0.0012	-	-0.0016
b	0.220	-	0.380	0.0087	-	0.0150
c	0.230	-	0.320	0.0091	-	0.0126
D	15.800	-	16.000	0.6220	-	0.6299
D1	9.400	-	9.800	0.3701	-	0.3858
D2	-	1.000	-	-	0.0394	-
E	13.900	-	14.500	0.5472	-	0.5709
E1	10.900	-	11.100	0.4291	-	0.4370
E2	-	-	2.900	-	-	0.1142
E3	5.800	-	6.200	0.2283	-	0.2441
E4	2.900	-	3.200	0.1142	-	0.1260
e	-	0.650	-	-	0.0256	-
e3	-	11.050	-	-	0.4350	-
G	0	-	0.075	0	-	0.0031
H	15.500	-	15.900	0.6102	-	0.6260
h	-	-	1.100	-	-	0.0433
L	0.800	-	1.100	0.0315	-	0.0433
N	-	-	10°	-	-	10°
s	-	-	8°	-	-	8°

- (1) "D and E1" do not include mold flash or protrusions.  
Mold flash or protrusions shall not exceed 0.15mm (0.006").  
(2) No intrusion allowed inwards the leads.

### OUTLINE AND MECHANICAL DATA



### PowerSO36 (SLUG UP)



7183931 G

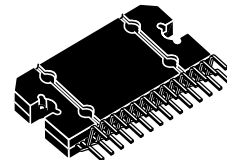
GAPGPS00098

Figure 40. Flexiwatt27 (vertical) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F <sup>(1)</sup>			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	25.75	26.00	26.25	1.014	1.023	1.033
H <sup>(2)</sup>	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L <sup>(2)</sup>	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 <sup>(2)</sup>	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included; (2): molding protusion included.

### OUTLINE AND MECHANICAL DATA



### Flexiwatt27 (vertical)

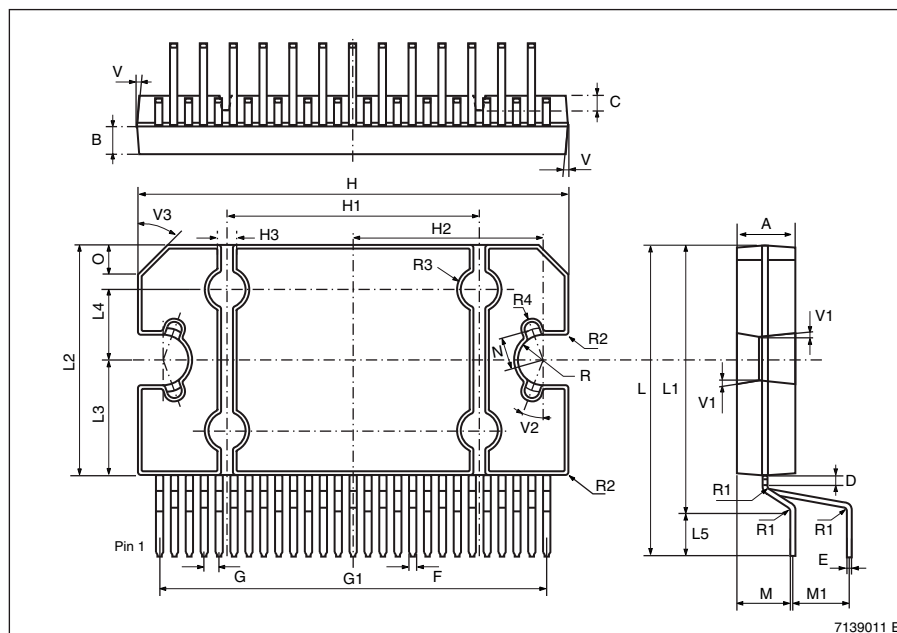
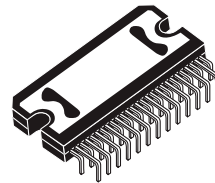


Figure 41. Flexiwatt27 (horizontal) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D		2.00			0.079	
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.75	1.00	1.25	0.0295	0.040	0.0492
G1	25.70	26.00	26.30	1.0118	1.023	1.0354
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	21.64	22.04	22.44	0.852	0.868	0.883
L1	10.15	10.5	10.85	0.40	0.413	0.427
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5	5.15	5.45	5.85	0.203	0.214	0.23
L6	1.80	1.95	2.10	0.070	0.077	0.083
M	2.75	3.00	3.50	0.108	0.118	0.138
M1		4.73			0.186	
M2		5.61			0.220	
N		2.20			0.086	
P	3.20	3.50	3.80	0.126	0.138	0.15
R		1.70			0.067	
R1		0.50			0.02	
R2		0.30			0.12	
R3		1.25			0.049	
R4		0.50			0.02	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included; (2): molding protusion included

### OUTLINE AND MECHANICAL DATA



### Flexiwatt27 (Horizontal)

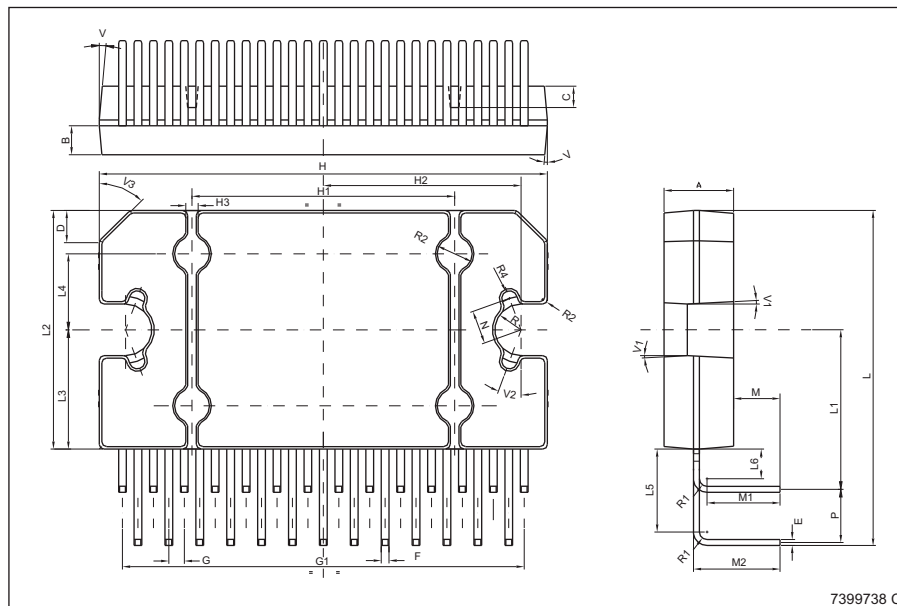
7399738 C  
GAPGPS00095

Figure 42. Flexiwatt27 (SMD) mechanical data and package dimensions

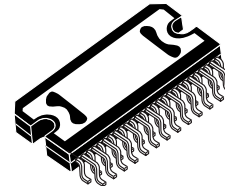
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.1752	0.1772	0.1831
B	2.12	2.22	2.32	0.0835	0.0874	0.0913
C		1.40			0.0551	
D		2.00			0.0787	
E	0.36	0.40	0.44	0.0142	0.0157	0.0173
F(**)	0.47	0.51	0.57	0.0185	0.0201	0.0224
G(**)	0.75	1.00	1.25	0.0295	0.0394	0.0492
G1	25.70	26.00	26.30	1.0118	1.0236	1.0354
G2(**)	1.75	2.00	2.25	0.0689	0.0787	0.0886
H(**)	28.85	29.23	29.40	1.1358	1.1508	1.1575
H1		17.00			0.6693	
H2		12.80			0.5039	
H3		0.80			0.0315	
L(**)	15.50	15.70	15.90	0.6102	0.6181	0.6260
L1	7.70	7.85	7.95	0.3031	0.3091	0.3130
L2	14.00	14.20	14.40	0.5512	0.5591	0.5669
L3	11.80	12.00	12.20	0.4646	0.4724	0.4803
L4	1.30	1.48	1.66	0.0512	0.0583	0.0654
L5	2.42	2.50	2.58	0.0953	0.0984	0.1016
L6	0.42	0.50	0.58	0.0165	0.0197	0.0228
M		1.50			0.0591	
N		2.20			0.0866	
N1	1.30	1.48	1.66	0.0512	0.0583	0.0654
N2(**)	2.73	2.83	2.93	0.1075	0.1114	0.1154
P(**)	4.73	4.83	4.93	0.1862	0.1902	0.1941
R		1.70			0.0669	
R1		0.30			0.0118	
R2	0.35	0.40	0.45	0.0138	0.0157	0.0177
R3	0.35	0.40	0.45	0.0138	0.0157	0.0177
R4		0.50			0.0197	
T(**)	-0.08		0.10	-0.0031		0.0039
aaa(**)		0.1			0.0039	
V		45°			45°	
V1		3°			3°	
V2	3°	5°	7°	3°	5°	7°
V3	12°	15°	18°	12°	15°	18°
V4		5°			5°	
V5		20°			20°	

(\*) Golden parameters

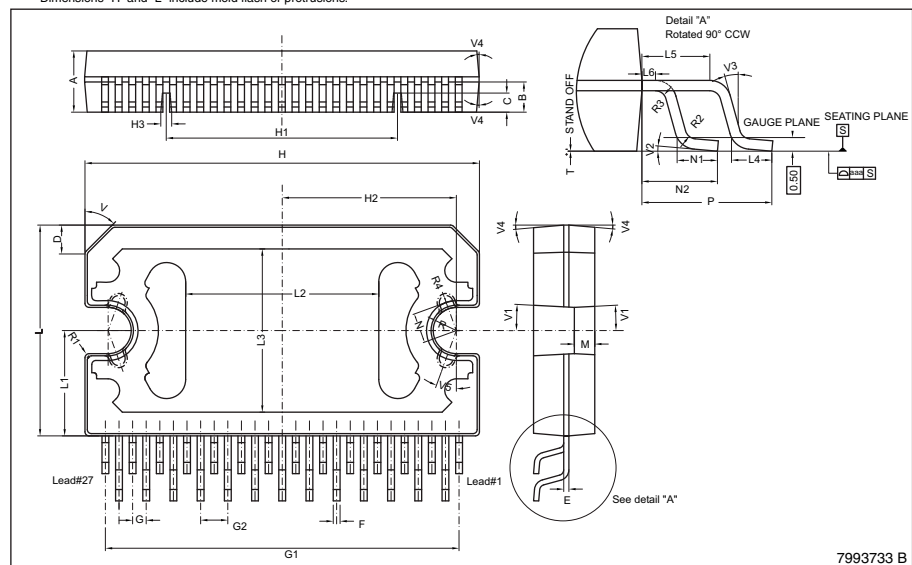
(\*\*) – Dimension "F" doesn't include dam-bar protrusion.

– Dimensions "H" and "L" include mold flash or protrusions.

### OUTLINE AND MECHANICAL DATA



### Flexiwatt27 (SMD)



7993733 B

GAPGPS00097

## 11 Revision history

**Table 21. Document revision history**

Date	Revision	Changes
13-Feb-2012	1	Initial release.
11-Dec-2012	2	Corrected typeset error of the "a1" dimension on the <a href="#">Figure 39: PowerSO36 (slug-up) mechanical data and package dimensions on page 43</a> .
26-Feb-2013	3	Updated <a href="#">Table 4: Absolute maximum ratings on page 12</a> .
18-Sep-2013	4	Updated Disclaimer.

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