

N-channel 30 V, 0.0076 Ω typ., 48 A STripFET™ H5 Power MOSFET in an IPAK package

Datasheet - production data

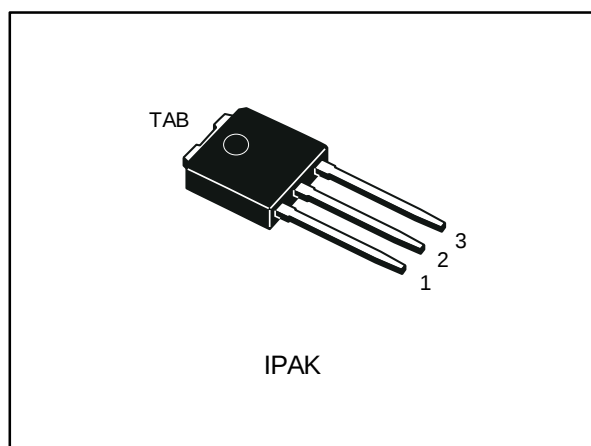
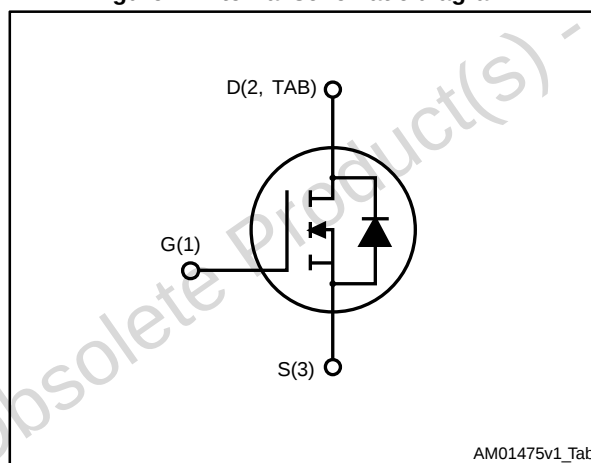


Figure 1: Internal schematic diagram



Features

Order code	$V_{DS}@ T_{jmax}$	$R_{DS(on)}$ max.	I_D
STU60N3LH5	35 V	0.0084 Ω	48 A

- Low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™ H5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Table 1: Device summary

Order code	Marking	Package	Packing
STU60N3LH5	60N3LH5	IPAK	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{DS}	Drain-source voltage @ T_{jmax}	35	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	48	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	42.8	A
$I_{DM}^{(2)}$	Drain current (pulsed)	192	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	60	W
	Derating factor	0.4	W/ $^{\circ}\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	160	mJ
T_J	Operating junction temperature range	-55 to 175	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		

Notes:⁽¹⁾Limited by wire bonding.⁽²⁾Pulse width limited by safe operating area.⁽³⁾Starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = 24\text{ A}$, $V_{DD} = 12\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.5	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	100	

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Table 4: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}; T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			10	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	1.8	3	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 24\text{ A}$		0.0076	0.0084	Ω
		$V_{GS} = 5\text{ V}, I_D = 24\text{ A}$		0.0092	0.0114	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	1350	1620	pF
C_{oss}	Output capacitance		-	265	318	pF
C_{rss}	Reverse transfer capacitance		-	32	38	pF
Q_g	Total gate charge	$V_{DD} = 15\text{ V}, I_D = 48\text{ A}, V_{GS} = 5\text{ V},$ (see Figure 14: "Test circuit for gate charge behavior")	-	8.8	12.3	nC
Q_{gs}	Gate-source charge		-	4.7	6.6	nC
Q_{gd}	Gate-drain charge		-	2.2	3.1	nC
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0\text{ A}$	-	1.1	1.3	Ω

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 10\text{ V}, I_D = 24\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	6	-	ns
t_r	Rise time		-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	19	-	ns
t_f	Fall time		-	4.2	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		48	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		192	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 24\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 48\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 20\text{ V}$, (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	25		ns
Q_{rr}	Reverse recovery charge		-	18.5		μC
I_{RRM}	Reverse recovery current		-	1.5		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.2 Electrical characteristics (curves)

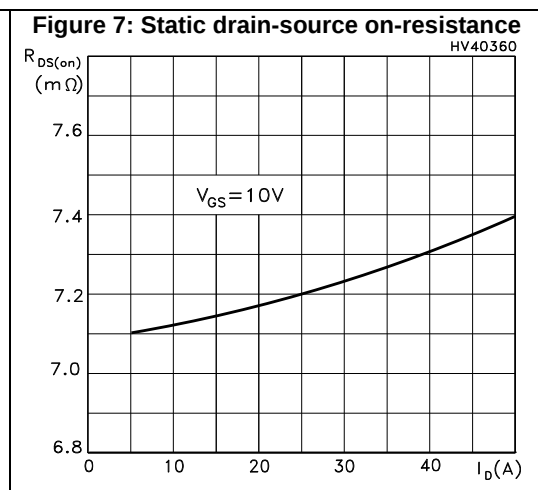
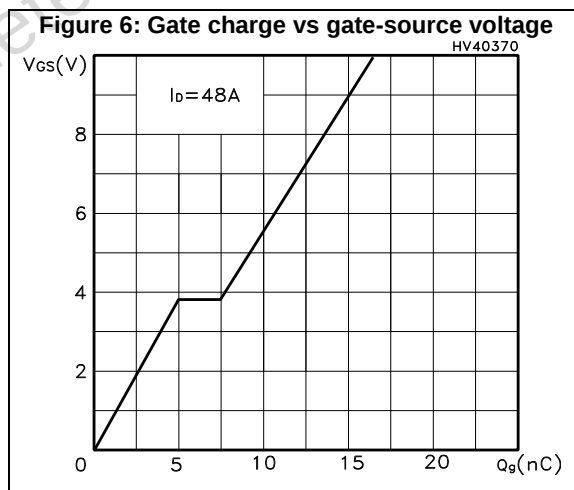
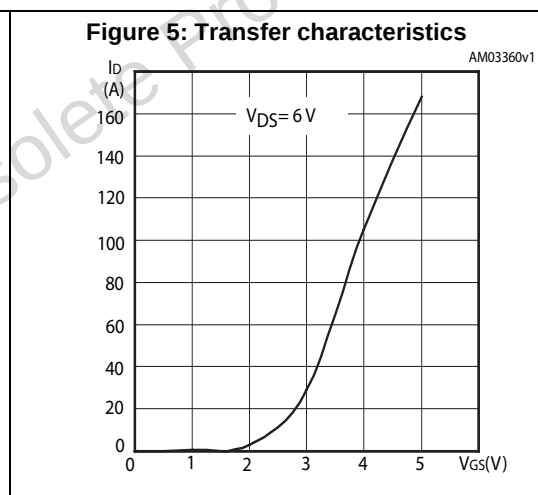
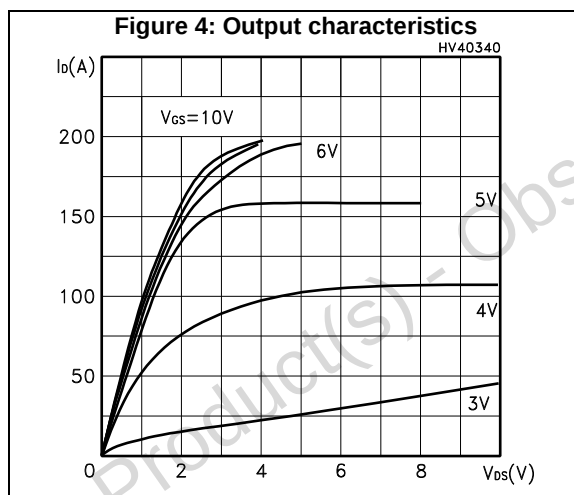
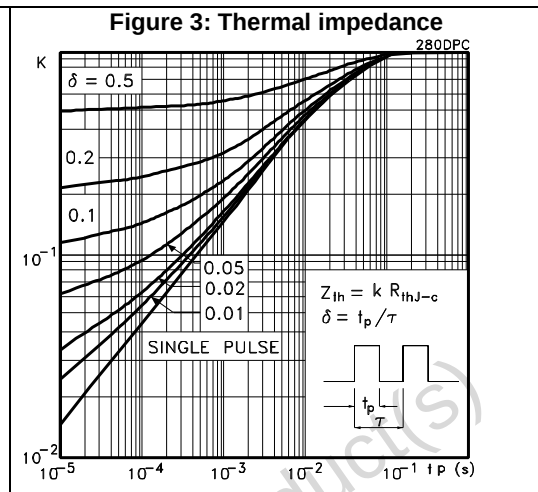
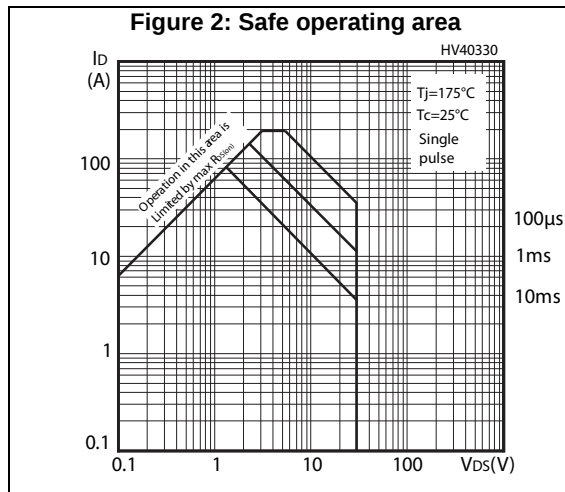


Figure 8: Capacitance variations

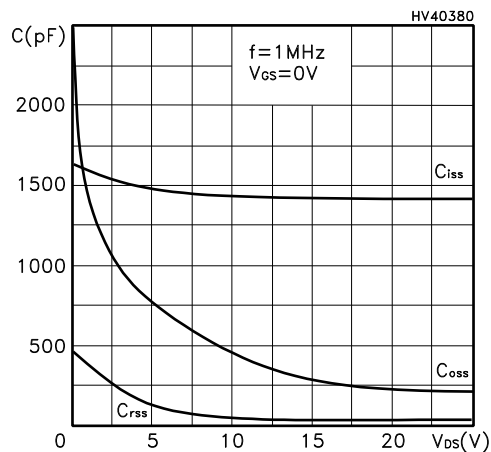


Figure 9: Normalized gate threshold voltage vs temperature

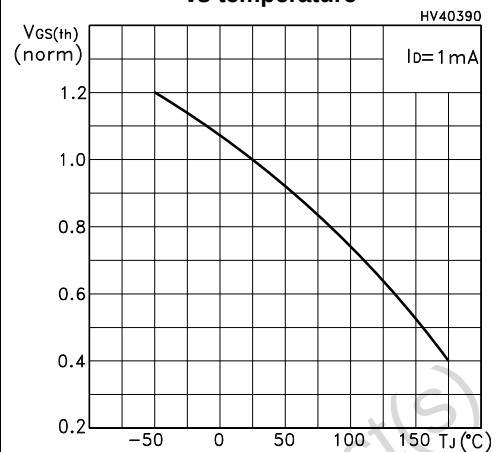


Figure 10: Normalized on-resistance vs temperature

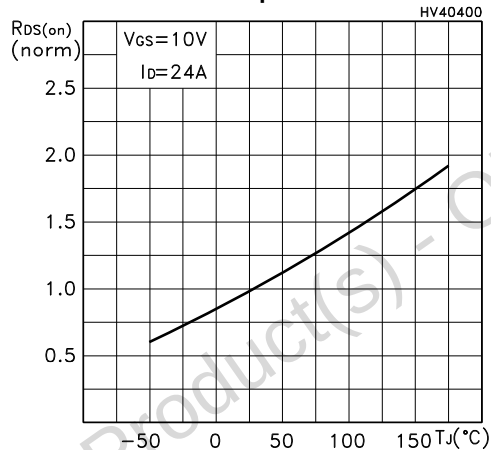
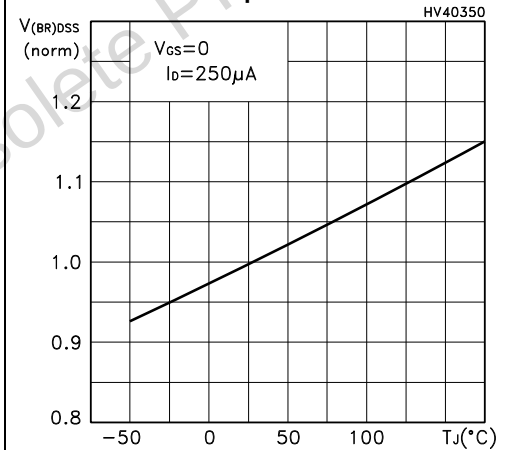
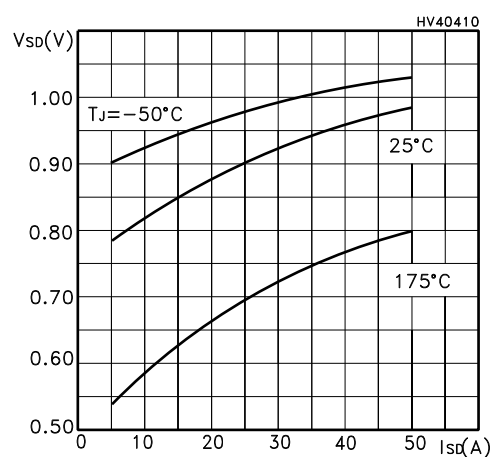
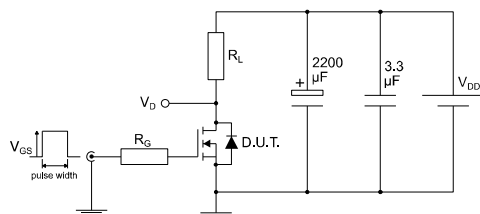
Figure 11: Normalized V_{(BR)DSS} vs temperature

Figure 12: Source-drain diode forward characteristics



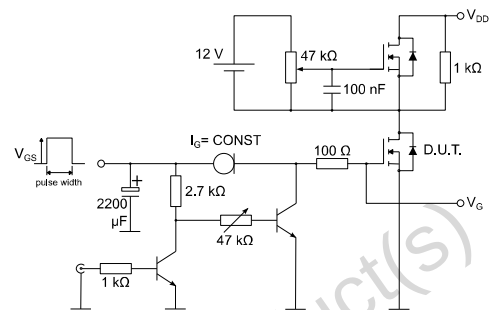
3 Test circuits

Figure 13: Test circuit for resistive load switching times



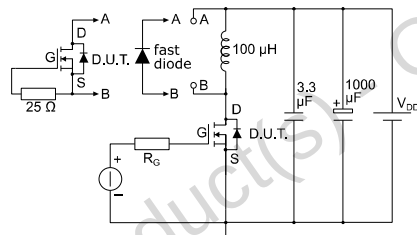
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Figure 14: Test circuit for gate charge behavior



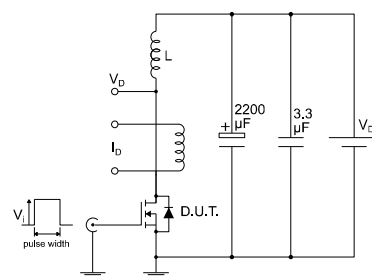
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Figure 15: Test circuit for inductive load switching and diode recovery times



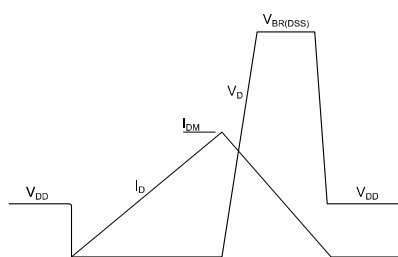
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Figure 16: Unclamped inductive load test circuit



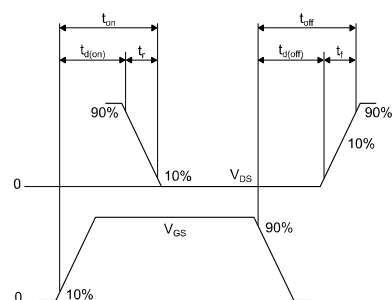
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 IPAK package information

Figure 19: IPAK (TO-251) type A package outline

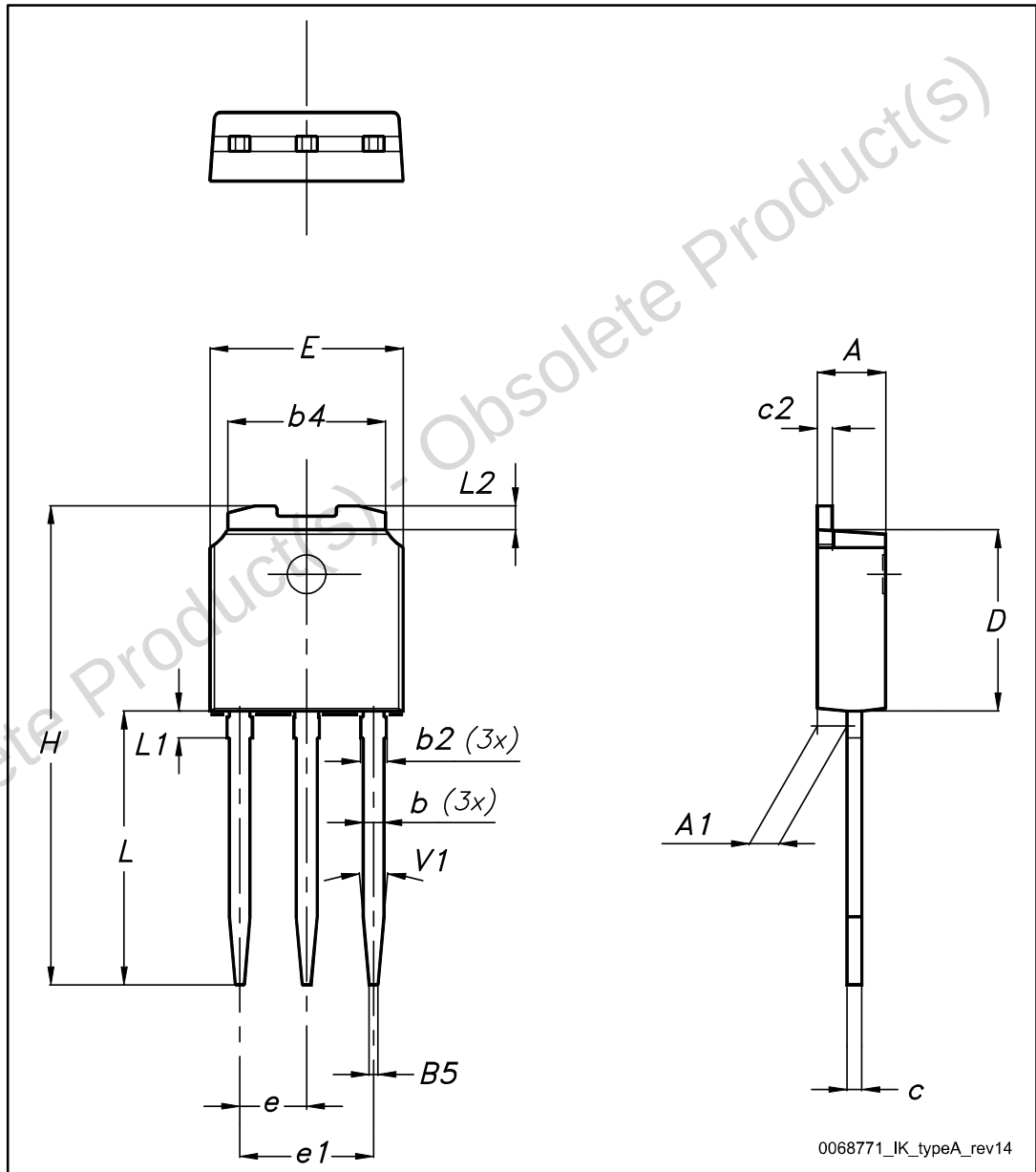


Table 8: IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
09-Jun-2016	1	Initial release.

Obsolete Product(s) - Obsolete Product(s)

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