



# STP70NS04ZC

N-channel clamped 8mΩ - 80A TO-220  
Fully protected SAFeFET™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP70NS04ZC	Clamped	< 10mΩ	80A

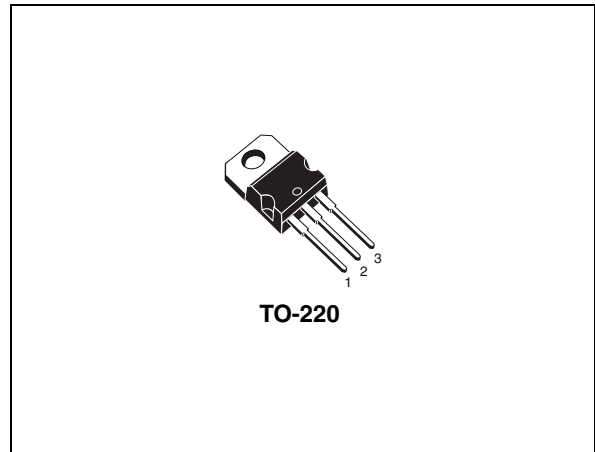
- Low capacitance and gate charge
- 100% avalanche tested
- 175°C maximum junction temperature

## Description

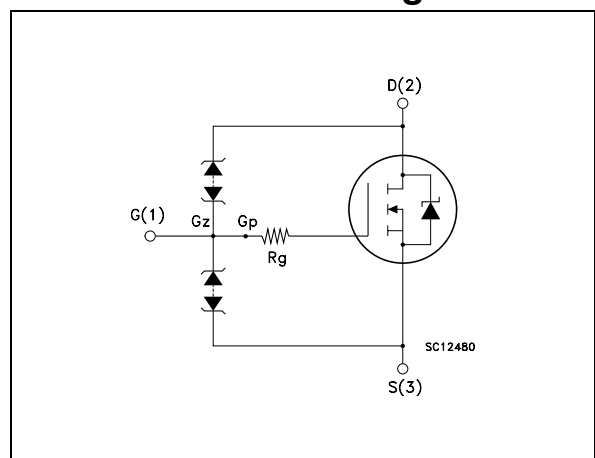
This fully clamped Power MOSFET is produced by using the latest advanced company's Mesh OVERLAY process which is based on a novel strip layout. The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encountered in the automotive environment. Any other application requiring extra ruggedness is also recommended.

## Applications

- Switching applications
  - ABS, solenoid drivers
  - Motor control
  - Dc-dc converters



## Internal schematic diagram



## Order code

Part number	Marking	Package	Packaging
STP70NS04ZC	P70NS04ZC	TO-220	Tube

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	33 <sup>(1)</sup>	V
$V_{DG}$	drain-gate voltage	33 <sup>(1)</sup>	V
$V_{GS}$	Gate-source voltage	$\pm 20$ <sup>(1)</sup>	V
$I_D$ <sup>(2)</sup>	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80	A
$I_D$ <sup>(2)</sup>	Drain current (continuous) at $T_C = 100^\circ\text{C}$	63	A
$I_{DG}$	Drain gate current (continuous)	$\pm 50$	A
$I_{GS}$	Gate-source current (continuous)	$\pm 50$	A
$I_{DM}$ <sup>(3)</sup>	Drain current (pulsed)	320	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	180	W
	Derating factor	1.2	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate-source ESD (HBM-C=100pF, R=1.5K $\Omega$ )	$\pm 8$	kV
$V_{ESD(G-D)}$	Gate-drain ESD (HBM-C=100pF, R=1.5K $\Omega$ )	$\pm 8$	kV
$V_{ESD(D-S)}$	Drain-source ESD (HBM-C=100pF, R=1.5K $\Omega$ )	$\pm 8$	kV
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Voltage is limited by zener diodes
2. Current limited by wire bonding
3. Pulse width limited by safe operating area

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.83	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
$T_I$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

**Table 3. Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	30	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{V}$ )	720	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DG}$	Clamped voltage	$I_D = 1\text{mA}$ , $V_{GS} = 0$	33			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 16\text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 10\text{V}$			2	$\mu\text{A}$
$V_{GSS}$	Gate-source breakdown voltage	$I_{GS} = \pm 100\mu\text{A}$	18			V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 1\text{mA}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$ , $I_D = 40\text{A}$		8	11	$\text{m}\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$ , $I_D = 30\text{A}$		35		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$ , $V_{GS} = 0$		1930 700 230		pF pF pF
$t_{r(Voff)}$ $t_f$ $t_c$	Off voltage rise time Fall time Cross-over time	$V_{CLAMP} = 32\text{V}$ , $I_D = 60\text{A}$ , $V_{GS} = 10\text{V}$ , $R_G = 4.7\Omega$ (see Figure 14)		110 90 140		ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 32\text{V}$ , $I_D = 60\text{A}$ $V_{GS} = 10\text{V}$ (see Figure 15)		58 14 26		nC nC nC
$R_G$	Internal gate resistor			14		$\Omega$

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				80 320	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=80A$ , $V_{GS}=0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=80A$ , $di/dt = 100A/\mu s$ , $V_{DD}= 30 V$ , $T_j=150^{\circ}C$ (see Figure 19)		90 0.18 4		ns $\mu C$ A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

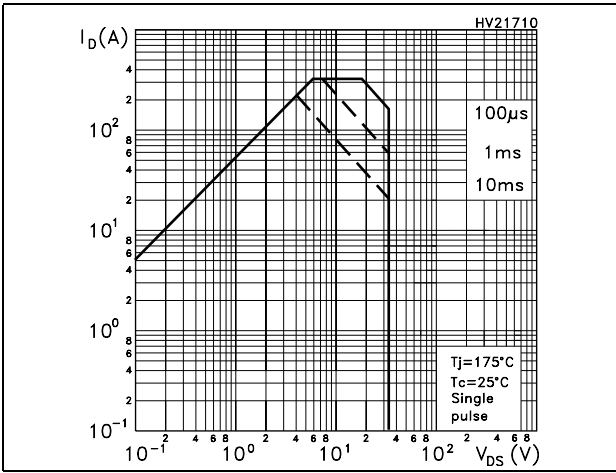


Figure 2. Thermal impedance

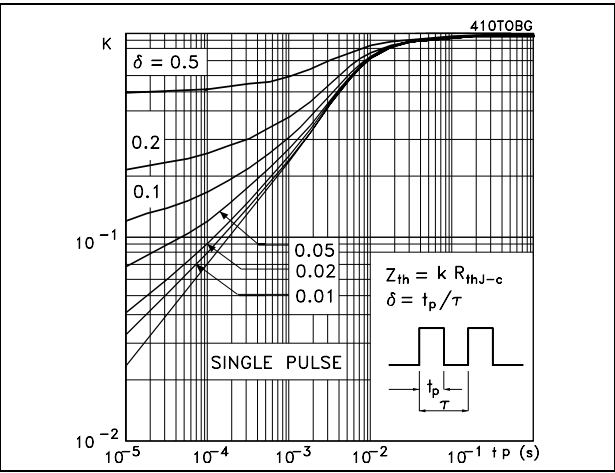


Figure 3. Output characteristics

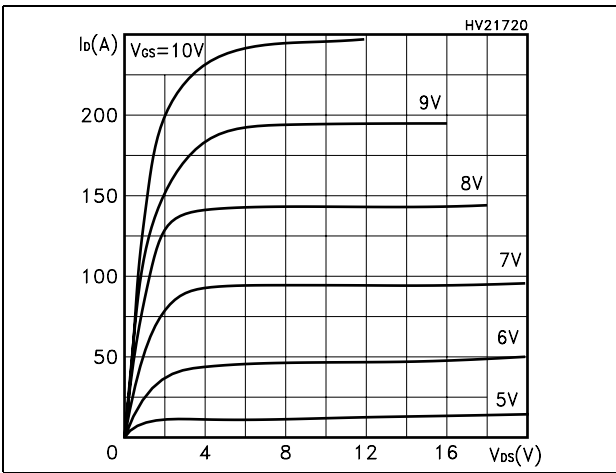


Figure 4. Transfer characteristics

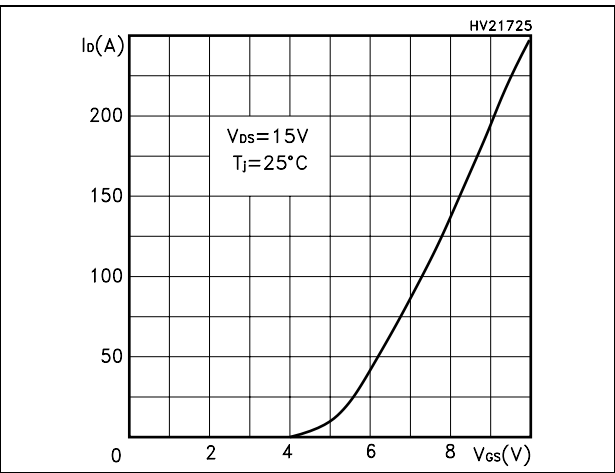


Figure 5. Transconductance

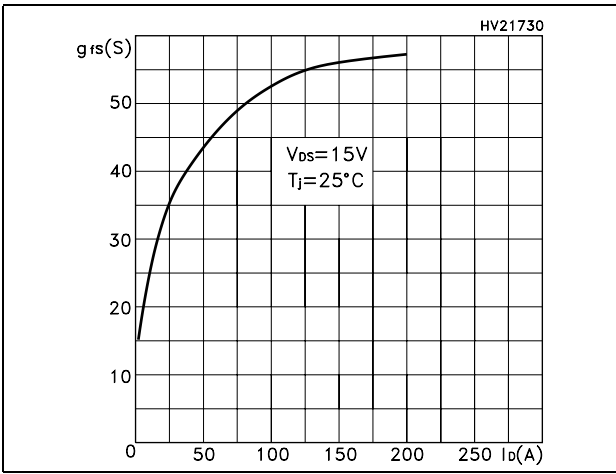


Figure 6. Static drain-source on resistance

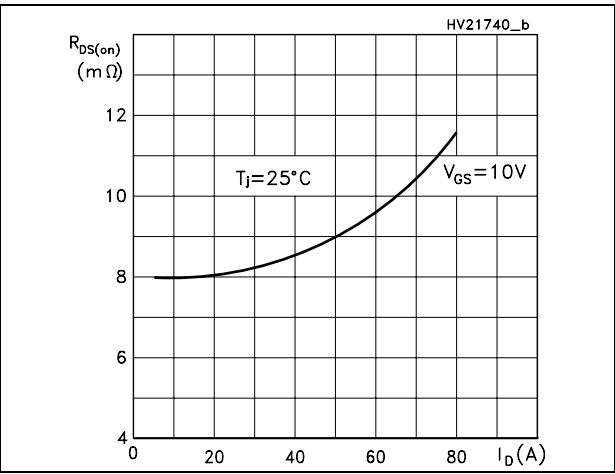


Figure 7. Gate charge vs gate-source voltage    Figure 8. Capacitance variations

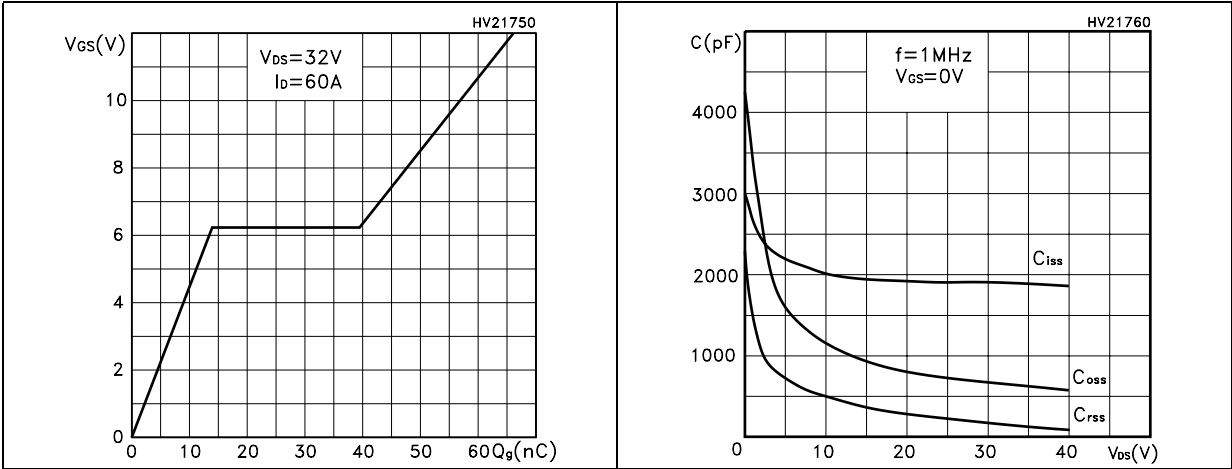


Figure 9. Normalized gate threshold voltage vs temperature    Figure 10. Normalized on resistance vs temperature

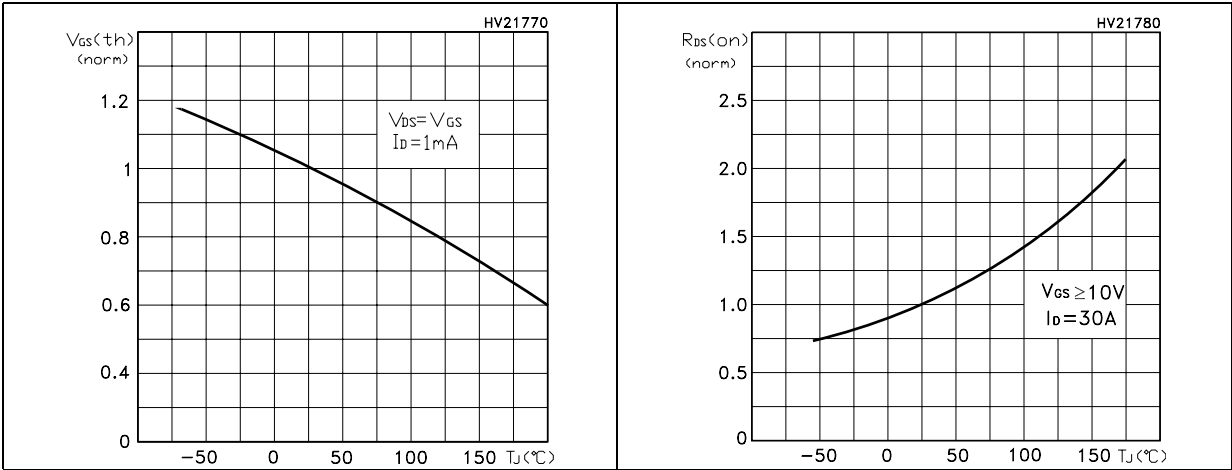
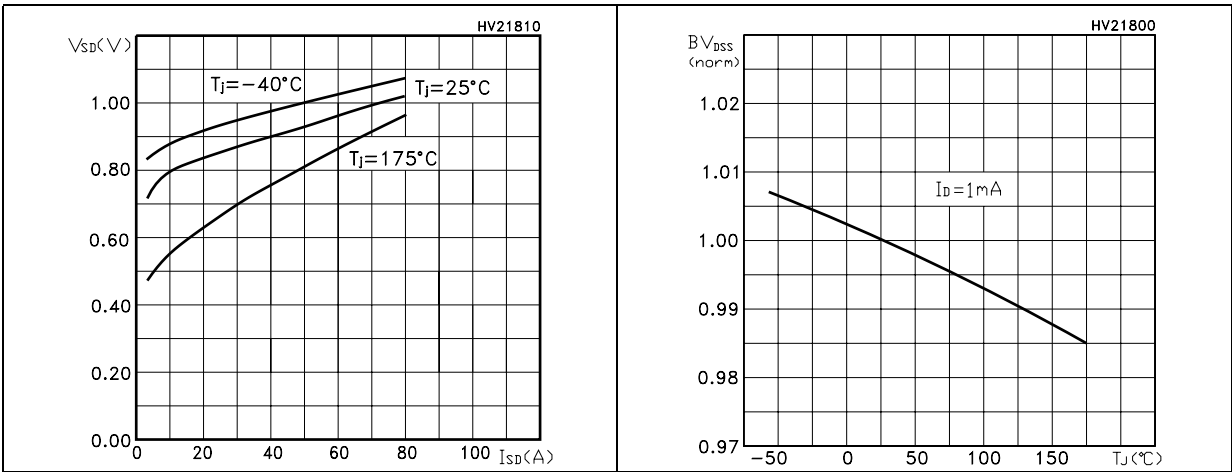
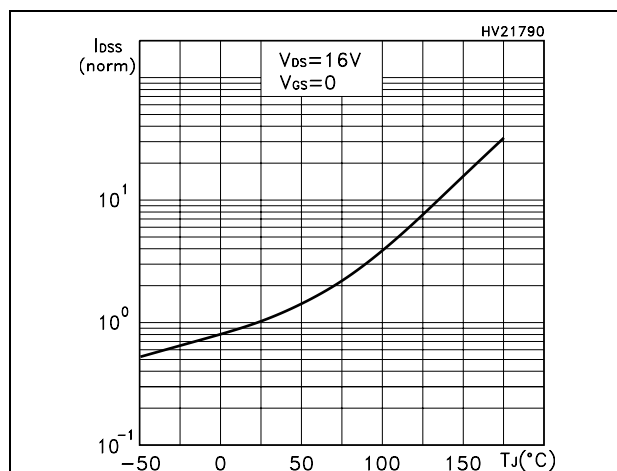


Figure 11. Source-drain diode forward characteristics    Figure 12. Normalized  $BV_{DSS}$  vs temperature

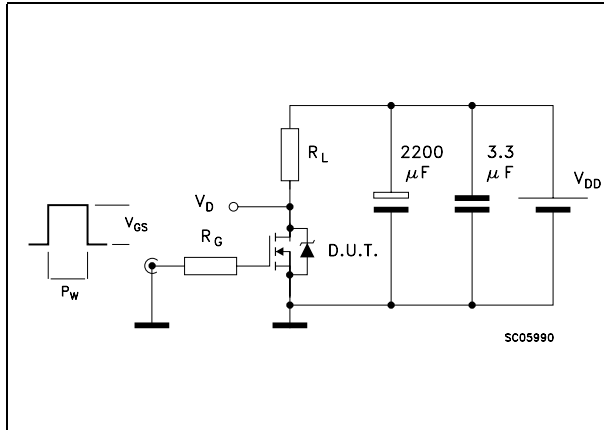


**Figure 13. Normalized  $I_{DSS}$  vs temperature**

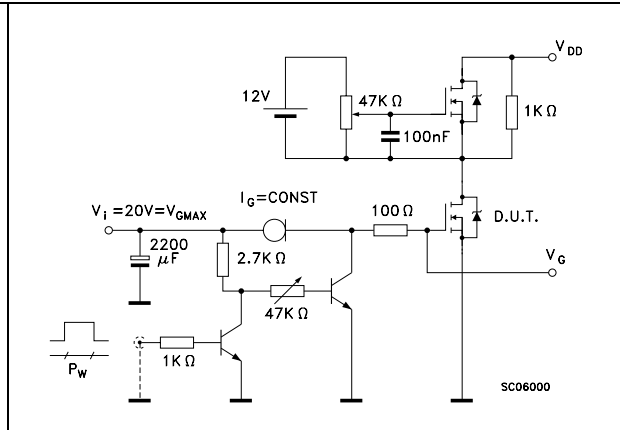


### 3 Test circuit

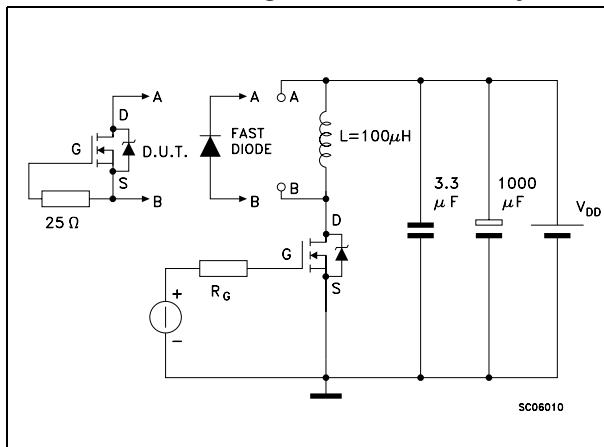
**Figure 14. Switching times test circuit for resistive load**



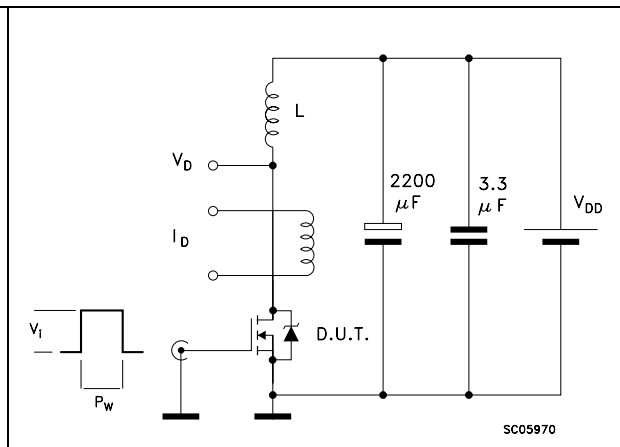
**Figure 15. Gate charge test circuit**



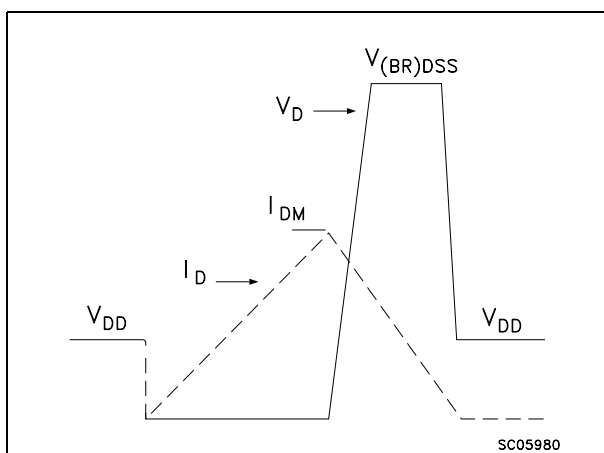
**Figure 16. Test circuit for inductive load switching and diode recovery times**



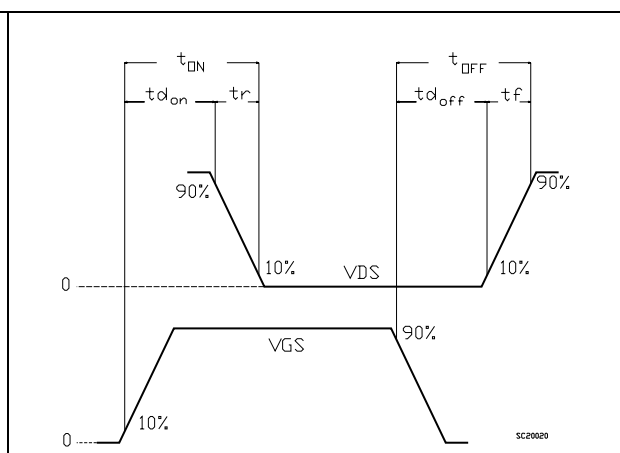
**Figure 17. Unclamped Inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



**Figure 19. Switching time waveform**

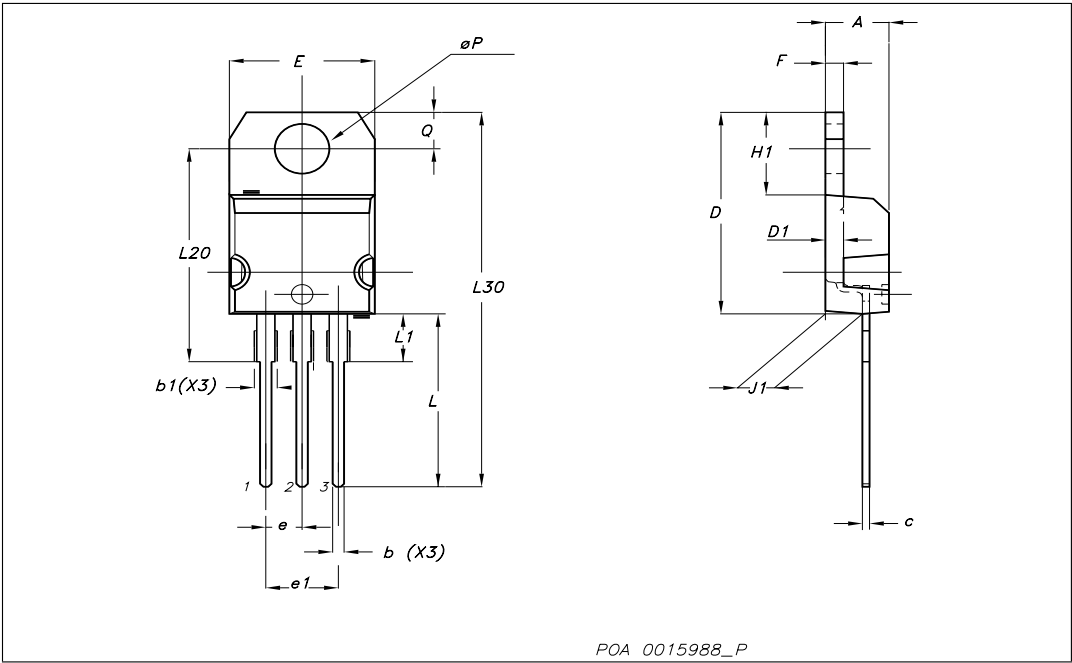


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



## 5 Revision history

**Table 7. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
04-May-2007	1	First release

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