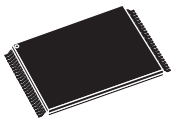
NAND128-A NAND256-A

128-Mbit or 256-Mbit, 528-byte/264-word page, 3 V, SLC NAND flash memories

Features

- High density NAND flash memories
  - Up to 256-Mbit memory array
  - Up to 32-Mbit spare area
  - Cost effective solutions for mass storage applications
- NAND interface
  - x8 or x16 bus width
  - Multiplexed address/ data
  - Pinout compatibility for all densities
- Supply voltage
  - V_{DD} = 2.7 to 3.6 V
- Page size
  - x8 device: (512 + 16 spare) bytes
  - x16 device: (256 + 8 spare) words
- Block size
  - x8 device: (16 K + 512 spare) bytes
  - x16 device: (8 K + 256 spare) words
- Page read/program
  - Random access: 12 µs (3V)/15 us (1.8V) (max)
  - Sequential access: 50 ns (min)
  - Page program time: 200 µs (typ)
- Copy back program mode
  - Fast page copy without external buffering
- Fast block erase
  - Block erase time: 2 ms (typical)
- Status register
- Electronic signature
- Chip enable 'don't care'
  - Simple interface with microcontroller
- Security features
  - OTP area
  - Serial number (unique ID)



TSOP48 12 x 20mm

VFBGA55 8 x 10 x 1.05mm

- Hardware data protection
  - Program/erase locked during power transitions
- Data integrity
  - 100,000 program/erase cycles
  - 10 years data retention
- RoHS compliance
  - Lead-free components are compliant with the RoHS directive
- Development tools
  - Error correction code software and hardware models
  - Bad blocks management and wear leveling algorithms
  - File system OS native reference software
  - Hardware simulation models

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1 Description

The NAND flash 528 byte/ 264 word page is a family of non-volatile flash memories that uses the single level cell (SLC) NAND cell technology, referred to as the SLC small page family. The devices are either 128 Mbits or 256 Mbits and operate with a 3 V voltage supply. The size of a page is either 528 bytes (512 + 16 spare) or 264 words (256 + 8 spare) depending on whether the device has a x8 or x16 bus width.

The address lines are multiplexed with the data input/output signals on a multiplexed x8 or x16 input/output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased up to 100,000 cycles. To extend the lifetime of NAND flash devices it is strongly recommended to implement an error correction code (ECC). A Write Protect pin is available to provide hardware protection against program and erase operations.

The devices feature an open-drain ready/busy output that identifies if the program/erase/read (P/E/R) controller is currently active. The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor.

A Copy Back command is available to optimize the management of defective blocks. When a page program operation fails, the data can be programmed in another page without having to resend the data to be programmed.

Table 1 lists the individual part numbers of the device.

Table 1. NAND128-A and NAND256-A device summary

Reference	Part Number
NAND128-A	NAND128W3A
NAND256-A(1)	NAND256W3A
	NAND256W4A

1. x16 organization only available for MCP.

The NAND128-A devices are only available in the TSOP48 (12 x 20 mm), while the NAND256-A devices are available in both the TSOP48 and the VFBGA55 (8 x 10 x 1.05 mm) packages.

The devices are available in two different versions:

- No option (Chip Enable ‘care’, sequential row read enabled): the sequential row read feature allows to download up to all the pages in a block with one read command and addressing only the first page to read
- With Chip Enable ‘don’t care’ feature. This enables the sharing of the bus between more active memories that are simultaneously active as Chip Enable transitions during latency do not stop read operations. Program and erase operations are not interrupted by Chip Enable transitions.

The devices come with the following security features:

- OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permanently. The access sequence and further details about this feature are subject to an NDA (non disclosure agreement)
- Serial number (unique identifier), which enables each device to be uniquely identified. It is subject to an NDA and is, therefore, not described in the datasheet.

For more details about these security features, contact your nearest Micron sales office.

For information on how to order these devices, refer to *Table 24: Ordering information scheme*. Devices are shipped from the factory with Block 0 always valid and the memory content bits in valid blocks erased to '1'.

See *Table 2* for all the devices available in the family.

Table 2. Product description

Reference	Part Number	Density	Bus Width	Page Size	Block Size	Memory Array	Operating Voltage	Timings				Package
								Rand Access Max	Seq Access Min	Page Program Typical	Block Erase Typical	
NAND128-A	NAND128W3A	128 Mbit	x8	512+16 Bytes	16K+512 Bytes	32 pages x 1024 Blocks	2.7 to 3.6V	12µs	50ns	200µs	2ms	TSOP48
NAND256-A(1)	NAND256W3A	256 Mbit	x8	512+16 Bytes	16K+512 Bytes	32 pages x 2048 Blocks						TSOP48 VFBGA55
	NAND256W4A		x16	256+8 Words	8K+256 Words							

1. x16 organization only available for MCP.

Figure 1. Logic diagram

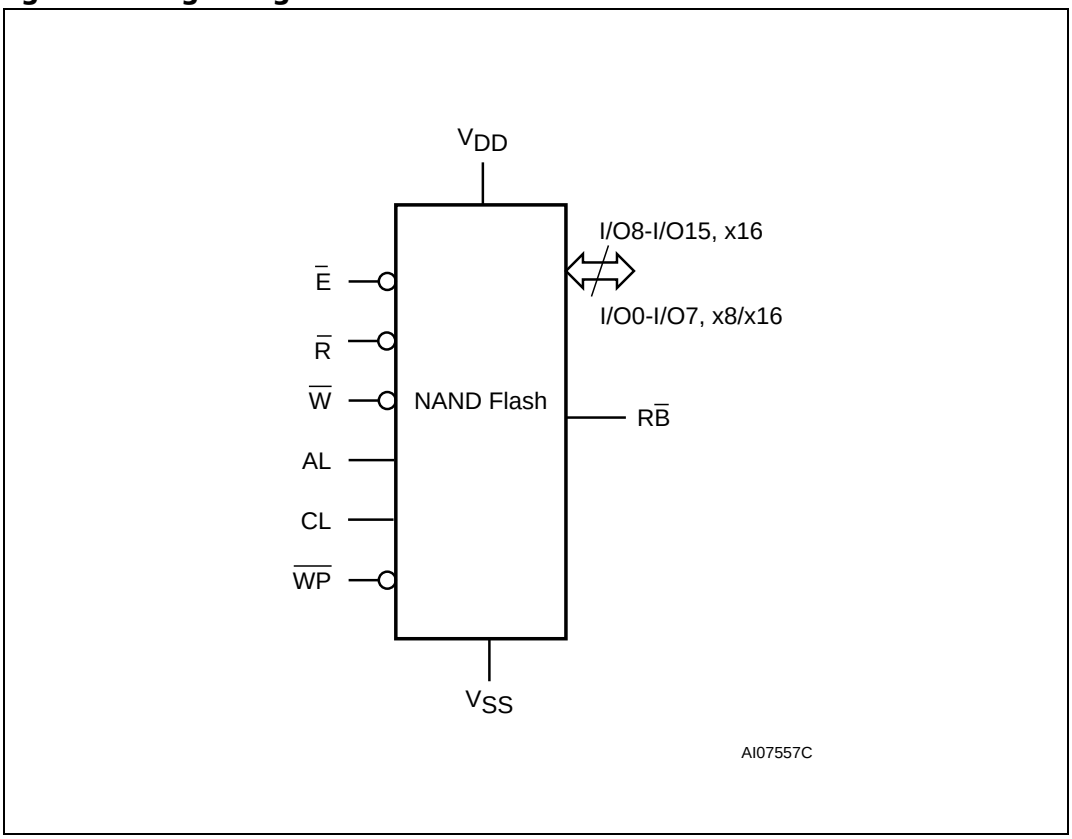


Table 3. Signal names

Symbol	Function
I/O8-15	Data input/outputs for x16 devices
I/O0-7	Data input/outputs, address inputs, or command inputs for x8 and x16 devices
AL	Address Latch Enable
CL	Command Latch Enable
E	Chip Enable
R	Read Enable
RB	Ready/Busy (open-drain output)
W	Write Enable
WP	Write Protect
V_{DD}	Supply voltage
V_{SS}	Ground
NC	Not connected internally
DU	Do not use

Figure 2. Logic block diagram

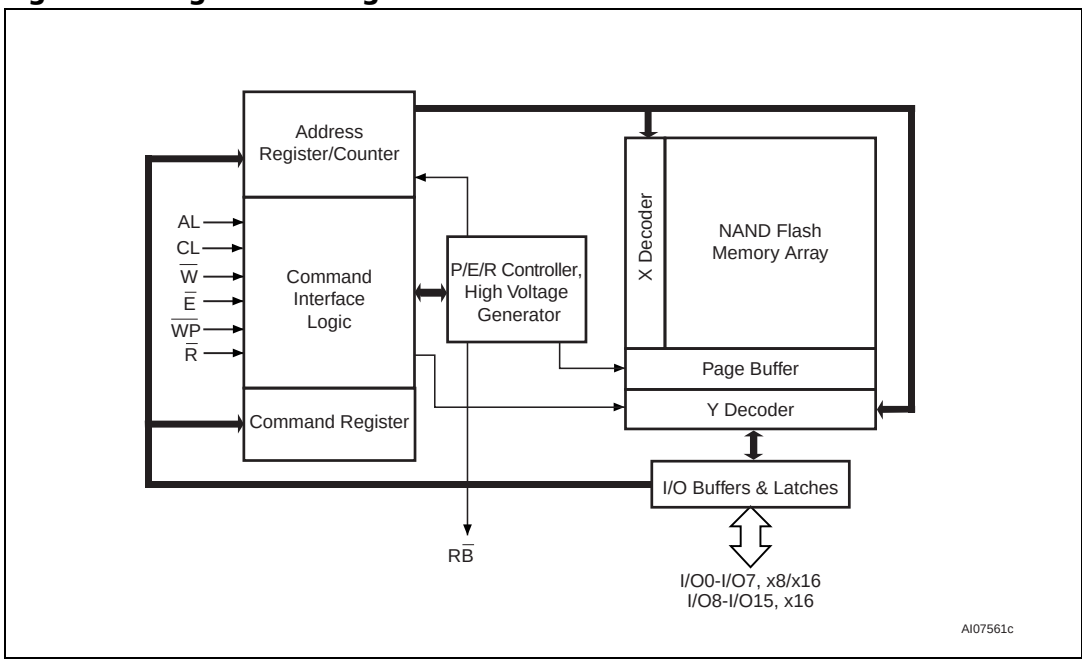
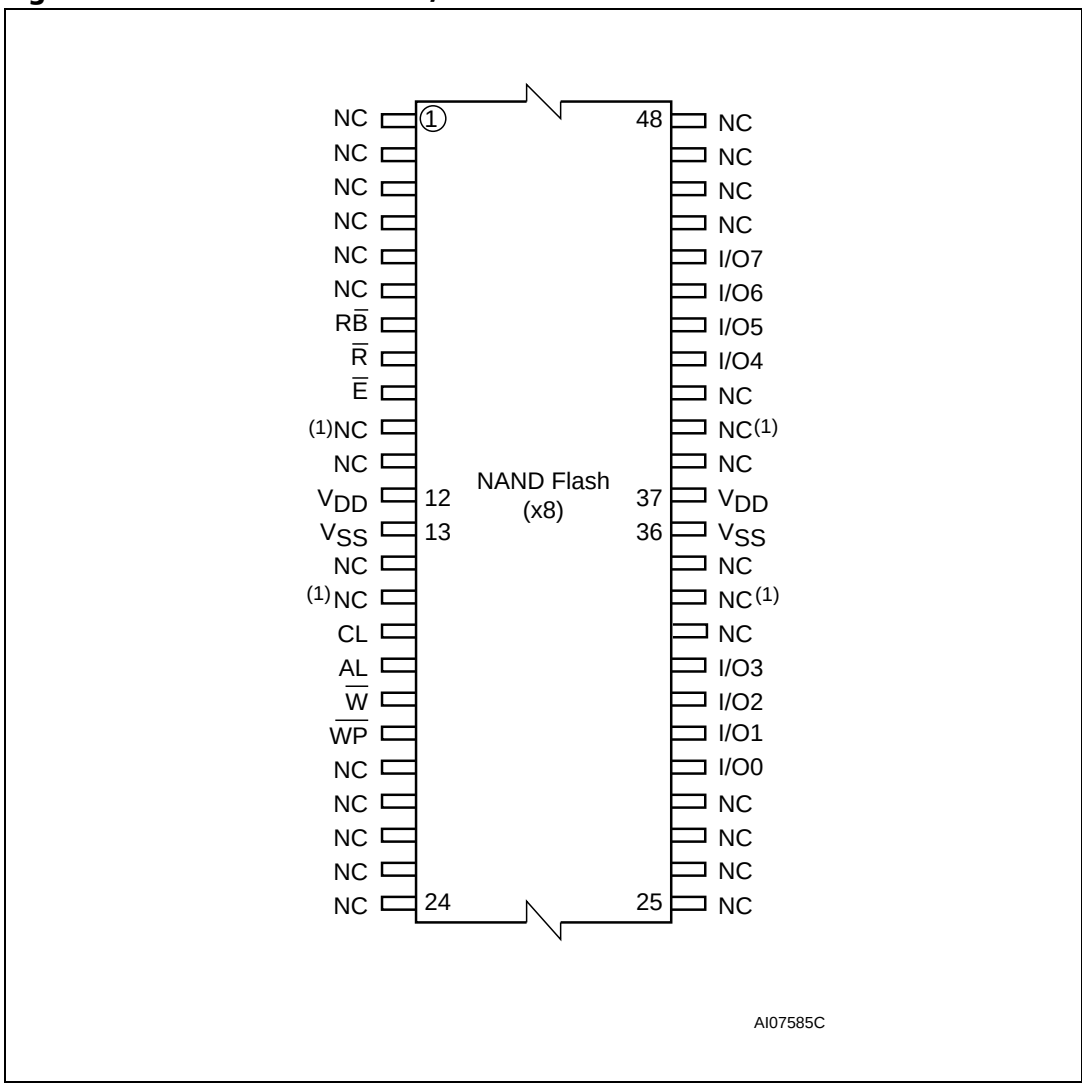
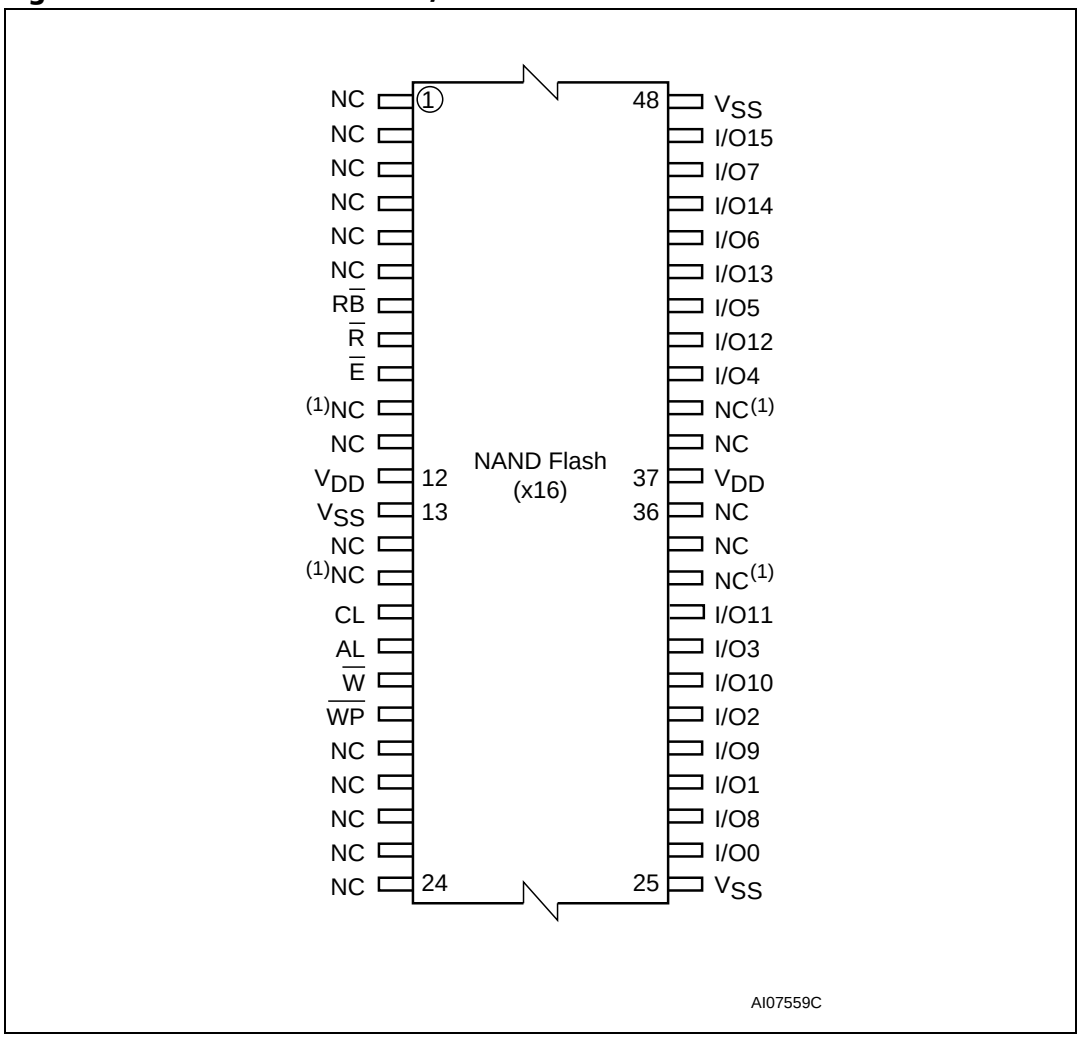


Figure 3. TSOP48 connections, x8 devices



1. This pin is DU in the USOP48 package

Figure 4. TSOP48 connections, x16 devices



1. This pin is DU in the USOP48 package.

Figure 5. VFBGA55 connections, x8 devices (top view through package)

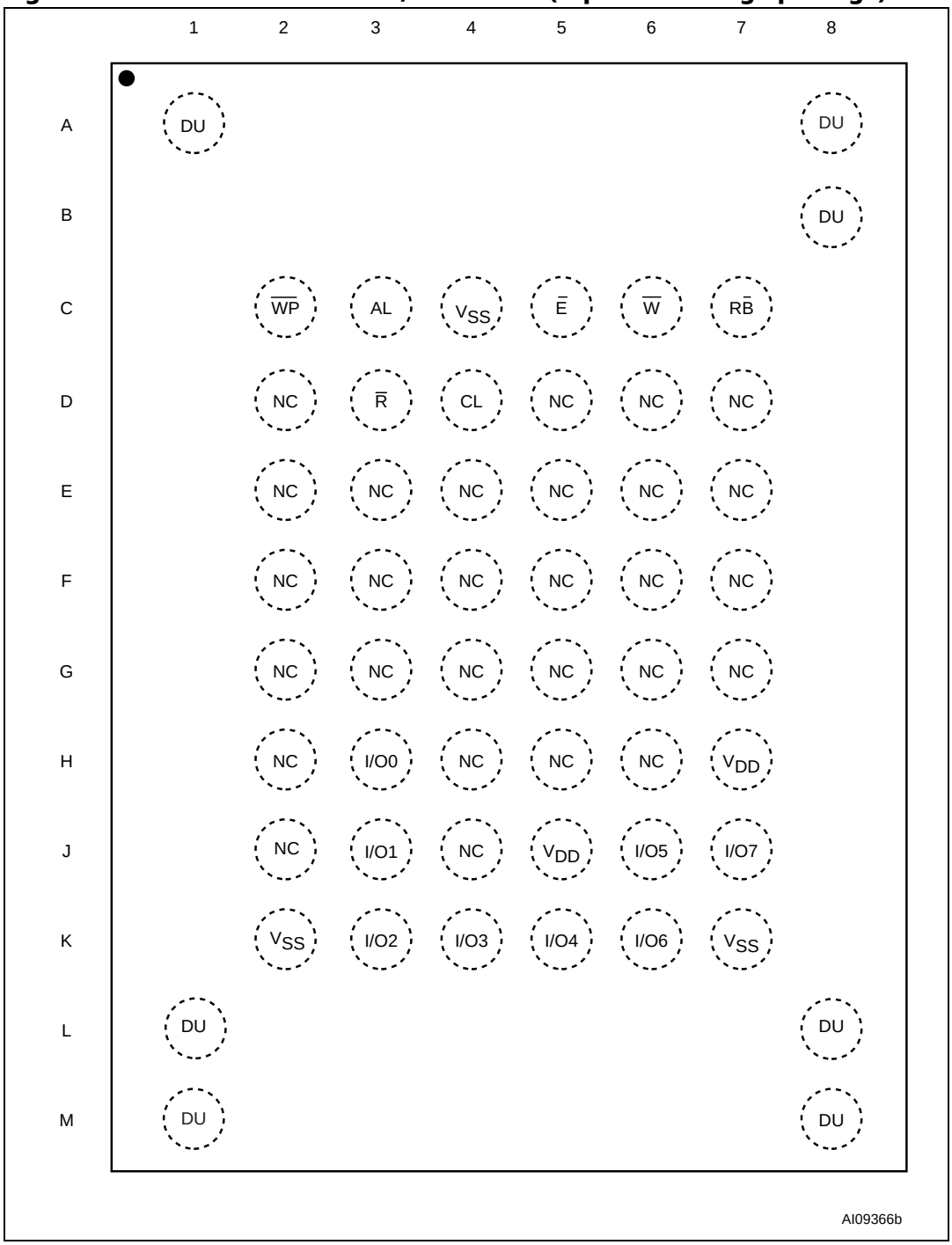
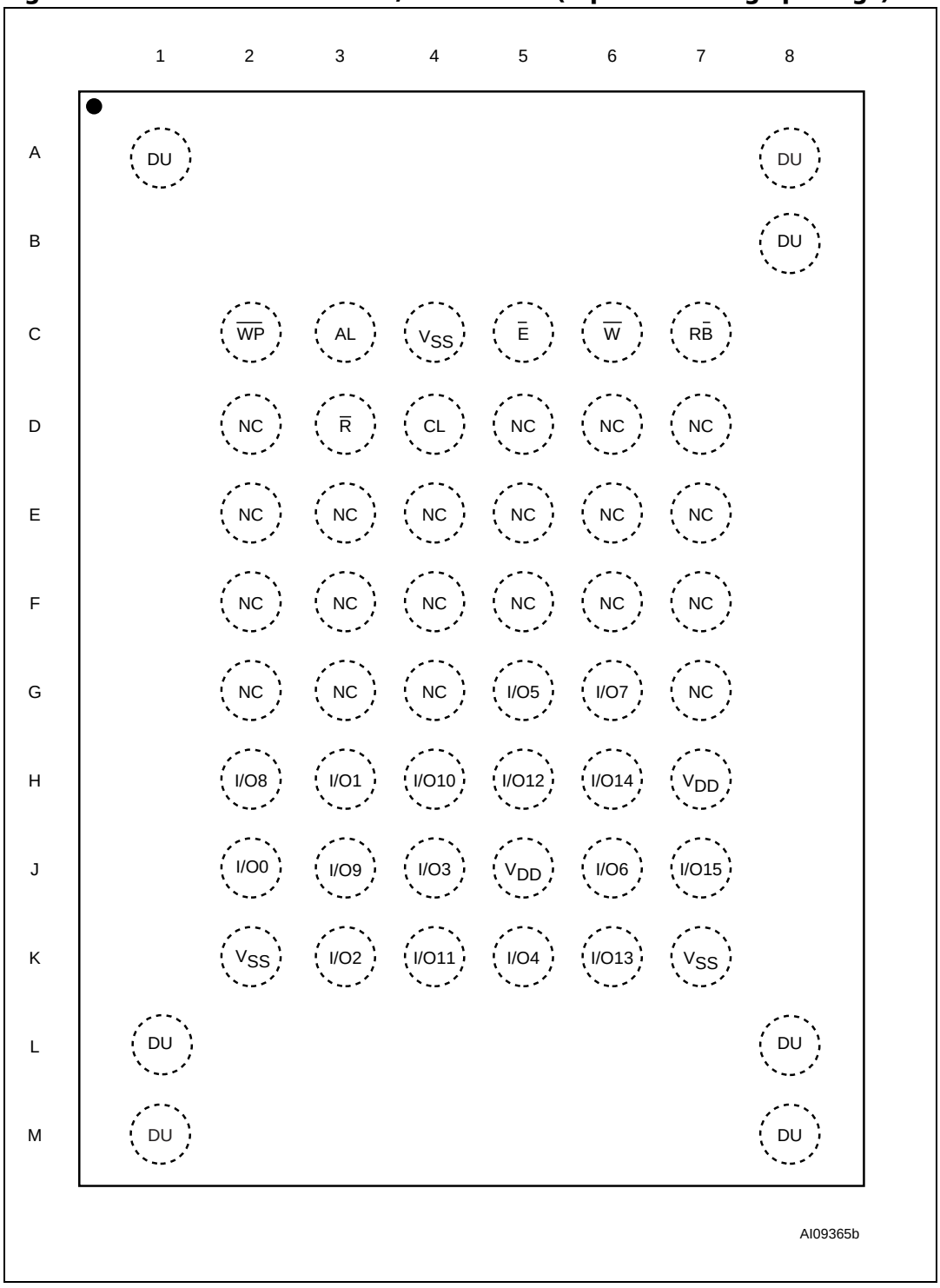


Figure 6. VFBGA55 connections, x16 devices (top view through package)



2 Memory array organization

The memory array comprises NAND structures where 16 cells are connected in series.

The memory array is organized in blocks where each block contains 32 pages. The array is split into two areas, the main area and the spare area. The main area of the array stores data, whereas the spare area is typically used to store error correction codes, software flags or bad block identification.

In x8 devices the pages are split into a main area with two half pages of 256 bytes each and a spare area of 16 bytes. In the x16 devices the pages are split into a 256-word main area and an 8-word spare area. Refer to *Figure 7: Memory array organization*.

2.1 Bad Blocks

The NAND flash 528 byte/ 264 word page devices may contain bad blocks, that is blocks that contain one or more invalid bits whose reliability is not guaranteed. Additional bad blocks may develop during the lifetime of the device.

The bad block information is written prior to shipping (refer to *Section 2.1: Bad Blocks* for more details).

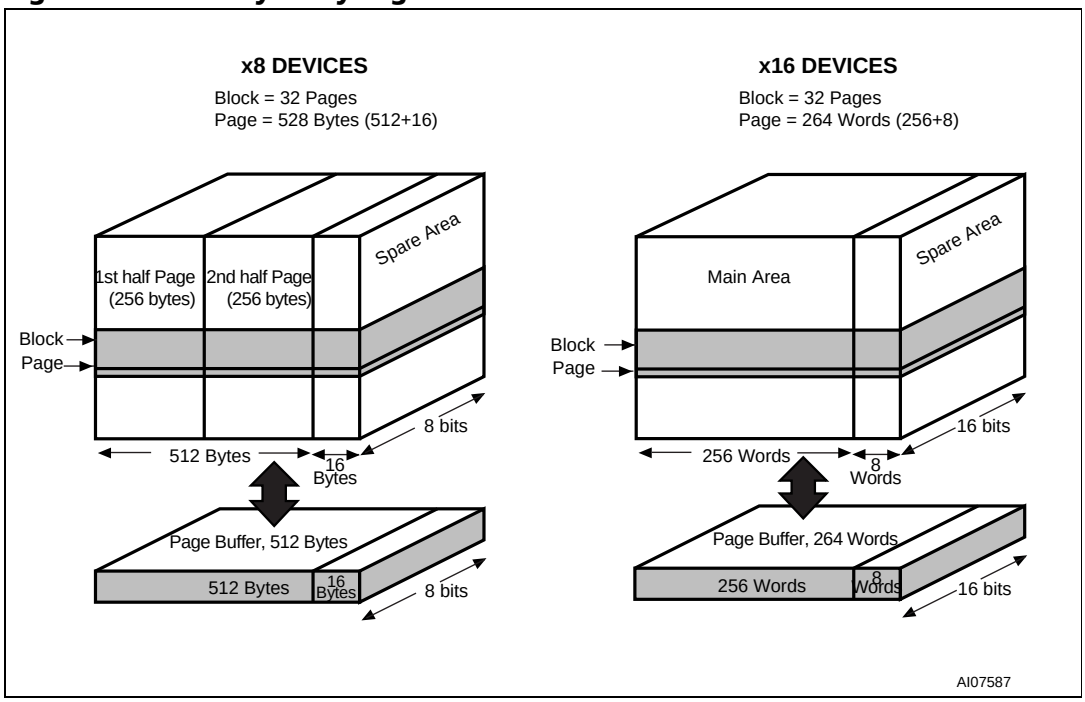
Table 4 shows the minimum number of valid blocks in each device. The values shown include both the bad blocks that are present when the device is shipped and the bad blocks that could develop later on.

These blocks need to be managed using bad blocks management, block replacement or error correction codes (refer to *Section 7: Software algorithms*).

Table 4. Valid blocks

Density of device	Minimum	Maximum
256 Mbits	2008	2048
128 Mbits	1004	1024

Figure 7. Memory array organization



3 Signal descriptions

See *Figure 1: Logic diagram* and *Table 3: Signal names* for a brief overview of the signals connected to this device.

3.1 Inputs/outputs (I/O0-I/O7)

Input/Outputs 0 to 7 input the selected address, output the data during a read operation or input a command or data during a write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Inputs/outputs (I/O8-I/O15)

Input/outputs 8 to 15 are only available in x16 devices. They output the data during a read operation or input data during a write operation. Command and address inputs only require I/O0 to I/O7.

The inputs are latched on the rising edge of Write Enable. I/O8-I/O15 are left floating when the device is deselected or the outputs are disabled.

3.3 Address Latch Enable (AL)

Address Latch Enable activates the latching of the address inputs in the command interface. When AL is high, the inputs are latched on the rising edge of Write Enable.

3.4 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the command inputs in the command interface. When CL is high, the inputs are latched on the rising edge of Write Enable.

3.5 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and read circuitry. When Chip Enable is low, V_{IL}, the device is selected. If Chip Enable goes High (V_{IH}) while the device is busy, the device remains selected and does not go into standby mode.

3.6 Read Enable ($\overline{R}$)

Read Enable, $\overline{R}$, controls the sequential data output during read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.7 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10µs (min) is required before the Command Interface is ready to accept a command. It is recommended to keep Write Enable high during the recovery time.

3.8 Write Protect ($\overline{WP}$)

The Write Protect pin is an input that provides hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.9 Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that can be used to identify if the P/E/R controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low then indicates that one or more of the memories is busy.

Refer to the *Section 10.1: Ready/busy signal electrical characteristics* for details on how to calculate the value of the pull-up resistor.

3.10 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever V_{DD} is below the V_{LKO} threshold (see paragraph *Figure 35: Data protection*) to protect the device from any involuntary program/erase operations durings power-transitions.

Each device in a system should have V_{DD} decoupled with a 0.1 µF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents

3.11 V_{SS} ground

Ground, V_{SS}, is the reference for the power supply. It must be connected to the system ground.

4 Bus operations

There are six standard bus operations that control the memory. Each of these is described in this section, see *Table 5: Bus operations* for a summary.

4.1 Command input

Command input bus operations give commands to the memory. Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low, and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 input commands.

See *Figure 21: Command latch AC waveforms* and *Table 14: Program, erase times and program erase endurance cycles* for details of the timings requirements.

4.2 Address input

Address input bus operations input the memory address. Three bus cycles are required to input the addresses (refer to Tables *Table 6: Address insertion, x8 devices* and *Table 7: Address insertion, x16 device*).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low, and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Only I/O0 to I/O7 input addresses.

See *Figure 22: Address latch AC waveforms* and *Table 14: Program, erase times and program erase endurance cycles* for details of the timings requirements.

4.3 Data input

Data input bus operations input the data to be programmed.

Data is accepted only when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low, and Read Enable is High. The data is latched on the rising edge of the Write Enable signal and is input sequentially using the Write Enable signal.

See *Figure 23: Data input latch AC waveforms* and *Table 14: Program, erase times and program erase endurance cycles* and *Table 21: AC characteristics for operations* for details of the timings requirements.

4.4 Data output

Data output bus operations read the data in the memory array, the status register, the electronic signature, and the serial number.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low.

The data is output sequentially using the Read Enable signal.

See *Figure 24: Sequential data output after read AC waveforms* and *Table 21: AC characteristics for operations* for details of the timings requirements.

4.5 Write protect

Write protect bus operations protect the memory against program or erase operations. When the Write Protect signal is Low the device does not accept program or erase operations, therefore, the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection, even during power-up.

4.6 Standby

When Chip Enable is High the memory enters standby mode: the device is deselected, outputs are disabled and power consumption is reduced.

Table 5. Bus operations

Bus operation	E	AL	CL	R	W	WP	I/O0 - I/O7	I/O8 - I/O15(1)
Command input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(2)	Command	X
Address input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address	X
Data input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	X	Data input	Data input
Data output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data output	Data output
Write protect	X	X	X	X	X	V_{IL}	X	X
Standby	V_{IH}	X	X	X	X	X	X	X

1. Only for x16 devices.
2. $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 6. Address insertion, x8 devices(1) (2)

Bus Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	A16	A15	A14	A13	A12	A11	A10	A9
3rd	A24	A23	A22	A21	A20	A19	A18	A17

1. A8 is set Low or High by the 00h or 01h command (see *Section 6.1: Pointer operations*)
2. Any additional address input cycles are ignored.

Table 7. Address insertion, x16 device(1) (2) (3)

Bus Cycle	I/O8-I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	X	A7	A6	A5	A4	A3	A2	A1	A0
2nd	X	A16	A15	A14	A13	A12	A11	A10	A9
3rd	X	A24	A23	A22	A21	A20	A19	A18	A17

1. A8 is 'don't care' in x16 devices.
2. Any additional address input cycles are ignored.
3. The 01h command is not used in x16 devices

Table 8. Address definitions

Address	Definition
A0 - A7	Column address
A9 - A26	Page address
A9 - A13	Address in block
A14 - A26	Block address
A8	A8 is set Low or High by the 00h or 01h command, and is 'don't care' in x16 devices

5 Command set

All bus write operations to the device are interpreted by the command interface. The commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is high. Device operations are selected by writing specific commands to the command register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The commands are summarized in *Table 9*.

Table 9. Commands

Command	Bus write operations(1) (2)			Command accepted during busy
	1st cycle	2nd cycle	3rd cycle	
Read A	00h	-	-	
Read B	01h(2)	-	-	
Read C	50h	-	-	
Read Electronic Signature	90h	-	-	
Read Status Register	70h	-	-	Yes
Page Program	80h	10h	-	
Copy Back Program	00h	8Ah	10h	
Block Erase	60h	D0h	-	
Reset	FFh	-	-	Yes

1. The bus cycles are only shown for issuing the codes. The cycles required to input the addresses or input/output data are not shown.
2. Any undefined command sequence is ignored by the device.

6 Device operations

6.1 Pointer operations

As the NAND flash memories contain two different areas for x16 devices and three different areas for x8 devices (see *Figure 8*) the read command codes (00h, 01h, 50h) act as pointers to the different areas of the memory array (they select the most significant column address).

The Read A and Read B commands act as pointers to the main memory area. Their use depends on the bus width of the device.

- In x16 devices the Read A command (00h) sets the pointer to Area A (the whole of the main area), that is words 0 to 255.
- In x8 devices the Read A command (00h) sets the pointer to Area A (the first half of the main area), that is bytes 0 to 255, and the Read B command (01h) sets the pointer to Area B (the second half of the main area), that is bytes 256 to 511.

In both the x8 and x16 devices the Read C command (50h) acts as a pointer to Area C (the spare memory area), that is bytes 512 to 527 or words 256 to 263.

Once the Read A and Read C commands have been issued the pointer remains in the respective areas until another pointer code is issued. However, the Read B command is effective for only one operation, once an operation has been executed in Area B the pointer returns automatically to Area A.

The pointer operations can also be used before a program operation, that is the appropriate code (00h, 01h or 50h) can be issued before the program command 80h is issued (see *Figure 9: Pointer operations for programming*).

Figure 8. Pointer operations

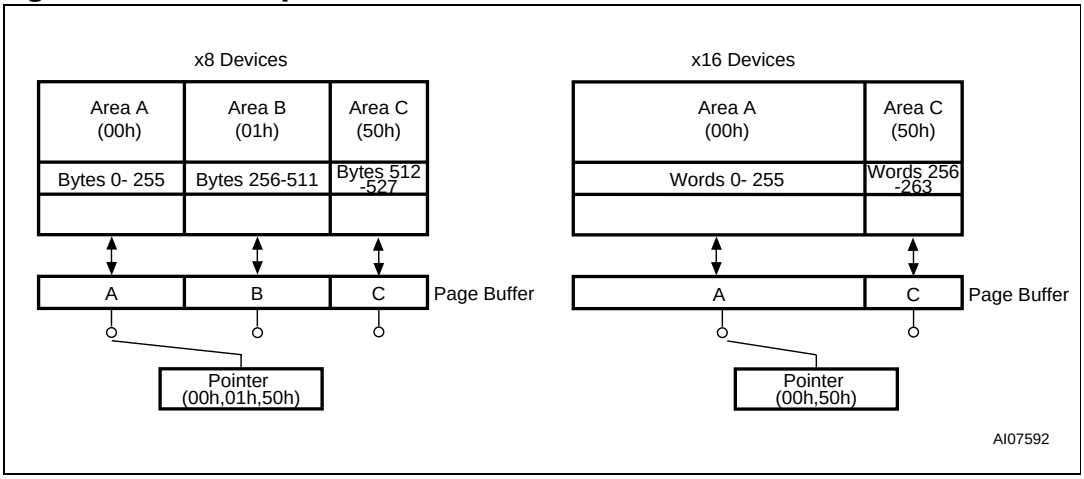
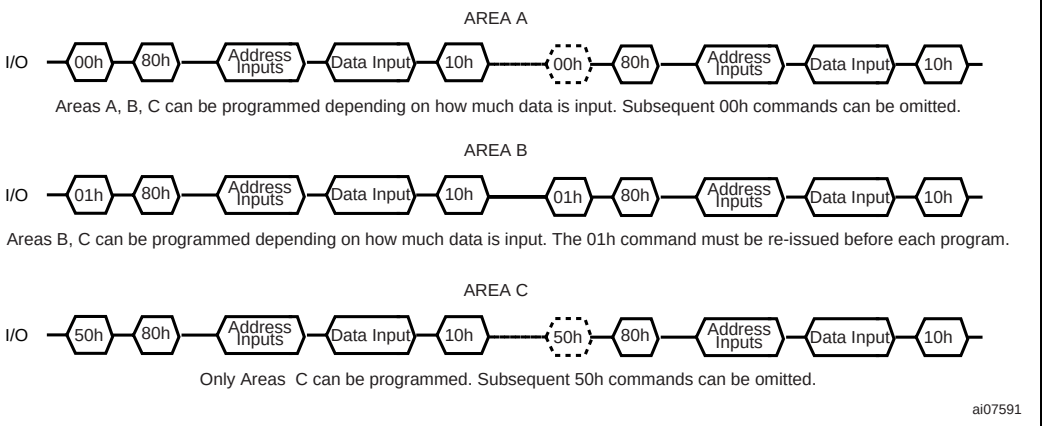


Figure 9. Pointer operations for programming



6.2 Read memory array

Each operation to read the memory area starts with a pointer operation as shown in the *Section 6.1: Pointer operations*. Once the area (main or spare) has been selected using the Read A, Read B or Read C commands three bus cycles are required to input the address of the data to be read.

The device defaults to Read A mode after power-up or a reset operation.

When reading the following spare area addresses:

- A0 to A3 (x8 devices)
- A0 to A2 (x16 devices)

set the start address of the spare area, while the following addresses are ignored:

- A4 to A7 (x8 devices)
- A3 to A7 (x16 devices)

Once the Read A or Read C commands have been issued they do not need to be reissued for subsequent read operations as the pointer remains in the respective area. However, the Read B command is effective for only one operation; once an operation has been executed in Area B the pointer returns automatically to Area A. Another Read B command is required to start another read operation in Area B.

Once a read command is issued two types of operations are available: random read and page read.

- Random read

  Each time the command is issued the first read is random read.
- Page read

  After the random read access the page data is transferred to the page buffer in a time of t_{WHBH} (refer to *Table 21: AC characteristics for operations* for the value). Once the transfer is complete the Ready/Busy signal goes High. The data can then be read out sequentially (from the selected column address to the last column address) by pulsing the Read Enable signal.
- Sequential row read
  After the data in last column of the page is output, if the Read Enable signal is pulsed

and Chip Enable remains Low, then the next page is automatically loaded into the page buffer and the read operation continues. A sequential row read operation can only be used to read within a block. If the block changes a new read command must be issued. Refer to *Figure 12: Sequential row read operations* and *Figure 13: Sequential row read block diagrams* for details about sequential row read operations. To terminate a sequential row read operation, set to High the Chip Enable signal for more than t_{EHEL}. Sequential row read is not available when the Chip Enable don't care option is enabled.

Figure 10. Read (A, B, C) operations

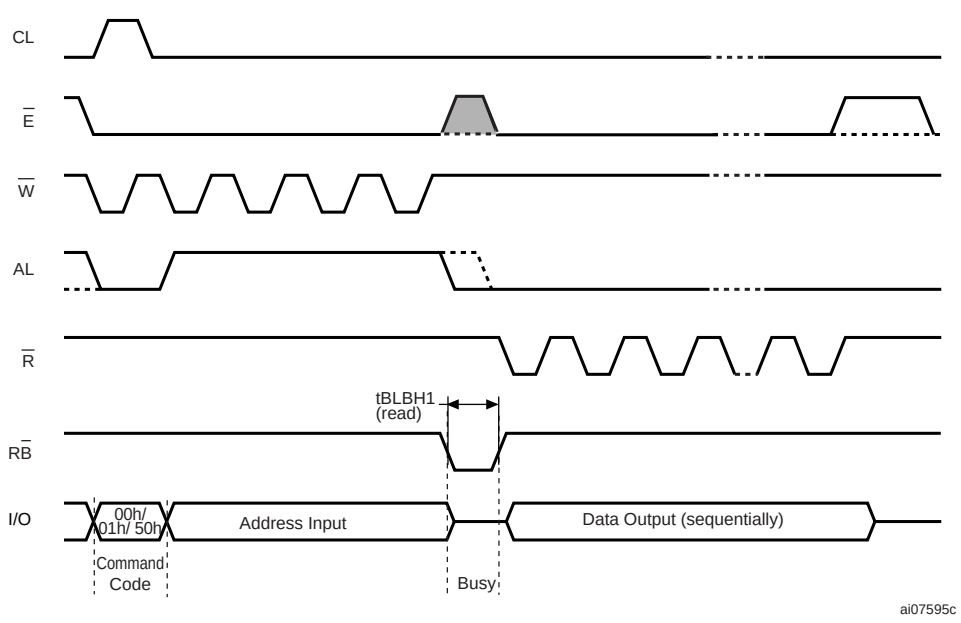
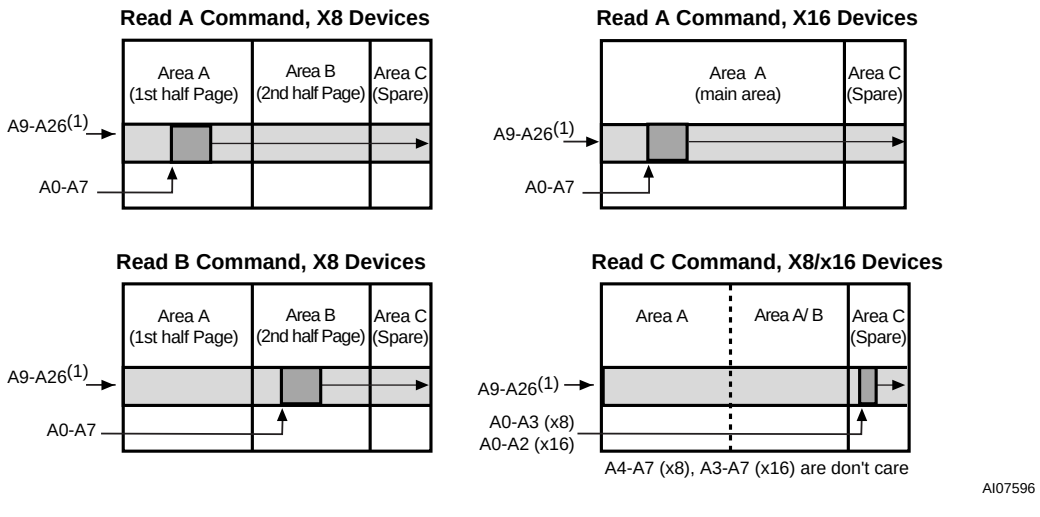


Figure 11. Read block diagrams



1. The highest address depends on the device density.

Figure 12. Sequential row read operations

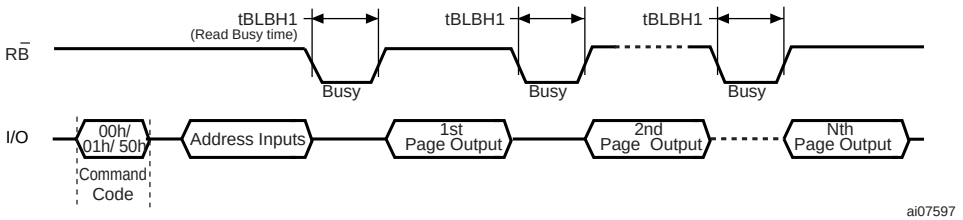
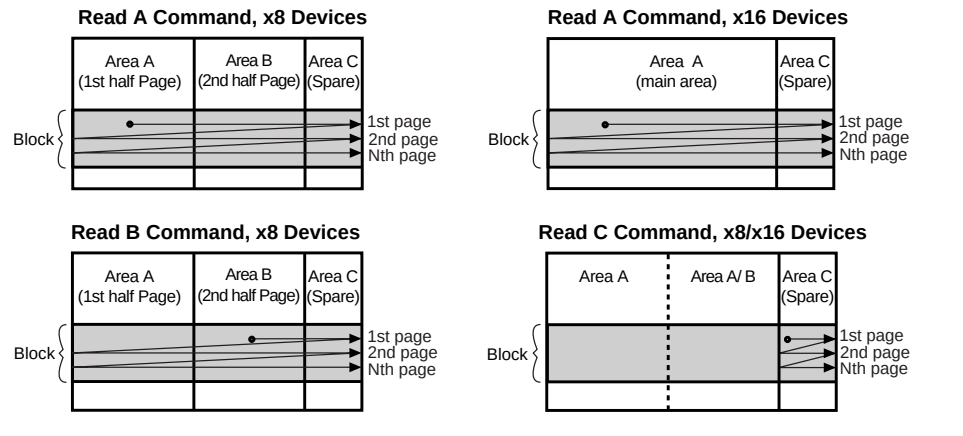


Figure 13. Sequential row read block diagrams



6.3 Page program

The page program operation is the standard operation to program data to the memory array.

The main area of the memory array is programmed by page, however partial page programming is allowed where any number of bytes (1 to 528) or words (1 to 264) can be programmed.

The maximum number of consecutive partial page program operations allowed in the same page is three. After exceeding this a Block Erase command must be issued before any further program operations can take place in that page.

Before starting a page program operation a pointer operation can be performed to point to the area to be programmed. Refer to *Section 6.1: Pointer operations* and *Figure 9: Pointer operations for programming* for details.

Each page program operation consists of the following five steps (see *Figure 14: Page program operation*):

1. One bus cycle is required to setup the Page Program command
2. Four bus cycles are then required to input the program address (refer to *Table 6: Address insertion, x8 devices*)
3. The data is then input (up to 528 bytes/ 264 words) and loaded into the page buffer
4. One bus cycle is required to issue the confirm command to start the P/E/R controller.
5. The P/E/R controller then programs the data into the array.

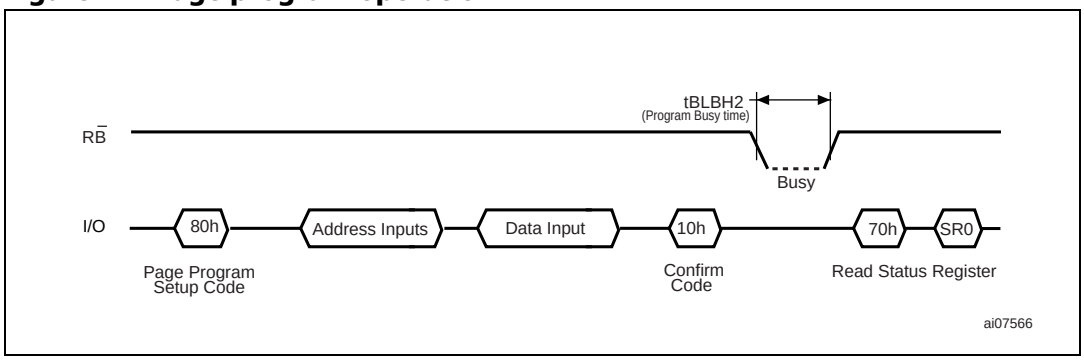
Once the program operation has started the status register can be read using the Read Status Register command. During program operations the status register only flags errors for bits set to '1' that have not been successfully programmed to '0'.

During the program operation, only the Read Status Register and Reset commands are accepted; all other commands are ignored.

Once the program operation has completed the P/E/R controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High.

The device remains in read status register mode until another valid command is written to the command interface.

Figure 14. Page program operation



1. Before starting a page program operation a pointer operation can be performed. Refer to *Section 6.1: Pointer operations* for details.

6.4 Copy back program

The copy back program operation copies the data stored in one page and reprogram it in another page.

The copy back program operation does not require external memory and so the operation is faster and more efficient because the reading and loading cycles are not required. The operation is particularly useful when a portion of a block is updated and the rest of the block needs to be copied to the newly assigned block.

If the copy back program operation fails an error is signalled in the status register. However, as the standard external ECC cannot be used with the copy back operation bit error due to charge loss cannot be detected. For this reason it is recommended to limit the number of copy back operations on the same data and or to improve the performance of the ECC.

The copy back program operation requires the following three steps:

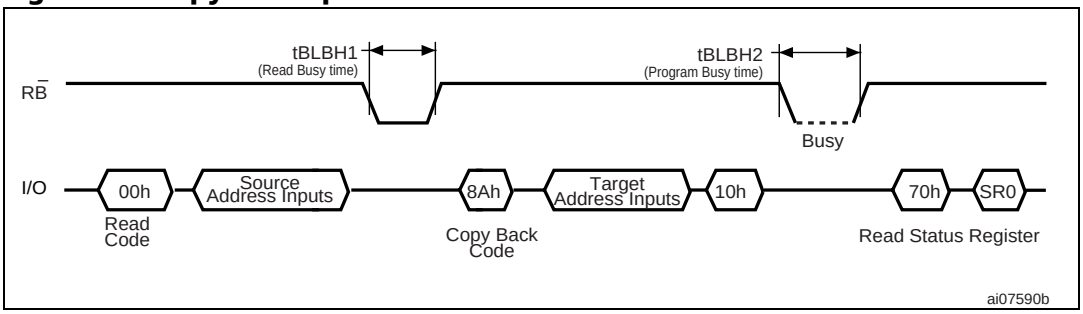
1. The source page must be read using the Read A command (one bus write cycle to setup the command and then 4 bus write cycles to input the source page address). This operation copies all 264 words/ 528 bytes from the page into the page buffer.
2. When the device returns to the ready state (Ready/Busy High), the second bus write cycle of the command is given with the 4 bus cycles to input the target page address. Refer to *Table 10* for the addresses that must be the same for the source and target pages.
3. Then the confirm command is issued to start the P/E/R controller.

After a copy back program operation, a partial-page program is not allowed in the target page until the block has been erased. See *Figure 15* for an example of the copy back operation.

Table 10. Copy back program addresses

Density	Same address for source and target pages
128 Mbit	A23
256 Mbit	A24

Figure 15. Copy back operation



6.5 Block erase

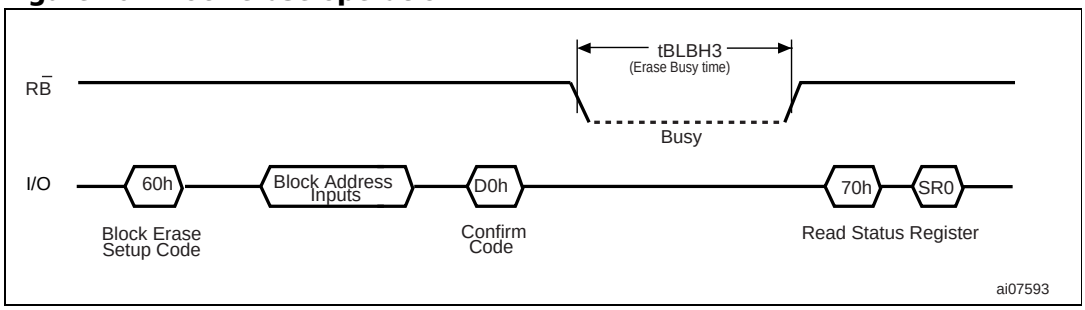
Erase operations are done one block at a time. An erase operation sets all of the bits in the addressed block to '1'. All previous data in the block is lost.

An erase operation consists of the following three steps (refer to *Figure 16: Block erase operation*):

1. One bus cycle is required to set up the Block Erase command.
2. Only two bus cycles are required to input the block address. The first cycle (A0 to A7) is not required as only addresses A14 to A26 (highest address depends on device density) are valid, A9 to A13 are ignored. In the last address cycle I/O2 to I/O7 must be set to V_{IL}.
3. One bus cycle is required to issue the confirm command to start the P/E/R controller.

Once the erase operation has completed the status register can be checked for errors.

Figure 16. Block erase operation



6.6 Reset

The Reset command resets the command interface and status register. If the Reset command is issued during any operation, the operation is aborted. If it was a program or erase operation that was aborted, the contents of the memory locations being modified are no longer valid as the data is partially programmed or erased.

If the device has already been reset then the new Reset command is not accepted.

The Ready/Busy signal goes Low for t_{BLBH4} after the Reset command is issued. The value of t_{BLBH4} depends on the operation that the device was performing when the command was issued (refer to *Table 21: AC characteristics for operations* for the values.)

6.7 Read status register

The device contains a status register which provides information on the current or previous program or erase operation. the various bits in the status register convey information and errors on the operation.

the status register is read by issuing the read status register command. the status register information is present on the output data bus (I/O0-I/O7) on the falling edge of chip enable or read enable, whichever occurs last. when several memories are connected in a system, the use of chip enable and read enable signals allows the system to poll each device separately, even when the ready/busy pins are common-wired. it is not necessary

to toggle the chip enable or read enable signals to update the contents of the status register.

After the read status register command has been issued, the device remains in read status register mode until another command is issued. therefore if a read status register command is issued during a random read cycle a new read command must be issued to continue with a page read.

The status register bits are summarized in *Table 11: Status register bits*, to which you should refer in conjunction with the following sections.

6.7.1 Write Protection Bit (SR7)

The Write Protection bit identifies if the device is protected or not. If the Write Protection bit is set to '1' the device is not protected and program or erase operations are allowed. If the Write Protection bit is set to '0' the device is protected and program or erase operations are not allowed.

6.7.2 P/E/R controller bit (SR6)

The program/erase/read controller bit indicates whether the P/E/R controller is active or inactive. When the P/E/R controller bit is set to '0', the P/E/R controller is active (device is busy); when the bit is set to '1', the P/E/R controller is inactive (device is ready).

6.7.3 Error bit (SR0)

The error bit identifies if any errors have been detected by the P/E/R controller. The error bit is set to '1' when a program or erase operation has failed to write the correct data to the memory. If the error bit is set to '0' the operation has completed successfully.

SR5, SR4, SR3, SR2 and SR1 are reserved.

Table 11. Status register bits

Bit	Name	Logic level	Definition
SR7	Write protection	'1'	Not protected
		'0'	Protected
SR6	Program/erase/read controller	'1'	P/E/R C inactive, device ready
		'0'	P/E/R C active, device busy
SR5, SR4, SR3, SR2, SR1	Reserved	'don't care'	
SR0	Generic error	'1'	Error – operation failed
		'0'	No error – operation successful

6.8 Read electronic signature

The device contains a manufacturer code and device code. To read these codes the following two steps are required:

1. First use one bus write cycle to issue the Read Electronic Signature command (90h), followed by an address input of 00h.
2. Then, perform two bus read operations. The first one reads the manufacturer code and the second reads the device code. Further bus read operations are ignored.

Refer to *Table 12* for information on the addresses.

Table 12. Electronic signature

Part number	Manufacturer code	Device code
NAND128W3A	20h	73h
NAND256R3A	20h	35h
NAND256W3A		75h
NAND256R4A	0020h	0045h
NAND256W4A		0055h

7 Software algorithms

This section gives information on the software algorithms that Numonyx recommends to implement to manage the bad blocks and extend the lifetime of the NAND device.

NAND flash memories are programmed and erased by Fowler-Nordheim tunneling using a high voltage. Exposing the device to a high voltage for extended periods can cause the oxide layer to be damaged. For this reason, the number of program and erase cycles is limited (see *Table 14: Program, erase times and program erase endurance cycles* for the values) and it is recommended to implement garbage collection, a wear-leveling algorithm and an error correction code to extend the number of program and erase cycles and increase the data retention.

For the integration of NAND memories into an application, Numonyx provides a full range of software solutions such as file systems, sector managers, drivers, and code management.

Contact the nearest Numonyx sales office or visit www.numonyx.com for more details.

7.1 Bad block management

Devices with bad blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A bad block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor.

The devices are supplied with all the locations inside valid blocks erased (FFh). The bad block information is written prior to shipping. Any block where the 6th byte (x8 device)/1st word (x16 device) in the spare area of the 1st page does not contain FFh is a bad block.

The bad block information must be read before any erase is attempted as the bad block information may be erased. For the system to be able to recognize the bad blocks based on the original information it is recommended to create a bad block table following the flowchart shown in *Figure 17: Bad block management flowchart*.

7.2 Block replacement

Over the lifetime of the device additional bad blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional bad blocks can be identified as attempts to program or erase them outputs errors to the status register.

As the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. The Copy Back Program command can be used to copy the data to a valid block.

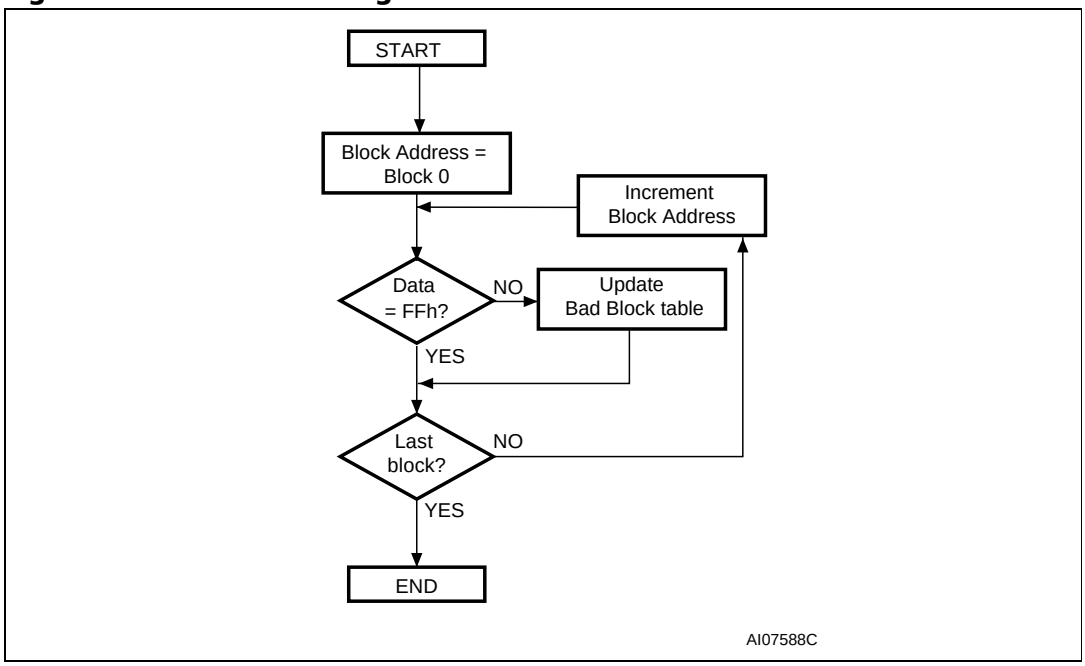
Refer to *Section 6.4: Copy back program* for more details.

Refer to *Table 13* for the recommended procedure to follow if an error occurs during an operation.

Table 13. Block failure

Operation	Recommended procedure
Erase	Block replacement
Program	Block replacement or ECC
Read	ECC

Figure 17. Bad block management flowchart

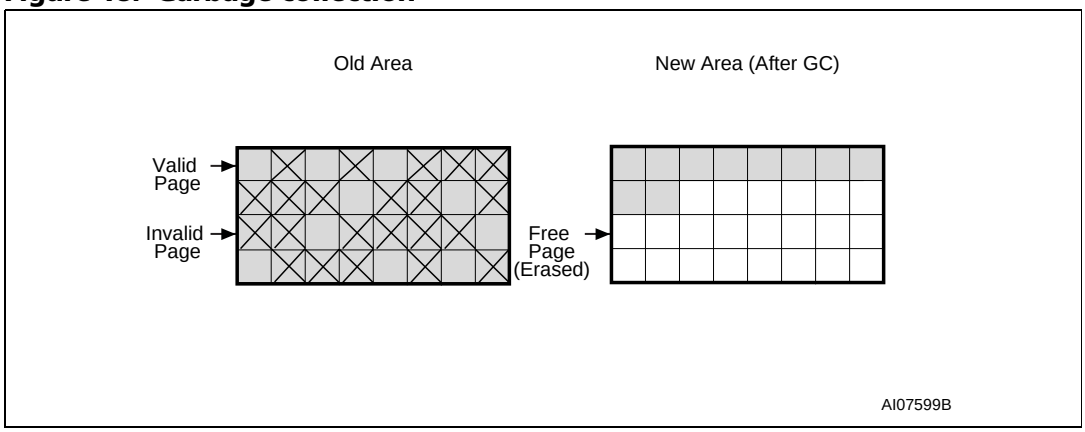


7.3 Garbage collection

When a data page needs to be modified, it is faster to write to the first available page, and the previous page is marked as invalid. After several updates it is necessary to remove invalid pages to free some memory space.

To free this memory space and allow further program operations it is recommended to implement a garbage collection algorithm. In a garbage collection software the valid pages are copied into a free area and the block containing the invalid pages is erased (see *Figure 18: Garbage collection*).

Figure 18. Garbage collection



7.4 Wear-leveling algorithm

For write-intensive applications, it is recommended to implement a wear-leveling algorithm to monitor and spread the number of write cycles per block.

In memories that do not use a wear-leveling algorithm not all blocks get used at the same rate. Blocks with long-lived data do not endure as many write cycles as the blocks with frequently-changed data.

The wear-leveling algorithm ensures that equal use is made of all the available write cycles for each block. There are two wear-leveling levels:

- First level wear-leveling: new data is programmed to the free blocks that have had the fewest write cycles.
- Second level wear-leveling: long-lived data is copied to another block so that the original block can be used for more frequently-changed data.

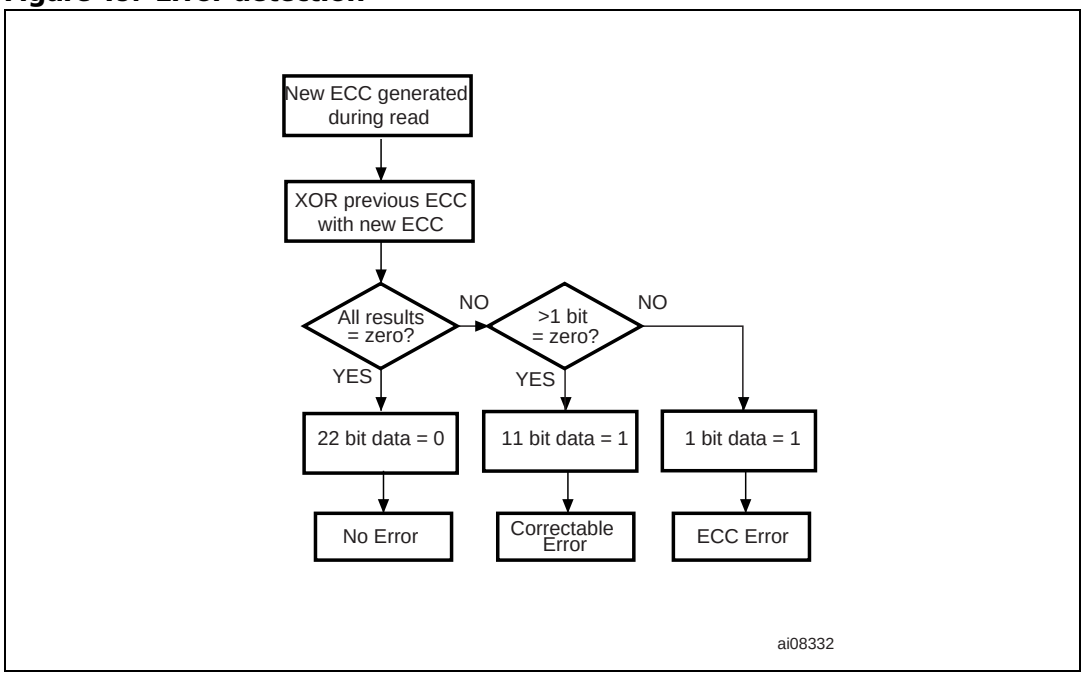
The second level wear-leveling is triggered when the difference between the maximum and the minimum number of write cycles per block reaches a specific threshold.

7.5 Error correction code

An error correction code (ECC) can be implemented in the NAND flash memories to identify and correct errors in the data.

The recommendation is to implement 23 bits of ECC for every 4096 bits in the device.

Figure 19. Error detection



7.6 Hardware simulation models

7.6.1 Behavioral simulation models

Denali Software Corporation models are platform-independent functional models designed to assist customers in performing entire system simulations (typical VHDL/Verilog). These models describe the logic behavior and timings of NAND flash devices, and, therefore, allow software to be developed before hardware.

7.6.2 IBIS simulations models

IBIS (I/O buffer information specification) models describe the behavior of the I/O buffers and electrical characteristics of flash devices.

These models provide information such as AC characteristics, rise/fall times, and package mechanical data, all of which are measured or simulated at voltage and temperature ranges wider than those allowed by target specifications.

IBIS models simulate PCB connections and can resolve compatibility issues when upgrading devices. They can be imported into SPICETOOLS.

8 Program and erase times and endurance cycles

The program and erase times and the number of program/ erase cycles per block are shown in *Table 14*.

Table 14. Program, erase times and program erase endurance cycles

Parameters	NAND flash			Unit
	Min	Typ	Max	
Page program time		200	500	µs
Block erase time		2	3	ms
Program/erase cycles (per block)	100,000			cycles
Data retention	10			years

9 Maximum ratings

Stressing the device above the ratings listed in *Table 15* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Table 15. Absolute maximum ratings

Symbol	Parameter		Value		Unit
			Min	Max	
T_{BIAS}	Temperature under bias		– 50	125	°C
T_{STG}	Storage temperature		– 65	150	°C
T_{LEAD}	Lead temperature during soldering (1)			260	°C
V_{IO} (2)	Input or output voltage	1.8 V devices	– 0.6	2.7	V
		3 V devices	– 0.6	4.6	V
V_{DD}	Supply voltage	1.8 V devices	– 0.6	2.7	V
		3 V devices	– 0.6	4.6	V

1. Compatibility with lead-free soldering processes in accordance with ECOPACK 7191395 specifications. Not exceeding 250°C for more than 10 s, and peaking at 260°C.
2. Minimum voltage may undershoot to –2 V for less than 20 ns during transitions on input and I/O pins. Maximum voltage may overshoot to VDD + 2 V for less than 20 ns during transitions on I/O pins.

10 DC and AC parameters

This section summarizes the operating and measurement conditions and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables in this section are derived from tests performed under the measurement conditions summarized in *Table 16*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 16. Operating and AC measurement conditions

Parameter		NAND flash		Units
		Min	Max	
Supply voltage (V_{DD})	1.8 V devices	1.7	1.95	V
	3 V devices	2.7	3.6	V
Ambient (T_A)	Grade 6	–40	85	°C
Load capacitance (C_L) (1 TTL GATE and C_L)	1.8 V devices	30		pF
	3 V devices (2.7 - 3.6 V)	50		pF
	3 V devices (3.0 - 3.6V)	100		pF
Input pulses voltages	1.8 V devices	0	V_{DD}	V
	3 V devices	0.4	2.4	V
Input and output timing ref. voltages	1.8 V devices	0.9		V
	3 V devices	1.5		V
Input rise and fall times		5		ns
Output circuit resistors, R_{ref}		8.35		kΩ

Table 17. Capacitance(1) (2)

Symbol	Parameter	Test condition	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		10	pF
$C_{I/O}$	Input/output capacitance	V_{IL} = 0 V		10	pF

1. TA = 25°C, f = 1 MHz. CIN and CI/O are not 100% tested.
2. Input/output capacitances double on stacked devices

Table 18. DC characteristics, 1.8 V devices(1)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
I_{DD1}	Operating Current	Sequential read	t_{RLRL} minimum $\overline{E}$=V_{IL}, I_{OUT} = 0 mA	-	8	15	mA
I_{DD2}		Program	-	-	8	15	mA
I_{DD3}		Erase	-	-	8	15	mA
I_{DD5}	Standby current (CMOS)		$\overline{E}$ = V_{DD}-0.2, $\overline{WP}$ = 0/V_{DD}	-	10	50	µA
				-	20	100	µA
I_{LI}	Input leakage current		V_{IN}= 0 to V_{DD}max	-	-	±10	µA
I_{LO}	Output leakage current		V_{OUT}= 0 to V_{DD}max	-	-	±10	µA
V_{IH}	Input High voltage		-	V_{DD}-0.4	-	V_{DD}+0.3	V
V_{IL}	Input Low voltage		-	-0.3	-	0.4	V
V_{OH}	Output High voltage level		I_{OH} = -100 µA	V_{DD}-0.1	-	-	V
V_{OL}	Output Low voltage level		I_{OL} = 100 µA	-	-	0.1	V
I_{OL} ($R\overline{B}$)	Output Low current ($R\overline{B}$)		V_{OL} = 0.1 V	3	4		mA
V_{LKO}	V_{DD} supply voltage (erase and program lockout)		-	-	-	1.1	V

1. Leakage currents double on stacked devices.

Figure 20. Equivalent testing circuit for AC characteristics measurement

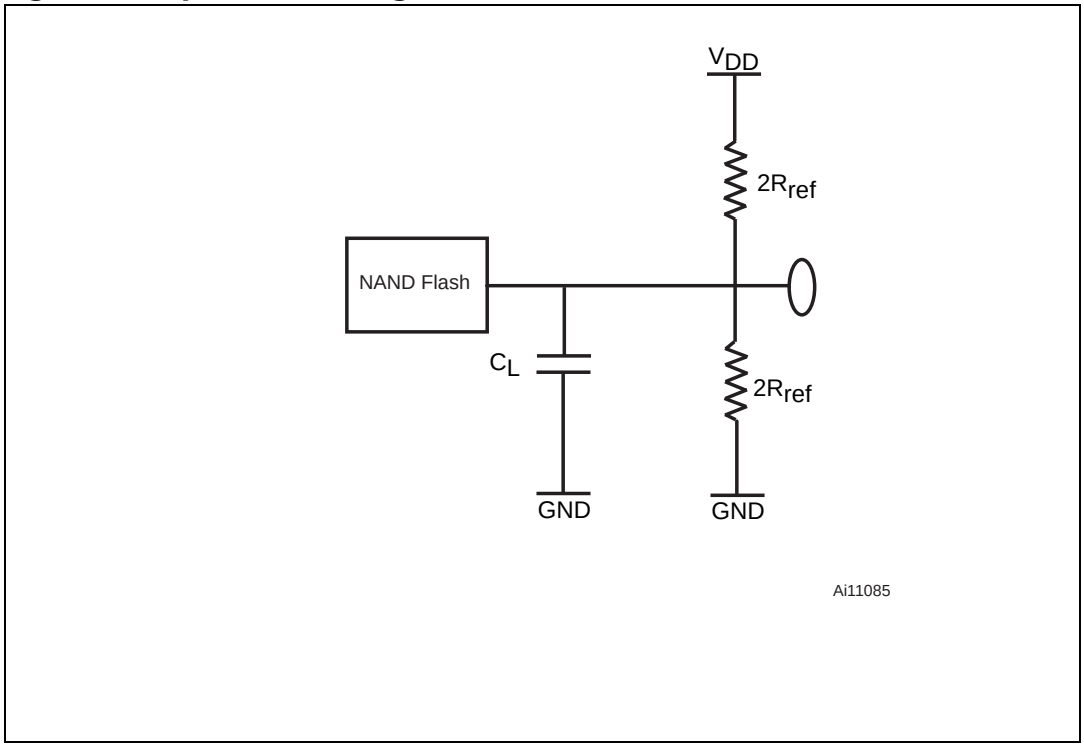


Table 19. DC characteristics, 3 V devices(1)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
I_{DD1}	Operating current	Sequential read	t_{RLRL} minimum $\overline{E}$=V_{IL}, I_{OUT} = 0 mA	-	10	20	mA
I_{DD2}		Program	-	-	10	20	mA
I_{DD3}		Erase	-	-	10	20	mA
I_{DD4}	Standby current (TTL)		$\overline{E}$ = V_{IH}, $\overline{WP}$ = 0 V/V_{DD}	-	-	1	mA
				-	-	2	mA
I_{DD5}	Standby current (CMOS)		$\overline{E}$ = V_{DD}-0.2 $\overline{WP}$ = 0 V/V_{DD}	-	10	50	µA
				-	20	100	µA
I_{LI}	Input leakage current		V_{IN} = 0 to V_{DD}max	-	-	±10	µA
I_{LO}	Output leakage current		V_{OUT}= 0 to V_{DD}max	-	-	±10	µA
V_{IH}	Input High voltage		-	2.0	-	V_{DD}+0.3	V
V_{IL}	Input Low voltage		-	–0.3	-	0.8	V
V_{OH}	Output High voltage level		I_{OH} = –400 µA	2.4	-	-	V
V_{OL}	Output Low voltage level		I_{OL} = 2.1 mA	-	-	0.4	V
I_{OL} ($R\overline{B}$)	Output Low current ($R\overline{B}$)		V_{OL} = 0.4 V	8	10		mA
V_{LKO}	V_{DD} supply voltage (erase and program lockout)		-	-	-	1.7	V

1. Leakage currents double on stacked devices.

Table 20. AC characteristics for command, address, data input

Symbol	Alt. Symbol	Parameter			1.8 V Devices	3 V Devices	Unit
t_{ALLWL}	t_{ALS}	Address Latch Low to Write Enable Low	AL Setup time	Min	0	0	ns
t_{ALHWL}		Address Latch High to Write Enable Low					
t_{CLHWL}	t_{CLS}	Command Latch High to Write Enable Low	CL Setup time	Min	0	0	ns
t_{CLLWL}		Command Latch Low to Write Enable Low					
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Data Setup time	Min	20	20	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	$\overline{E}$ Setup time	Min	0	0	ns
t_{WHALH}	t_{ALH}	Write Enable High to Address Latch High	AL Hold time	Min	10	10	ns
t_{WHALL}		Write Enable High to Address Latch Low					
t_{WHCLH}	t_{CLH}	Write Enable High to Command Latch High	CL hold time	Min	10	10	ns
t_{WHCLL}		Write Enable High to Command Latch Low					
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Data Hold time	Min	10	10	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	$\overline{E}$ Hold time	Min	10	10	ns
t_{WHWL}	t_{WH}	Write Enable High to Write Enable Low	$\overline{W}$ High Hold time	Min	20	15	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	$\overline{W}$ Pulse Width	Min	40	25(1)	ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write Cycle time	Min	60	50	ns

1. If t_{ELWL} is less than 10 ns, t_{WLWH} must be minimum 35 ns, otherwise, t_{WLWH} may be minimum 25 ns.

Table 21. AC characteristics for operations(1)

Sym-bol	Alt. Sym-bol	Parameter			1.8 V Devices	3 V Devices	Unit
t_{ALLRL1}	t_{AR}	Address Latch Low to Read Enable Low	Read electronic signature	Min	10	10	ns
t_{ALLRL2}			Read cycle	Min	10	10	ns
t_{BHRL}	t_{RR}	Ready/Busy High to Read Enable Low		Min	20	20	ns
t_{BLBH1}		Ready/Busy Low to Ready/Busy High	Read Busy time, 128-Mbit, 256 Mbit, dual die	Max	12	12	µs
t_{BLBH2}	t_{PROG}		Program Busy time	Max	500	500	µs
t_{BLBH3}	t_{BERS}		Erase Busy time	Max	3	3	ms
t_{BLBH4}			Reset Busy time, during ready	Max	5	5	µs
t_{WHBH1}	t_{RST}	Write Enable High to Ready/Busy High	Reset Busy time, during read	Max	5	5	µs
			Reset Busy time, during program	Max	10	10	µs
			Reset Busy time, during erase	Max	500	500	µs
t_{CLLRL}	t_{CLR}	Command Latch Low to Read Enable Low		Min	10	10	ns
t_{DZRL}	t_{IR}	Data Hi-Z to Read Enable Low		Min	0	0	ns
t_{EHQZ}	t_{CHZ}	Chip Enable High to Output Hi-Z		Max	20	20	ns
t_{ELQV}	t_{CEA}	Chip Enable Low to Output Valid		Max	45	45	ns
t_{RHRL}	t_{REH}	Read Enable High to Read Enable Low	Read Enable High Hold time	Min	15	15	ns
t_{RHQZ}	t_{RHZ}	Read Enable High to Output Hi-Z		Max	30	30	ns
T_{EHQX}	T_{OH}	Chip Enable high or Read Enable high to Output Hold		Min	10	10	ns
T_{RHQX}							
t_{RLRH}	t_{RP}	Read Enable Low to Read Enable High	Read Enable Pulse Width	Min	30	25	ns
t_{RLRL}	t_{RC}	Read Enable Low to Read Enable Low	Read Cycle time	Min	60	50	ns
t_{RLQV}	t_{REA}	Read Enable Low to Output Valid	Read Enable access time	Max	35	35	ns
			Read ES access time(1)				
t_{WHBH}	t_{R}	Write Enable High to Ready/Busy High	Read Busy time, 128-Mbit, 256-Mbit dual die	Max	12	12	µs
t_{WHBL}	t_{WB}	Write Enable High to Ready/Busy Low		Max	100	100	ns
t_{WHRL}	t_{WHR}	Write Enable High to Read Enable Low		Min	80	60	ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write Cycle time	Min	60	50	ns

1. ES = electronic signature

Figure 21. Command latch AC waveforms

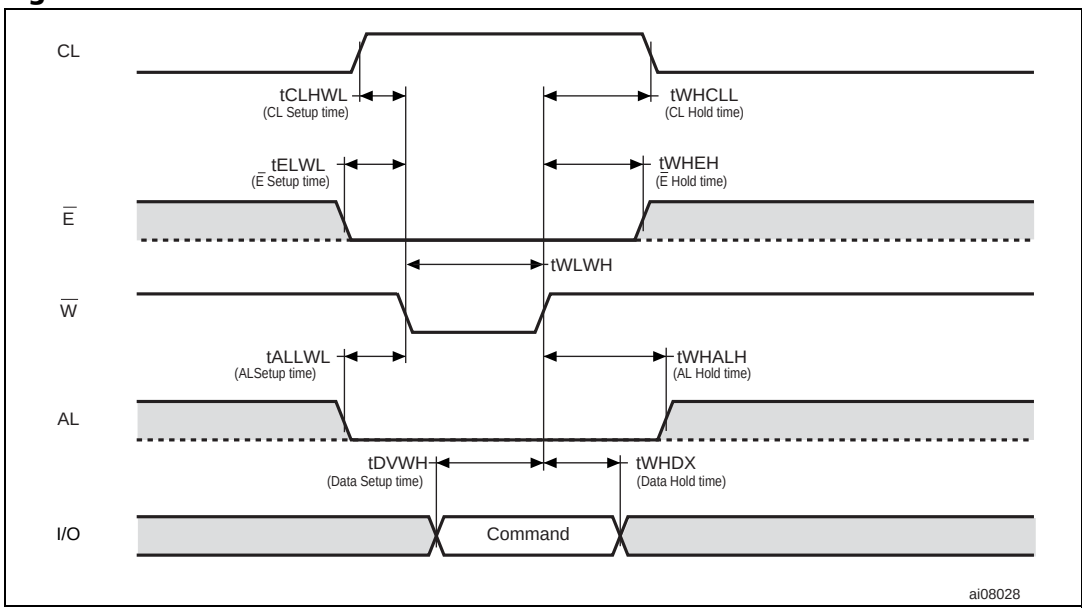


Figure 22. Address latch AC waveforms

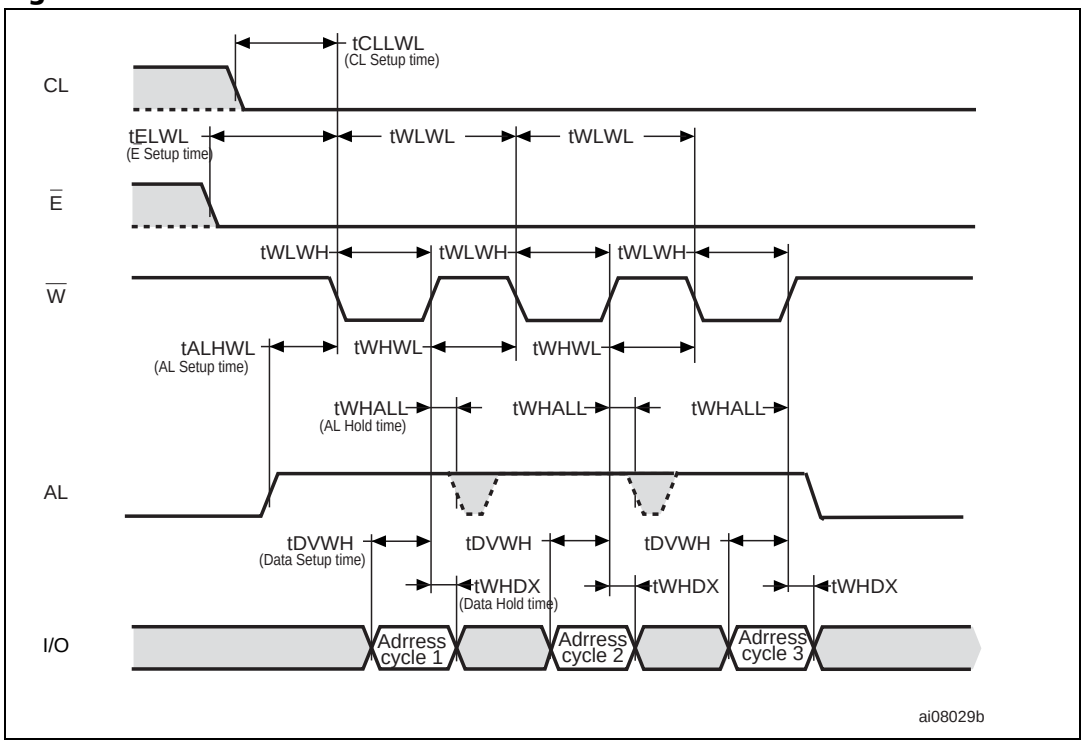


Figure 23. Data input latch AC waveforms

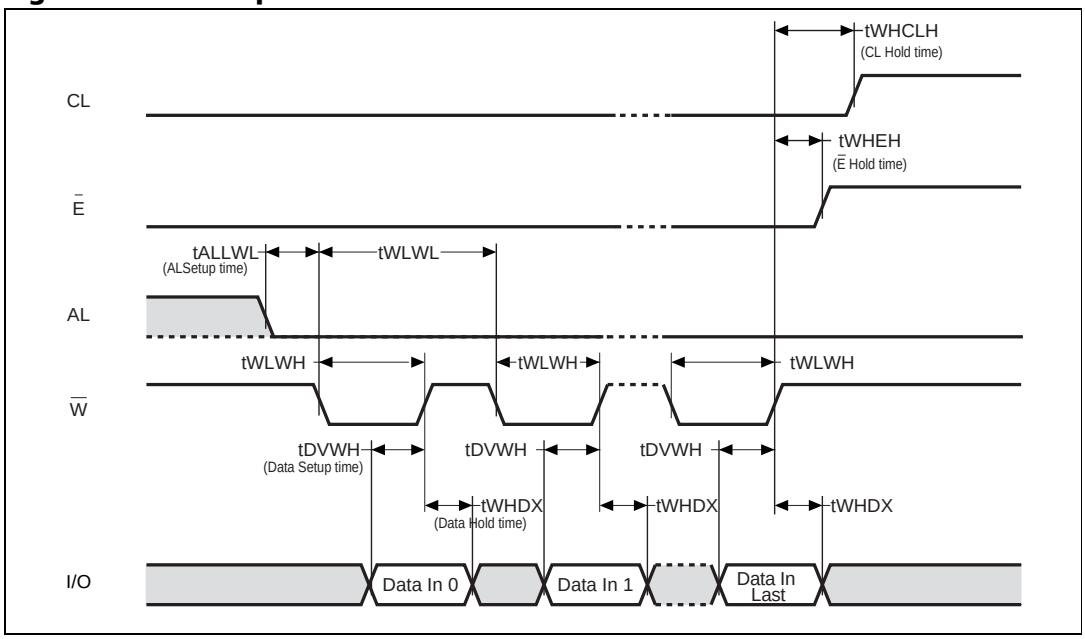
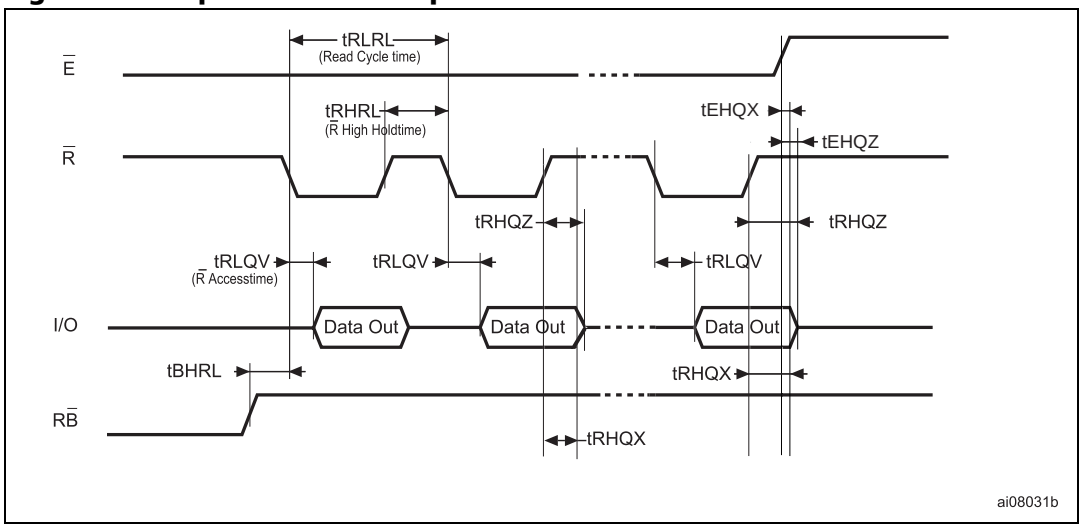


Figure 24. Sequential data output after read AC waveforms



1. CL = Low, AL = Low, $\overline{W}$ = High.

Figure 25. Read status register AC waveform

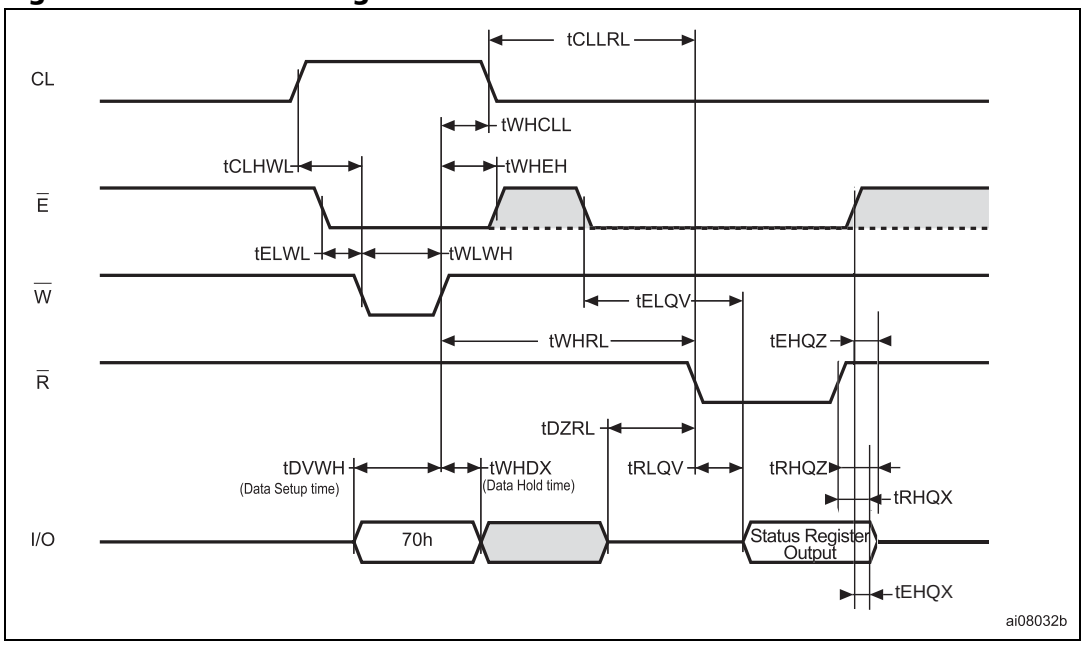
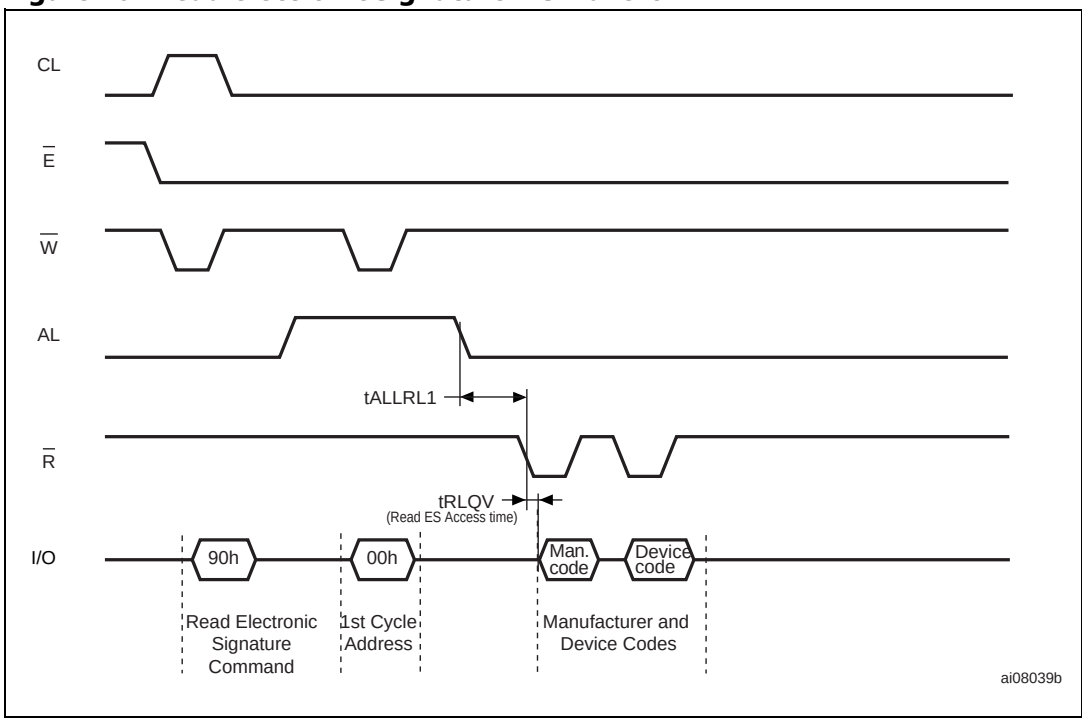


Figure 26. Read electronic signature AC waveform



1. Refer to *Table 12: Electronic signature* for the values of the manufacturer and device codes.

Figure 27. Page read A/read B operation AC waveform

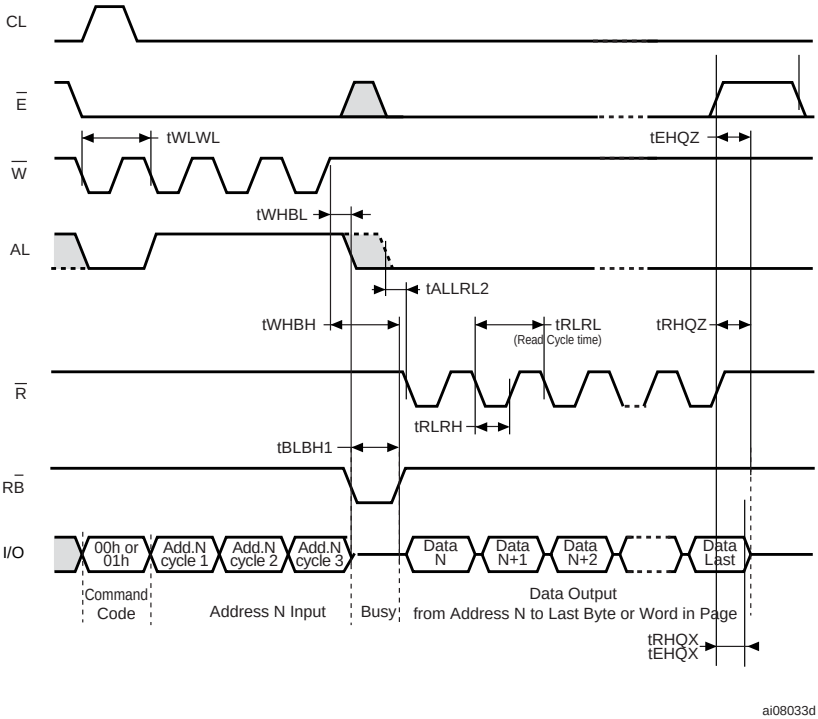
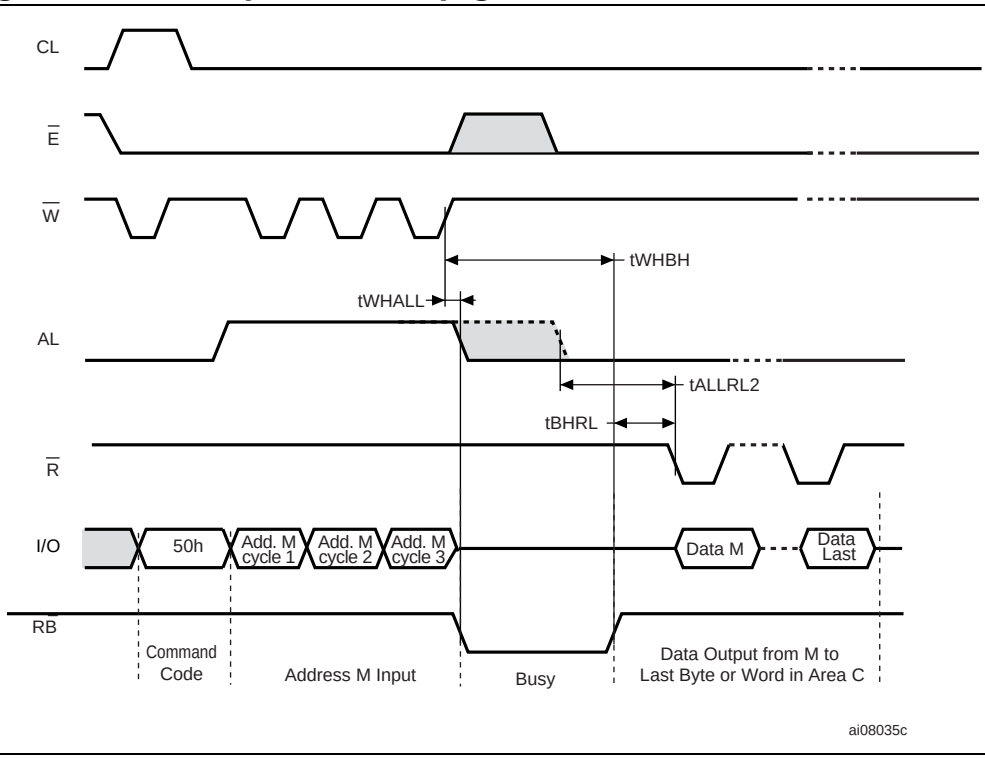


Figure 28. Read C operation, one page AC waveform



1. A0-A7 is the address in the spare memory area, where A0-A3 are valid and A4-A7 are ‘don’t care’.

Figure 29. Page program AC waveform

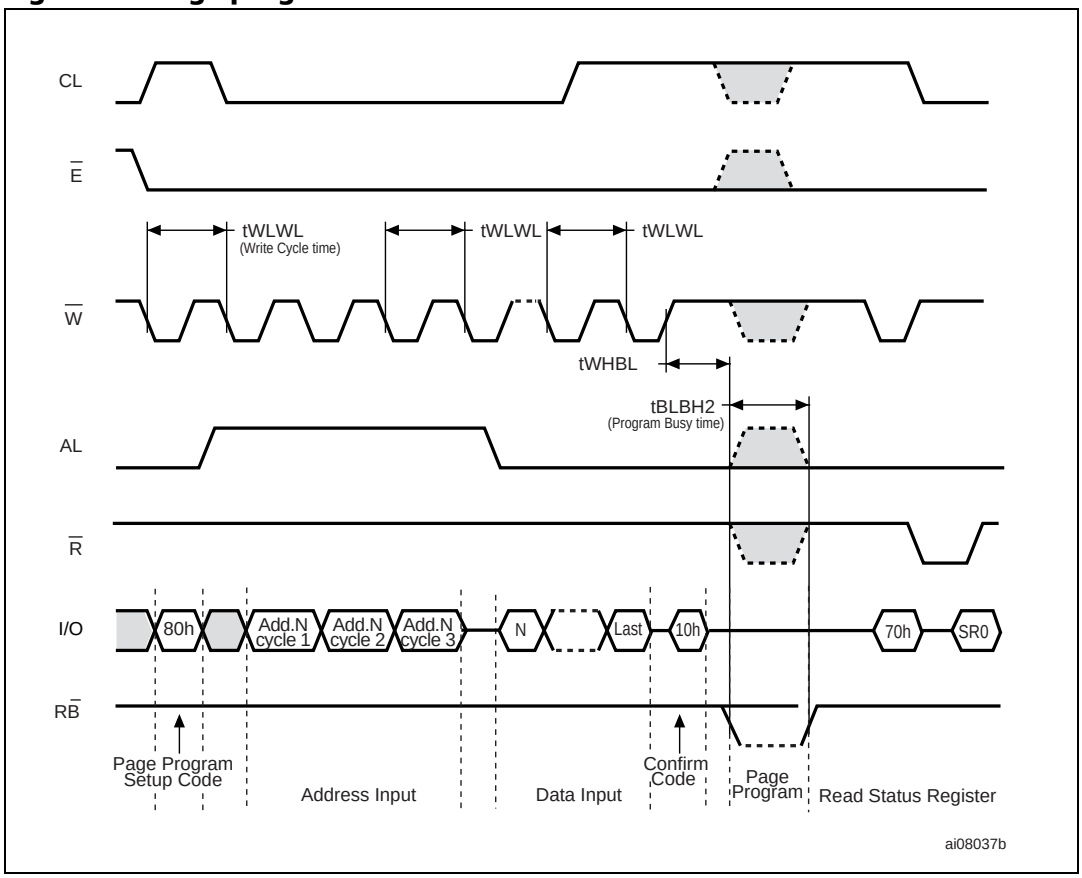


Figure 30. Block erase AC waveform

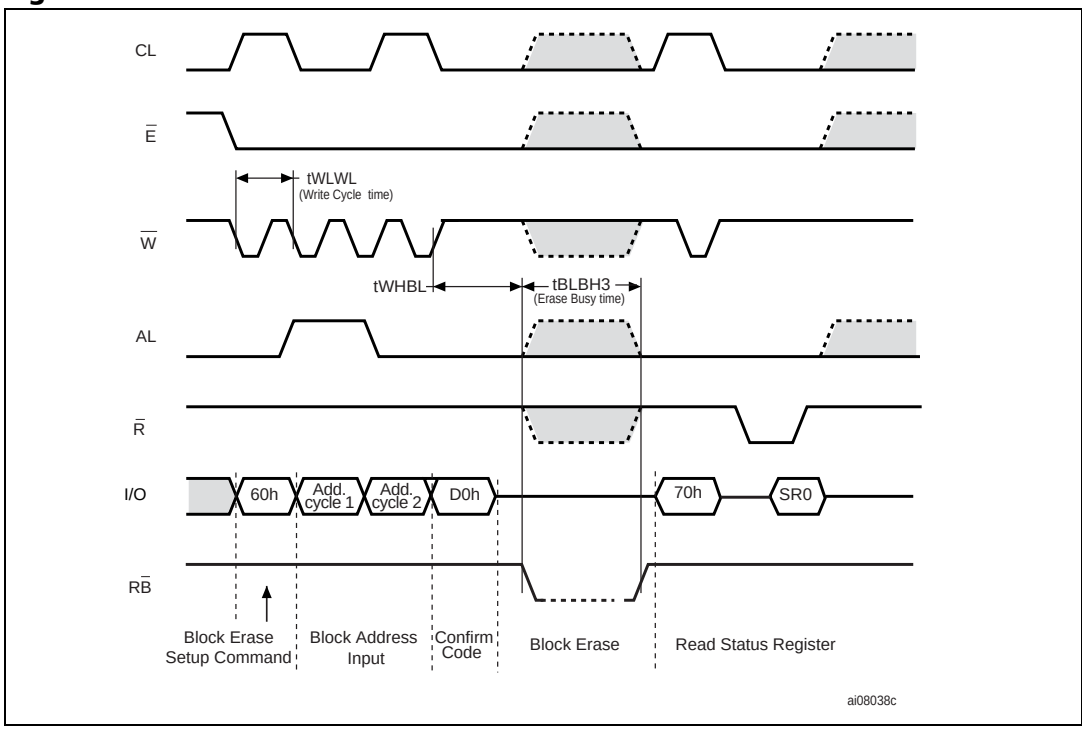
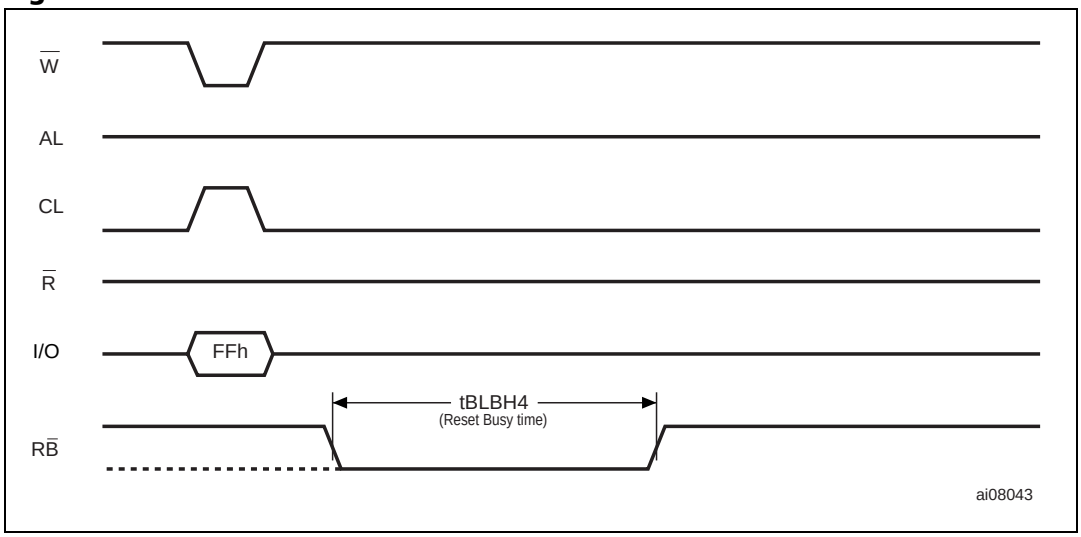


Figure 31. Reset AC waveform



10.1 Ready/busy signal electrical characteristics

Figures *Figure 32*, *Figure 33*, and *Figure 34* show the electrical characteristics for the Ready/Busy signal. The value required for the resistor R_P can be calculated using the following equation:

$$R_P min = \frac{(V_{DDmax} - V_{OLmax})}{I_{OL} + I_L}$$

Therefore,

$$R_P min(1.8V) = \frac{1.85V}{3mA + I_L}$$

$$R_P min(3V) = \frac{3.2V}{8mA + I_L}$$

where I_L is the sum of the input currents of all the devices tied to the Ready/Busy signal. R_P max is determined by the maximum value of t_r.

Figure 32. Ready/Busy AC waveform

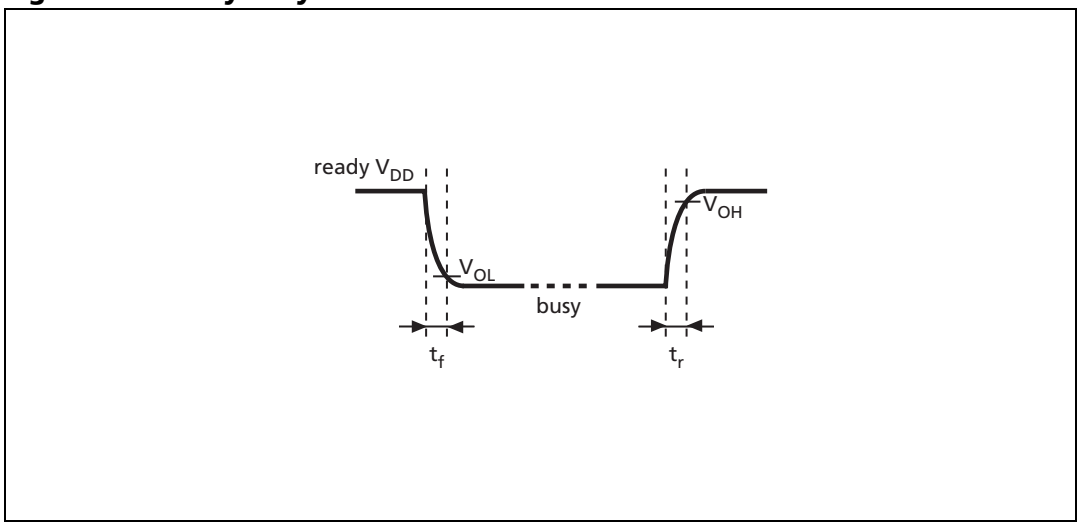


Figure 33. Ready/busy load circuit

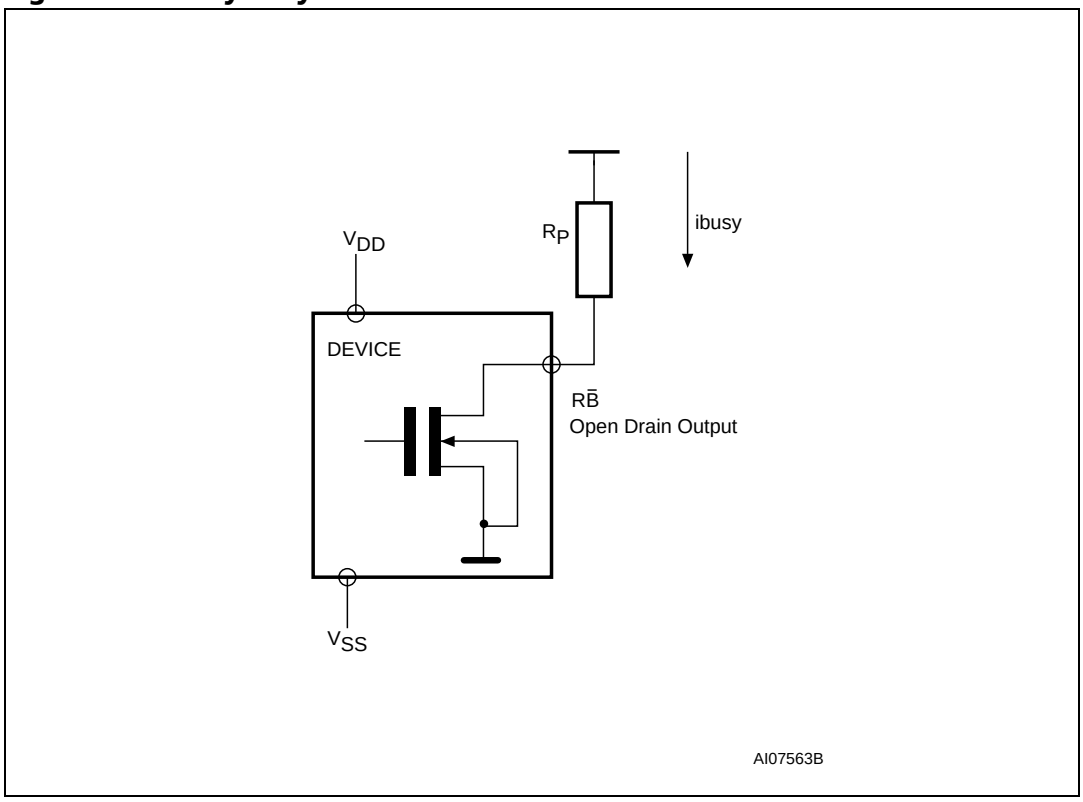
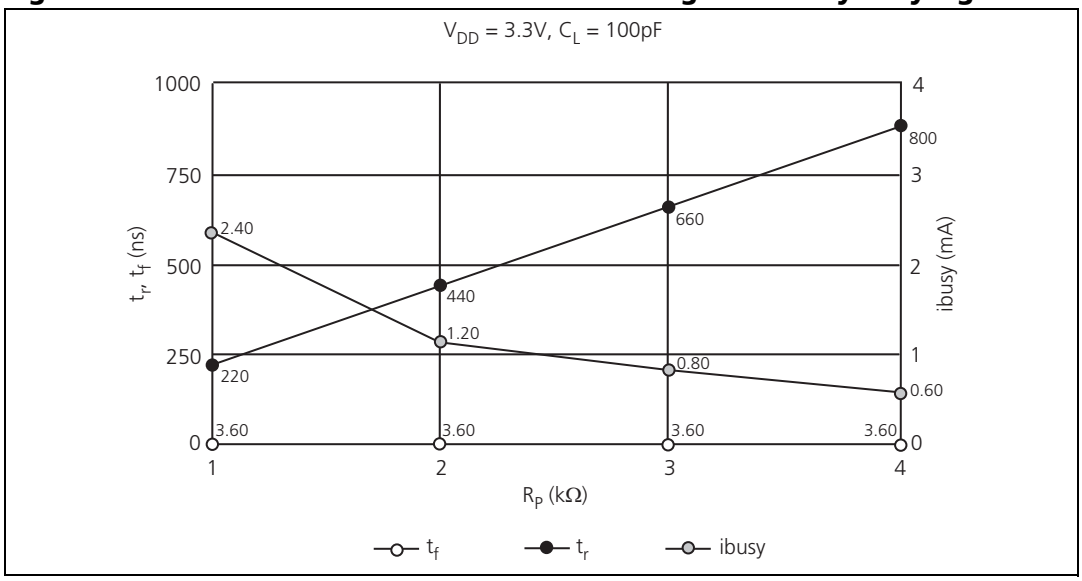


Figure 34. Resistor value versus waveform timings for Ready/Busy signal



1. T = 25°C.

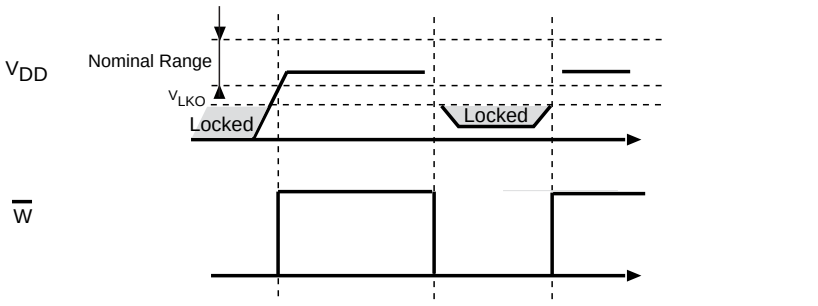
10.2 Data protection

The Numonyx NAND device is designed to guarantee data protection during power transitions.

A V_{DD} detection circuit disables all NAND operations, if V_{DD} is below the V_{LKO} threshold.

In the V_{DD} range from V_{LKO} to the lower limit of nominal range, the $\overline{WP}$ pin should be kept low (V_{IL}) to guarantee hardware protection during power transitions as shown in the below figure.

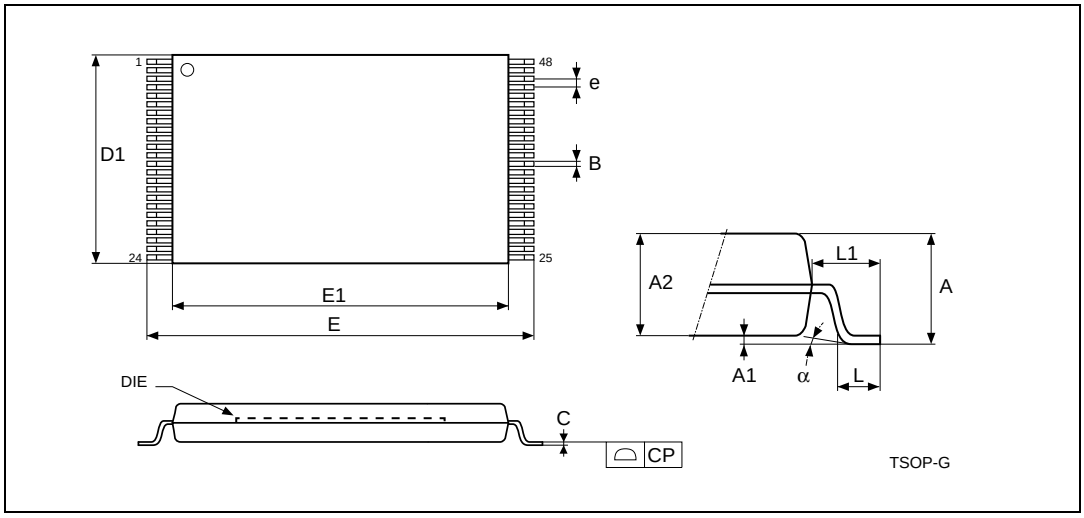
Figure 35. Data protection



11 Package mechanical

To meet environmental requirements, Numonyx offers these devices in RoHS compliant packages, which have a lead-free second-level interconnect. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. RoHS compliant specifications are available at www.micron.com.

Figure 36. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package outline

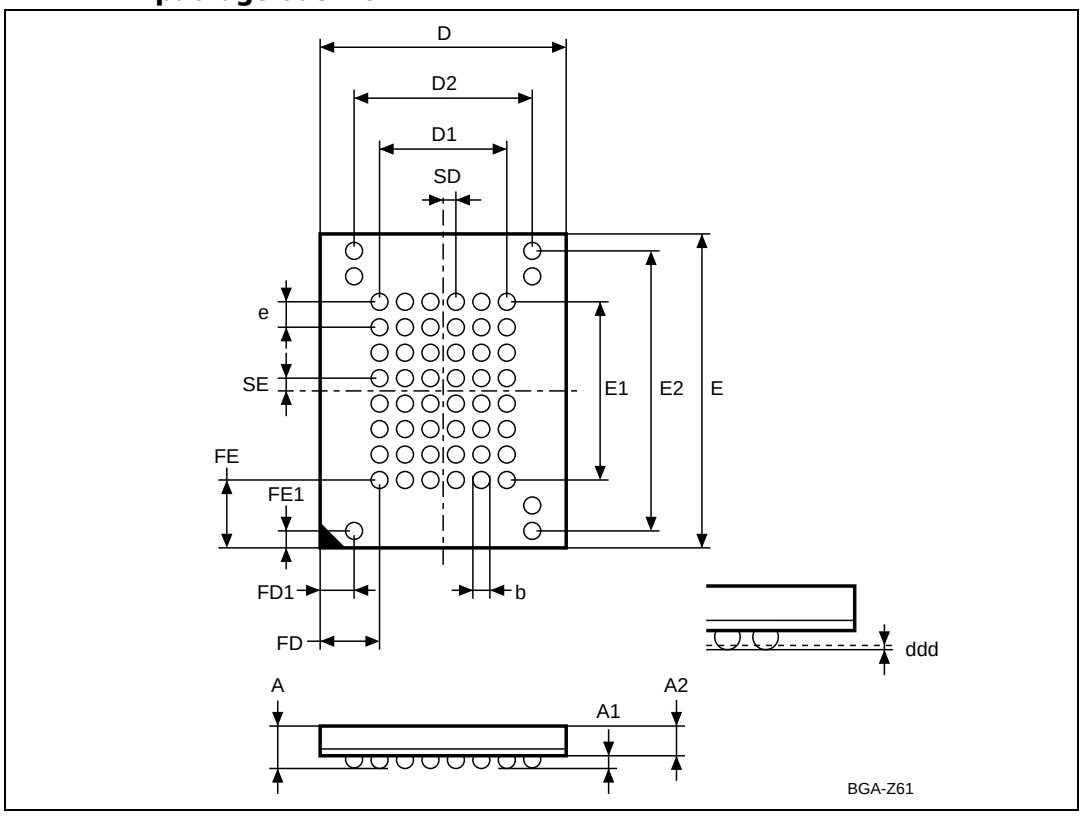


1. Drawing is not to scale.

Table 22. TSOP48 - 48 lead plastic thin small outline, 12 x 20mm, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.200	–	–	0.0472
A1	0.100	0.050	0.150	0.0039	0.0020	0.0059
A2	1.000	0.950	1.050	0.0394	0.0374	0.0413
B	0.220	0.170	0.270	0.0087	0.0067	0.0106
C	–	0.100	0.210	–	0.0039	0.0083
CP	–	–	0.080	–	–	0.0031
D1	12.000	11.900	12.100	0.4724	0.4685	0.4764
E	20.000	19.800	20.200	0.7874	0.7795	0.7953
E1	18.400	18.300	18.500	0.7244	0.7205	0.7283
e	0.500	–	–	0.0197	–	–
L	0.600	0.500	0.700	0.0236	0.0197	0.0276
L1	0.800	–	–	0.0315	–	–
a	3°	0°	5°	3°	0°	5°

Figure 37. VFBGA55 8 x 10 mm - 6 x 8 active ball array, 0.80 mm pitch, package outline



1. Drawing is not to scale

Table 23. VFBGA 8 x 10 x 1.05 mm- 6 x 8 + 7 ball array, 0.8 pitch, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.05	–	–	0.041
A1	–	0.25	–	–	0.010	–
A2	0.65	–	–	0.026	–	–
b	0.45	0.40	0.50	0.018	0.016	0.020
D	8.00	7.90	8.10	0.315	0.311	0.319
D1	4.00	–	–	0.157	–	–
D2	5.60	–	–	0.220	–	–
ddd	–	–	0.10	–	–	0.004
E	10.00	9.90	10.10	0.394	0.390	0.398
E1	5.60	–	–	0.220	–	–
E2	8.80	–	–	0.346	–	–
e	0.80			0.031		
FD	2.00	–	–	0.079	–	–
FD1	1.20	–	–	0.047	–	–
FE	2.20	–	–	0.087	–	–
FE1	0.60	–	–	0.024	–	–
SD	0.40			0.016		
SE	0.40			0.016		

12 Part numbering

Note: Not all combinations are necessarily available. For a list of available devices or for further information on any aspect of these products, please contact your nearest Numonyx sales office.

Table 24. Ordering information scheme

Example: NAND128 R 3 A 2 B ZA 6 E

Device type
NAND flash memory

Density
128 = 128 Mbits
256 = 256 Mbits

Operating voltage
W = V_{DD} = 2.7 to 3.6 V

Bus width
3 = x8
4 = x16(1)

Family identifier
A = 528 bytes/264 word page

Device options
0 = No options (Chip Enable 'care'; sequential row read enabled)
2 = Chip Enable 'don't care' enabled
A = Automotive testing

Product version
A = first version
B = second version
C = third version

Package
N = TSOP48 12 x 20 mm
ZA = VFBGA55 8 x 10 x 0.1 mm

Temperature range
6 = –40 to 85 °C
X = –40 to 85 °C; Included in product longevity program (PLP)

Option
E = RoHS compliant package, standard packing
F = RoHS compliant package, tape and reel packing

1. x16 organization only available for MCP.

Appendix A Hardware interface examples

NAND flash devices can be connected to a microcontroller system bus for code and data storage. For microcontrollers that have an embedded NAND controller the NAND flash can be connected without the addition of glue logic (see *Figure 38*). However, a minimum of glue logic is required for general purpose microcontrollers that do not have an embedded NAND controller. The glue logic usually consists of a flip-flop to hold the Chip Enable, Address Latch Enable, and Command Latch Enable signals stable during command and address latch operations, and some logic gates to simplify the firmware or make the design more robust.

Figure 39 provides an example of how to connect a NAND flash to a general purpose microcontroller. The additional OR gates allow the microcontroller's Output Enable and Write Enable signals to be used for other peripherals. The OR gate between A3 and CSn maps the flip-flop and NAND I/O in different address spaces inside the same chip select unit, which improves the setup and hold times and simplifies the firmware. The structure uses the microcontroller DMA (direct memory access) engines to optimize the transfer between the NAND flash and the system RAM.

For any interface with glue logic, the extra delay caused by the gates and flip-flop must be taken into account. This delay must be added to the microcontroller's AC characteristics and register settings to get the NAND flash setup and hold times.

For mass storage applications (hard disk emulations or systems where a huge amount of storage is required) NAND flash memories can be connected together to build storage modules (see *Figure 40*).

Figure 38. Connection to microcontroller, without glue logic

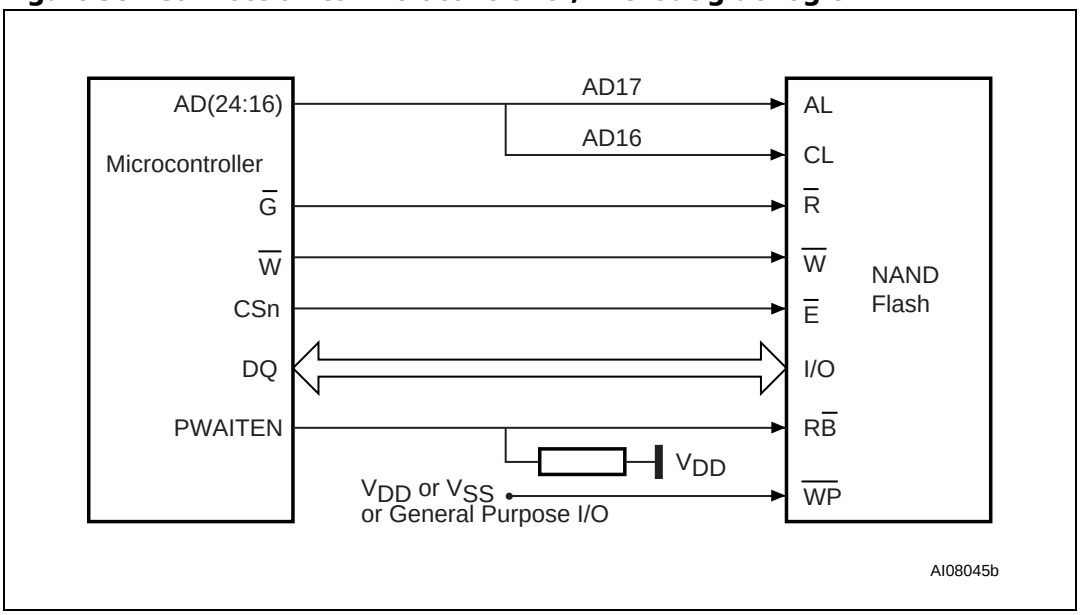


Figure 39. Connection to microcontroller, with glue logic

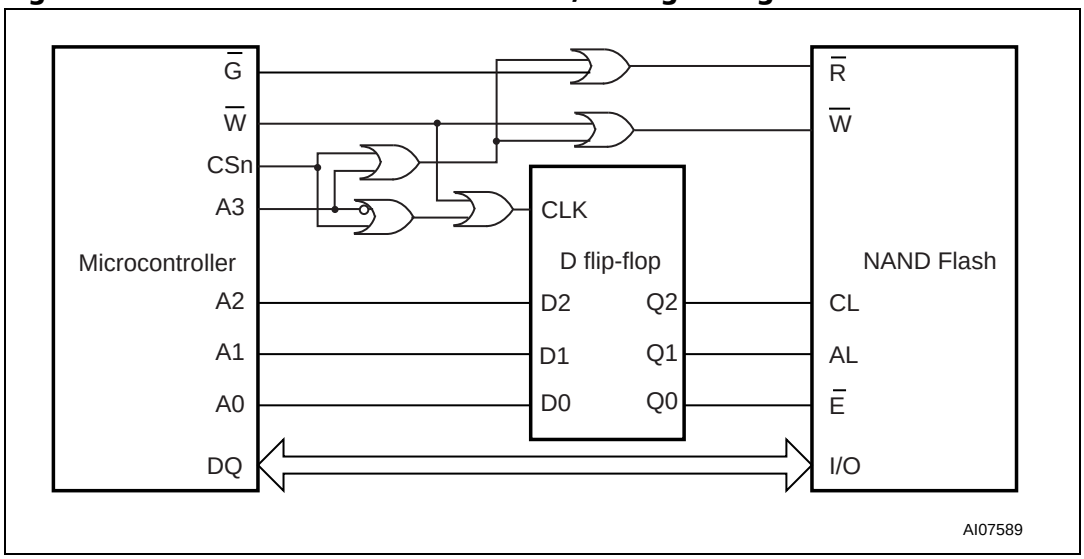
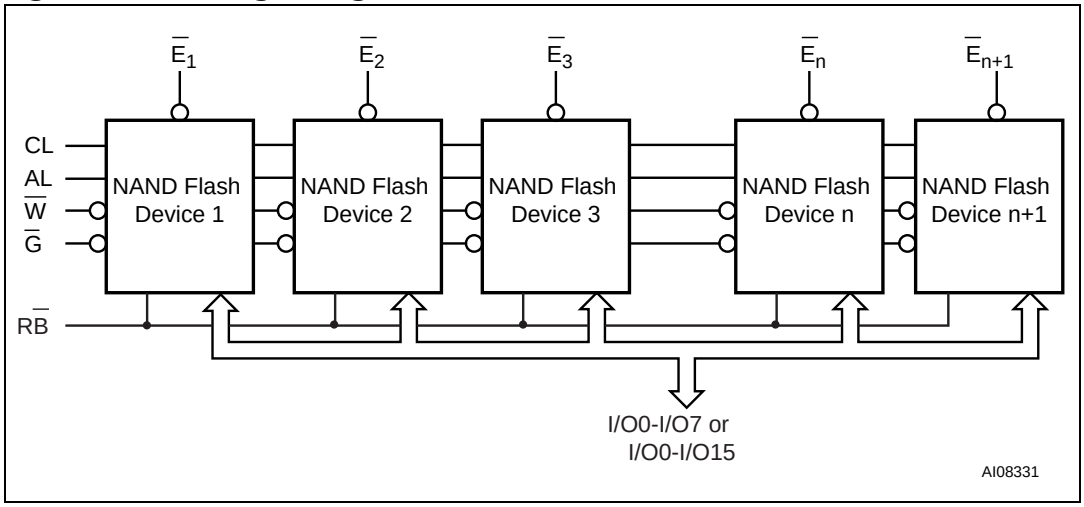


Figure 40. Building storage modules



13 Revision history

Table 25. Document revision history

Date	Ver.	Revision details
06-Jun-2003	1	First Issue
07-Aug-2003	2	Design Phase
27-Oct-2003	3	Engineering Phase
03-Dec-2003	4	Document promoted from Target Specification to Preliminary Data status. V_{CC} changed to V_{DD} and I_{CC} to I_{DD}. Changed title of *Table 2* "*Table 2.: Product description*" and page program typical timing for NANDXXXR3A devices corrected. *Table 1: NAND128-A and NAND256-A device summary*, inserted on page 2.
13-Apr-2004	5	WSOP48 and VFBGA55 packages added, VFBGA63 (9 x 11 x 1mm) removed. Figure 19., Cache Program Operation, modified and note 2 modified. Note removed for t_{WLWH} timing in *Table 20: AC characteristics for command, address, data input*. Meaning of t_{BLBH4} modified, partly replaced by t_{WHBH1} and t_{WHRL} min for 3V devices modified in <Blue>Table 21., AC characteristics for operations. References removed from *Section 13: Revision history* section and reference made to ST Website instead. *Figure 5: VFBGA55 connections, x8 devices (top view through package)*, *Figure 6: VFBGA55 connections, x16 devices (top view through package)*, *Figure 27: Page read A/read B operation AC waveform* and *Figure 30: Block erase AC waveform* modified. *Section 6.8: Read electronic signature* clarified and *Figure 26: Read electronic signature AC waveform*, modified. Note 2 to *Figure 28: Read C operation, one page AC waveform* removed. Only 00h Pointer operations are valid before a Cache Program operation. Note added to *Figure 30: Block erase AC waveform*. Small text changes.
28-May-2004	6	TFBGA55 package added (mechanical data to be announced). 512Mb Dual Die devices added. Figure 19., Cache Program Operation modified. Package code changed for TFBGA63 8.5 x 15 x 1.2mm, 6x8 ball array, 0.8mm pitch (1Gbit Dual Die devices) in *Table 24: Ordering information scheme*.
02-Jul-2004	7	Cache Program removed from document. TFBGA55 package specifications added (Figure 40., TFBGA55 8 x 10mm - 6x8 active ball array - 0.80mm pitch, Package Outline and Table 25., TFBGA55 8 x 10mm - 6x8 active ball array - 0.80mm pitch, Package Mechanical Data). Test conditions modified for V_{OL} and V_{OH} parameters in <Blue> , .
01-Oct-2004	8	*Section 6.5: Block erase* last address cycle modified. Definition of a Bad Block modified in *Section 7.1: Bad block management*. RoHS compliance added to *Section 1: Description*. *Figure 2: Logic block diagram* modified. Document promoted from Preliminary Data to Full Datasheet status.

Table 25. Document revision history (continua)

Date	Ver.	Revision details
03-Dec-2004	9	Automatic Page 0 Read at Power-Up option no longer available. PC Demo board with simulation software removed from list of available development tools. *Section 3.5: Chip Enable (E)* paragraph clarified.
13-Dec-2004	10	R_{ref} parameter added to the description of the family clarified in the *Section 1: Description*.
25-Feb-2005	11	WSOP48 replaced with USOP48 package, VFBGA63 (8.5 x 15 x 1mm) replaced with VFBGA63 (9 x 11 x 1mm) package, TFBGA63 (8.5 x 15 x 1mm) replaced with TFBGA63 (9 x 11 x 1.2mm) package. Changes to *Table 21: AC characteristics for operations*.
23-June-2005	12	t_{EHBH}, t_{EHEL}, t_{RHBL} removed throughout document. TFBGA63 and TFBGA55 packages removed throughout document. Sequential Row Read removed throughout document. T_{EHQX} and T_{RHQX} added throughout document. *Section 10.2: Data protection* section and *Figure 20: Equivalent testing circuit for AC characteristics measurement* added. Modified *Section 3.7: Write Enable (W)*, *Section 3.5: Chip Enable (E)*, *Section 6.2: Read memory array*, *Section 6.3: Page program*, *Section 6.8: Read electronic signature*, *Section 7.1: Bad block management* and *Section 12: Part numbering*. *Figure 10: Read (A, B, C) operations* and *Figure 26: Read electronic signature AC waveform* modified.
09-Aug-2005	13	Note added to *Figure 3: TSOP48 connections, x8 devices* and *Figure 4: TSOP48 connections, x16 devices* regarding the USOP package.
20-Jun-2008	14	Removed all information pertaining to the 512-Mbit and 1-Gbit devices. Applied Numonyx branding.
13-Aug-2008	15	Removed all the information pertaining the 1.8 V devices (VDD = 1.7 to 1.95 V) and the USOP48 and VFBGA63 packages. Added the sequential row read option throughout the document.
30-Nov-2009	16	Added security features on the cover page and in Section 1: Description. Updated Figure 32: Ready/Busy AC waveform and Figure 34: Resistor value versus waveform timings for Ready/Busy signal. References to ECOPACK removed and replaced by RoHS compliance. Modified dimension A2 of the VFBGA55 package in Table 22. Added automotive testing option in Table 23: Ordering information scheme.
19-Oct-2012	17	Added X = –40 to 85 °C; Included in product longevity program (PLP) under temperature range in ordering information scheme table.

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