



STW90NF20

N-channel 200 V, 0.019 Ω , 83 A, TO-247
low gate charge STripFET™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STW90NF20	200 V	< 0.023 Ω	83 A

- Exceptional dv/dt capability
- Low gate charge
- 100% Avalanche tested

Application

- Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters

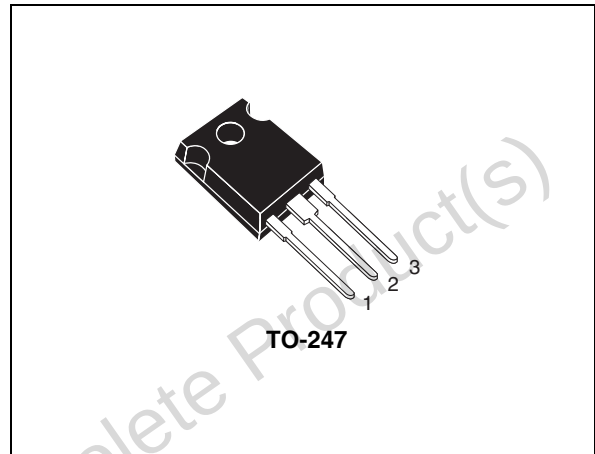


Figure 1. Internal schematic diagram

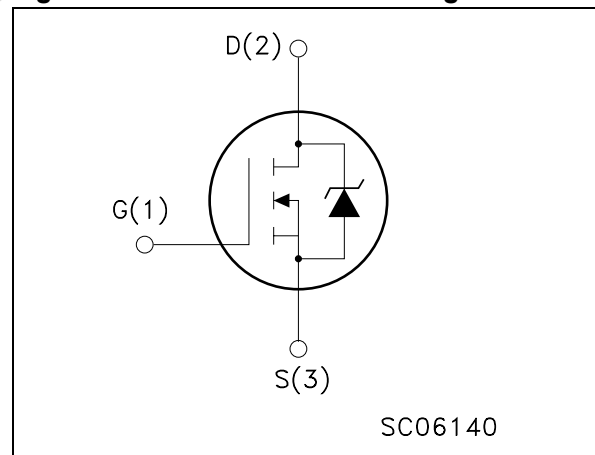


Table 1. Device summary

Order code	Marking	Package	Packaging
STW90NF20	90NF20	TO-247	Tube

Contents

1 **Electrical ratings** 3

2 **Electrical characteristics** 4

 2.1 Electrical characteristics (curves) 6

3 **Test circuits** 8

4 **Package mechanical data** 9

5 **Revision history** 11

Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	200	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	83	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	52	A
$I_{DM}^{(1)}$	Drain current (pulsed)	332	A
	Derating factor	2.4	W/ $^{\circ}\text{C}$
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	300	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-50 to 150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 83\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} \leq 80\% V_{(BR)DSS}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.42	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^{\circ}\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^{\circ}\text{C}$

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	83	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	400	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	200			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating @ } 125\text{ }^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{DS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 45\text{ A}$		0.018	0.023	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 45\text{ A}$		40		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		5736 1126 196		pF pF pF
$C_{oss\text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to } 160\text{ V}$, $V_{GS} = 0$		687		pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain		1.7		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 160\text{ V}$, $I_D = 83\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 15)		164 46 72		nC nC nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 100\text{ V}$, $I_D = 41.5\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$, (see Figure 14)		24		ns
t_r	Rise time			138		ns
$t_{d(off)}$	Turn-off delay time			148		ns
t_f	Fall time			142		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				83	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				332	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 83\text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 83\text{ A}$, $V_{DD} = 100\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ (see Figure 19)		200		ns
Q_{rr}	Reverse recovery charge			1.6		μC
I_{RRM}	Reverse recovery current			16		A
t_{rr}	Reverse recovery time	$I_{SD} = 83\text{ A}$, $V_{DD} = 100\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ $T_j = 150^\circ\text{C}$ (see Figure 19)		235		ns
Q_{rr}	Reverse recovery charge			2.2		μC
I_{RRM}	Reverse recovery current			18		A

1. Pulse with limited by maximum temperature

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

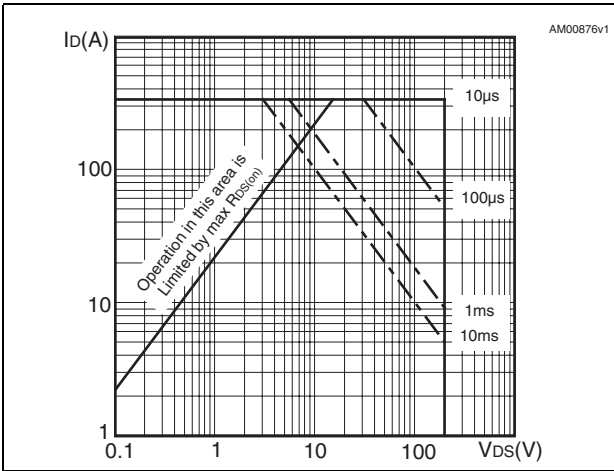


Figure 3. Thermal impedance

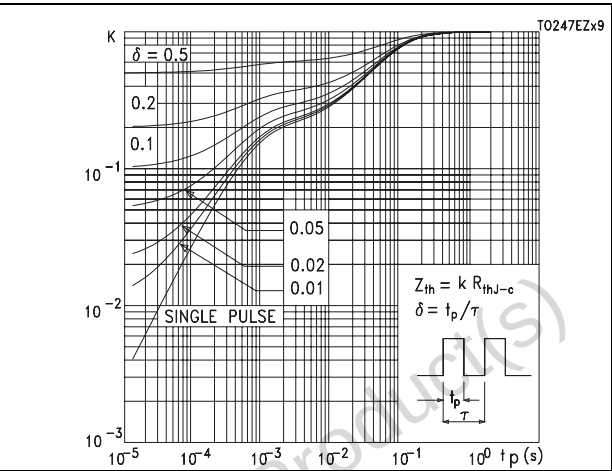


Figure 4. Output characteristics

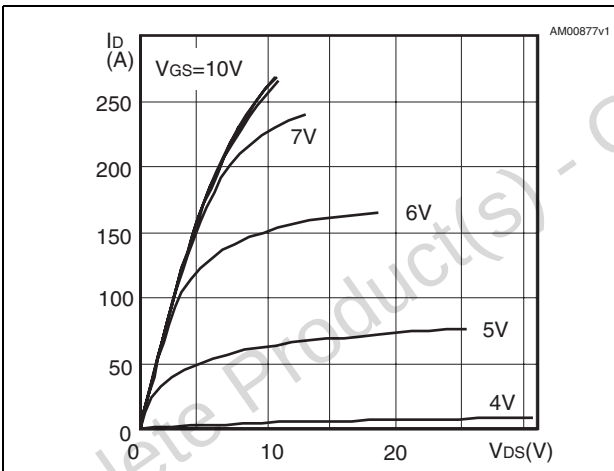


Figure 5. Transfer characteristics

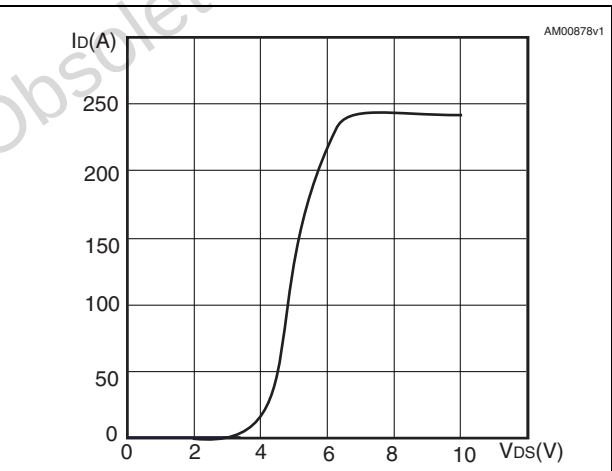


Figure 6. Normalized BV_{DSS} vs temperature

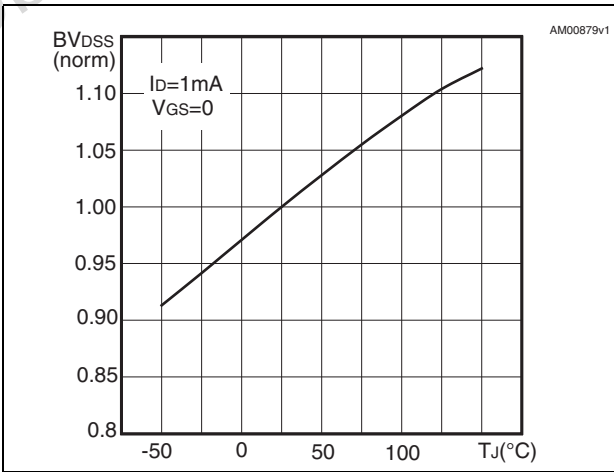


Figure 7. Static drain-source on resistance

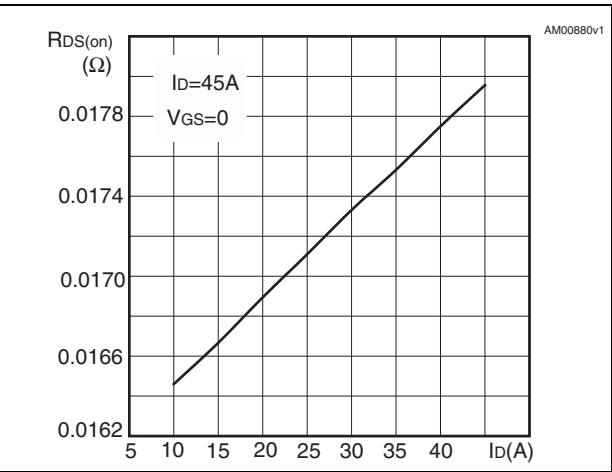


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

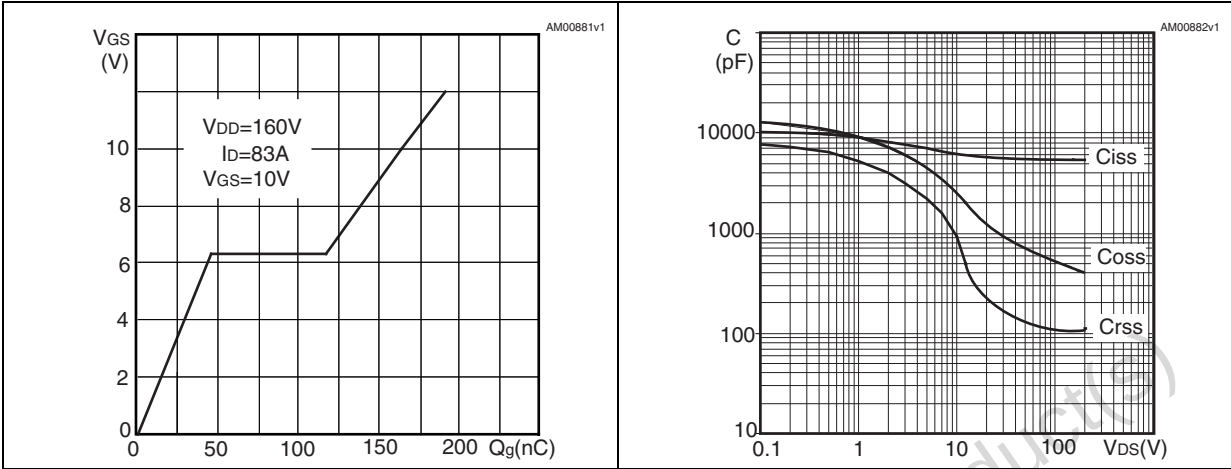


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

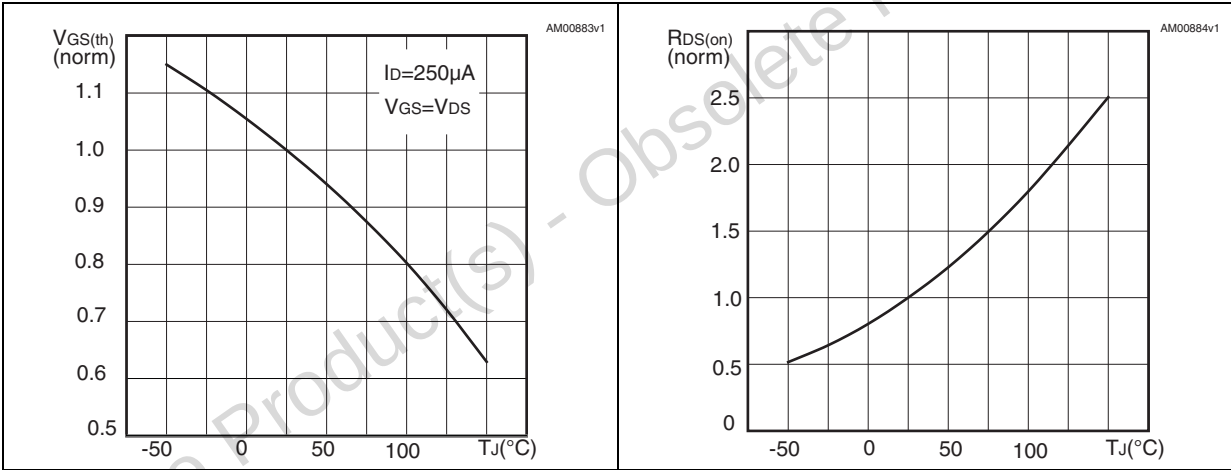
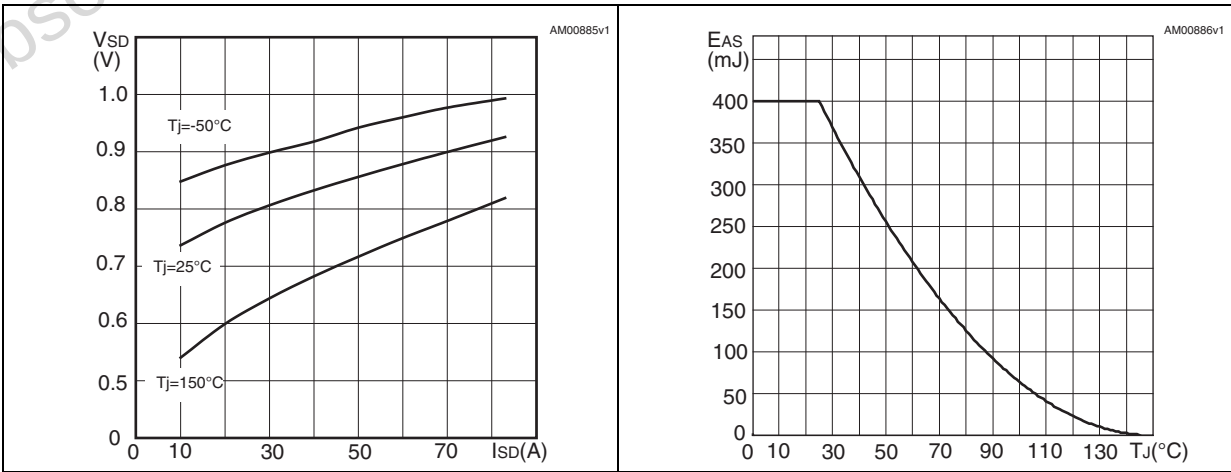


Figure 12. Source-drain diode forward characteristics Figure 13. Maximum avalanche energy vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load



Figure 15. Gate charge test circuit

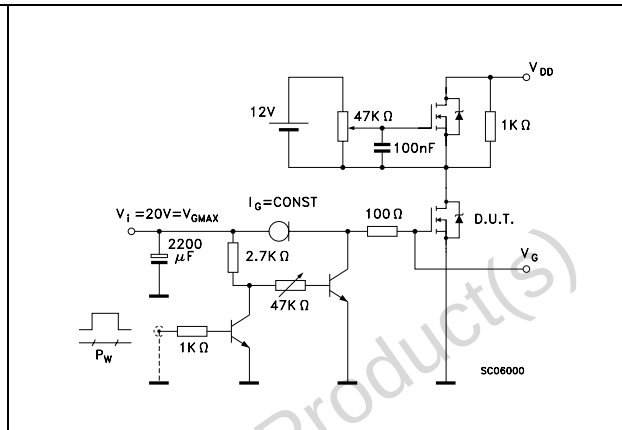


Figure 16. Test circuit for inductive load switching and diode recovery times

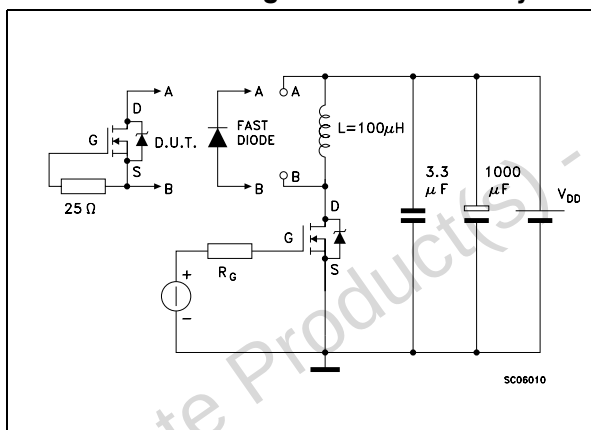


Figure 17. Unclamped inductive load test circuit

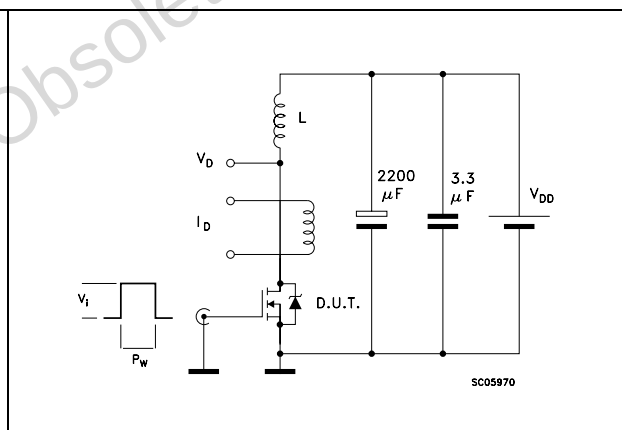


Figure 18. Unclamped inductive waveform

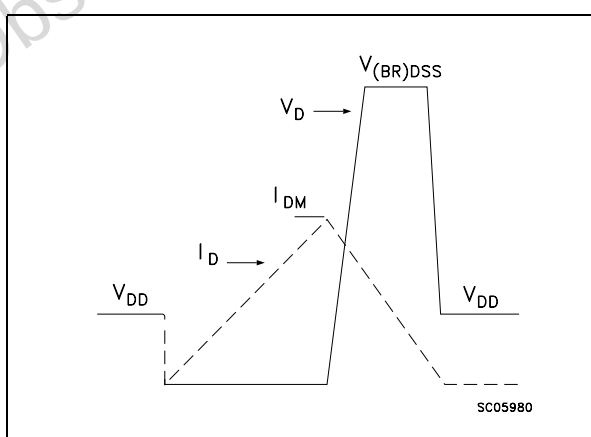
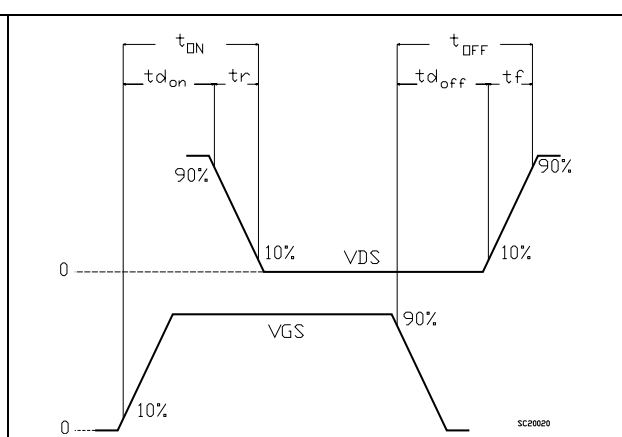


Figure 19. Switching time waveform



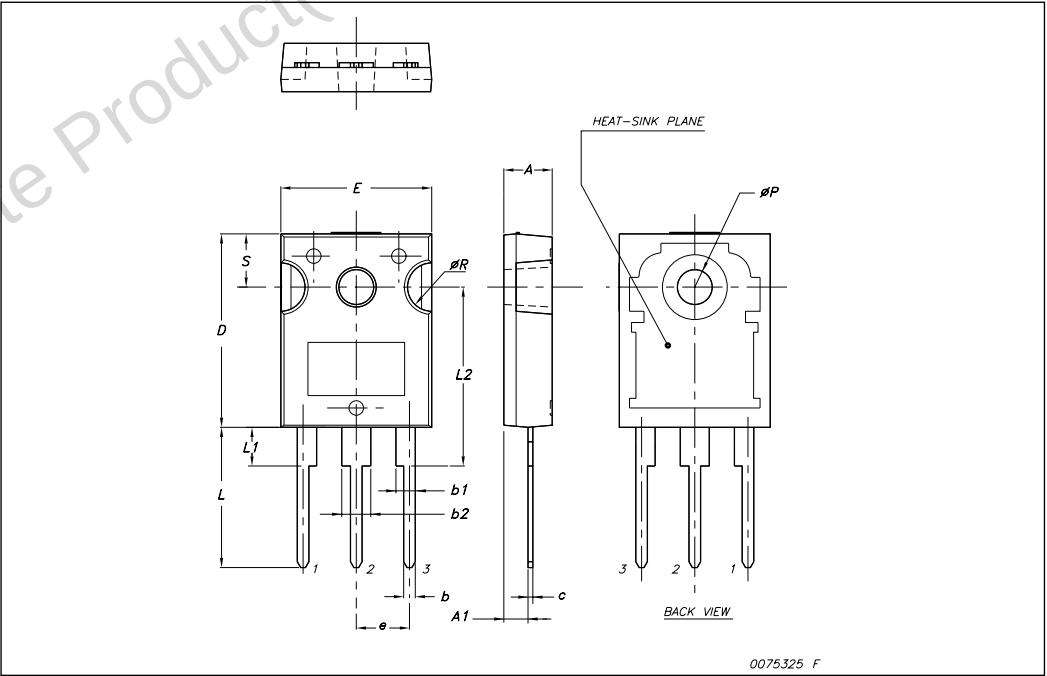
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Obsolete Product(s) - Obsolete Product(s)

TO-247 Mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
28-Aug-2007	1	First release
04-Aug-2008	2	Document status promoted from preliminary data to datasheet.

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