



## LIN BUS TRANSCEIVER

### **1 FEATURES**

- Single-wire transceiver for LIN-protocol
- Transmission rate up to 20 kbaud
- Operating power supply voltage range 6V ≤ Vs ≤ 26V (40V for transients)
- Low quiescent current in sleep mode (typ.10µA)
- Wake-up through LIN-bus, Enable input (from μC CMOS compatible) or Wake-up input (edge driven)
- Wide input and output range  $-24V \le V_{LIN} \le Vs$
- Integrated pull/down/up resistors for LIN, TxD, RxD, EN, INH
- Inhibit output with low resistance (<40Ω) versus</li>
  Vs and short circuit protection
- CMOS compatible TxD, RxD Interface
- EMI robustness optimised
- Thermal shutdown and LIN short circuit protection



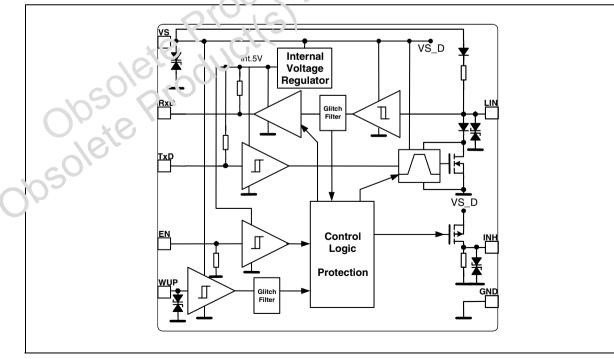
#### Table 1. Order Codes

Part Number	Packaje
L9638D	50-5
L9638D013TR	Tape & Roel

### 2 DESCRIPTION

The L9638 is a monolithic integrated circuit for LIN-bug interace function between the protocol hardle. In the controller and the physical bus in automotive  $a_i$  of cutions.

As well as it can be used in standard ISO 9141 systems.

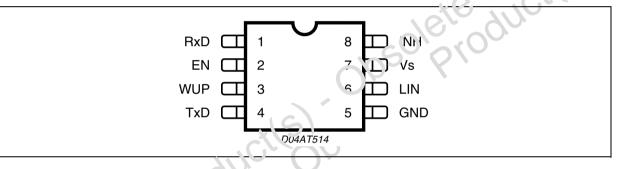


### Figure 1. Block Diagram

Pin No.	Pin Name	Function
1	RxD	Receive data Output
2	EN	Enable Input Digital control signal for low power modes
3	WUP	Wake-Up Input Local wake-up from sleep mode sensitive to positive and negative edges
4	TxD	Transmit data Input
5	GND	Ground
6	LIN	Bidirectional I/O
7	Vs	Supply voltage
8	INH	Inhibit Output, battery related high side switch for controlling externa, Voltage Regulator

### Table 2. Pin Description

### Figure 2. Pin Connection



### Table 3. Absolute Maximum Radings

Symbol	Parameter	Value	Unit
VS	Supply Voltage	-0.3 to 40	V
V <sub>LIM</sub>	Pir Voltage	-24 to 40	V
VINH WITE	r in Voltage	-0.3 to 40	V
V <sub>R (D</sub> ,T) D, ÉN	Pin Voltage	-0.3 to 6	V
VESD	HBM: all pins withstand ±2KV; pin 6 (LIN) is able to withstand ±8kV versus GND and +8/-5kV versus V <sub>S</sub>		

### Table 4. Thermal Data

Symbol	Parameter	Value	Unit
$T_{J_{OP}}$	Operating junction temperature	-40 to150	°C
R <sub>th j-amb</sub>	Thermal steady state junction to ambient resistance	145	K/W
$T_{J\_SD}$	Thermal shutdown temperature	170 ±20	°C
T <sub>stg</sub>	Storage temperature	-55 to 150	°C

### **Table 5. Electrical Characteristics**

(V\_S = 6V to 26V; T\_J = -40 to 150  $^\circ\text{C}$  unless otherwise specified)

Item	Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
1	Supplies						
1.1	Vs	Supply Voltage		6		26	V
1.2	I <sub>Sleep</sub>	Supply Vs Curent in sleep mode	V <sub>EN</sub> = V <sub>EN low</sub>		10	30	μA
1.3	I <sub>Short</sub>	Supply Vs Curent with bus short circuit	V <sub>EN</sub> = V <sub>EN low</sub>	150	500	1700	μA
1.4	I <sub>DStand-by</sub>	Supply Vs Current in Stand- by Mode with bus recessive	$ \begin{array}{l} V_{LIN} = V_{LINHigh} \\ V_{EN} = V_{ENLow} \\ V_{TxD} = V_{TxDHigh} \end{array} $	30	100	200	μA
1.5	I <sub>DStand-by</sub>	Supply Vs Current in Stand- by Mode with bus dominant (Receive only Mode)	V <sub>LIN</sub> = V <sub>LINLow</sub> V <sub>EN</sub> = V <sub>ENLow</sub>	0.5	1.1	25	mA
1.6	Is <sub>Normal</sub>	Supply Vs Current in Normal Mode with bus recessive	$V_{EN} = V_{ENHigh}$ $V_{LIN} = V_{LINHigh}$ $V_{TxD} = V_{TxDHigh}$	300	500	700	μA
1.7	Is <sub>Normal</sub>	Supply Vs Current in Normal Mode with bus dominant	V <sub>EN</sub> = V <sub>ENHigh</sub> V <sub>LIN</sub> = V <sub>LINLc</sub> , V <sub>TxD</sub> = V <sub>TxD</sub> ow	0.9	1.8	3.5	mA
2	LIN Bus Int	erface	10	1			
2.1	V <sub>BUSDom</sub>	Receive Threshold Voltage recessive to dominant strate	V <sub>LiN</sub> <13V	0.4	0.45	0.5	Vs
2.2	V <sub>BUSRec</sub>	Receive Threshold Voltage dominant to receive state	V <sub>LIN</sub> ≥8V	0.5	0.55	0.6	Vs
2.3	V <sub>HYS</sub>	Receive 7 nreshold Hysteresis	V <sub>BUSRec</sub> -V <sub>BUSDom</sub>	0.05	0.1	0.17	Vs
2.4	V <sub>BUScn</sub>	Tc.'erance centre value of Receiver	(VBUS <sub>Rec</sub> +VBUS <sub>Dom</sub> )/2	0.475	0.5	0.525	Vs
2.5		Input Current dominant state	$V_{TxD} = V_{TxDLow}$ $V_{LIN} = V_{S}$	40	100	160	mA
2.5.1	ILINOff	Input Current recessive state		-10		10	μA
2.5.2	ILINOff	Input Current recessive state	$V_{TxD} = V_{TxDHigh}; V_S = 12V;$ $V_{LIN} = 0V$ (Bus dominant )	-1			mA
2.6	VLINDom	Drive Voltage dominant state	$V_{TxD} = V_{TxDLow}$ $I_{LIN} = 40mA$			1.2	V
2.7	R <sub>LIN</sub>	Output pull up resistor		20	30	47	kΩ
2.8	f <sub>LIN-RxD</sub>	Transmission Frequency	$R_{Vs-LIN} = 1100\Omega$ $C_{LIN-GND} = 10nF$	20			kHz
2.9	d <sub>VLIN/dt</sub>	Slew rate rising edge	From 10% to 90% of V <sub>LIN</sub>	1	2	3	V/µs

### Table 5. Electrical Characteristics (continued)

Item	Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
2.10	d <sub>VLIN/dt</sub>	Slew rate falling edge	From 90% to 10% of V <sub>LIN</sub>	-3	-2	-1	V/µs
2.11	t <sub>sym</sub>	Rising/ Falling edge symmetry	t <sub>sym</sub> = t <sub>slope_fall</sub> - t <sub>slope_rise</sub>	-5		-5	μs
2.12	t <sub>trans_pd</sub>	Propagation delay of transmitter	See Fig.2 t <sub>trans_pd</sub> = max (t <sub>trans_pdr</sub> , trans_pdf)			4	μs
2.13	t <sub>rec_pd</sub>	Propagation delay of receiver	See Fig.2 trec_pd = max (trec_pdr, trec_pdf)			6	μs
2.14	t <sub>rec_sym</sub>	Symmetry of receiver propagation delay rising edge w.r.t. falling edge	See Fig.2 t <sub>rec_sym</sub> = (t <sub>rec_pdf</sub> -trec_pdr)	-2		2	μs
2.15	t <sub>trans_sym</sub>	Symmetry of transmitter propagation delay rising edge w.r.t. falling edge	See Fig.2 ttrans_sym = (ttrans_pdf -ttrans_pdr)	-2	250	2	μs
2.16	t <sub>LINgs</sub>	Bus wake-up glitch suppression time	See Fig.3 V <sub>LIN</sub> = V <sub>LINLow</sub>		40	100	μs
3	Transmissi	on Input TxD	055	27			
3.1	VT <sub>xDLow</sub>	Input Voltage dominant state	ete			1.5	V
3.2	VT <sub>xDHigh</sub>	Input Voltage recessive state	SISO	3.5			V
3.3	RT <sub>xD</sub>	TxD pull up resisto		5	10	25	KΩ
4	Receive Ou	Itput RxD					
4.1	VR <sub>xDLow</sub>	Output Voltage dominant	I <sub>RxD</sub> = 2mA			1.5	V
4.2	VR <sub>xDHigt</sub>	Dutput Voltage recessive	I <sub>RxD</sub> ≥10μA	4.5			V
4.2	<b>F</b> <sub>RxD</sub>	RxD pull up resistor		5	10	25	kΩ
5	Inhibit Out	out INH					
5.1	RON(INH)	Switch on resistance between Vs and INH	I <sub>INH</sub> =-15mA; Vs=13.5V		20	40	Ω
5.2	I <sub>ON(INH)</sub>	INH output current	Normal or stand-by mode	15	30	50	mA
5.3	R <sub>OFF(INH)</sub>	Switch off INH pull down resistor		5	10	25	kΩ
6	Wake Up In	put WUP					
6.1	V <sub>WUPLow</sub>	Low level input voltage				1.5	V
6.2	V <sub>WUPHigh</sub>	High level input voltage		3.5		Vs+0. 3	V

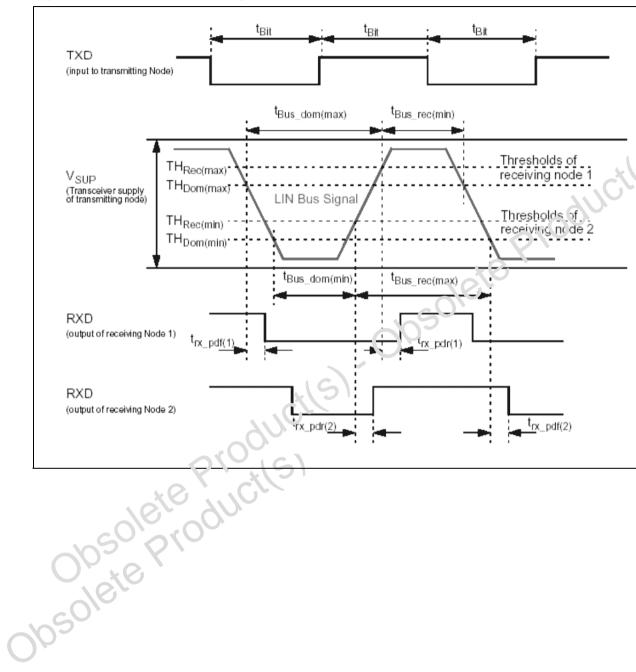
( $V_S = 6V$  to 26V;  $T_J = -40$  to 150 °C unless otherwise specified)

### Table 5. Electrical Characteristics (continued)

Item	Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
6.3	t <sub>WUPgs</sub>	Remote wake-up delay time	Transitioning on WUP		40	100	μs
7	Enable Inpu	ut EN	I				
7.1	VENLow	Low level input voltage				1.5	V
7.2	VEN <sub>High</sub>	High level input voltage		3.5			V
7.3	R <sub>EN</sub>	EN pull down resistor		5	10	25	KΩ
7.4	tgts	Go to sleep delay time	$V_{EN} = V_{ENlow}$		40	100	μs
7.5	t <sub>ENgs</sub>	EN wake-up glitch suppression time	$V_{EN} = V_{ENhigh}$		40	100	μs
8	AC Timing	Parameters	I	1		0	
8.1	D1	Duty Cycle 1	$\begin{array}{l} TH_{Rec(max)} = 0.744 \ x \ V_{SUP}; \\ TH_{Dom(max)} = 0.581 \ x \ V_{SUP}; \\ Vsup = 7.0 \ to \ 18V; \ t_{bit} = 50 \mu s; \\ D1 = t_{Bus\_rec(min)}/2 \ x \ t_{Bit} \\ (C_{BUS}; \ R_{BUS}) \ 1nF; \ 1k\Omega/3.8 \ n^{-}; \\ 660\Omega/10nF; \ 500\Omega \end{array}$	0.396	90	otle	5
8.2	D2	Duty Cycle 2	$\begin{array}{l} TH_{Rec(min)} = 0.2t\ 4\ x\ V_{SUP};\\ TH_{Dom(min)} = 0.+22\ x\ V_{SUP};\\ Vsu_{\mu} = 7.6\ to\ 18V;\ t_{bit} = 50\mu s;\\ D\ 2 - t_{E\ us\_rec(min)}/2\ x\ t_{Bit}\\ (C_{BUS};\ R_{BUS})\ 1nF;\ 1k\Omega/6.8nF;\\ \partial 60\Omega/10nF;\ 500\Omega \end{array}$			0.581	
8.3	D3	Duty Cycle 3	$\begin{array}{l} TH_{Bec(max)} = 0.778 \; x \; V_{SUP}; \\ TH_{Dom(max)} = 0.616 \; x \; V_{SUP}; \\ Vsup = 7.0 \; to \; 18V; \; t_{bit} = 96 \mu s; \\ D3 = t_{Bus\_rec(min)}/2 \; x \; t_{Bit} \\ (C_{BUS}; \; R_{BUS}) \; 1nF; \; 1k\Omega/6.8nF; \\ 660\Omega/10nF; \; 500\Omega \end{array}$	0.417			
8.4		Duty Cycle 4	$\begin{array}{l} TH_{Rec(min)} = 0.251 \ x \ V_{SUP}; \\ TH_{Dom(min)} = 0.389 \ x \ V_{SUP}; \\ Vsup = 7.6 \ to \ 18V; \ t_{bit} = 96\mu s; \\ D4 = t_{Bus\_rec(min)}/2 \ x \ t_{Bit} \\ (C_{BUS}; \ R_{BUS}) \ 1nF; \ 1k\Omega/6.8nF; \\ 660\Omega/10nF; \ 500\Omega \end{array}$			0.591	
9	Fault Cond	itions	1	1	1		
9.1	I <sub>LIN_NO_GND</sub>	LIN current with GND disconnected		-1		1	mA
9.2	I <sub>LIN_NO_Vs</sub>	LIN current with V <sub>S</sub> grounded	$V = GND, 0V < V_{LIN} < 18V $ (1)			100	μA
	L	L	ļ	I	I		

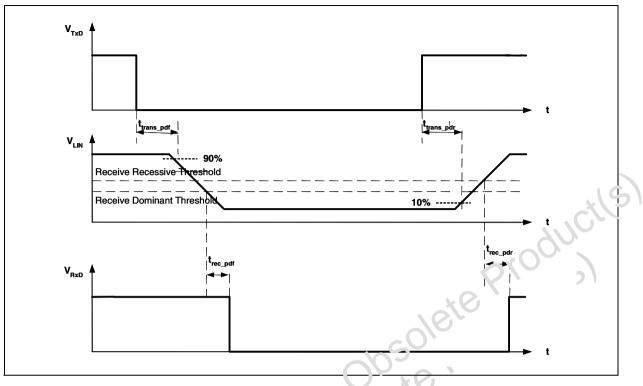
Note: 1. Room temperature evaluated - no 100% tested

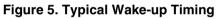
### **3 TIMING DIAGRAM**



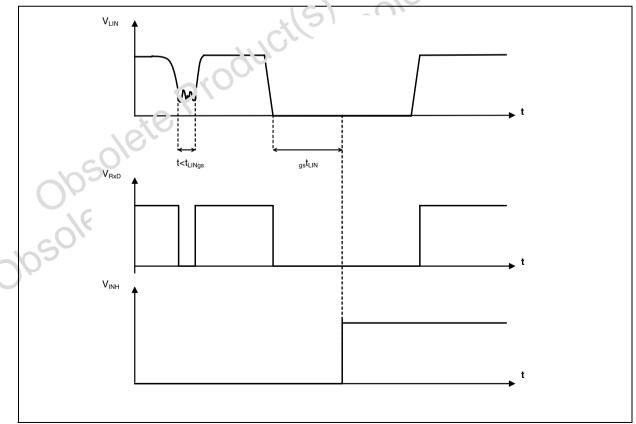
#### Figure 3. Definition of Bus Timing Parameters

### Figure 4. Typical Bus Timing





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### **4 FUNCTIONAL DESCRIPTION**

The L9638 is a monolithic bus driver designed to provide bidirectional serial communication in Local Interconnect Network (LIN).

In addition to the integrated physical layer (specified in LIN specification rev. 2.0), further control in- and output functions simplify various system requirements like controlled power saving modes or additional external wake up capability.

### 4.1 Operating modes

There are four possible modes of operation: normal, standby, sleep and short circuit. The transitions between the various operation modes are described in the diagram.

### 4.2 Standby mode

This mode is reached after power up the system or due to a received wake-up condition from sleep mode. The device is able to receive at RxD, but could not transmit any data. This prevents the disturbance of the LIN bus line due to a not correctly working  $\mu$ C. Entering the standby mode, the INH output will set to HIGH by simultaneous switching off the internal pull down resistor to reduce the current consumption. This allows the control of connected power supply devices.

Therefore for systems, that will be controlled only by the LIN bus line (particular ECUs, that works as slave node) a power management can easy build up on that function. It is recommended to power up the system before the communication will start, otherwise additional delay times have to be regarded.

Because of integrated filtering of external WUP input, the INH output can alternatively be used to simplify a software filtering procedure to detect an external edge sensitive signal by connecting INH versus a series resistor to an interrupt capable input of the  $\mu$ C.

### 4.3 Normal mode

This mode can only be reached from standby or sloep mode by setting the EN input to HIGH. Transmission and receiving of data stream via the LIN line is possible. An integrated pull up resistor in series with a diode at LIN provides either required recessive state (HIGH) as well as a protection against reverse power supply. In master node application, a LOW ohmic resistor in series with a diode has to be connected externally between LIN and battery to allow the maximum transmission rate.

The receiver converts the bettery supply related signal at LIN to a logic supply compatible output at RxD. Integrated filter in addition with the supply voltage related threshold and hysteresis provide optimal noise suppression.

The transmitter shifts the logic supply related data stream at TxD to battery level at LIN. A read back function is possible by evaluating the mirrored state from the LIN line at the output RxD.

### 4.4 Short circuit mode

The L9638 provides a special operation mode for shorted LIN bus lines to ground. In that case, the whole LIN network is blocked. If the protocol handler in the  $\mu$ C detects a "time out" condition, that could be unambiguously identified as a short to ground condition in the bus line, the whole LIN node could be disconnected from the network by setting EN input to LOW.

This will switch INH output from active HIGH to LOW. Additionally RxD output, that remains in the dominant state and maybe block the  $\mu$ C will set to HIGH ohmic state.

The L9638 won't accept any transition at TxD. This short circuit mode will be stable until the dominant state on LIN will be cleared. In that case, the device will switch to the sleep mode. According to that, the current consumption of a blocked LIN network will be reduced to the resulting short circuit current in the LIN line.

Especially for sporadically happening shorts due to damaged cable isolation, the LIN network will be automatically reset. Therefore no special power up procedure is required.



### 4.5 Sleep mode

This mode allows the lowest current consumption of the transceiver. It'll be reached either by setting the EN input to LOW (assuming no occurring wake-up event) while being in the normal mode or in case of a removed short to ground at LIN while being in the short circuit mode.

The INH output will be switched from HIGH to LOW. A further transmission via TxD is prevented. The device is waiting on any wake-up requests either by LIN (dominant level) or WUP (rising or falling edge). This will set the device from sleep mode to standby mode. An implemented filter prevents unwished wake-ups due to occurring glitches or EMI at LIN or WUP.

#### 4.6 Wake-up

The L9638 provides several wake-up conditions from sleep mode:

- Remote wake-up by a dominant level at LIN
- Local wake-up by a falling or rising edge at WUP
- Mode change by setting EN to HIGH

The INH output will be set from LOW to HIGH after each kind of valid wake-up conditions. For remote wake-up via LIN, RxD will be activated and set as well to a dominant state.

This allows fast reaction for powered  $\mu C$  with connected interrupt capable receive  $\therefore$  puts.

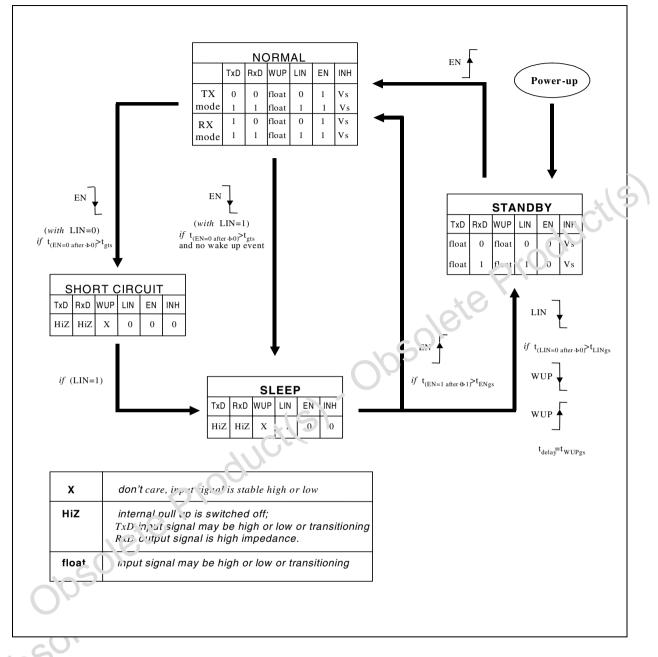
#### 4.7 Fail-safe features

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To prevent possible states, that will block the communication line in case of a failed  $\mu$ C operation, the L9638 has implemented some special fail-safe features:

- After detected a clear short to ground state at the LIN bin try the protocol handler in the μC, the transceiver or the complete power supply of the ECU control logic could be switched off by setting the EN input from HIGH to LOW. The device will stav that special short circuit mode until the state of the LIN bus will switch back from dominant to recessive. No power up or special reset procedures are required to clear that fail-safe state. LCo33 could be reactivated with the usual wake-up signals.
- The TxD and EN inputs support /'efai.!t recessive bus states by internal pull up or down sources
- The output stage of the transmitter is current limited to protect against a shorten LIN to battery
- A thermal shutdown protects the device against over temperature caused destruction. In case of a permanent overload condition, the output stage will be switched off after reaching the shut down temperature and reactionated after cooling down to the switch on temperature.
- Defined cutp is status in under voltage, loss of Vs or GND condition with no impact to the bus line or the compacted μC

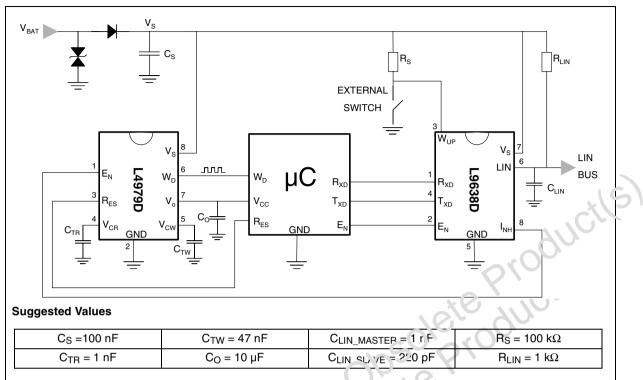
### Figure 6. State Diagram



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### Figure 7. Typical Application Circuit

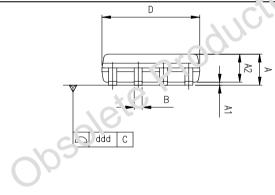
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DIM.		mm			inch	
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
В	0.33		0.51	0.013		0.020
С	0.19		0.25	0.007		0.010
D <sup>(1)</sup>	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
е		1.27			0.050	
н	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k		0	° (min.),	8° (max	.)	
ddd			0.10			0.004
Note: (	sions o Mold fla	r gate bui ash, potru	rrs. Isions or	include m gate burrs I (both sid	s shall not	

### OUTLINE AND MECHANICAL DATA





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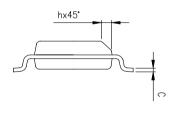
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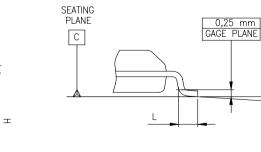
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#### **Table 6. Revision History**

April 2004		Description of Changes
April 2004	1	First Issue
April 2004	2	Changed maturity from Product Preview in Final;
		Corrected Order Codes; Changed min. value of the item 1.4 of the Table 4 in the page 3
October 2004	3	Add V <sub>ESD</sub> in table 3;
	Ũ	Changed numbers item of the table 5 and add item 9
October 2004	4	Updated figure 7 on page11/14.
		obsolete Product

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