



## TDA8139, TDA8139/D

Double (5.1 V and adjustable) voltage regulator with reset and disable functions

### Features

- Input voltage range: 7 V to 18 V
- Output currents up to 750 mA
- Fixed Precision output 1 voltage: 5.1 V  $\pm 2\%$
- Adjustable output 2 voltage: 2.8 to 16 V
- Output 1 with reset function
- Output 2 with disable function by TTL input
- Short-circuit protection at both outputs
- Thermal protection
- Low dropout voltage

### Description

The TDA8139 and the TDA8139/D are monolithic dual positive voltage regulators designed to provide a fixed precision output voltage of 5.1 V and an adjustable voltage between 2.8 and 16 V for currents up to 750 mA.

An internal reset circuit generates a reset pulse when the voltage of OUTPUT1 drops below the regulated voltage value.

OUTPUT2 can be disabled via the TTL input.

Short-circuit and thermal protections are included in all versions.

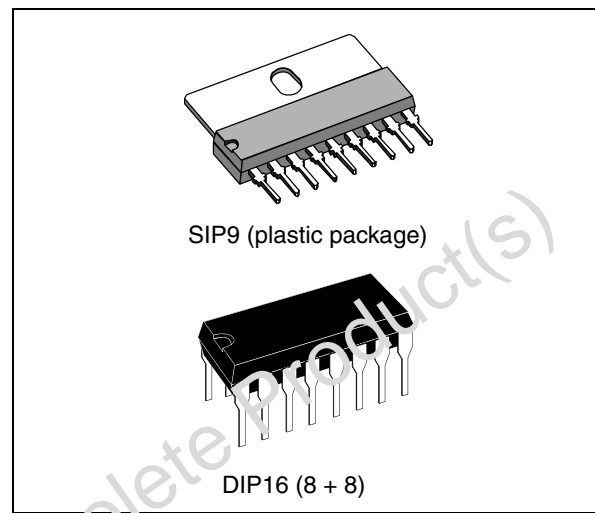
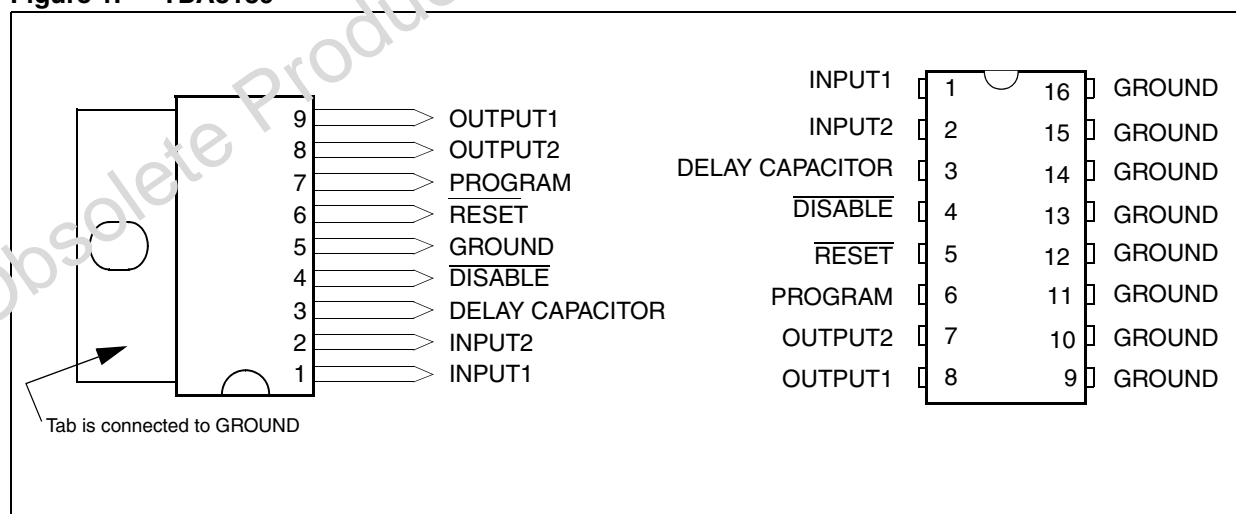


Table 1. Device summary

Order code	Packaging
TDA8139	Tray
TDA8139/D	Tray

Figure 1. TDA8139



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# 1 Description

Figure 2. TDA8139 block diagram

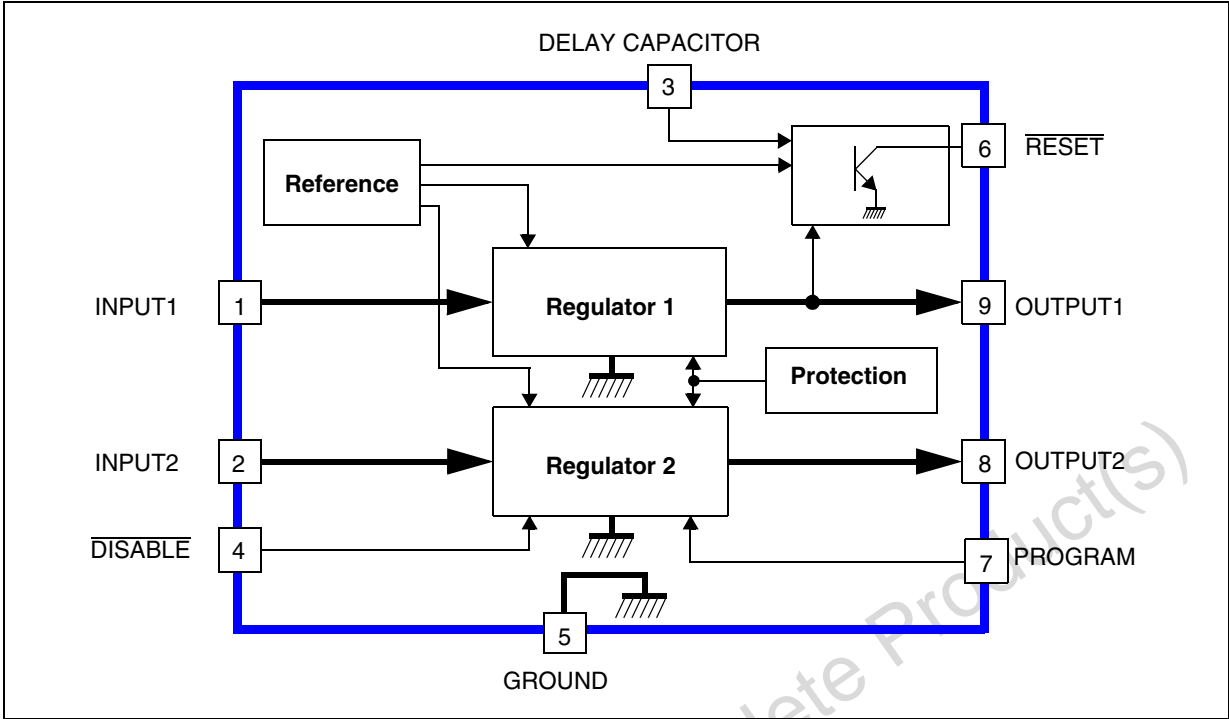
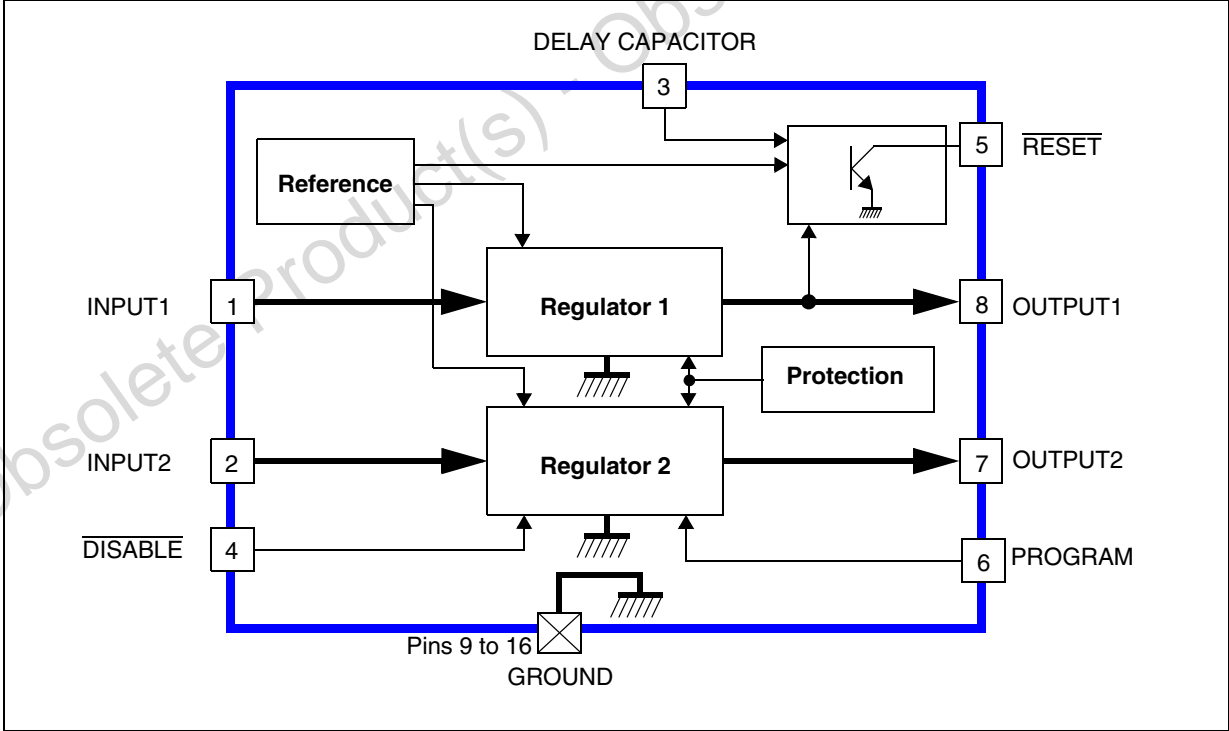


Figure 3. TDA8139/D



## 2 Electrical characteristics

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{IN}$	C input voltage on pins INPUT1 and INPUT2	20	V
$V_{DIS}$	Disable input voltage	20	V
$V_{RST}$	Output voltage on pin $\overline{RESET}$	20	V
$I_{O1,2}$	Output currents	Internally limited	
$P_t$	Power dissipation	Internally limited	
$T_{STG}$	Storage temperature	-65 to +150	°C
$T_J$	Junction temperature	0 to +150	°C

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance (junction-to-case)	TDA8139 TDA8139/D 9 15	°C/W
$R_{thJA}$	Thermal resistance <sup>(1)</sup> (junction-to-ambient)	TDA8139 TDA8139/D 50 56	°C/W
$T_J$	Maximum recommended junction temperature	140	°C
$T_{OPER}$	Operating free air temperature range	0 to +70	°C

1. Mounted on board, refer to [Section 5](#).

### 2.1 Electrical characteristics

$T_{AMB} = 25^\circ \text{C}$ ,  $V_{IN1} = 7 \text{ V}$ ,  $V_{IN2} = 10 \text{ V}$ , unless otherwise specified.

**Table 4. Electrical characteristics**

Symbol	Parameter	Test conditions	Minimum	Typical	Maximum	Unit
$V_{O1}$	Output voltage	$I_{O1} = 10 \text{ mA}$	5	5.1	5.2	V
$V_{O2}$	Output voltage	$I_{O2} = 10 \text{ mA}$	2.8		16.0	V
$V_{IO1,2}$	Dropout voltage	$I_{O1,2} = 750 \text{ mA}$			1.4	V
$V_{O1,2LI}$	Line regulation	$7 \text{ V} < V_{IN1} < 14 \text{ V}$ $12 \text{ V} < V_{IN2} < 18 \text{ V}$ $I_{O1,2} = 200 \text{ mA}$ , $V_{O2} = 10 \text{ V}$			50 100	mV
$V_{O1,2LO}$	Load regulation	$5 \text{ mA} < I_{O1} < 600 \text{ mA}$ $5 \text{ mA} < I_{O2} < 600 \text{ mA}$ $V_{O2} = 10 \text{ V}$			100 200	mV

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Minimum	Typical	Maximum	Unit
$I_Q$	Quiescent current	$I_{O1} = 10 \text{ mA}$ , OUTPUT2 Disabled			2	mA
$V_{O1RST}$	Reset threshold voltage	$K = V_{O1}$ , $V_{IN1} \geq 7 \text{ V}$	$K - 0.4$	$K - 0.25$	$K - 0.1$	V
$V_{RTH}$	Reset threshold hysteresis	See circuit description.	20	50	75	mV
$t_{RD}$	Reset pulse delay	$C_e = 100 \text{ nF}$ See circuit description.		25		ms
$V_{RL}$	Saturation voltage in reset condition	$I_{RESET} = 5 \text{ mA}$			0.4	V
$I_{RH}$	Leakage current in normal condition	$I_{RESET} = 10 \text{ V}$			10	$\mu\text{A}$
$K_{O1,2}$	Output voltage thermal drift	$K_0 = \frac{\Delta V_0 \cdot 10^6}{\Delta T \cdot V_0}$ $T_J = 0 \text{ to } +125^\circ\text{C}$		100		ppm/ $^\circ\text{C}$
$I_{O1,2SC}$	Short circuit output current	$V_{IN1,2} = 7 \text{ V}$ $V_{IN1,2} = 16 \text{ V}^{(1)}$			1.6 1.0	A
$V_{DISH}$	Disable voltage high (OUT2 active)		2			V
$V_{DISL}$	Disable voltage low (OUT2 disabled)				0.8	V
$I_{DIS}$	Disable bias current	$0 \text{ V} < V_{DIS} < 7 \text{ V}$	-100		2	$\mu\text{A}$
$V_{REF}$	Reference voltage at PROGRAM Pin			2.5		V
$T_{JSD}$	Junction temperature for thermal shutdown			145		$^\circ\text{C}$

1. The output short-circuit currents are tested one channel at time. During a short-circuit, a large consumption of power occurs, but the thermal protection circuit prevents any excessive temperatures. A safe permanent short-circuit protection is only guaranteed for input voltages up to 16 V.

### 3 Circuit description

The TDA8139 and the TDA8139/D are dual-voltage regulators with reset and disable functions.

The two regulation parts are supplied from a single voltage reference circuit trimmed by zener zapping during EWS testing. Since the supply voltage of this voltage reference is connected to pin INPUT1 ( $V_{IN1}$ ), the second regulator will not work if pin INPUT1 is not supplied.

The adjustable voltage of pin OUTPUT2 ( $V_{O2}$ ) is defined by output bridge resistors ( $R1$ ,  $R2$ ): the values of these resistors are calculated to obtain, with the targetted value for  $V_{O2}$ , the reference voltage ( $V_{REF} = 2.5$  V) on the median point connected to pin PROGRAM.

The output stages have been realized using a Darlington configuration with a typical dropout voltage of 1.2 V.

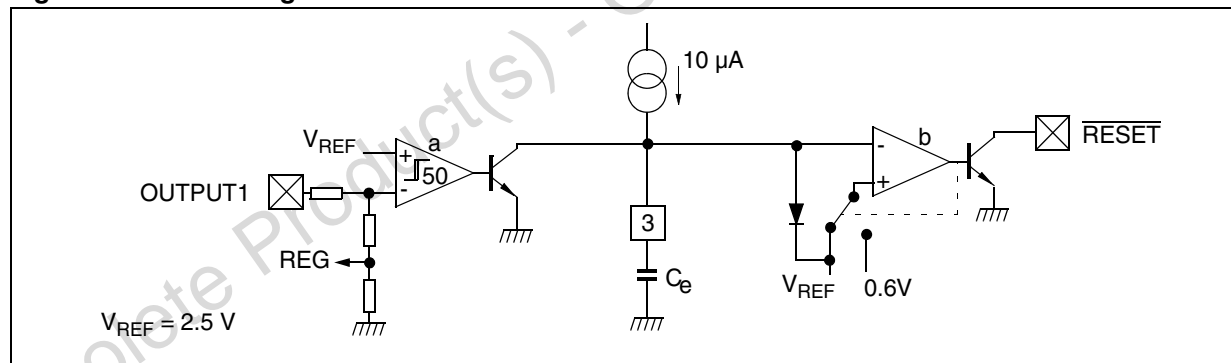
The disable circuit will switch off pin OUTPUT2 if a voltage less than 0.8 V is applied to pin DISABLE.

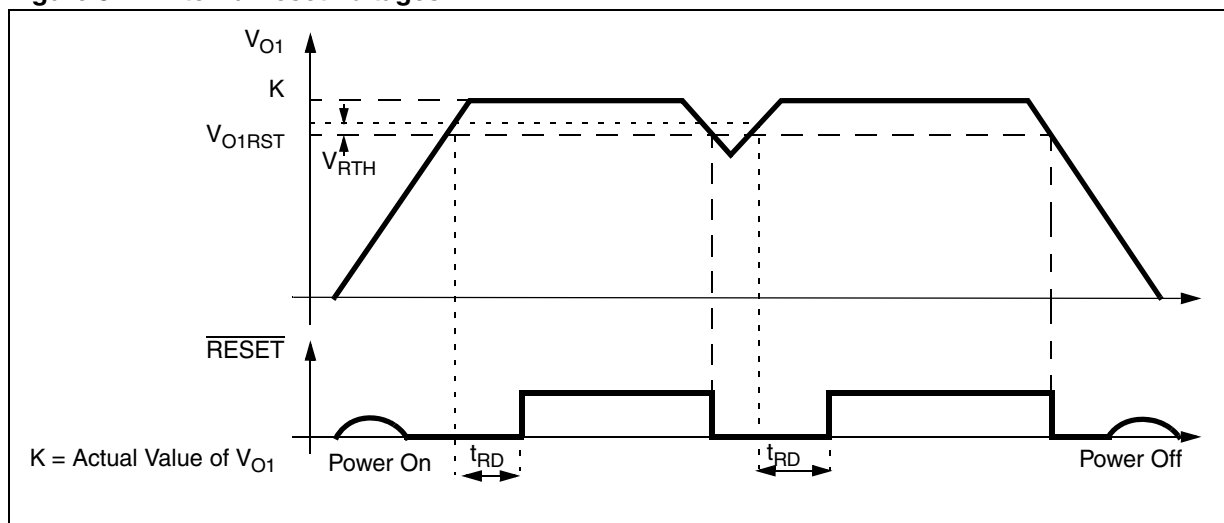
The reset circuit checks the voltage at pin OUTPUT1. If this voltage drops below  $V_{O1} - 0.25$  V (4.85 V Typ.), the "a" comparator (Figure 4) rapidly discharges capacitor  $C_e$  and the reset output immediately switches to low. When the voltage at pin OUTPUT1 exceeds  $V_{O1} - 0.2$  V (4.9 V Typ.), the external capacitor voltage ( $V_{C_e}$ ) increases linearly to the reference voltage ( $V_{REF} = 2.5$  V) corresponding to a reset pulse delay  $t_{RD}$  as shown in Figure 5.

$$t_{RD} = \frac{C_e \times 2.5V}{10\mu A}$$

Afterwards, the reset output returns to high. To avoid glitches in the reset output, the second comparator "b" has a large hysteresis (1.9 V).

**Figure 4. Reset diagram**



**Figure 5. Internal reset voltages**

## 4 Application diagrams

Figure 6. TDA8139 typical application

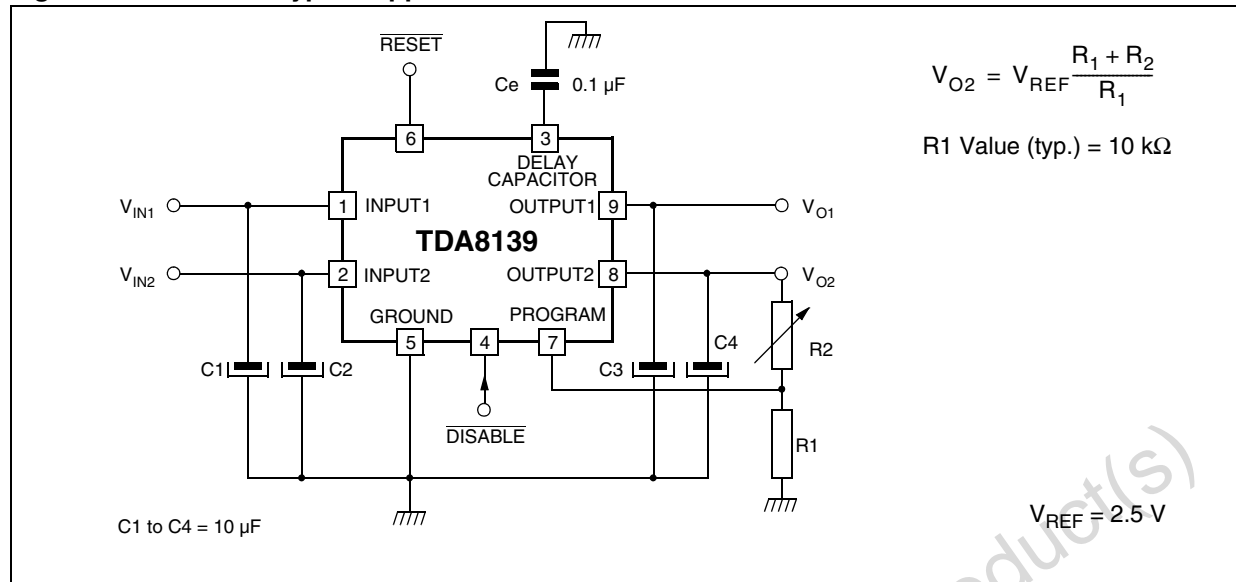
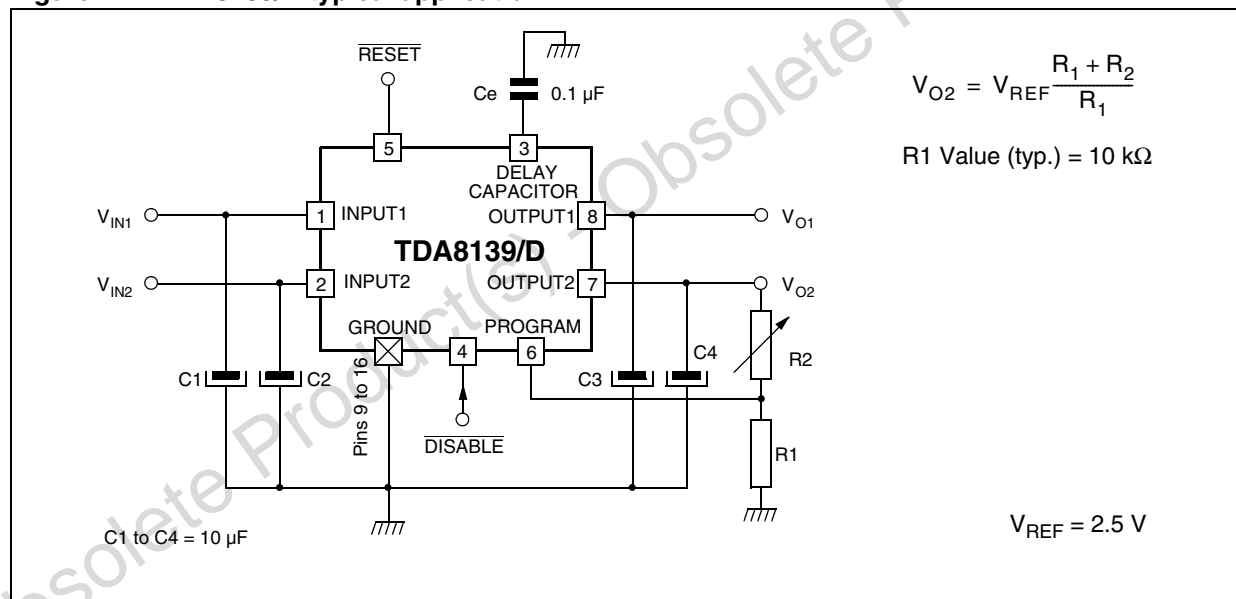


Figure 7. TDA8139/D typical application





## 5 Power dissipation and layout indications

The power is mainly dissipated by the two device buffers. It can be calculated by the equation:

$$P = (V_{IN1} - V_{O1}) \times I_{OUT1} + (V_{IN2} - V_{O2}) \times I_{O2}$$

The following table lists the different  $R_{thJA}$  values of these packages with or without a heatsink and the corresponding maximum power dissipation assuming:

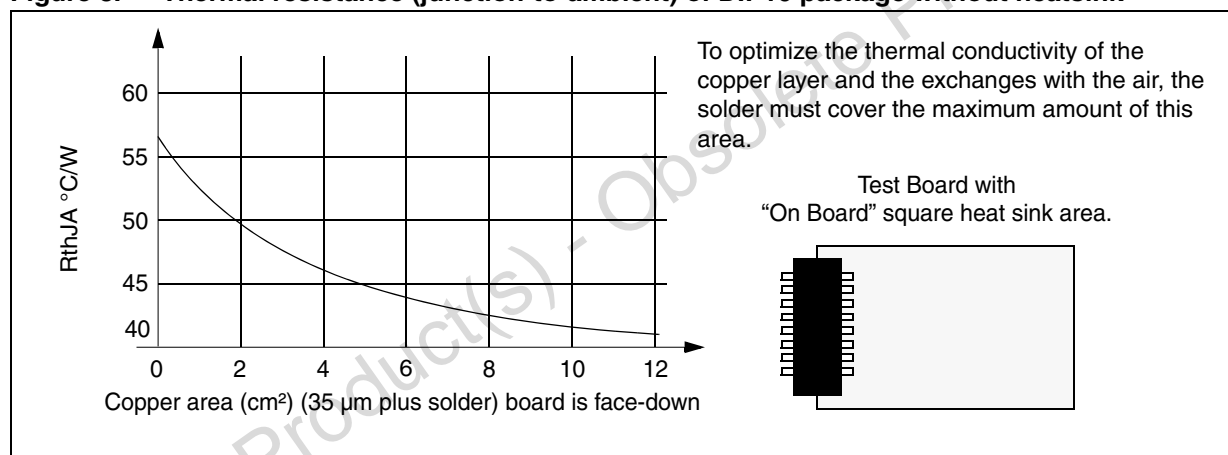
Maximum ambient temperature = 70 °C

Maximum junction temperature = 140 °C

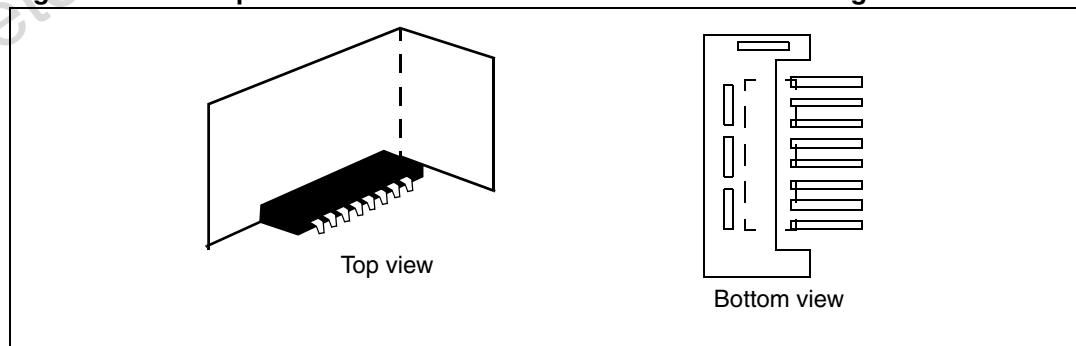
**Table 5.  $R_{thJA}$  values with or without heatsinks**

Device	Heatsink	$R_{thJA}$ in °C/W	$P_{MAX}$ in W
TDA8139	No	50	1.4
	Yes	20	3.5
TDA8139/D	No	56 to 40	1.25 to 1.75
	Yes	32	2.2

**Figure 8. Thermal resistance (junction-to-ambient) of DIP16 package without heatsink**



**Figure 9. Metal plate mounted near the TDA8139A for heatsinking**



## 6 Package mechanical data

Figure 10. 9-pin plastic single in-line package

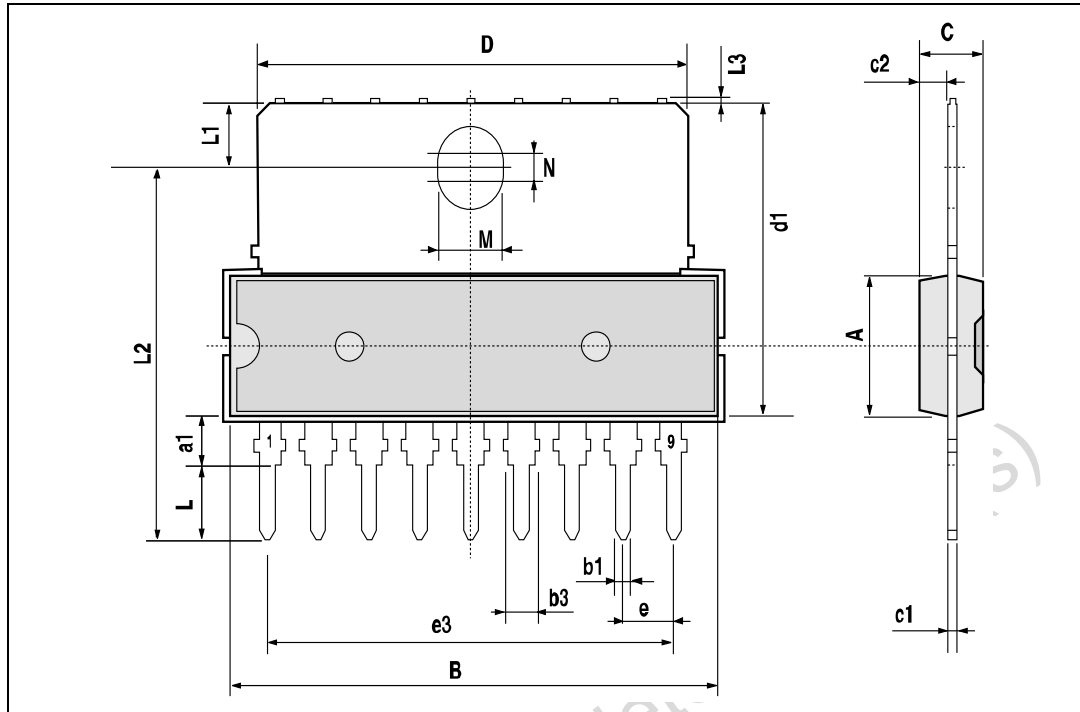
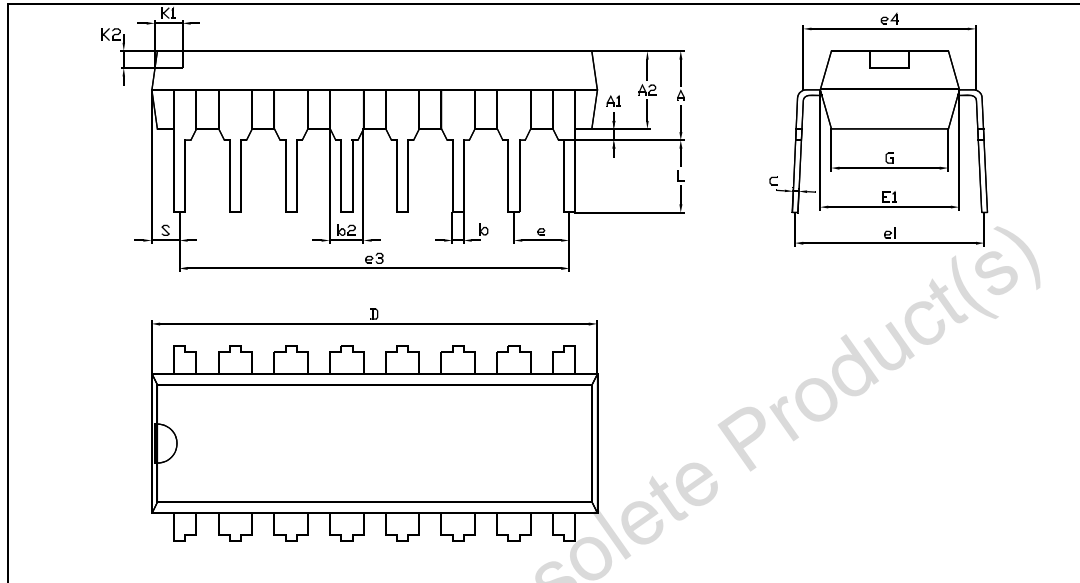


Table 6. JEDEC standard package dimensions (9-pin plastic single in-line)

Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			21.2			0.835
d1		14.5			0.571	
e		2.54			0.100	
e3		20.32			0.800	
L	3.1			1.122		
L1		3			0.116	

**Table 6. JEDEC standard package dimensions (9-pin plastic single in-line) (continued)**

Dim.	mm			Inches		
L2		17.6		0.693		
L3			0.25			0.010
M		3.2		0.126		
N		1		0.039		

**Figure 11. 16-pin plastic dual in-line package, 300-mil width****Table 7. JEDEC standard package dimensions (16-pin plastic dual in-line)**

Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36		0.56	0.014		0.022
b2		1.52	1.78		0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	18.67	19.18	19.69	0.735	0.755	0.775
e		2.54			0.100	
E1	6.10	6.35	7.11	0.240	0.250	0.280
L	2.92	3.30	3.81	0.115	0.130	0.150

## 6.1 Environmentally-friendly packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance.

ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).  
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Obsolete Product(s) - Obsolete Product(s)

## 7 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
March 1994	1.0	First Issue
October 2000	1.3	
July 2001	1.4	Datasheet update and addition of DIP16 package
August 2001	1.5	General update; DISABLE pin renamed $\overline{\text{DISABLE}}$ (function remains unchanged)
September 2001	1.6	Thermal data updated
October 2001	1.7	Thermal data updated, figures 1 and 2 updated
25-Feb-2009	2	Template updated, section 6.1 added

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