



## STB70NH03L

N-channel 60V -  $0.0075\Omega$  - 70A - D<sup>2</sup>PAK  
STripFET™ III Power MOSFET for DC-DC conversion

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STB70NH03L	30V	< 0.009Ω	60A <sup>(1)</sup>

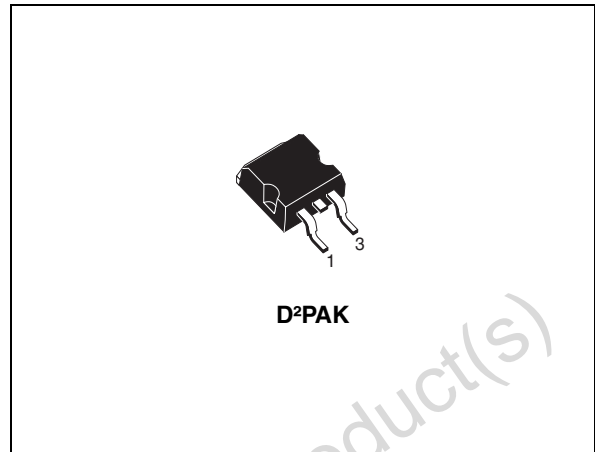
- R<sub>DS(on)</sub> x Qg industry benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device

### Description

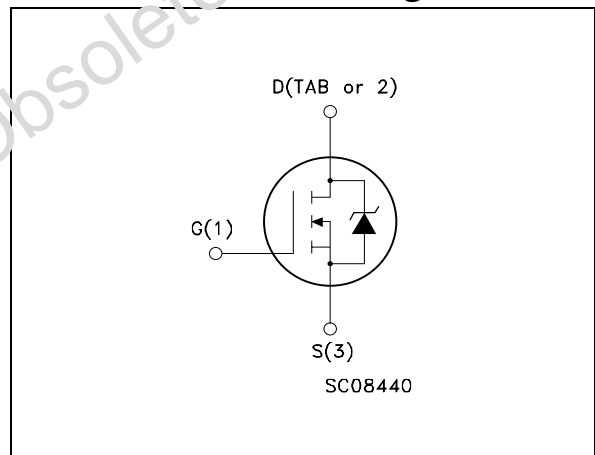
The device utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. It is ideal in high performance DC-DC converter applications where efficiency is to be achieved at very high output currents.

### Applications

- Switching application



### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STB70NH03LT4	B70NH03L	D <sup>2</sup> PAK	Tape & reel

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	30	V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20\text{ k}\Omega$ )	30	V
$V_{GS}$	Gate- source Voltage	$\pm 20$	V
$I_D^{(1)}$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	60	A
$I_D^{(1)}$	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	43	A
$I_{DM}^{(2)}$	Drain Current (pulsed)	240	A
$P_{TOT}$	Total Dissipation at $T_C = 25^\circ\text{C}$	858	W
	Derating Factor		W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single Pulse Avalanche Energy	300	mJ
$T_{stg}$	Storage Temperature	-55 to 175	$^\circ\text{C}$
$T_J$	Operating Junction Temperature		

1. Value limited by wire bonding

2. Pulse width limited by safe operating area

3. Starting  $T_J = 25^\circ\text{C}$ ,  $I_D = 30\text{A}$ ,  $V_{DD} = 20\text{V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance junction-case max	1.87	$^\circ\text{C/W}$
$R_{thJA}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C/W}$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_{CASE} = 25^{\circ}\text{C}$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage Drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}$ $T_C = 125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\ \text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}$ $I_D = 30\ \text{A}$ $V_{GS} = 5\ \text{V}$ $I_D = 30\ \text{A}$		0.0075 0.0135	0.0095 0.009	$\Omega$ $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10\ \text{V}$ $I_D = 18\ \text{A}$		25		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 10\ \text{V}$ $f = 1\ \text{MHz}$ $V_{GS} = 0$		2200 380 49		pF pF pF
$R_G$	Gate Input Resistance	$f = 1\ \text{MHz}$ gate DC bias = 0 test signal level = 20 mV open drain		1.5		$\Omega$
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay Time Fall time	$V_{DD} = 15\ \text{V}$ $I_D = 30\ \text{A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 5\ \text{V}$		21 95 19 15		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 15\ \text{V}$ $I_D = 70\ \text{A}$ $V_{GS} = 5\ \text{V}$		15.7 8.3 3.4	21	nC nC nC
$Q_{gls}^{(2)}$	Third-quadrant gate charge	$V_{DS} < 0\ \text{V}$ $V_{GS} = 10\ \text{V}$		15		nC

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

2. Gate charge for synchronous operation . See [Chapter 6: Appendix A](#)

**Table 5. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				60 240	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 30\text{ A}$ $V_{GS} = 0$			1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 60\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$ $T_J = 150^\circ\text{C}$		32 51 3.2		ns nC A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

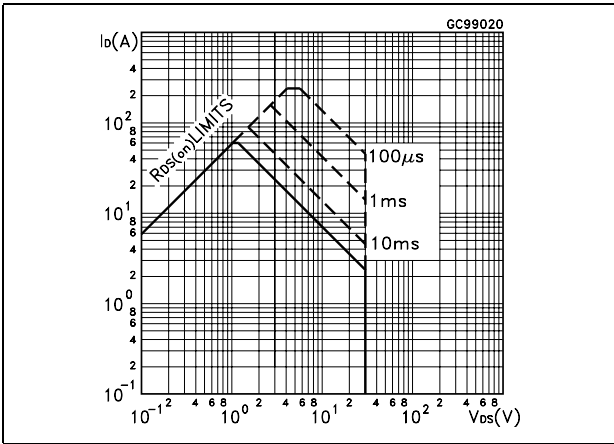


Figure 2. Thermal impedance

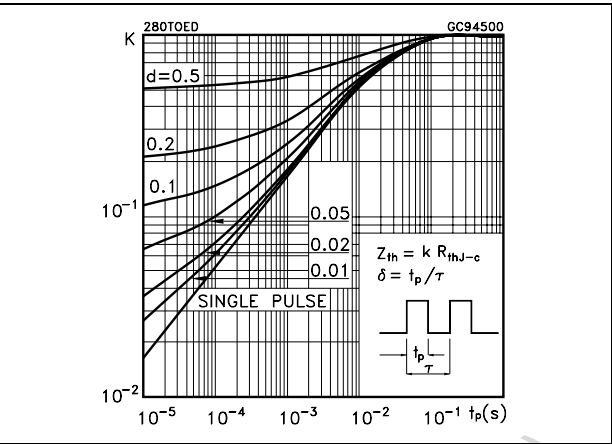


Figure 3. Output characteristics

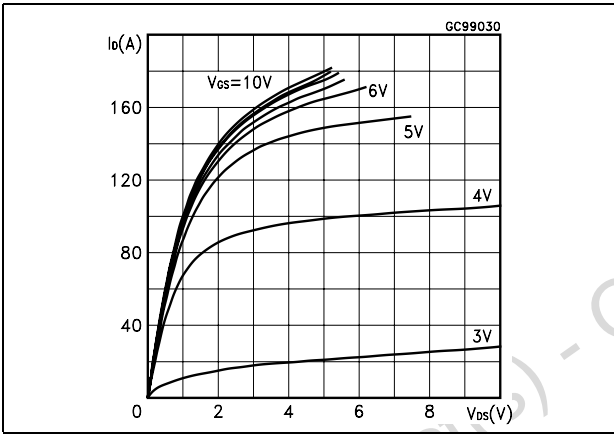


Figure 4. Transfer characteristics

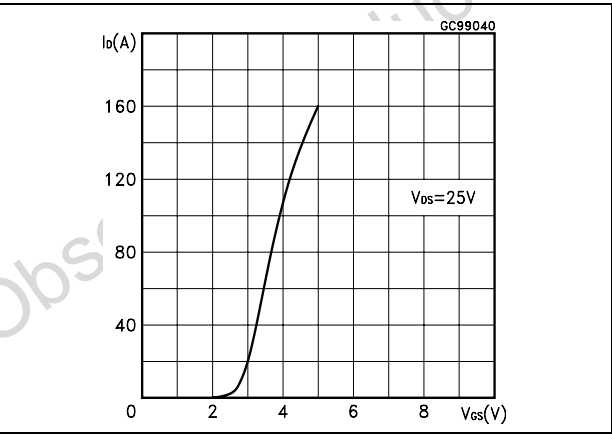


Figure 5. Transconductance

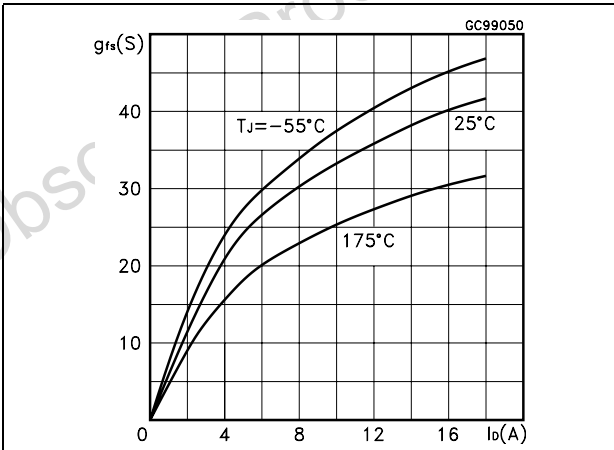


Figure 6. Static drain-source on resistance

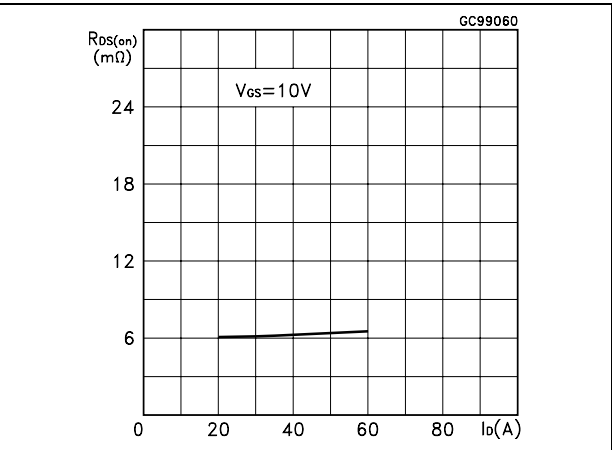


Figure 7. Gate charge vs gate-source voltage    Figure 8. Capacitance variations

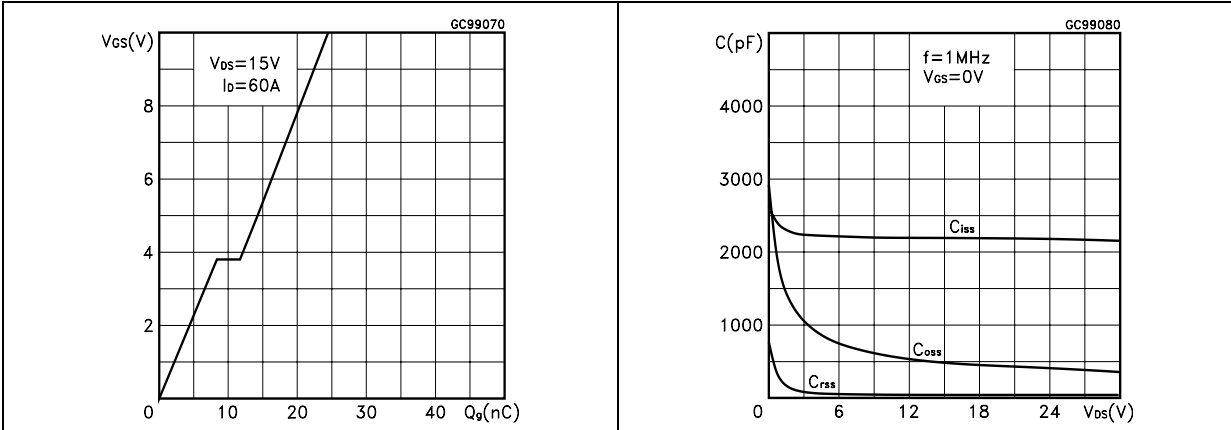


Figure 9. Normalized gate threshold voltage vs temperature    Figure 10. Normalized on resistance vs temperature

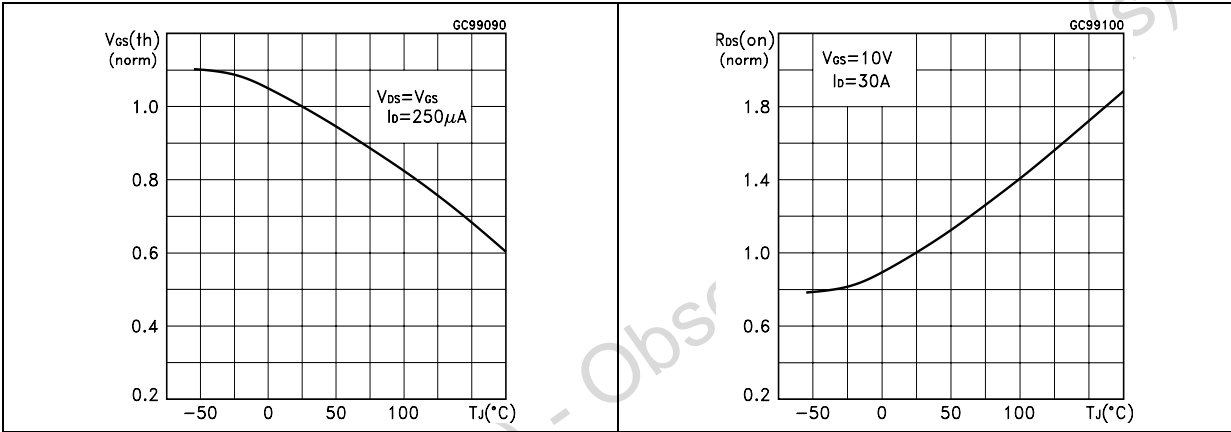
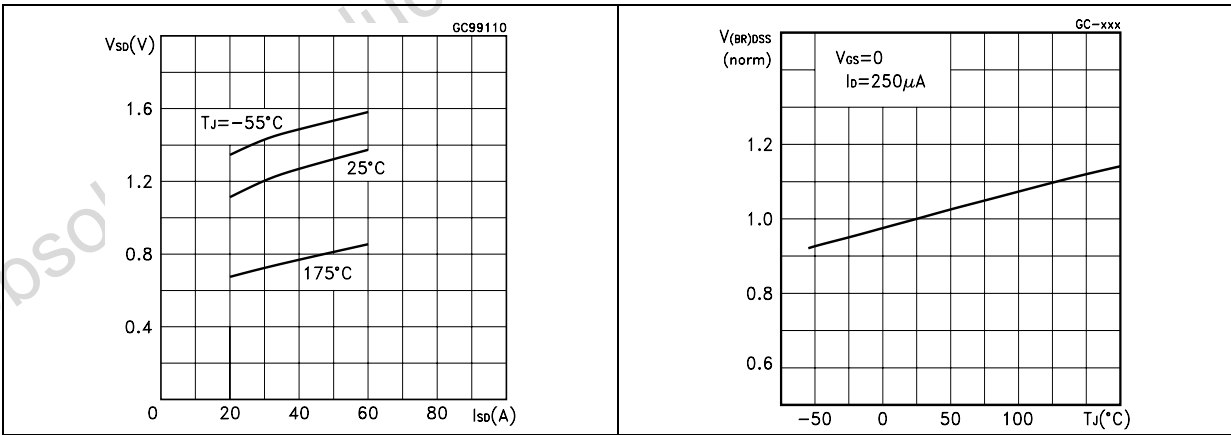
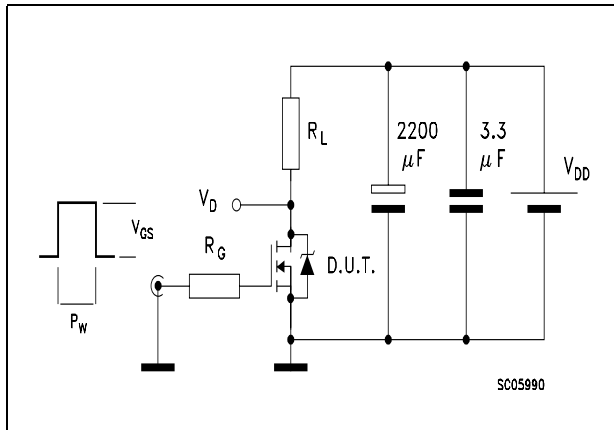


Figure 11. Source-drain diode forward characteristics    Figure 12. Normalized Breakdown vs temperature

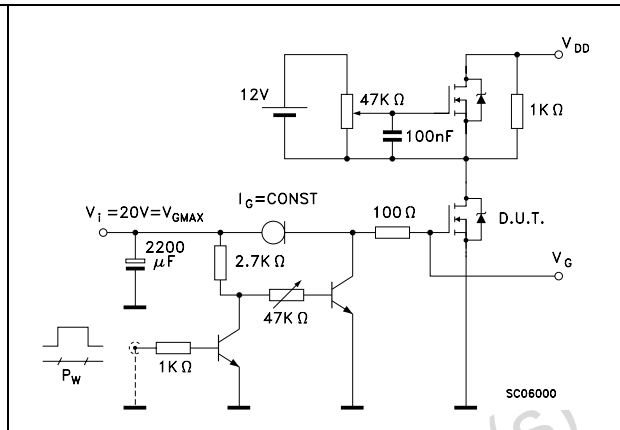


### 3 Test circuit

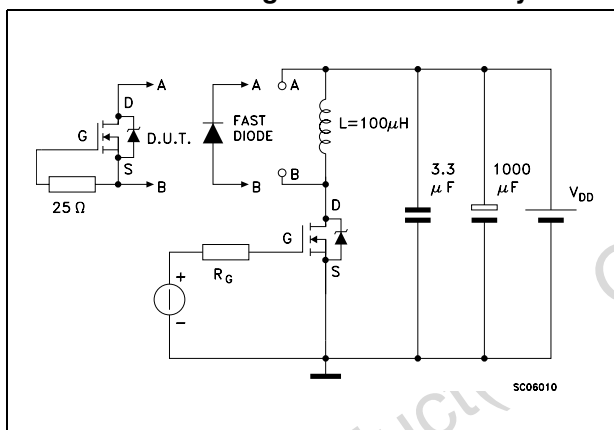
**Figure 13. Switching times test circuit for resistive load**



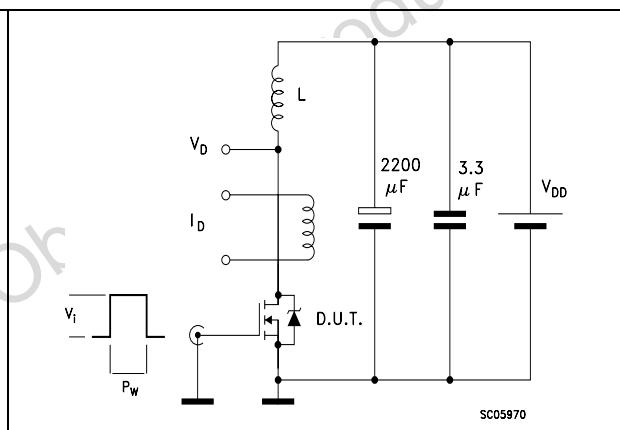
**Figure 14. Gate charge test circuit**



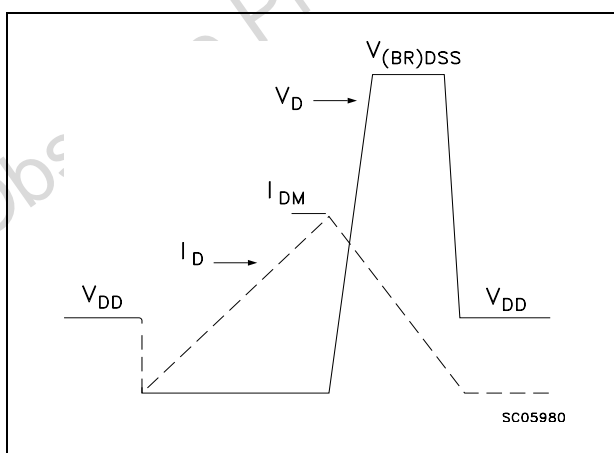
**Figure 15. Test circuit for inductive load switching and diode recovery times**



**Figure 16. Unclamped Inductive load test circuit**



**Figure 17. Unclamped inductive waveform**





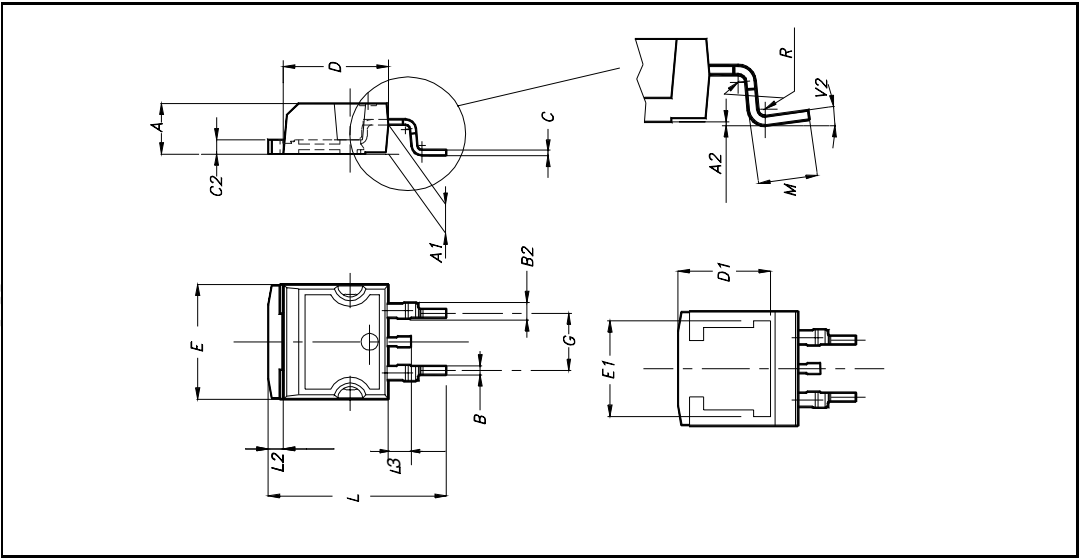
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

Obsolete Product(s) - Obsolete Product(s)

D<sup>2</sup>PAK MECHANICAL DATA

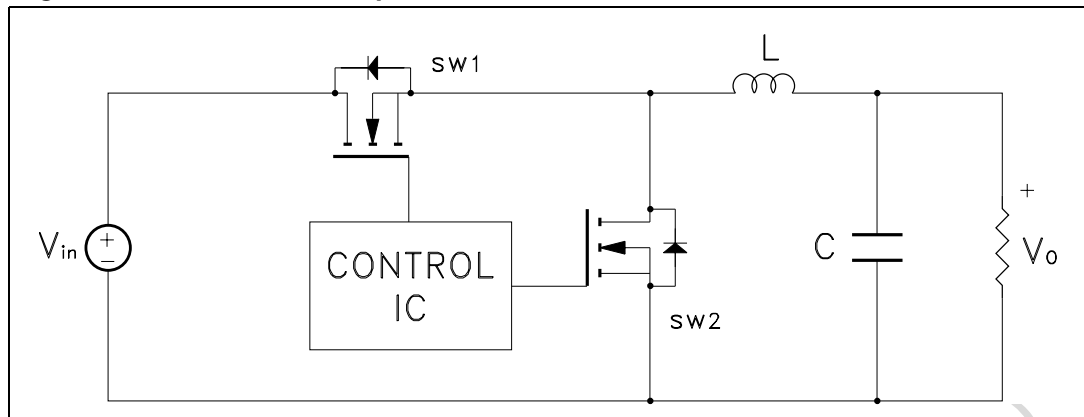
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			





## 6 Appendix A

**Figure 18. Buck converter: power losses estimation**



The power losses associated with the FETs in a synchronous buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

- The low side (SW2) device requires:
  - Very low  $R_{DS(on)}$  to reduce conduction losses
  - Small  $Q_{gl}$ s to reduce the gate charge losses
  - Small  $C_{oss}$  to reduce losses due to output capacitance
  - Small  $Q_{rr}$  to reduce losses on SW1 during its turn-on
  - The  $C_{gd}/C_{gs}$  ratio lower than  $V_{th}/V_{gg}$  ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;
- The high side (SW1) device requires:
  - Small  $R_g$  and  $L_s$  to allow higher gate current peak and to limit the voltage feedback on the gate
  - Small  $Q_g$  to have a faster commutation and to reduce gate charge losses
  - Low  $R_{DS(on)}$  to reduce the conduction losses.

**Table 6. Power losses calculation**

		High side switching (SW1)	Low side switch (SW2)
Pconduction		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1 - \delta)$
Pswitching		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
Pdiode	Recovery <sup>(1)</sup>	Not applicable	$V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
Pgate(Q <sub>G</sub> )		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P <sub>Qoss</sub>		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

1. Dissipated by SW1 during turn-on

**Table 7. Paramiters meaning**

Parameter	Meaning
d	Duty-cycle
Q <sub>gsth</sub>	Post threshold gate charge
Q <sub>gls</sub>	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
P <sub>Qoss</sub>	Output capacitance losses

## 7 Revision history

**Table 8. Revision history**

Date	Revision	Changes
21-Jun-2004	5	Complete document
20-Jul-2006	6	New template, no content change

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