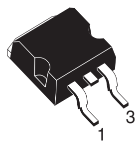
STB70NH03L

N-channel 60V - 0.0075Ω - 70A - D^2PAK
STripFET™ III Power MOSFET for DC-DC conversion

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STB70NH03L	30V	< 0.009Ω	60A (1)

- $R_{DS(on)}$ x Qg industry benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device



D²PAK

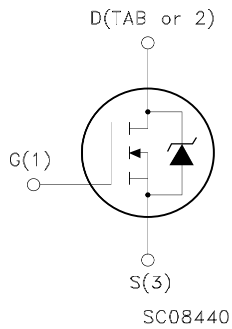
Description

The device utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. It is ideal in high performance DC-DC converter applications where efficiency is to be achieved at very high output currents.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB70NH03LT4	B70NH03L	D²PAK	Tape & reel

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	30	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	30	V
V_{GS}	Gate- source Voltage	± 20	V
I_D (1)	Drain Current (continuous) at T_C = 25°C	60	A
I_D (1)	Drain Current (continuous) at T_C = 100°C	43	A
I_{DM} (2)	Drain Current (pulsed)	240	A
P_{TOT}	Total Dissipation at T_C = 25°C	858	W
	Derating Factor		W/°C
E_{AS} (3)	Single Pulse Avalanche Energy	300	mJ
T_{stg}	Storage Temperature	-55 to 175	°C
T_J	Operating Junction Temperature		

1. Value limited by wire bonding
2. Pulse width limited by safe oper`ting area
3. Starting T_J = 25 °C, ID = 30A, V_{DD} = 20V

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case max	1.87	°C/W
R_{thJA}	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE} = 25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 30 A V_{GS} = 5 V I_D = 30 A		0.0075 0.0135	0.0095 0.009	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 10 V I_D = 18 A		25		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 10V f = 1 MHz V_{GS} = 0		2200 380 49		pF pF pF
R_G	Gate Input Resistance	f = 1 MHz gate DC bias = 0 test signal level = 20 mV open drain		1.5		Ω
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay Time Fall time	V_{DD} = 15 V I_D = 30 A R_G = 4.7 Ω V_{GS} = 5 V		21 95 19 15		ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}= 15V I_D= 70A V_{GS}= 5V		15.7 8.3 3.4	21	nC nC nC
Q_{gls} (2)	Third-quadrant gate charge	V_{DS}< 0 V V_{GS}= 10 V		15		nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
2. Gate charge for synchronous operation . See *Chapter 6: Appendix A*

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				60 240	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 30 A V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 60 A di/dt = 100A/µs V_{DD} = 20 V T_J = 150°C		32 51 3.2		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

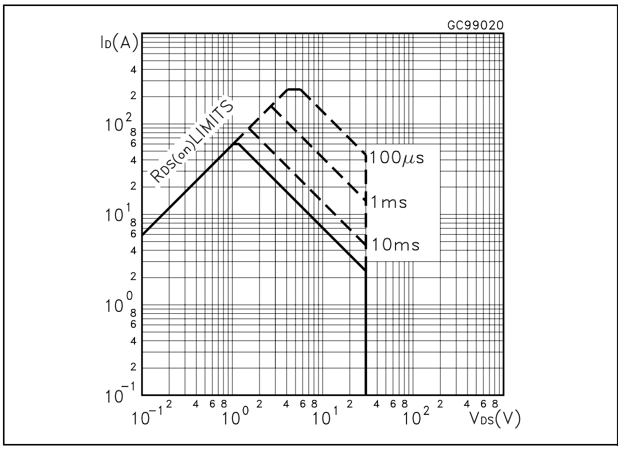


Figure 2. Thermal impedance

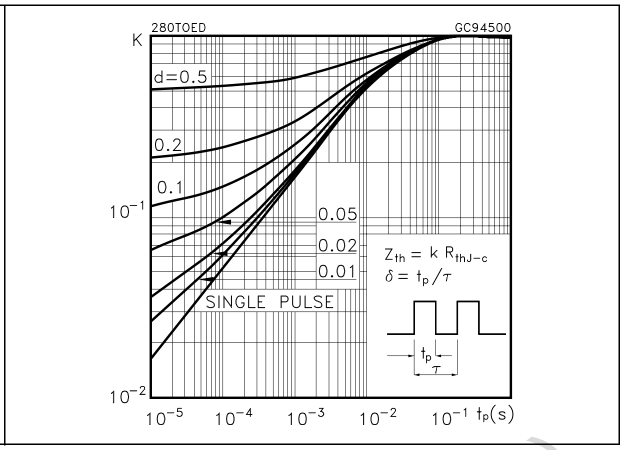


Figure 3. Output characterisics

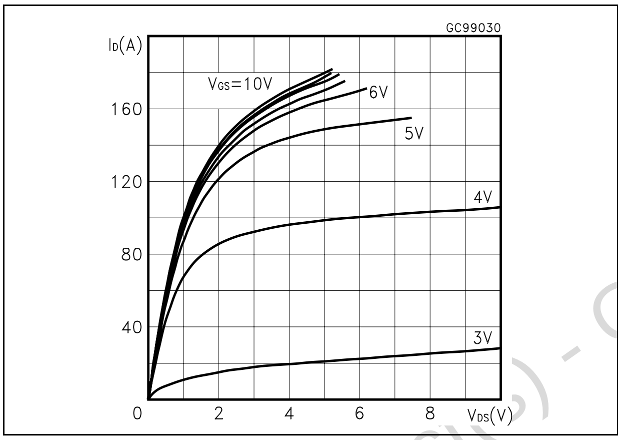


Figure 4. Transfer characteristics

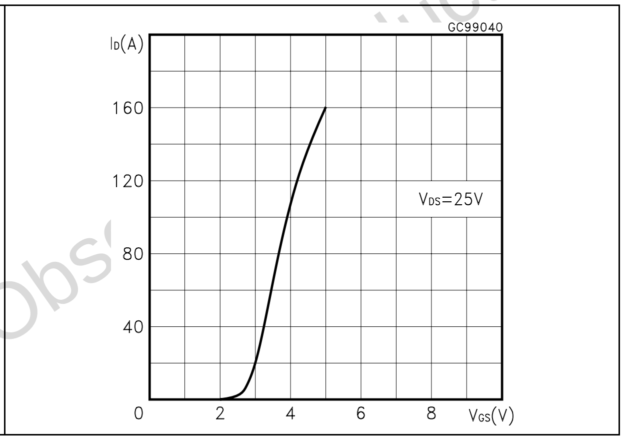


Figure 5. Transconductance

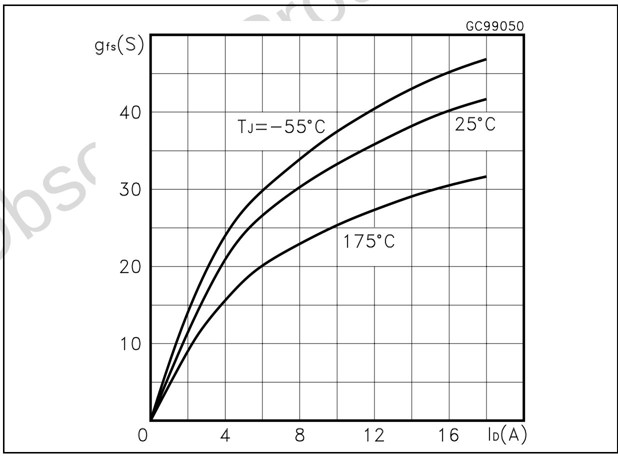


Figure 6. Static drain-source on resistance

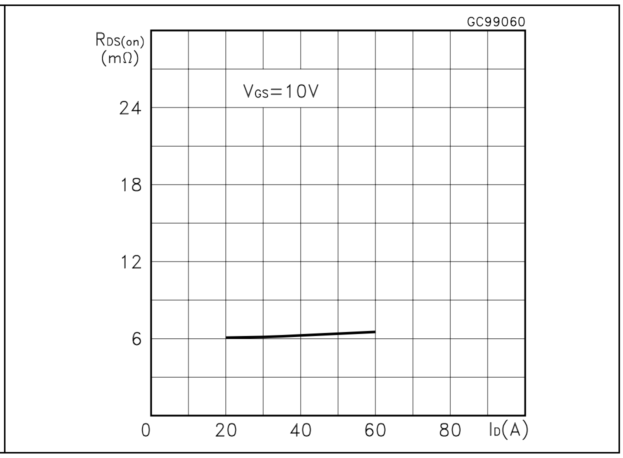


Figure 7. Gate charge vs gate-source voltage

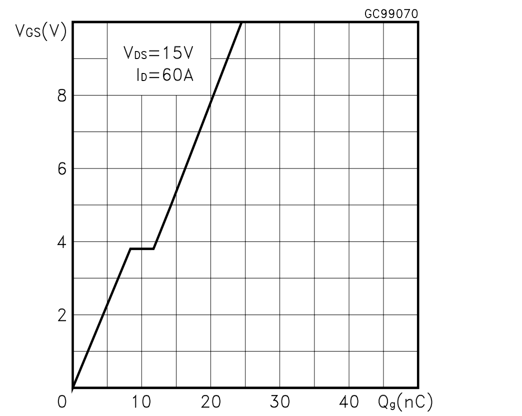


Figure 8. Capacitance variations

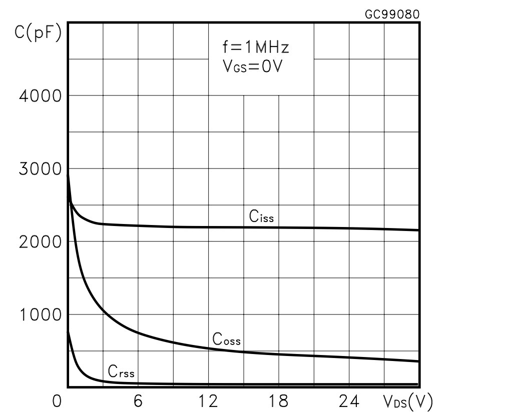


Figure 9. Normalized gate threshold voltage vs temperature

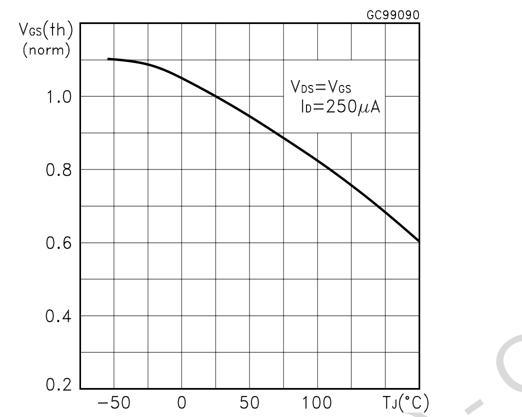


Figure 10. Normalized on resistance vs temperature

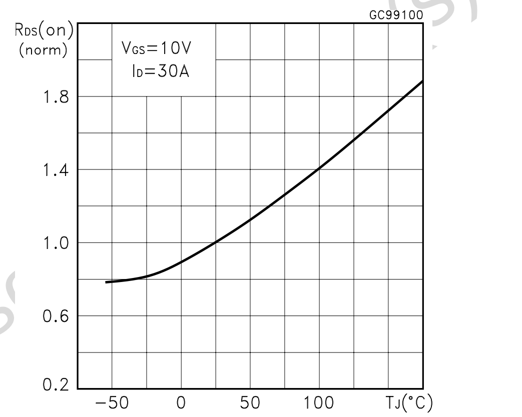


Figure 11. Source-drain diode forward characteristics

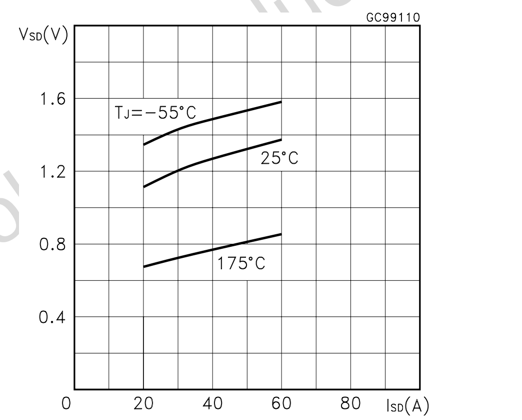
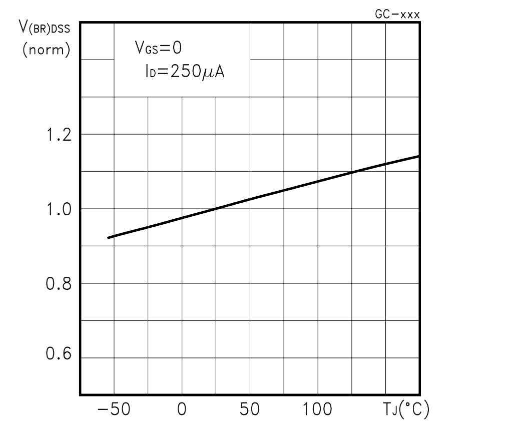


Figure 12. Normalized Breakdown vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

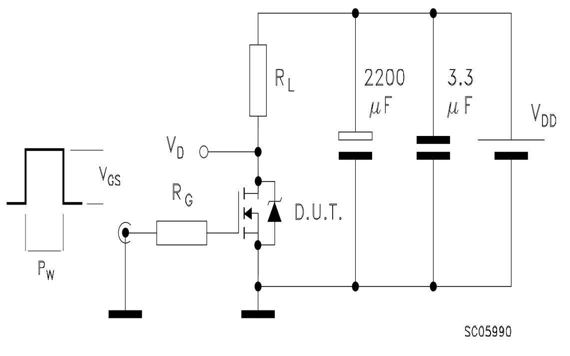


Figure 14. Gate charge test circuit

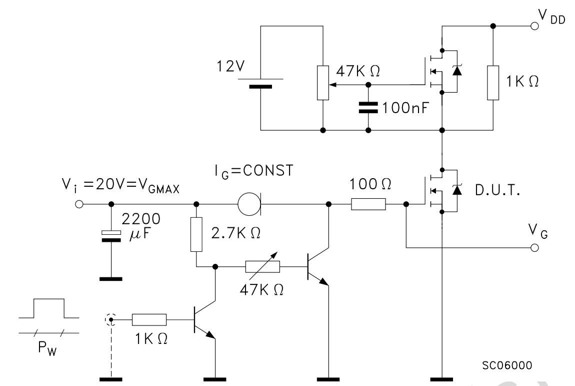


Figure 15. Test circuit for inductive load switching and diode recovery times

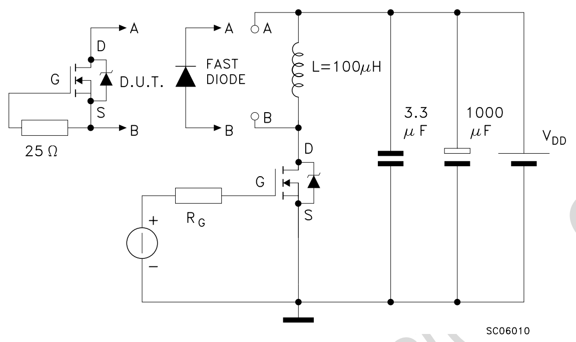


Figure 16. Unclamped Inductive load test circuit

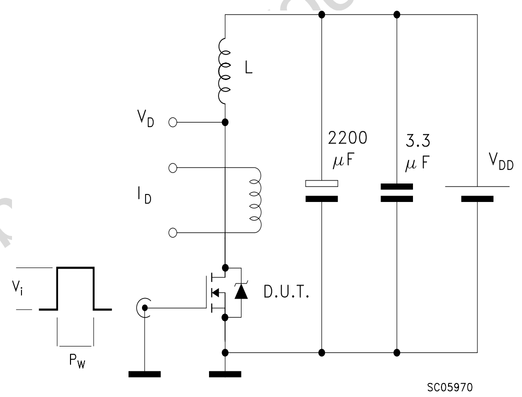
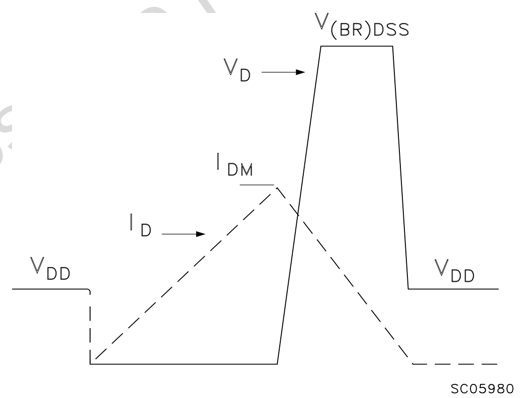


Figure 17. Unclamped inductive waveform

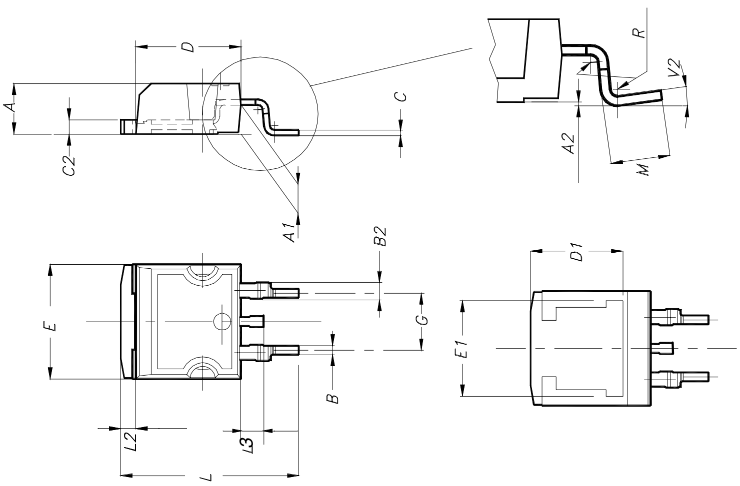


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

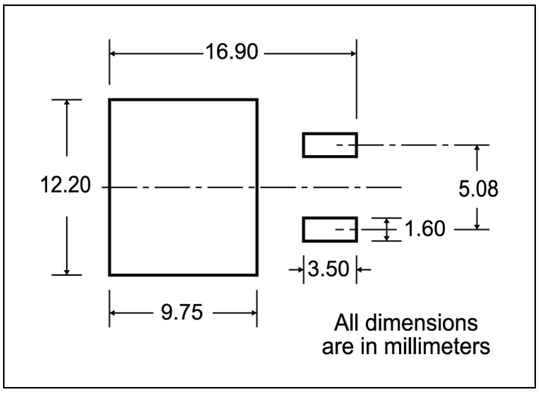
D^2PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0º		4º			

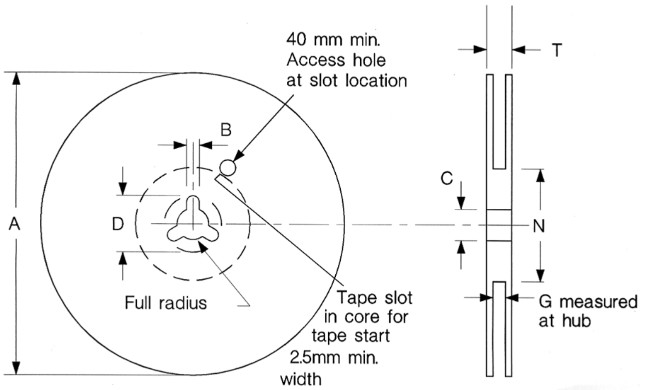


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



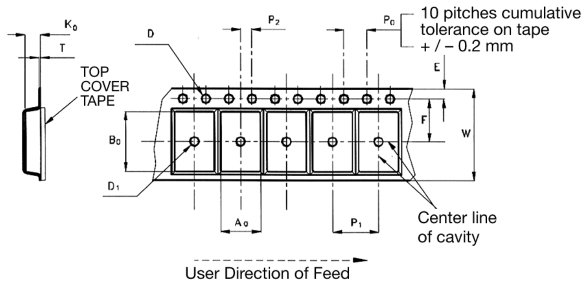
REEL MECHANICAL DATA

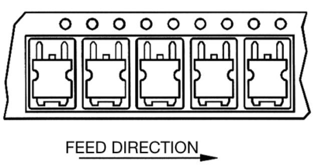
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

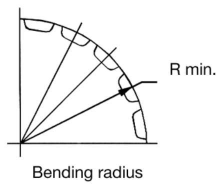
BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956



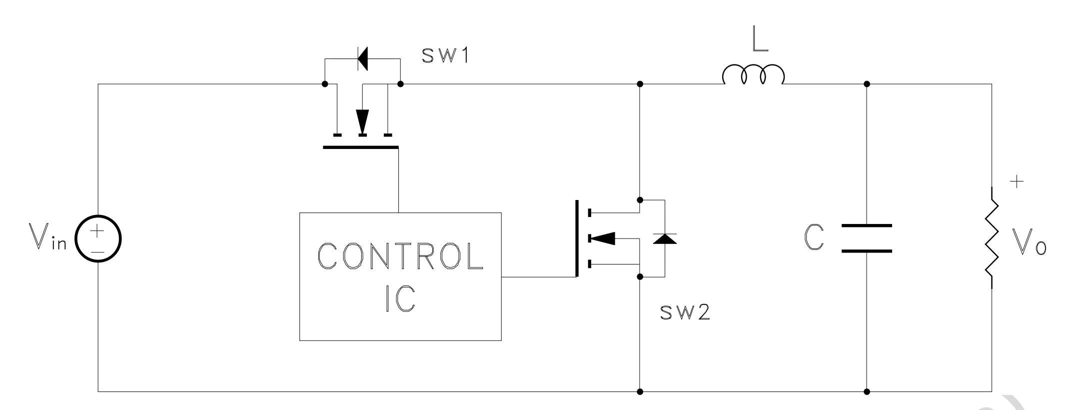




* on sales type

6 Appendix A

Figure 18. Buck converter: power losses estimation



The power losses associated with the FETs in a synchronous buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

- The low side (SW2) device requires:
- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Qgls to reduce the gate charge losses
- Small Coss to reduce losses due to output capacitance
- Small Qrr to reduce losses on SW1 during its turn-on
- The Cgd/Cgs ratio lower than Vth/Vgg ratio especially with low drain to source
- voltage to avoid the cross conduction phenomenon;
- The high side (SW1) device requires:
- Small Rg and Ls to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Qg to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses.

Table 6. Power losses calculation

		High side switching (SW1)	Low side switch (SW2)
Pconduction		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1-\delta)$
Pswitching		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
Pdiode	Recovery [1]	Not applicable	$V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
Pgate(Q_G)		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P_{Qoss}		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

1. Dissipated by SW1 during turn-on

Table 7. Paramiters meaning

Parameter	Meaning
d	Duty-cycle
Q_{gsth}	Post threshold gate charge
Q_{gls}	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
P_{Qoss}	Output capacitance losses

7 Revision history

Table 8. Revision history

Date	Revision	Changes
21-Jun-2004	5	Complete document
20-Jul-2006	6	New template, no content change