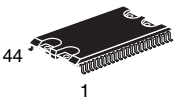
M48Z32V

3.3V, 256Kbit (32Kbit x 8) ZEROPOWER® SRAM

Features

- Integrated, ultra low power SRAM, and power-fail control circuit
- READ cycle time equals WRITE cycle time
- Automatic power-fail chip deselect and WRITE protection
- WRITE protect voltages:
  (V_{PFD} = Power-fail deselect voltage)
  - M48Z32V: 2.7V ≤ V_{PFD} ≤ 3.0V
- Ultra-low standby current
- RoHS COMPLIANT
  - Lead-free second level interconnect



SO44 (MT)
44-pin SOIC

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1 Summary

The M48Z32V ZEROPOWER® RAM is a 32K x 8, non-volatile static RAM that integrates power-fail deselect circuitry and battery control logic on a single die.

The 44-pin, 330mil SOIC provides a battery pin for an external, user-supplied battery. This is all that is required to fully non-volatize the SRAM.

Figure 1. Logic diagram

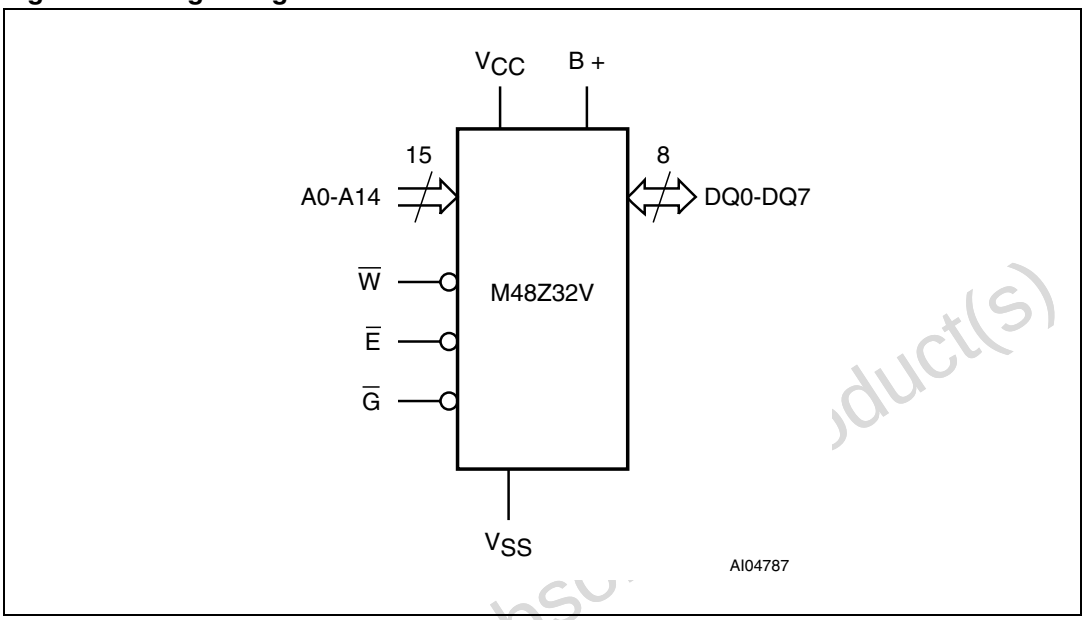
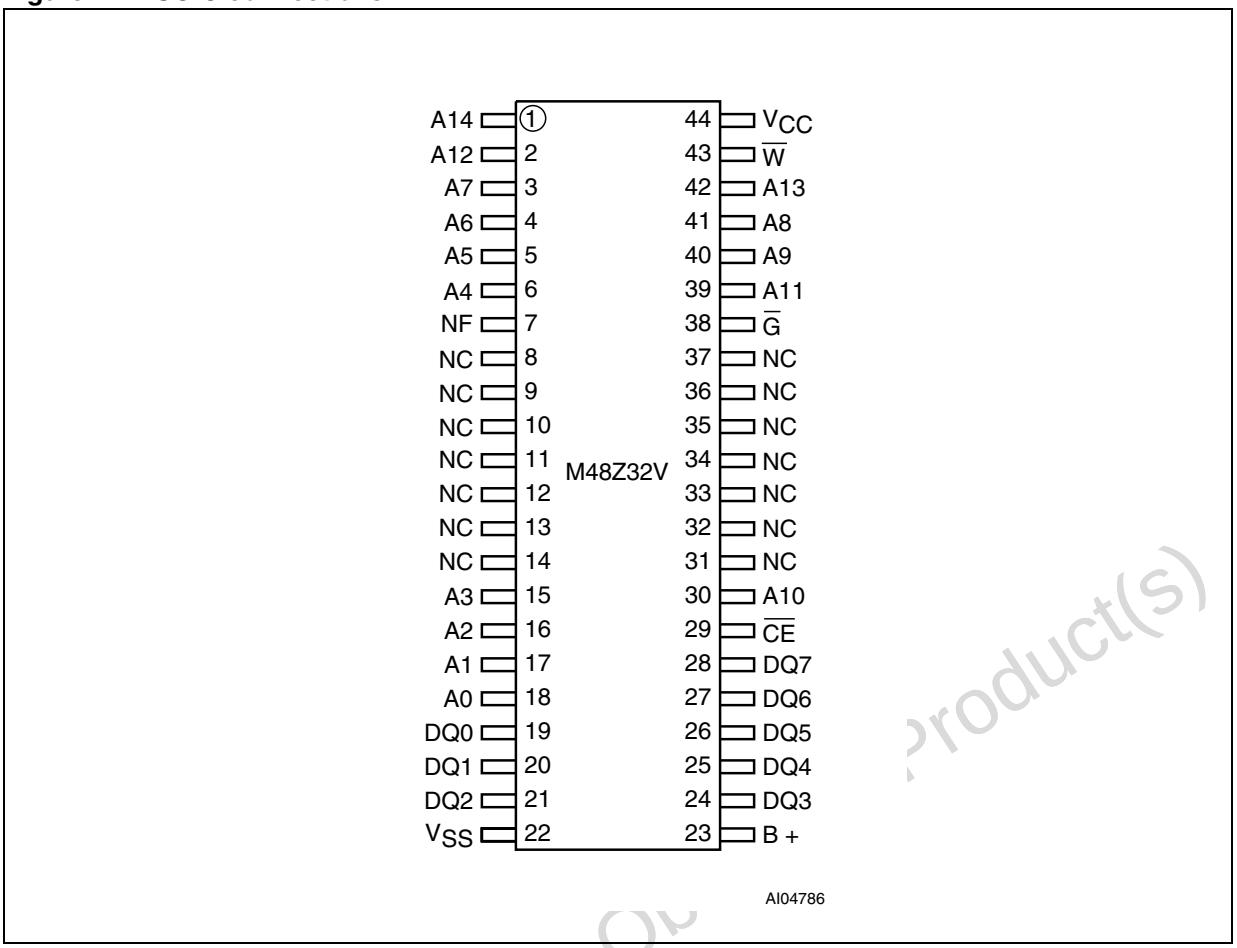


Table 1. Signal names

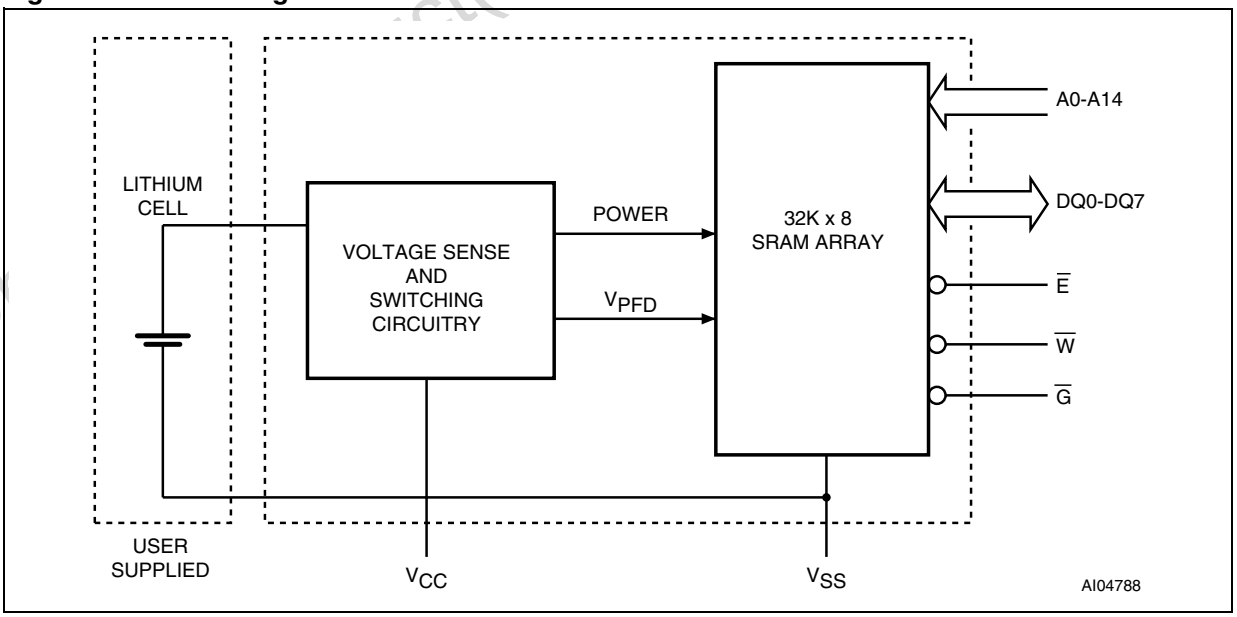
A0-A14	Address inputs
DQ0-DQ7	Data inputs / outputs
$\overline{E}$	Chip enable input
$\overline{G}$	Output enable input
$\overline{W}$	WRITE enable input
V_{CC}	Supply voltage
V_{SS}	Ground
B +	Positive battery pin
NC	Not connected

Figure 2. SOIC connections



Note: NF, Pin 7 must be tied to V_{SS}.

Figure 3. Block diagram



2 Operating modes

The M48Z32V also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single power supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately V_{SO}, the control circuitry connects the battery which maintains data until valid power returns.

Table 2. Operating modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	3.0 to 3.6V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)(1)	X	X	X	High Z	CMOS standby
Deselect	$\leq V_{SO}$(1)	X	X	X	High Z	Battery back-up mode

1. See *Table 12 on page 15* for details.

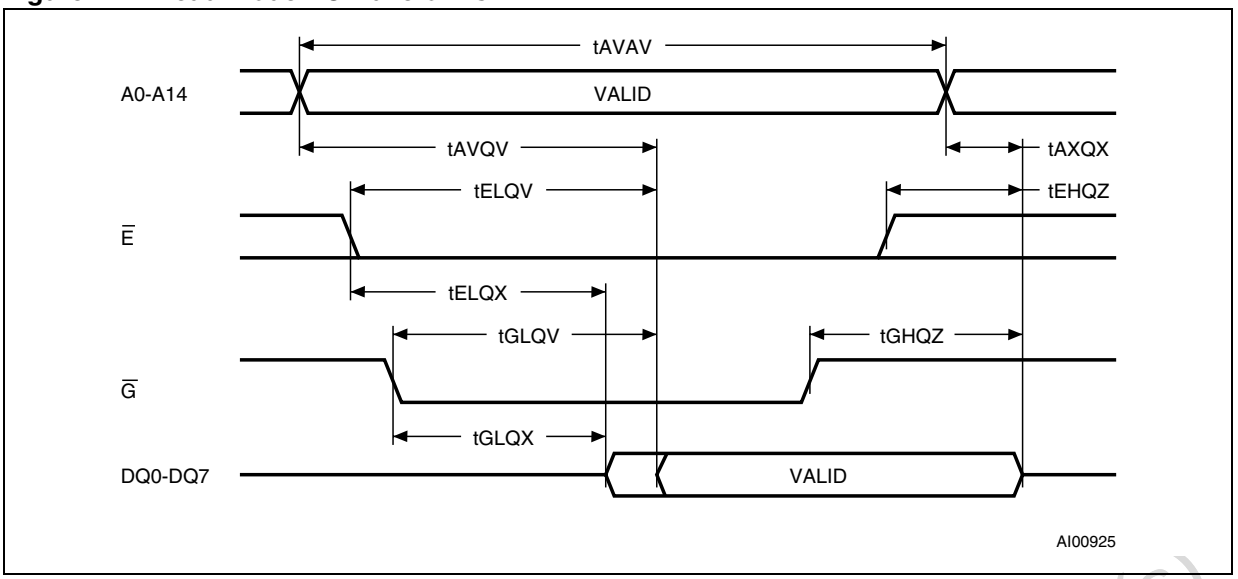
Note: X = V_{IH} or V_{IL}; V_{SO} = Battery back-up switchover voltage.

2.1 Read mode

The M48Z32V is in the READ Mode whenever $\overline{W}$ (WRITE Enable) is high, $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access time (t_{ELQV}) or Output Enable Access time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for Output Data Hold time (t_{AXQX}) but will go indeterminate until the next Address Access.

Figure 4. Read mode AC waveforms



Note: WRITE Enable ($\overline{W}$) = High.

Table 3. Read mode AC characteristics

Symbol	Parameter[1]	M48Z32V –35		Unit
		Min	Max	
t_{AVAV}	READ cycle time	35		ns
t_{AVQV}	Address valid to output valid		35	ns
t_{ELQV}	Chip enable low to output valid		35	ns
t_{GLQV}	Output enable low to output valid		15	ns
t_{ELQX}[2]	Chip enable low to output transition	5		ns
t_{GLQX}[2]	Output enable low to output transition	0		ns
t_{EHQZ}[2]	Chip enable high to output Hi-Z		13	ns
t_{GHQZ}[2]	Output enable high to output Hi-Z		13	ns
t_{AXQX}	Address transition to output transition	5	0	ns

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{cc} = 3.0 to 3.6V (except where noted).
2. C_L = 5pf (see *Figure 8 on page 16*).

2.2 Write mode

The M48Z32V is in the WRITE Mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from Chip Enable or t_{WHAX} from WRITE Enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 5. Write enable controlled, write mode AC waveforms

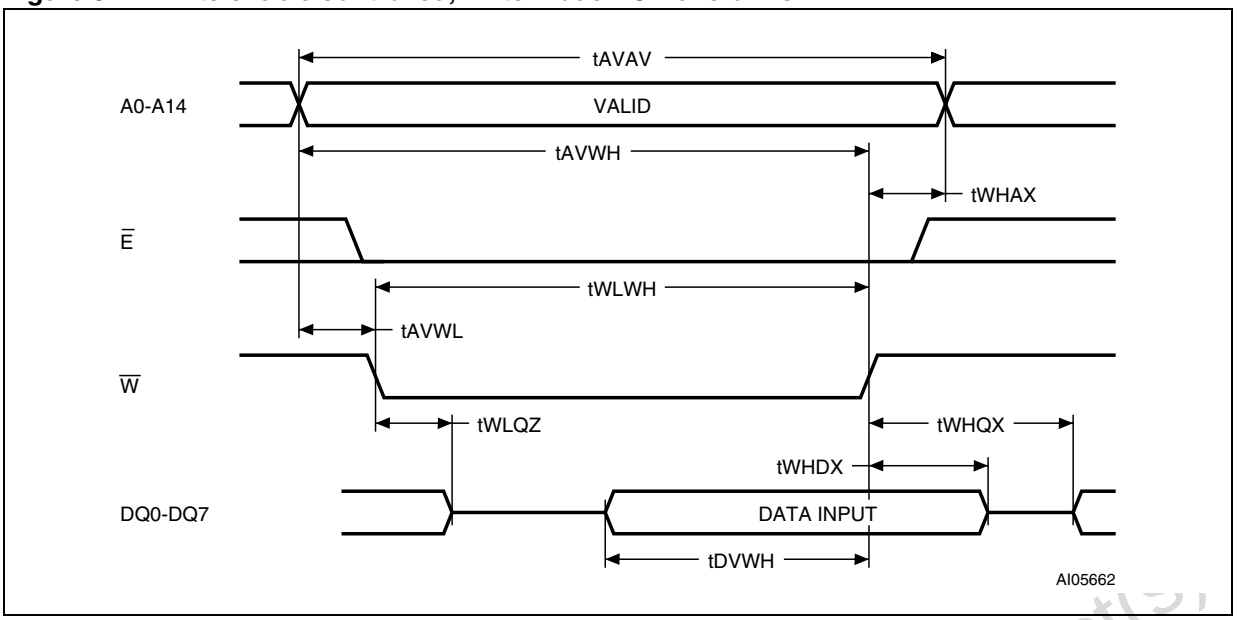


Figure 6. Chip enable controlled, write mode AC waveforms

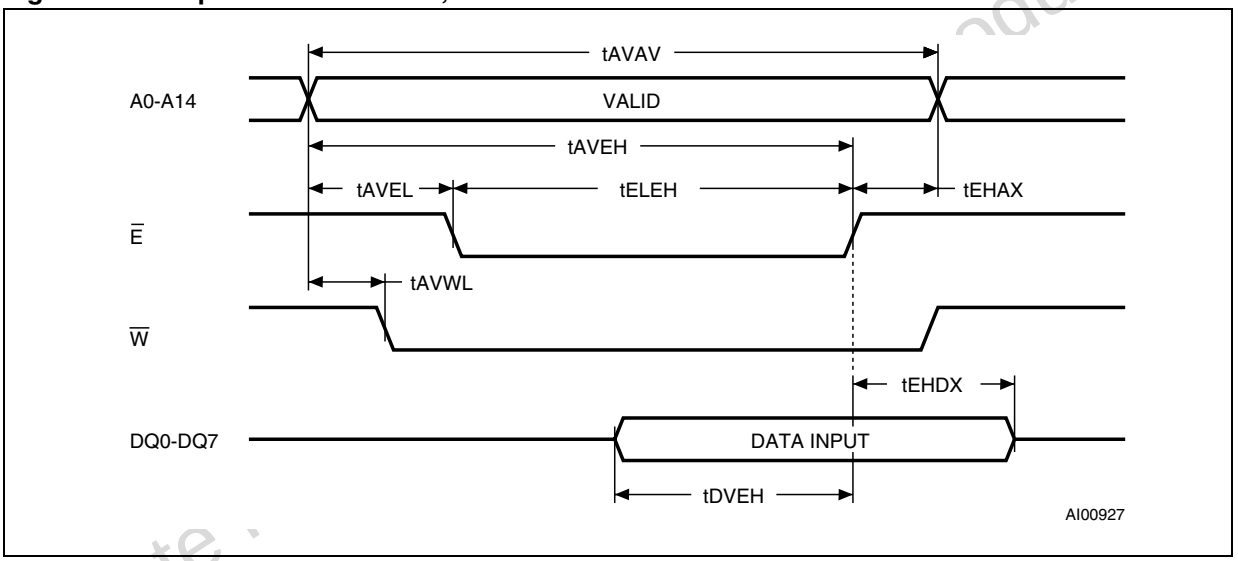


Table 4. Write mode AC characteristics

Symbol	Parameter[1]	M48Z32V		Unit
		–35		
		Min	Max	
t_{AVAV}	WRITE cycle time	35		ns
t_{AVWL}	Address valid to WRITE enable low	0		ns
t_{AVEL}	Address valid to chip enable low	0		ns
t_{WLWH}	WRITE enable pulse width	25		ns
t_{ELEH}	Chip enable low to chip enable high	25		ns
t_{WHAX}	WRITE enable high to address transition	0		ns
t_{EHAX}	Chip enable high to address transition	0		ns
t_{DVWH}	Input valid to WRITE enable high	12		ns
t_{DVEH}	Input valid to chip enable high	12		ns
t_{WHDX}	WRITE enable high to input transition	0		ns
t_{EHDX}	Chip enable high to input transition	0		ns
t_{WLQZ}[2][3]	WRITE enable low to output Hi-Z		13	ns
t_{AVWH}	Address valid to WRITE enable high	25		ns
t_{AVEH}	Address valid to chip enable high	25		ns
t_{WHQX}[2][3]	WRITE enable high to output transition	5		ns

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where noted).
2. C_L = 5pF (see *Figure 8 on page 16*).
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

2.3 Data retention mode

With valid V_{CC} applied, the M48Z32V operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance, and all inputs are treated as “Don't care.”

Note: A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z32V may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the external battery which preserves data.

As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD}(min) plus t_{REC}(min). Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

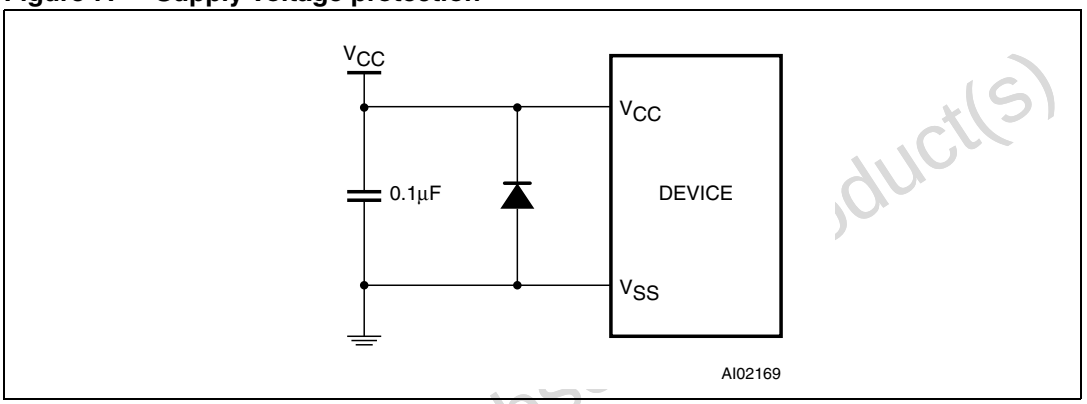
For more information on Battery Storage Life refer to the Application Note AN1012.

2.4 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1µF (see *Figure 7*) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, ST recommends connecting a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). (Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount).

Figure 7. Supply voltage protection



3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 5. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_A	Ambient operating temperature	Grade 1	0 to 70	°C
T_{STG}	Storage temperature (V_{CC} Off, Oscillator Off)	SOIC	–55 to 125	°C
T_{SLD} (1)	Lead solder temperature for 10 seconds		260	°C
V_{IO}	Input or output voltages		–0.3 to V_{CC} + 0.3	V
V_{CC}	Supply voltage		–0.3 to 4.6	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W

1. For Lead-free (Pb-free) lead finish: Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

Caution: *Negative undershoots below –0.3V are not allowed on any pin while in the battery back-up mode.*

4 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in *Table 6: Operating and AC measurement conditions*. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 6. Operating and AC measurement conditions

Parameter[1]		M48Z32V	Unit
Supply voltage (V_{CC})		3.0 to 3.6	V
Ambient operating temperature (T_A)	Grade 1	0 to 70	°C
Load Capacitance (C_L)		50	pF
Input rise and fall times		≤ 5	ns
Input pulse voltages		0 to 3	V
Input and output timing ref. voltages		1.5	V

1. Output Hi-Z is defined as the point where data is no longer driven.

Table 7. AC measurement load circuit

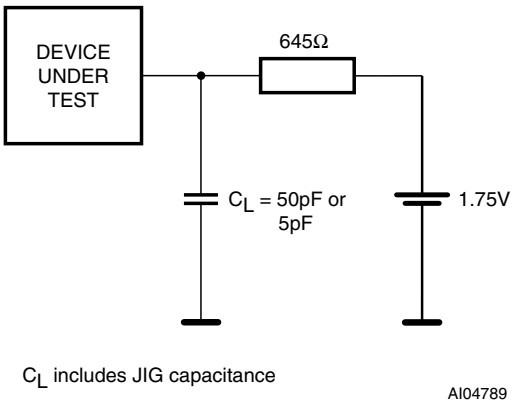


Table 8. Capacitance

Symbol	Parameter[1][2]	Min	Max	Unit
C_{IN}	Input capacitance		10	pF
C_{IO}[3]	Input / output capacitance		10	pF

1. Effective capacitance measured with power supply at 3.3V; sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected.

Table 9. DC characteristics

Sym	Parameter	Test condition(1)	Min	Typ	Max	Unit
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$			±1	µA
I_{LO}(2)	Output leakage current	$0V \le V_{OUT} \le V_{CC}$			±1	µA
I_{BAT}	Battery current	T_A = 40°C; V_{CC} = 0V V_{BAT} = 3V		0.2	1.2	µA
I_{CC1}	Supply current	I_O = 0mA; Cycle Time = Min $\overline{E}$ = 0.2V, other input = V_{CC} – 2V or 0.2V			45	mA
I_{CC2}	Supply current (TTL standby)	$\overline{E} = V_{IH}$			800	µA
I_{CC3}	Supply current (CMOS standby)	$\overline{E} = V_{CC} - 0.2V$			500	µA
V_{IL}(3)	Input low voltage		–0.3		0.8	V
V_{IH}	Input high voltage		2.2		V_{CC} + 0.3	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA			0.4	V
V_{OH}	Output high voltage	I_{OH} = –1mA	0.8V_{CC}			V

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where noted).
2. Outputs deselected.
3. Negative spikes of –1V allowed for up to 10ns once per cycle.

Table 10. Power down/up mode AC waveforms

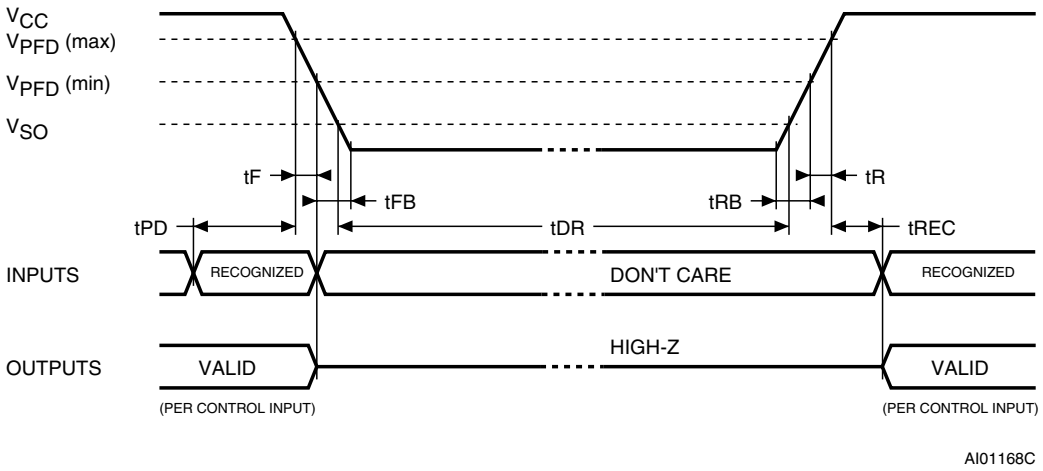


Table 11. Power down/up AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before power down	0		µs
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time	300		µs
t_{FB}[3]	V_{PFD} (min) to V_{SS} V_{CC} fall time	10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time	10		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} rise time	1		µs
t_{REC}[4]	V_{PFD} (max) to inputs recognized	40	200	ms

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.
4. t_{REC} (min) = 20ms for industrial temperature Grade (6) device.

Table 12. Power down/up trip points DC characteristics

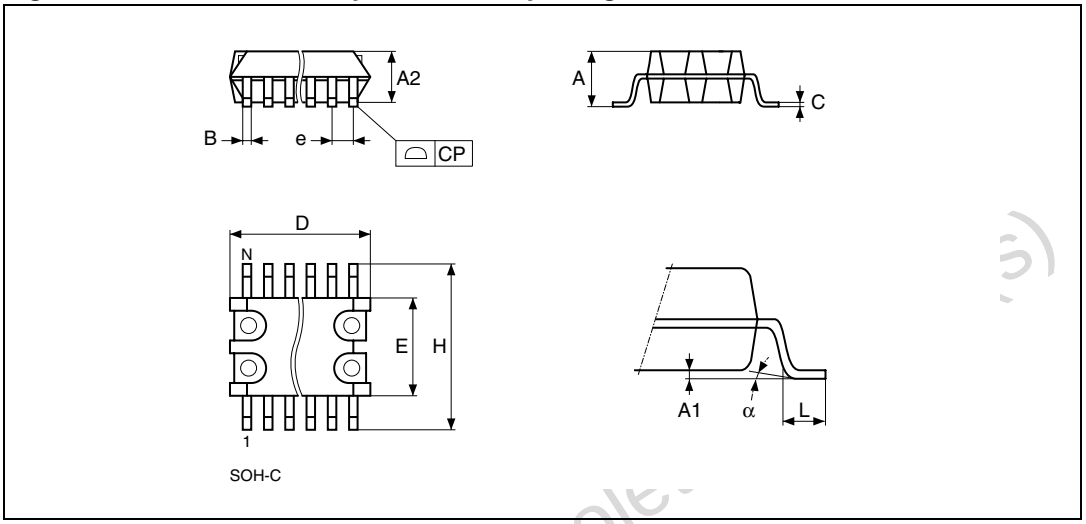
Symbol	Parameter[1][2]	Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect voltage	2.7	2.85	3.0	V
V_{SO}	Battery back-up switchover voltage		V_{PFD} – 100mV		V

1. All voltages referenced to V_{SS}.
2. Valid for ambient operating temperature: T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.0 to 3.6V (except where noted).

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 8. SO44 – 44-lead plastic, small package outline



Note: Drawing is not to scale.

Table 13. SO44 – 44-lead plastic, small package mechanical data

Symbol	mm			inch		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.46		0.014	0.018
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	0.81	–	–	0.032	–	–
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
a		0°	8°		0°	8°
N	44			44		
CP			0.10			0.004

6 Part numbering

Table 14. Ordering information scheme

Example: M48Z 32V –35 MT 1 F

Device type

M48Z

Supply voltage and write protect voltage

32V = V_{CC} = 3.0 to 3.6V; V_{PFD} = 2.7 to 3.0V

Speed

–35 = 35ns

Package

MT = 44-lead SOIC

Temperature range

1 = 0 to 70°C

Shipping method

E = Lead-free package (ECOPACK®), tubes

F = Lead-free package (ECOPACK®), tape & reel

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

7 Revision history

Table 15. Document revision history

Date	Revision	Changes
Oct-2002	1.0	First Issue
07-Nov-2002	1.1	Update Absolute Maximum Ratings, DC Characteristics (*Table 5*, *8*)
22-Mar-2004	2.0	Reformatted; updated Lead-free information (*Table 5*, *12*)
02-Nov-2007	3.0	Reformatted; added lead-free second level interconnect information to cover page and *Section 5: Package mechanical data*; package name change from SOH44 to SO44 throughout document; updated *Section 1: Summary*; updated *Table 3*; *4*, *5*, *6*, *9*, *11*, *13*, *14* and *Figure 8*.

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