



STB80NE03L-06

N-channel 30V - 0.005 Ω - 85A - D²PAK
STripFET™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STB80NE03L-06	30V	<0.006 Ω	80A

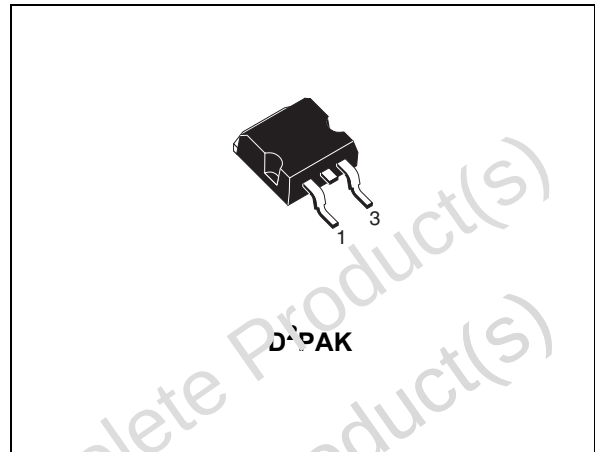
- Exceptional dv/dt capability
- Low gate charge 100°C
- 100% Avalanche tested

Description

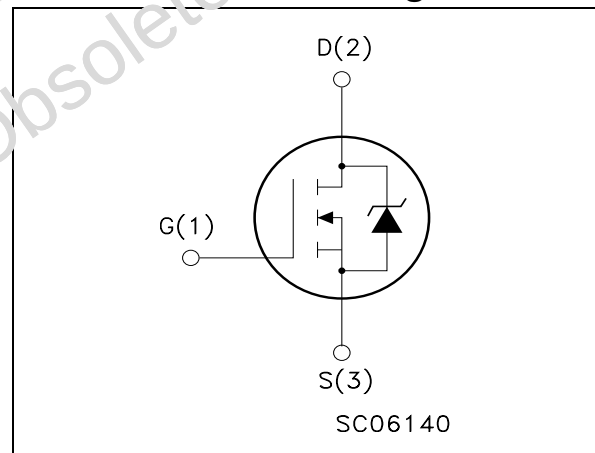
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB80NE03L-06	B80NE03L	D ² PAK	Tape & reel

Contents

1 **Electrical ratings** 3

2 **Electrical characteristics** 4

 2.1 Electrical characteristics (curves) 6

3 **Test circuit** 8

4 **Package mechanical data** 9

5 **Packaging mechanical data** 11

6 **Revision history** 12

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	60	A
$I_{DM}^{(1)}$	Drain current (pulsed)	320	A
	Derating factor	1	
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	150	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	7	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 20\text{A}$, $di/dt \leq 100\text{A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case Max	1	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
T_{sld}	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Table 3. Avalanche characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	80	A
E_{AS}	Single pulse avalanche energy (starting $T_J=25^\circ\text{C}$, $I_d=I_{AR}$, $V_{dd}=50\text{V}$)	600	mJ

2 Electrical characteristics

($T_{CASE} = 25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating @ } 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{DS} = \pm 20\text{V}$			± 1.00	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 40\text{A}$ $V_{GS} = 4.5\text{V}$, $I_D = 40\text{A}$		0.005	0.006 0.008	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D = 40\text{A}$	30	50		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		6500		pF
C_{oss}	Output capacitance			1500		pF
C_{rss}	Reverse Transfer Capacitance			500		pF
Q_g	Total gate charge	$V_{DD} = 24\text{V}$, $I_D = 80\text{A}$, $V_{GS} = 5\text{V}$		95	130	nC
Q_{gs}	Gate-source charge			30		nC
Q_{gd}	Gate-drain charge			44		nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{V}$, $I_D = 40\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 4.5\text{V}$ Figure 12.		40	55	ns
t_r	Rise time			260	350	ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD} = 24\text{V}$, $I_D = 80\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 5\text{V}$ Figure 12.		70	95	ns
t_f	Fall time			165	220	ns
t_c	Cross over time			250	340	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				320	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 80A, V_{GS} = 0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 80A, di/dt = 100A/\mu s, V_{DD} = 15V, T_J = 150^\circ C$ Figure 15.		75		ns
Q_{rr}	Reverse recovery charge			0.14		nC
I_{RRM}	Reverse recovery current			4		A

1. Pulse with limited by safe operating area

2. Pulsed: pulse duration = 300 μ s, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

Figure 2. Thermal impedance

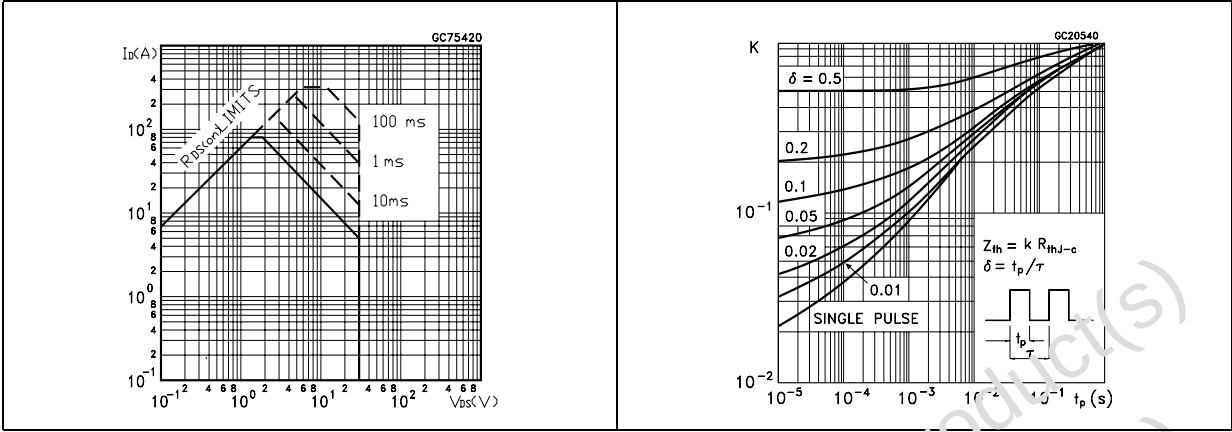


Figure 3. Output characteristics

Figure 4. Transfer characteristics

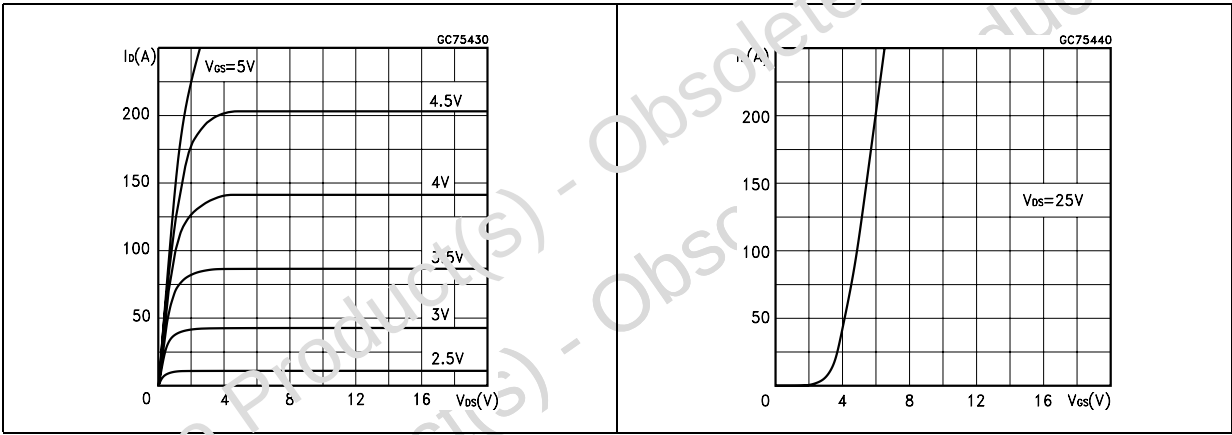


Figure 5. Transconductance

Figure 6. Static drain-source on resistance

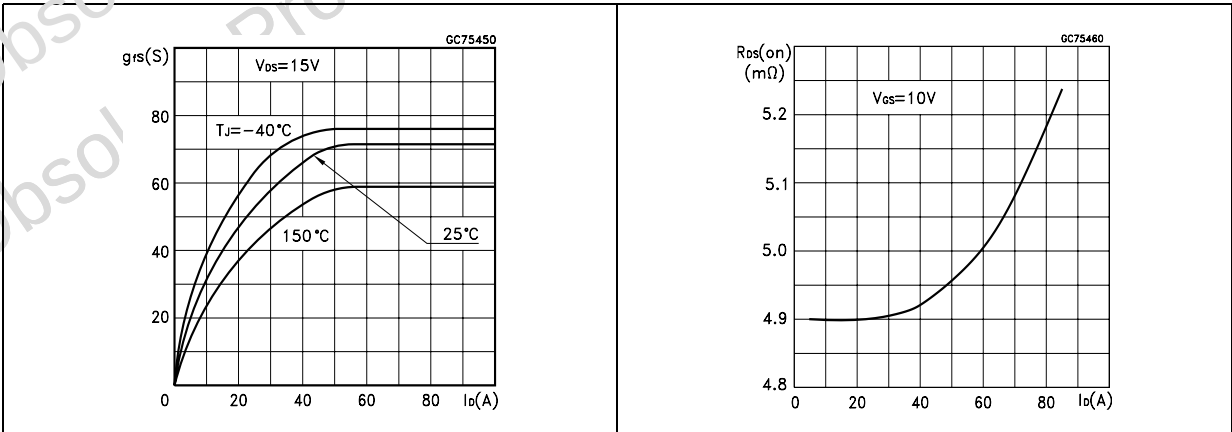


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

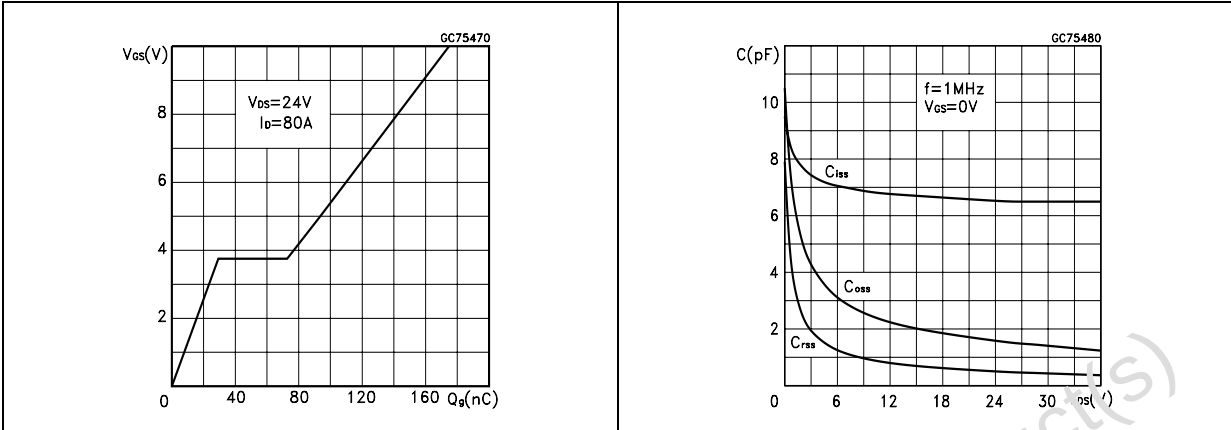


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

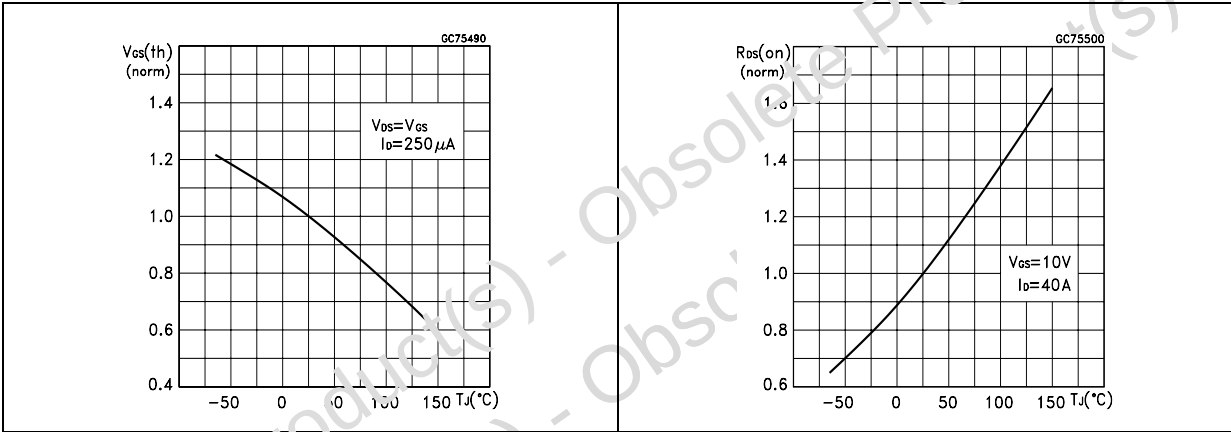
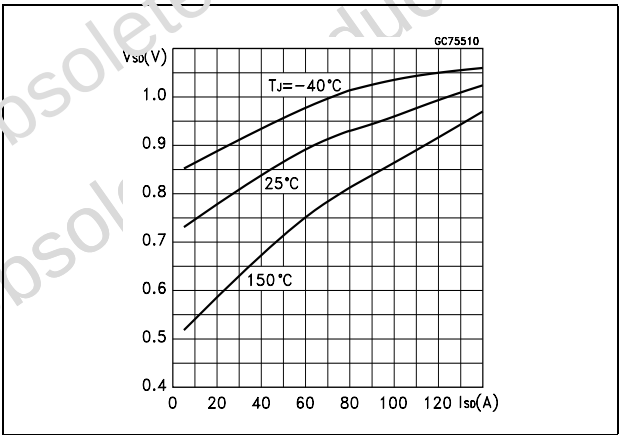


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load



Figure 13. Gate charge test circuit

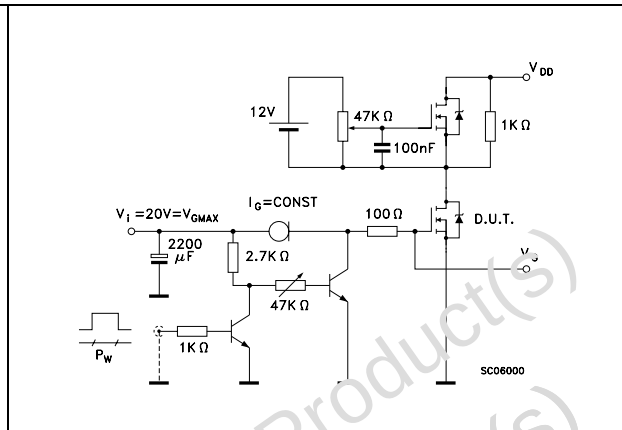


Figure 14. Test circuit for inductive load switching and diode recovery times

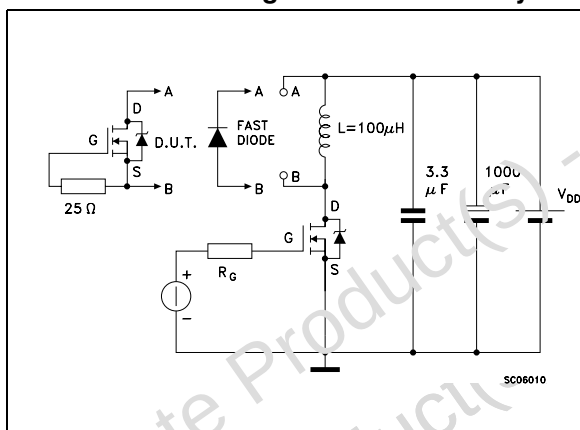


Figure 15. Unclamped inductive load test circuit

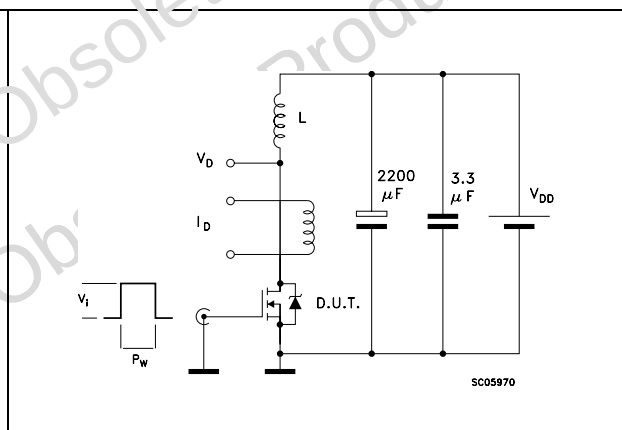
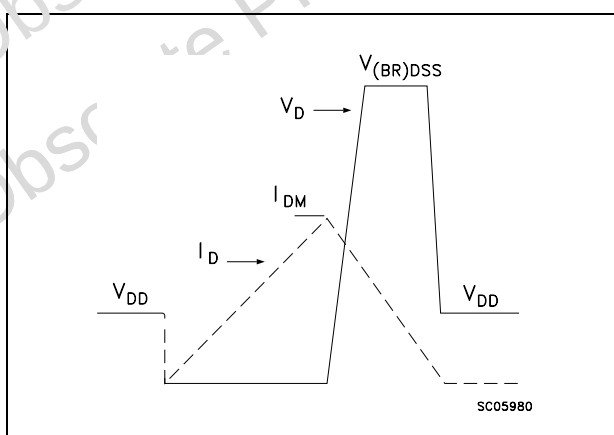


Figure 16. Unclamped inductive waveform



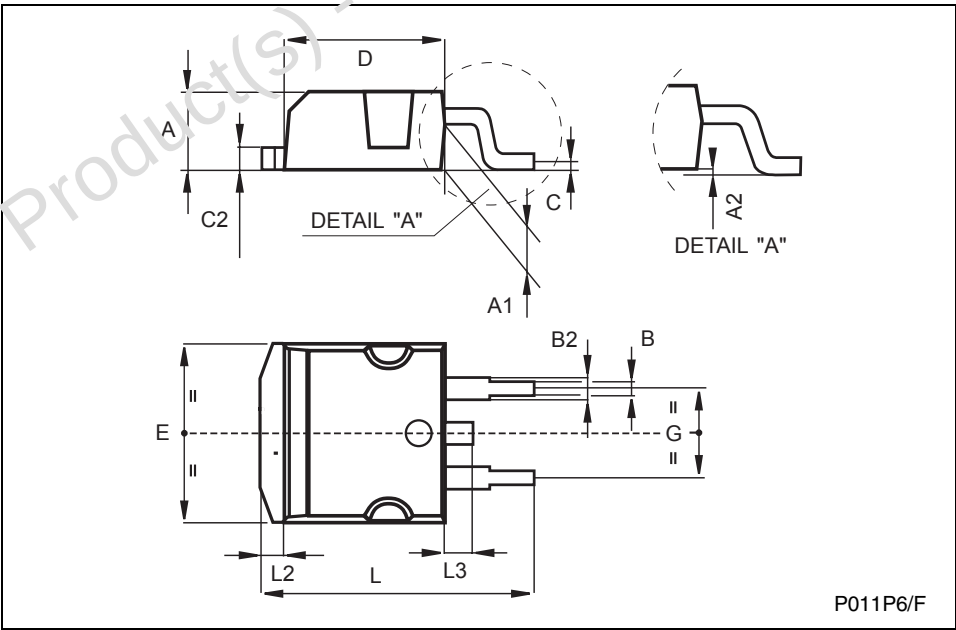
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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Obsolete Product(s) - Obsolete Product(s)

TO-263 (D²PAK) MECHANICAL DATA

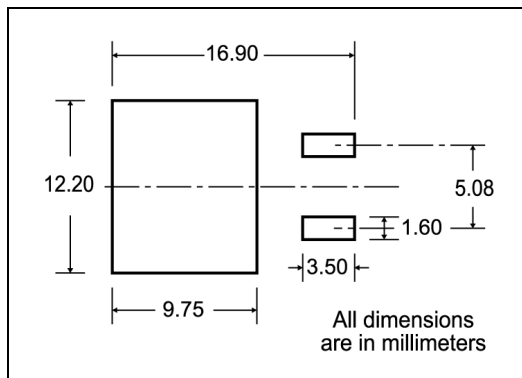
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
E	10		10.4	0.393		0.409
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068



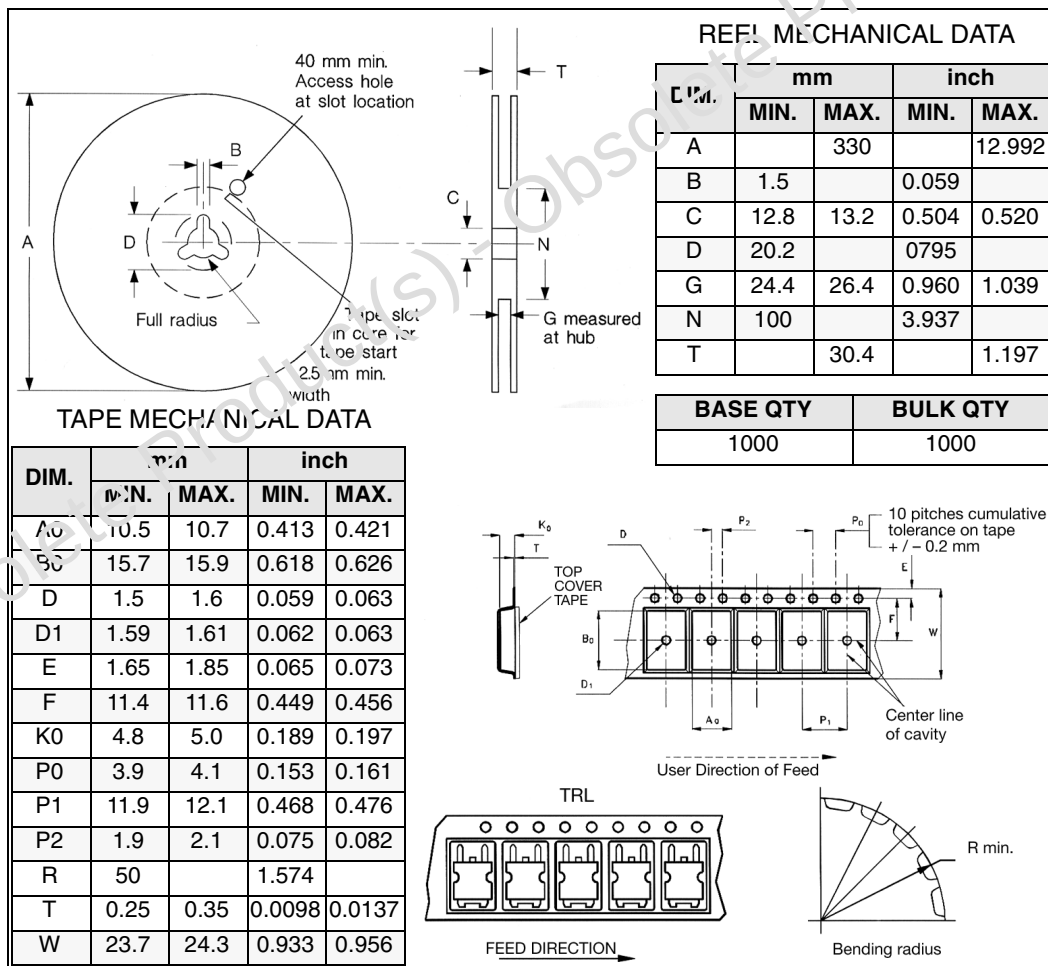
P011P6/F

5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 8. Revision history

Date	Revision	Changes
21-Jun-2004	5	Preliminary version
25-Jul-2006	6	New template, SOA updated

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