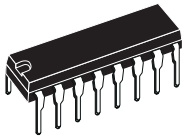
HCF4536B

PROGRAMMABLE TIMER

- 24 FLIP-FLOP STAGES - COUNTS FROM 2^0 TO 2^{24}
- LAST 16 STAGES SELECTABLE BY BCD SELECT CODE
- GROUP SELECT INDICATES ONE OR MORE PRIORITY INPUTS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP

ORDER CODES

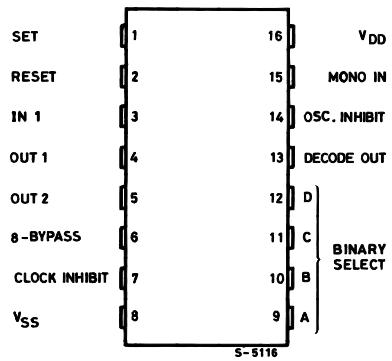
PACKAGE	TUBE	T & R
DIP	HCF4536BEY	

DESCRIPTION

HCF4536B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP package.

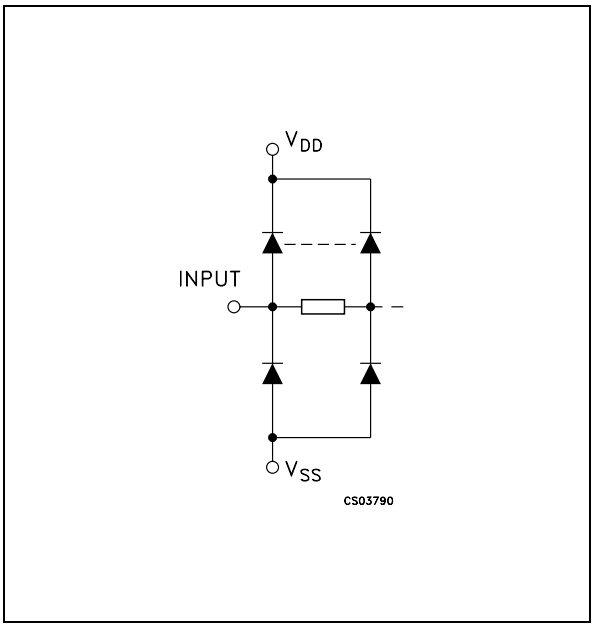
HCF4536B is a programmable timer consisting of 24 ripple-binary counter stages. The salient feature of this device is its flexibility. The device can count from 1 to 2^{24} or the first 8 stages can be bypassed to allow an output selectable by a 4-bit code, from any one of the remaining 16 stages. It can be driven by an external clock or an RC oscillator that can be constructed using on-chip components. Input IN1 serves as either the external clock input or the input to the on-chip RC oscillator. OUT1 and OUT2 are connection terminals for the external RC components. In addition, an on-chip monostable circuit is provided to allow a variable pulse width output. Various timing functions can be achieved using combinations of these capabilities. A logic "1" on the 8-BYPASS input enables a bypass of the first 8 stages and makes stage 9 the first counter stage of the last 16 stages. Selection of 1 of 16 outputs is accomplished by the decoder and the BCD inputs A, B, C, and D. MONO IN is the timing input

PIN CONNECTION



for the on-chip monostable oscillator. Grounding of the MONO IN terminal through a resistor of 10 KΩ or higher, disables the one shot circuit and connects the decoder directly to the DECODE OUT terminal. A resistor to V_{DD} and a capacitor to ground from the MONO IN terminal enables the one-shot circuit and controls its pulse width. A fast test mode is enabled by a logic "1" on 8-BYPASS, SET, and RESET. This mode divides the 24-stage counter into three 8-stage sections to facilitate a fast test sequence.

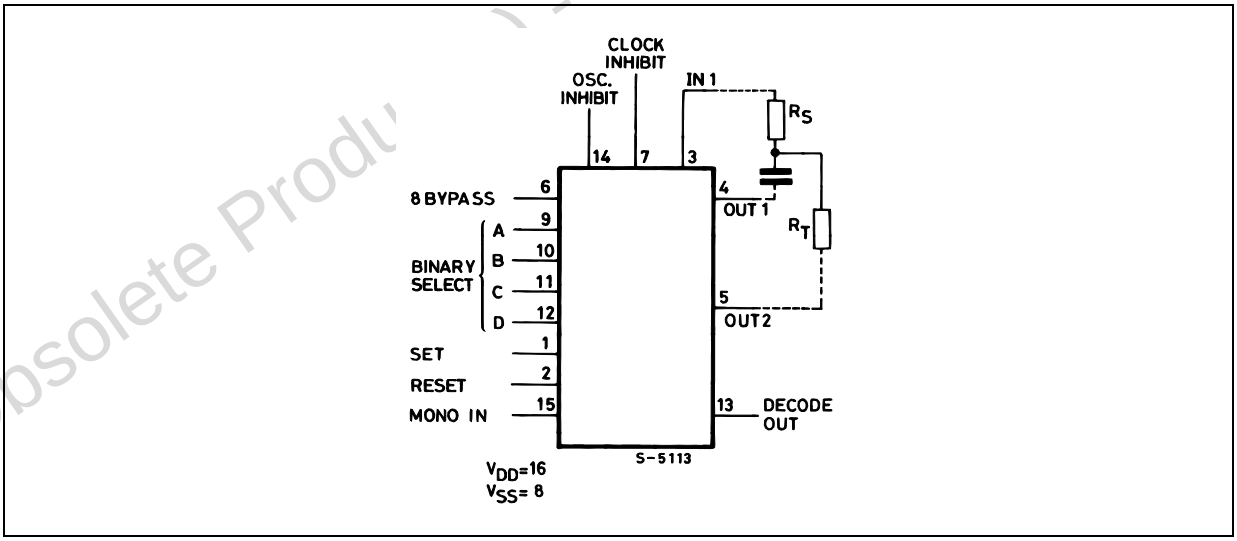
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
9, 10, 11, 12	A, B, C, D	Binary Select Input
1	SET	Set input
2	RESET	Reset Input
15	MONO IN	Monostable OscillatorTim-ing Input
6	8BYPASS	8Bypass input(bypass the first 8 stages)
3	IN1	External Clock Input or RC oscillator Input
4, 5	OUT1, OUT2	Outputs
13	DECODE OUT	Decode Out Terminal
7	CLOCK INHIBIT	Clock Inhibit Input
14	OSC. INHIBIT	Oscillator Inhibit Input
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM



TRUTH TABLE

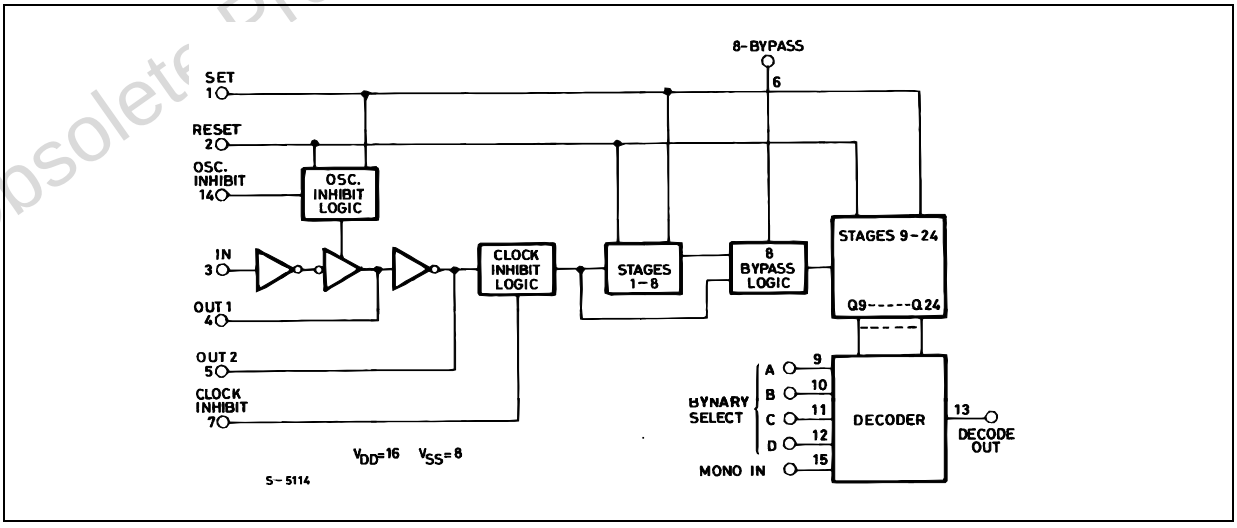
In1	Set	Reset	Clock Inh	Osc. Inh	Out1	Out2	Decode Out
⎍	L	L	L	L	⎍	⎎	No Change
⎎	L	L	L	L	⎎	⎍	Advance to Next State
X	H	L	L	L	L	H	H
X	L	H	L	L	L	H	L
X	L	L	H	L			No Change
L	L	L	L	X	L	H	No Change
H	L	L	L	⎍	⎎	⎍	Advance to Next State

X : Don't Care

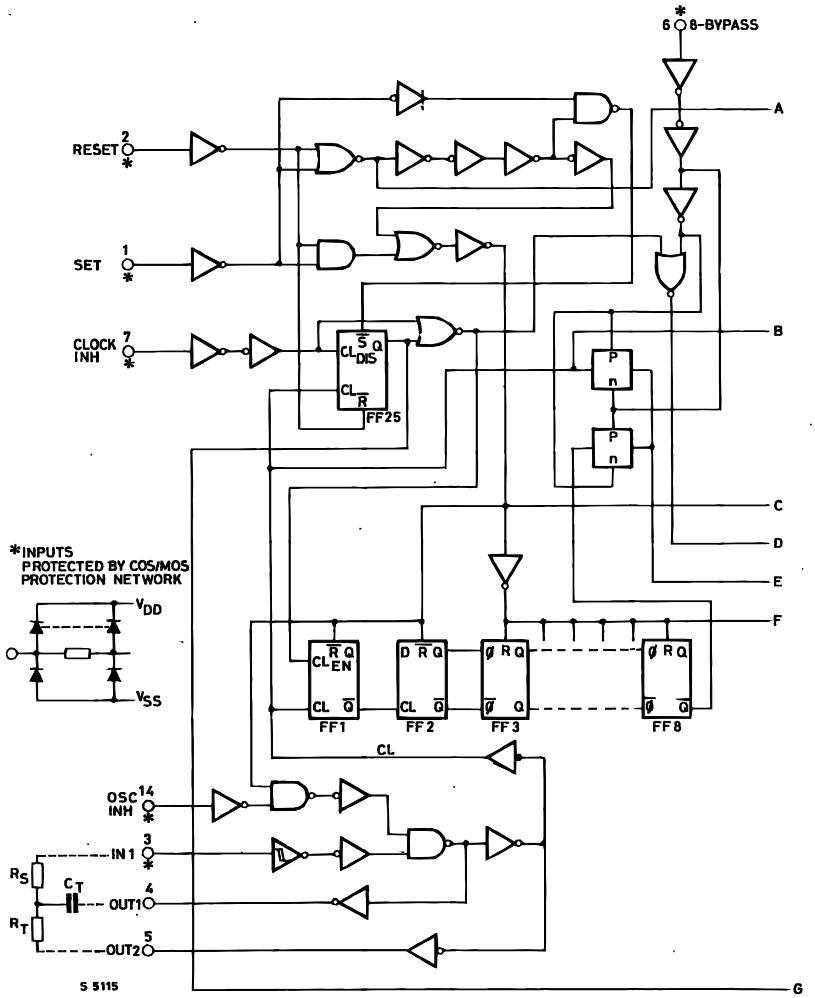
DECODE OUT SELECTION TABLE

D	C	B	A	NUMBER OF STAGES IN DIVIDER CHAIN	
				8-BYPASS = 0	8-BYPASS = 1
L	L	L	L	9	1
L	L	L	H	10	2
L	L	H	L	11	3
L	L	H	H	12	4
L	H	L	L	13	5
L	H	L	H	14	6
L	H	H	L	15	7
L	H	H	H	16	8
H	L	L	L	17	9
H	L	L	H	18	10
H	L	H	L	19	11
H	L	H	H	20	12
H	H	L	L	21	13
H	H	L	H	22	14
H	H	H	L	23	15
H	H	H	H	24	16

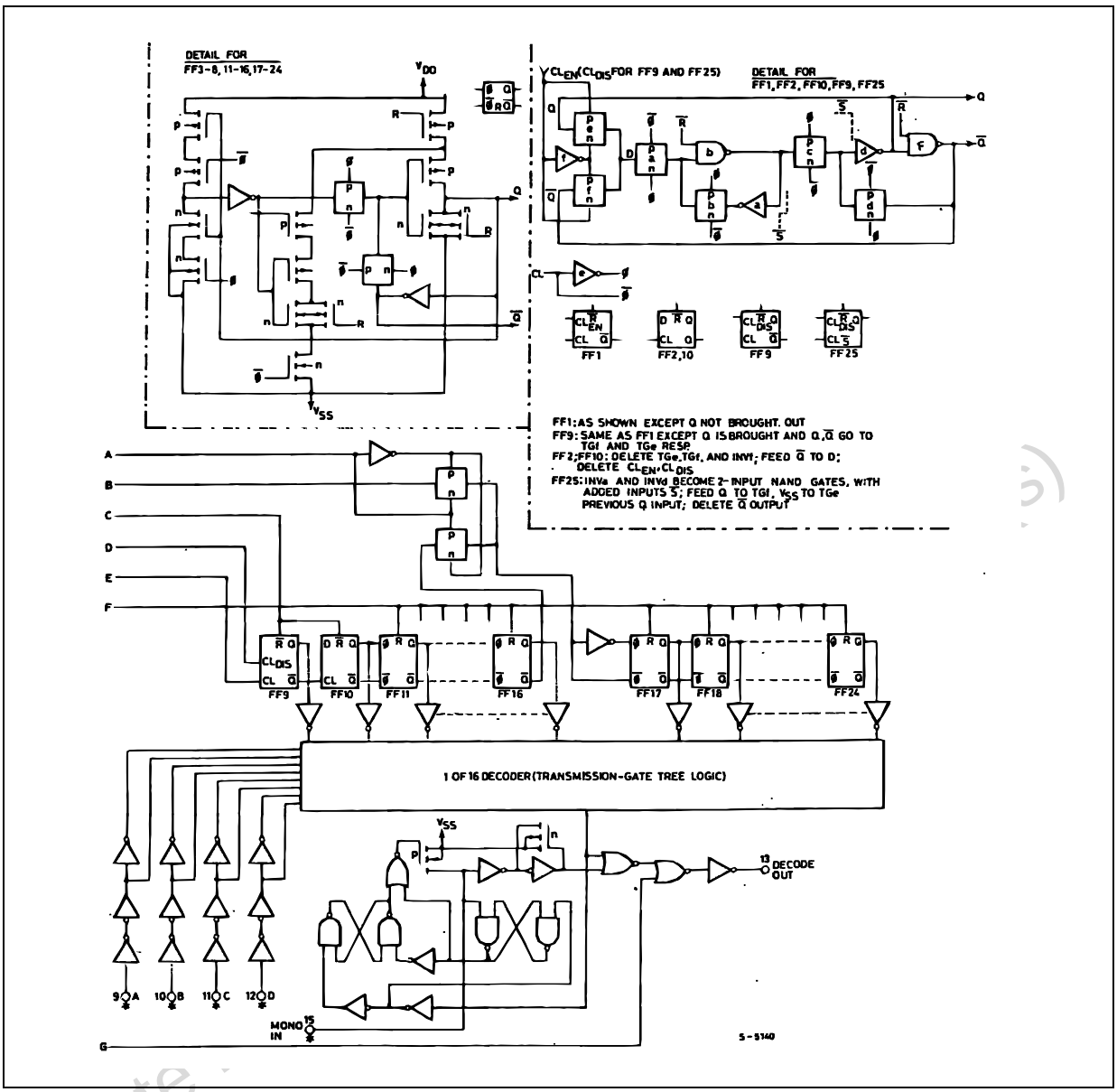
BLOCK DIAGRAM



LOGIC DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

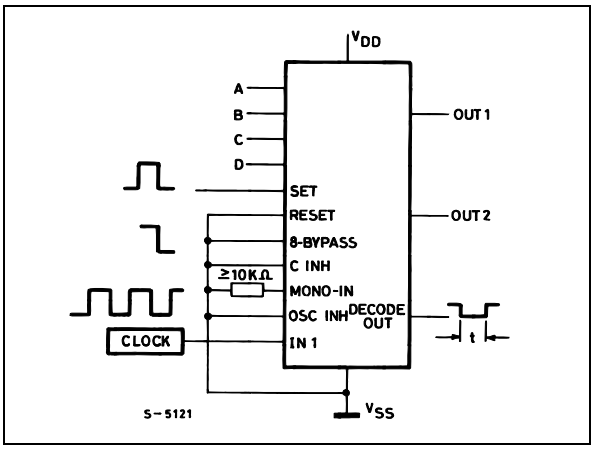
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (Clock to Q1, 8-Bypass High)	5			1	2	µs
		10			0.5	1	
		15			0.35	0.7	
	Propagation Delay Time (Clock to Q1, 8-Bypass Low)	5			2.5	5	µs
		10			0.8	0.6	
		15			0.6	1.2	
	Propagation Delay Time (Clock to Q16)	5			4	8	µs
		10			1.5	3	
		15			1	2	
	Propagation Delay Time (Qn to Qn+1)	5			150	300	ns
		10			75	150	
		15			50	100	
t_{PLH}	Propagation Delay Time	5			300	600	ns
		10			125	250	
		15			80	160	
t_{PHL}	Reset to Qn	5			3	6	µs
		10			1	2	
		15			0.75	1.5	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_W	Pulse Width Clock	5			200	400	ns
		10			75	150	
		15			50	100	
	Set	5			200	400	ns
		10			100	200	
		15			60	120	
	Reset	5			3	6	µs
		10			1	2	
		15			0.75	1.5	
	Recovery Time Set	5			2.5	5	µs
		10			1	2	
		15			0.6	1.6	
	Reset	5			3.5	7	µs
		10			1.5	3	
		15			1	2	
t_r, t_f	Clock Input Rise or Fall Time	5		Unlimited			µs
		10					
		15					
f_{CL}	Maximum Clock Input Frequency	5		0.5	1		MHz
		10		1.5	3		
		15		2.5	5		

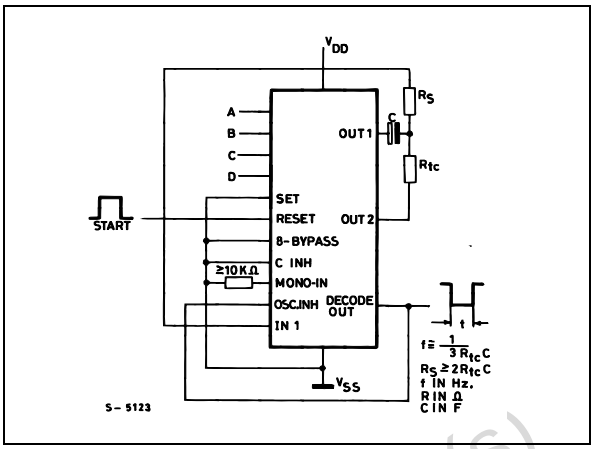
(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

TYPICAL APPLICATIONS

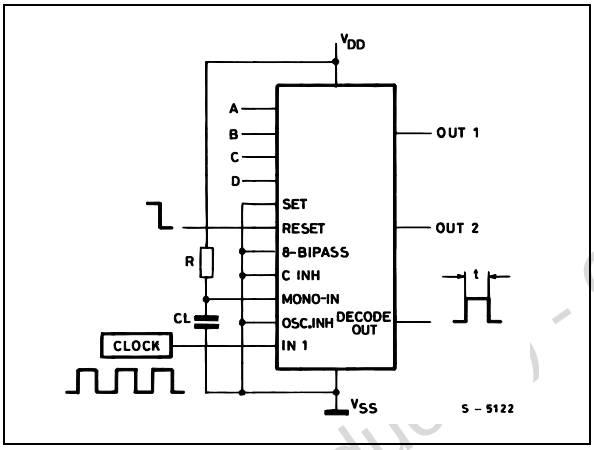
Time Internal Configuration Using External Clock; Set and Clock Inhibit Functions



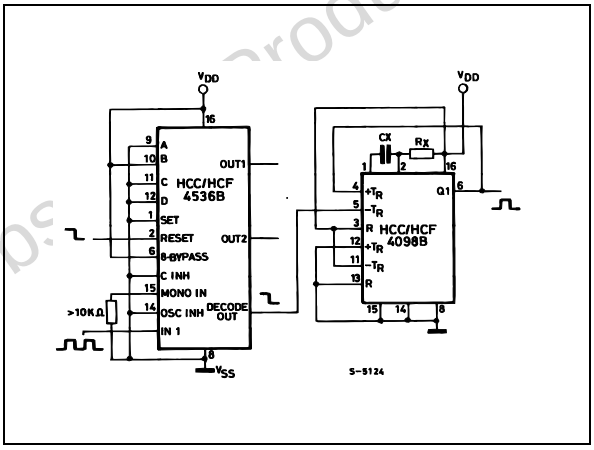
Time Internal Configuration Using On-Chip RC oscillator and Reset Input to Initiate Time Interval



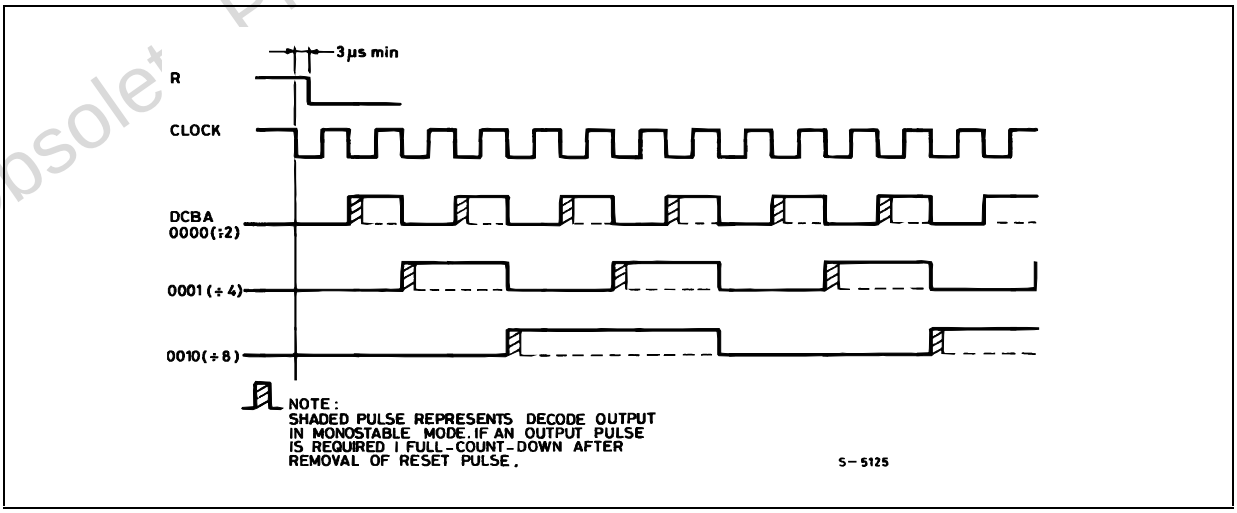
Time Internal Configuration Using Ext. Ck; Reset and Output Monostable to Achieve a Pulse Out



Use of HCF4098B and HCF4536B to get Decode Pulse 8 Clock Pulses after Reset Pulses



TIMING DIAGRAM

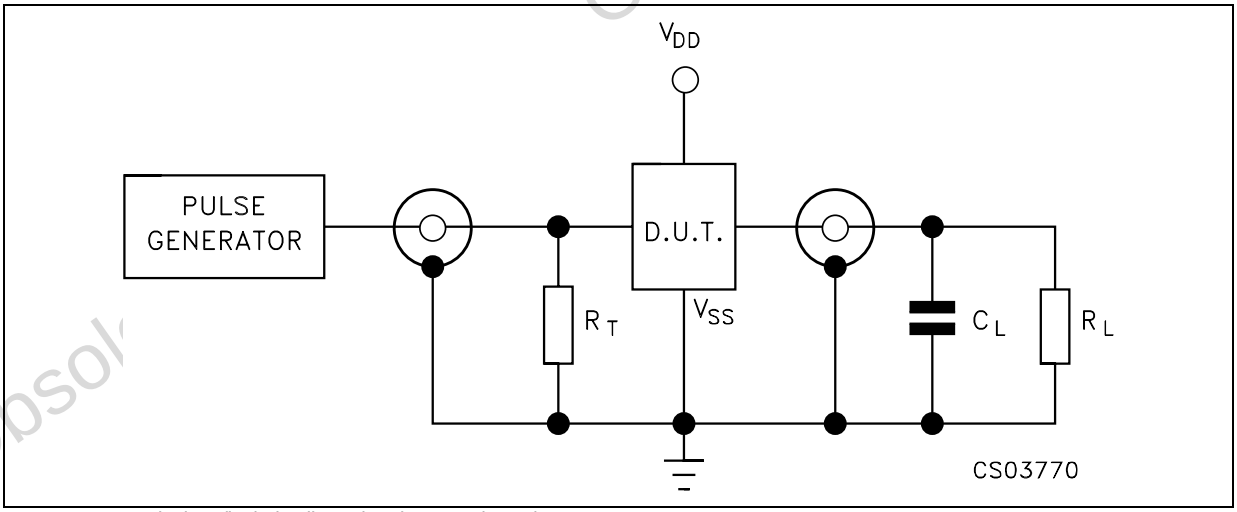


FUNCTIONAL TEST SEQUENCE					
Inputs				Outputs	COMMENTS
In 1	Set	Reset	8-Bypass	Decade Out Q1 Thru Q24	All 24 steps are in reset mode
H	L	H	H	L	Counter is in three 8-stage section in parallel mode
H	H	H	H	L	
L	H	H	H	L	First "H" to "L" Transition of Clock
H					255 "H" to "L" transitions are clocked in the counter
L	H	H	H		
L	H	H	H	H	The 255 "H" to "L" Transition
L	L	L	L	H	Counter converted back to 24 stages in series mode. Set and Reset must be connected together and simultaneously go from "H" to "L"
H	L	L	L	H	In_1 switches to a "H"
L	L	L	L	L	Counter Ripples from an all "H" state to an all "L" state

FUNCTIONAL TEST SEQUENCE

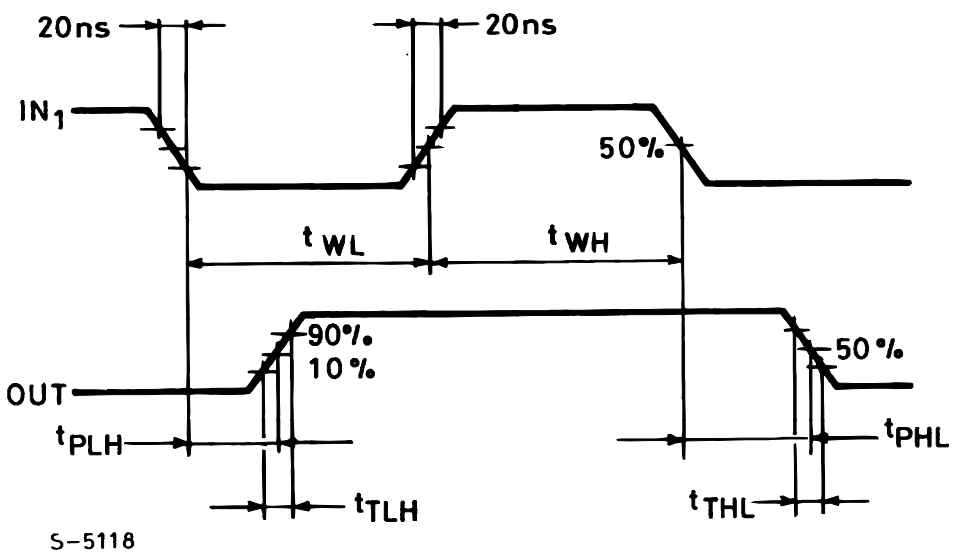
Test function has been included for the reduction of test time required to exercise all 24 counter stages.This test function divides the counter into three 8-stage section and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "H". The counter is now returned to the normal 24-steps in series configuration. One more pulse is entered into In1 which will cause the counter to ripple from an all "H" state to an all "L" state.

TEST CIRCUIT



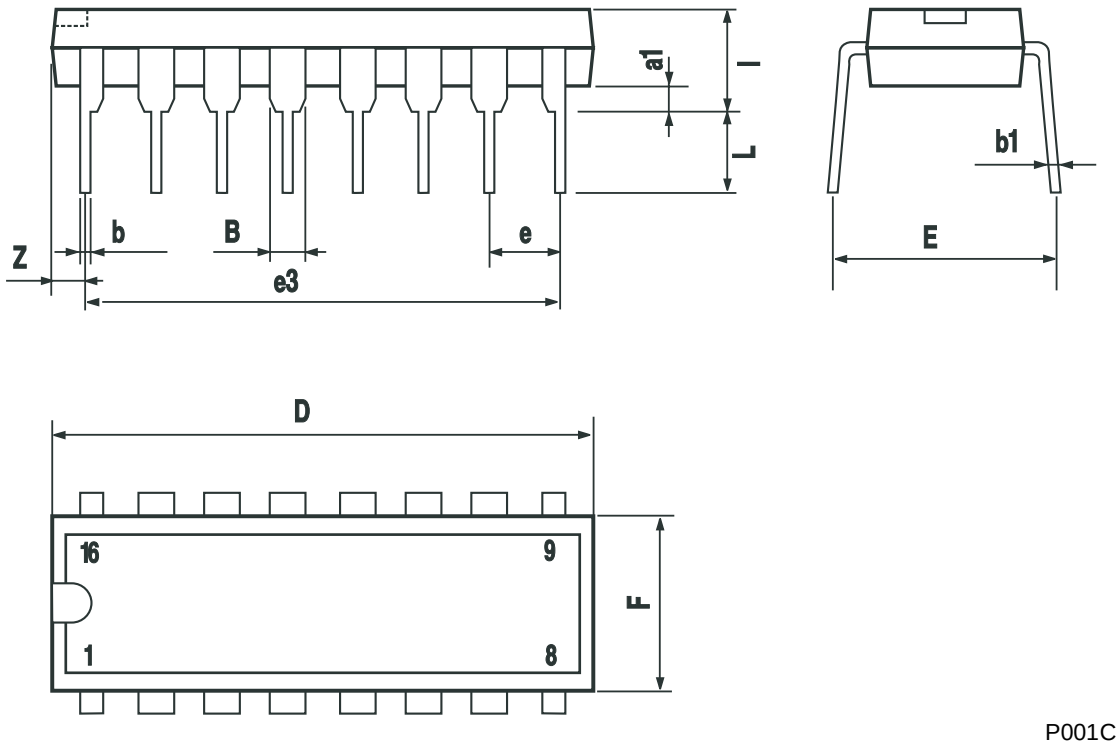
C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM : PROPAGATION DELAY TIMES, PULSE WIDTH CLOCK



Plastic DIP-16 (0.25) MECHANICAL DATA

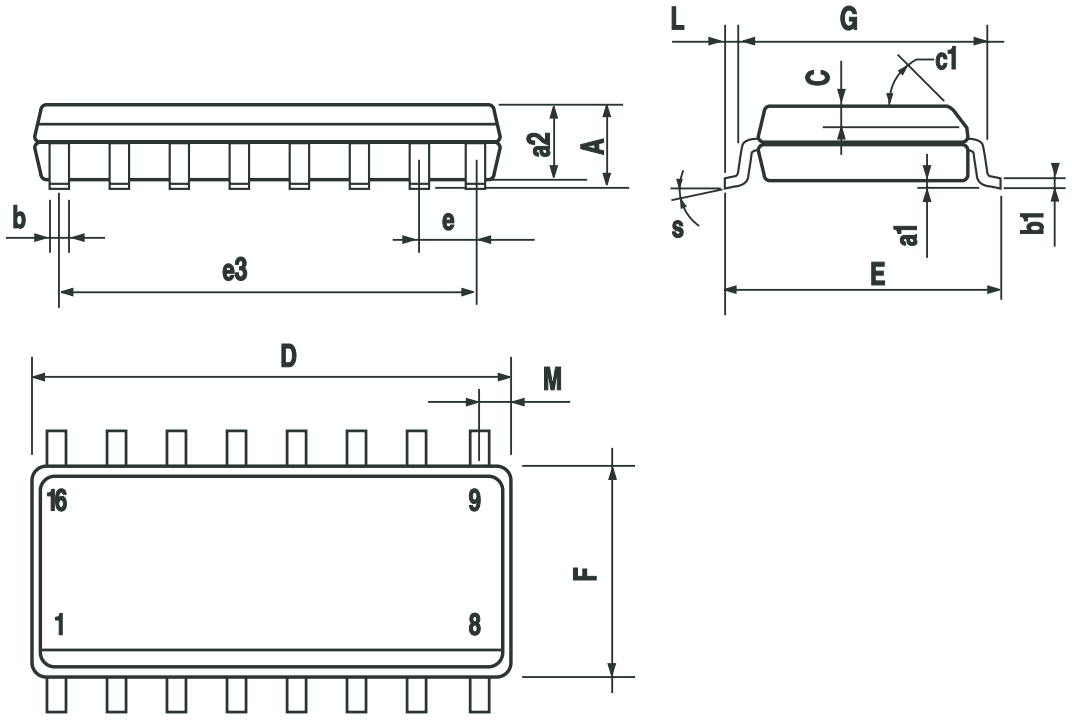
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



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