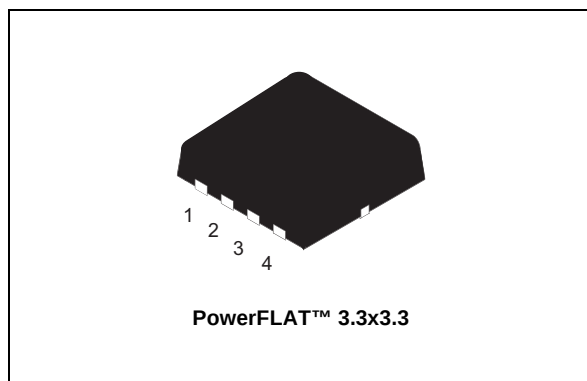


## N-channel 100 V, 0.027 $\Omega$ typ., 7 A STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 3.3x3.3 package

Datasheet - production data



### Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max | $I_D$ |
|------------|----------|------------------|-------|
| STL7N10F7  | 100 V    | 0.035 $\Omega$   | 7 A   |

- N-channel enhancement mode
- Lower  $R_{DS(on)}$  x area vs previous generation
- 100% avalanche rated

### Applications

- Switching applications

### Description

This device utilizes the 7<sup>th</sup> generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest  $R_{DS(on)}$  in all packages.

Figure 1. Internal schematic diagram

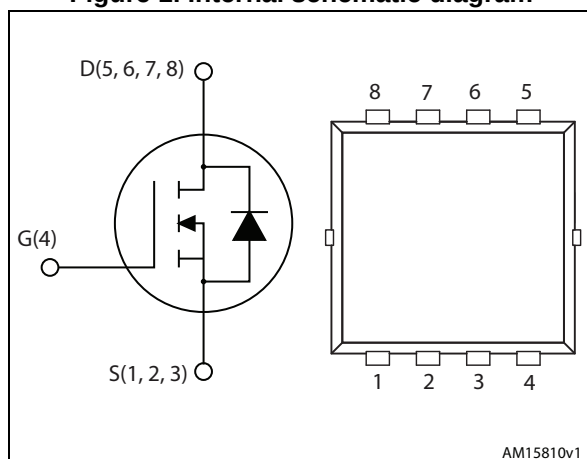


Table 1. Device summary

| Order code | Marking | Package            | Packaging     |
|------------|---------|--------------------|---------------|
| STL7N10F7  | 7N10F   | PowerFLAT™ 3.3x3.3 | Tape and reel |

Contents

1      **Electrical ratings** ..... 3

2      **Electrical characteristics** ..... 4

      2.1    **Electrical characteristics (curves)** ..... 6

3      **Test circuits** ..... 8

4      **Package mechanical data** ..... 9

5      **Revision history** ..... 13



# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol            | Parameter                                                           | Value      | Unit               |
|-------------------|---------------------------------------------------------------------|------------|--------------------|
| $V_{DS}$          | Drain-source voltage                                                | 100        | V                  |
| $V_{GS}$          | Gate-source voltage                                                 | $\pm 20$   | V                  |
| $I_D^{(1)}$       | Drain current (continuous) at $T_{pcb}=25\text{ }^{\circ}\text{C}$  | 7          | A                  |
| $I_D^{(1)}$       | Drain current (continuous) at $T_{pcb}=100\text{ }^{\circ}\text{C}$ | 5          | A                  |
| $I_{DM}^{(1)(2)}$ | Drain current (pulsed)                                              | 28         | A                  |
| $P_{TOT}^{(1)}$   | Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$         | 2.9        | W                  |
| $P_{TOT}^{(3)}$   | Total dissipation at $T_c = 25\text{ }^{\circ}\text{C}$             | 50         | W                  |
| $T_J$             | Operating junction temperature                                      | -55 to 150 | $^{\circ}\text{C}$ |
| $T_{stg}$         | Storage temperature                                                 |            | $^{\circ}\text{C}$ |

1. The value is rated according  $R_{thj-pcb}$
2. Pulse width limited by safe operating area.
3. This value is rated according to  $R_{thj-c}$ .

**Table 3. Thermal resistance**

| Symbol              | Parameter                        | Value | Unit                        |
|---------------------|----------------------------------|-------|-----------------------------|
| $R_{thj-case}$      | Thermal resistance junction-case | 2.5   | $^{\circ}\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb  | 42.8  | $^{\circ}\text{C}/\text{W}$ |

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{sec}$

## 2 Electrical characteristics

( $T_{CASE}=25\text{ }^{\circ}\text{C}$  unless otherwise specified)

Table 4. On/off states

| Symbol        | Parameter                                       | Test conditions                                           | Min. | Typ.  | Max.  | Unit          |
|---------------|-------------------------------------------------|-----------------------------------------------------------|------|-------|-------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage, $V_{GS}=0$      | $I_D = 250\text{ }\mu\text{A}$                            | 100  |       |       | V             |
| $I_{DSS}$     | Zero gate voltage drain current, ( $V_{GS}=0$ ) | $V_{DS}=100\text{ V}$                                     |      |       | 1     | $\mu\text{A}$ |
|               |                                                 | $V_{DS}=100\text{ V}$ , $T_C=125\text{ }^{\circ}\text{C}$ |      |       | 100   | $\mu\text{A}$ |
| $I_{GSS}$     | Gate body leakage current                       | $V_{GS}=20\text{ V}$ , ( $V_{DS}=0$ )                     |      |       | 100   | nA            |
| $V_{GS(th)}$  | Gate threshold voltage                          | $V_{DS}=V_{GS}$ , $I_D=250\text{ }\mu\text{A}$            | 2.5  |       | 4.5   | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance               | $V_{GS}=10\text{ V}$ , $I_D=3.5\text{ A}$                 |      | 0.027 | 0.035 | $\Omega$      |

Table 5. Dynamic

| Symbol    | Parameter                    | Test conditions                                                                    | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|------------------------------------------------------------------------------------|------|------|------|------|
| $C_{iss}$ | Input capacitance            | $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$ ,<br>$V_{GS}=0$                            | -    | 920  | -    | pF   |
| $C_{oss}$ | Output capacitance           |                                                                                    | -    | 215  | -    | pF   |
| $C_{rss}$ | Reverse transfer capacitance |                                                                                    | -    | 19   | -    | pF   |
| $Q_g$     | Total gate charge            | $V_{DD}=50\text{ V}$ , $I_D=7\text{ A}$<br>$V_{GS}=10\text{ V}$<br>(see Figure 14) | -    | 14   | -    | nC   |
| $Q_{gs}$  | Gate-source charge           |                                                                                    | -    | 7    | -    | nC   |
| $Q_{gd}$  | Gate-drain charge            |                                                                                    | -    | 3    | -    | nC   |

Table 6. Switching times

| Symbol       | Parameter           | Test conditions                                                                                                  | Min. | Typ. | Max. | Unit |
|--------------|---------------------|------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD}=50\text{ V}$ , $I_D=3.5\text{ A}$ ,<br>$R_G=4.7\text{ }\Omega$ , $V_{GS}=10\text{ V}$<br>(see Figure 13) | -    | 9.8  | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                  | -    | 14   | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |                                                                                                                  | -    | 14.8 | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                  | -    | 4.6  | -    | ns   |

Table 7. Source drain diode

| Symbol          | Parameter                     | Test conditions                                                                                                                                  | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                  | -    |      | 7    | A    |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                  | -    |      | 28   | A    |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 7\text{ A}$ , $V_{GS} = 0$                                                                                                             | -    |      | 1.1  | V    |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 7\text{ A}$ ,<br>$di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 80\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$<br>(see Figure 18) | -    | 38   |      | ns   |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                  | -    | 29   |      | nC   |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                  | -    | 1.7  |      | A    |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

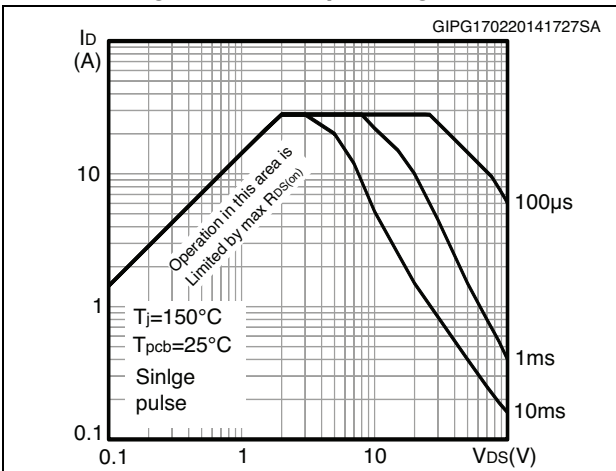


Figure 3. Thermal impedance

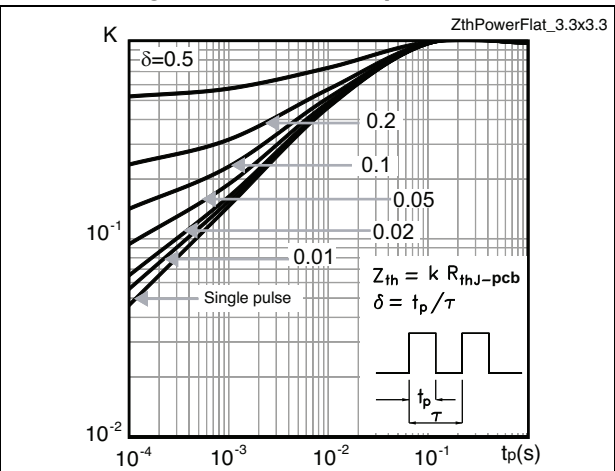


Figure 4. Output characteristics

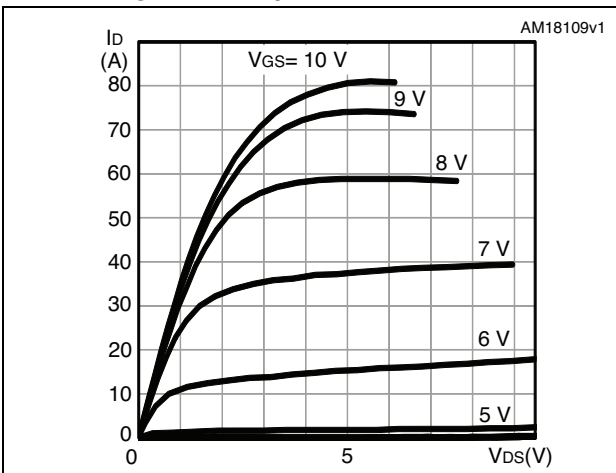


Figure 5. Transfer characteristics

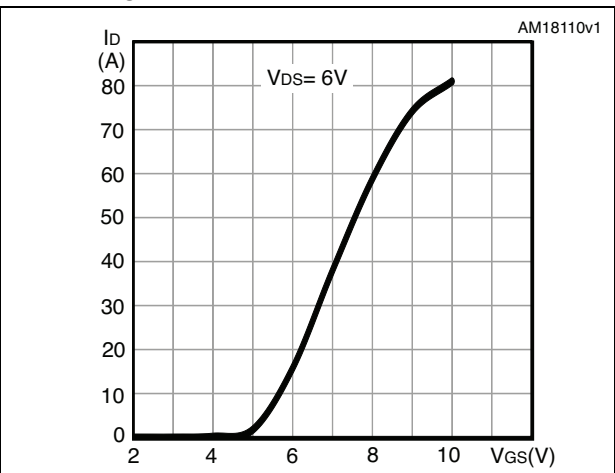


Figure 6. Gate charge vs gate-source voltage

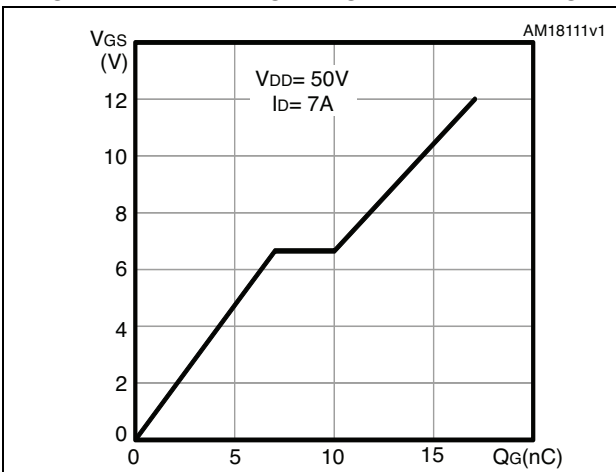


Figure 7. Static drain-source on-resistance

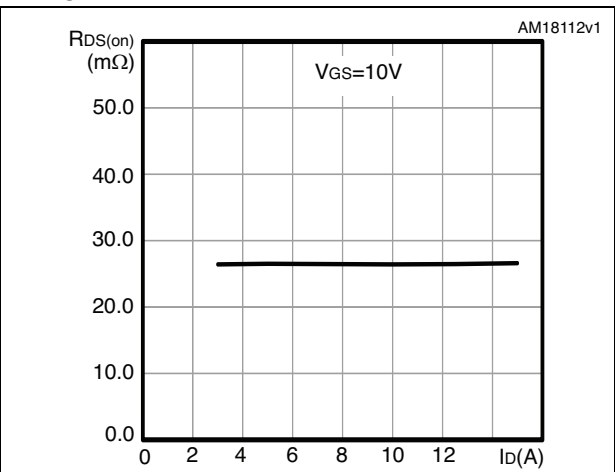


Figure 8. Capacitance variations

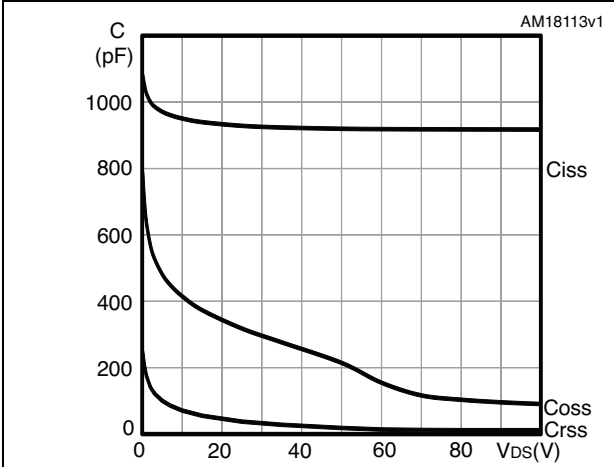


Figure 9. Normalized  $V_{(BR)DSS}$  vs temperature

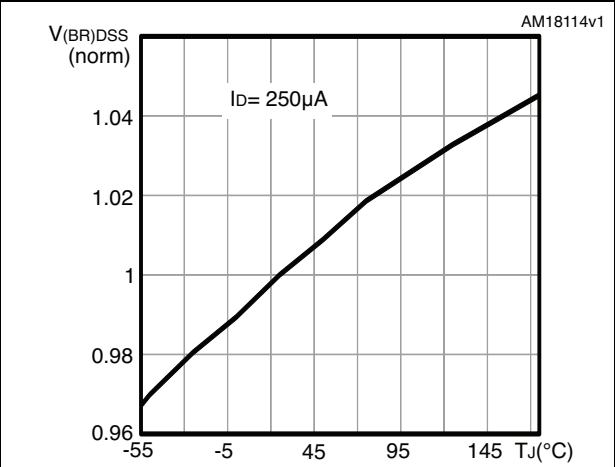


Figure 10. Normalized gate threshold voltage vs temperature

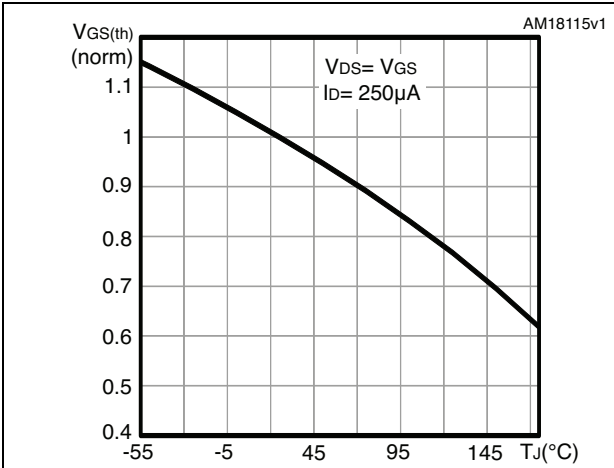


Figure 11. Normalized on-resistance vs temperature

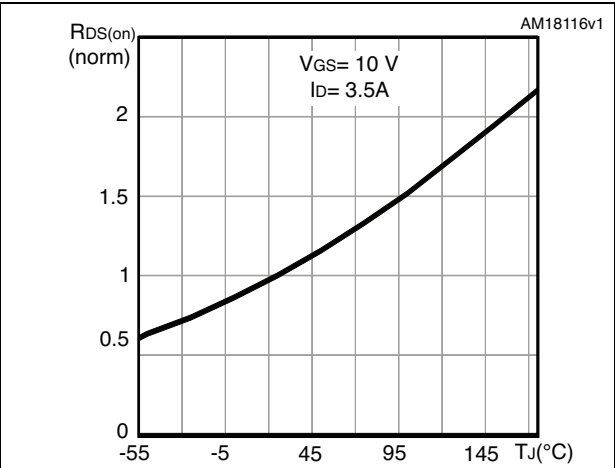
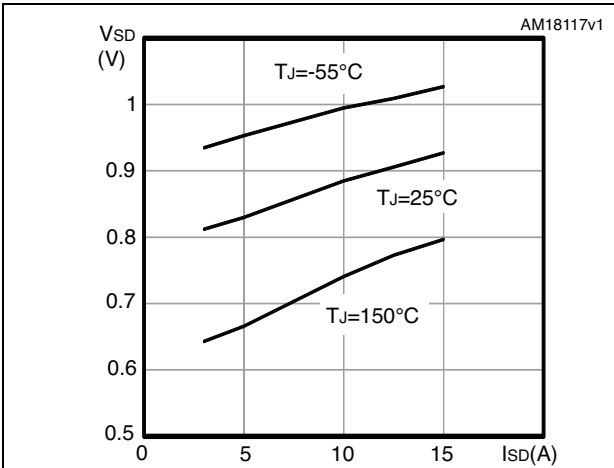
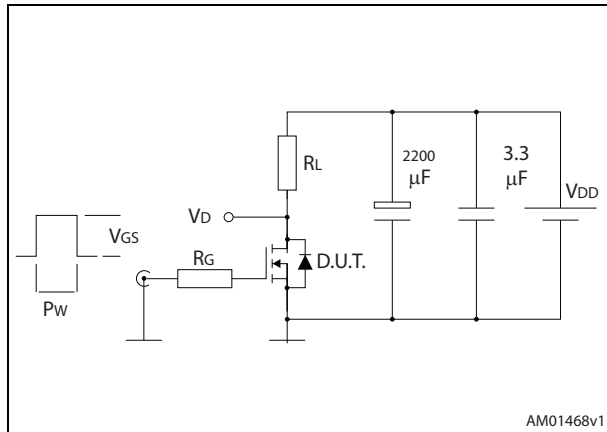


Figure 12. Source-drain diode forward characteristics

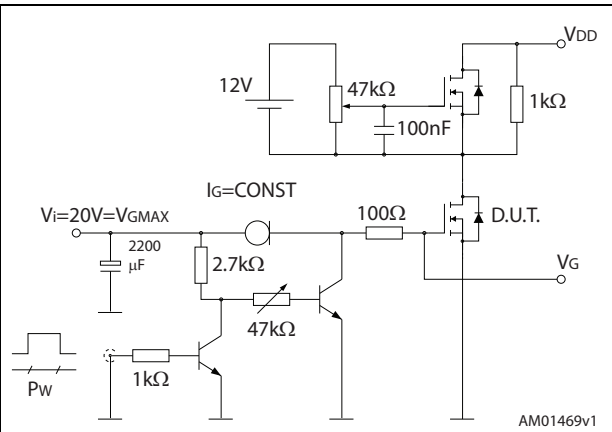


### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**



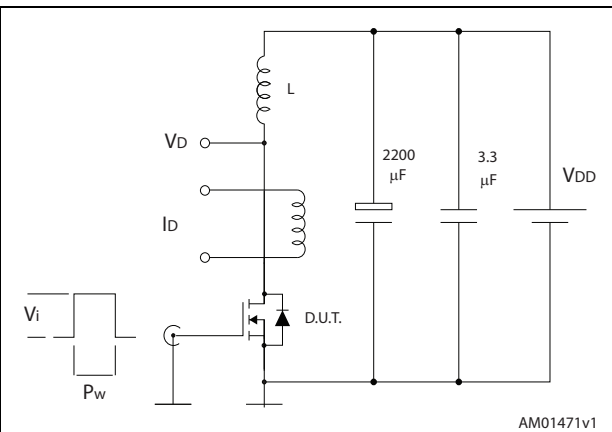
**Figure 14. Gate charge test circuit**



**Figure 15. Test circuit for inductive load switching and diode recovery times**



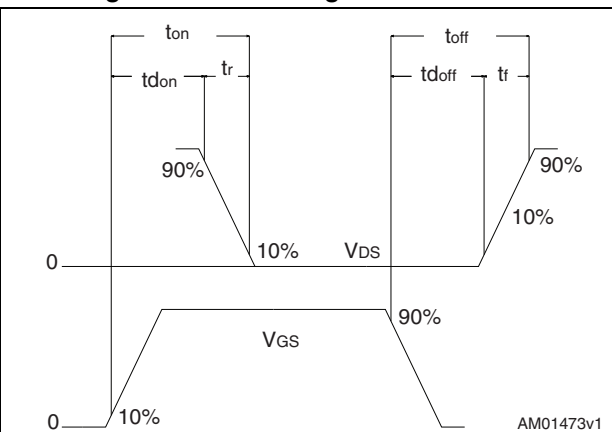
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 19. PowerFLAT™ 3.3 x 3.3 drawing

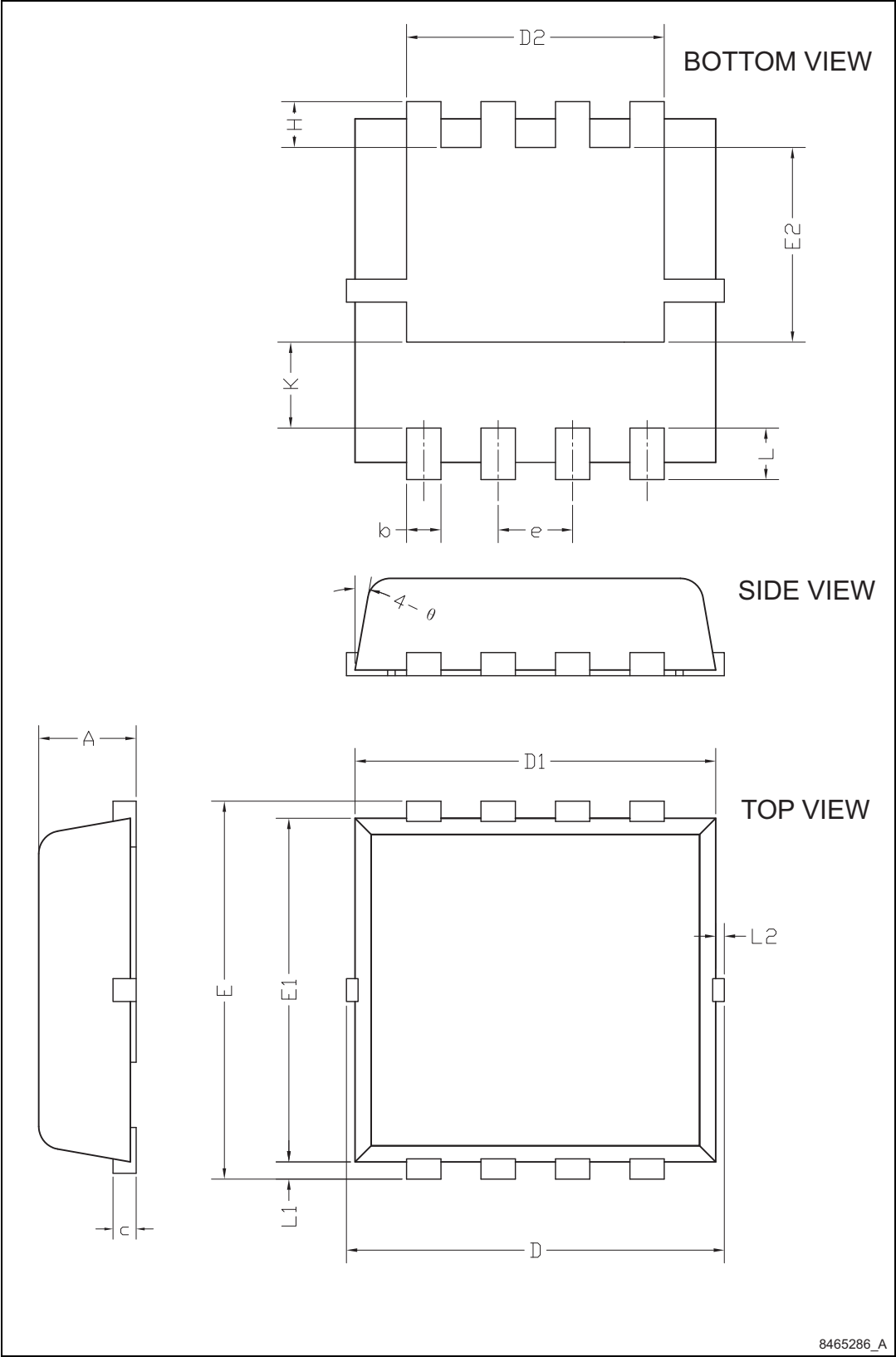
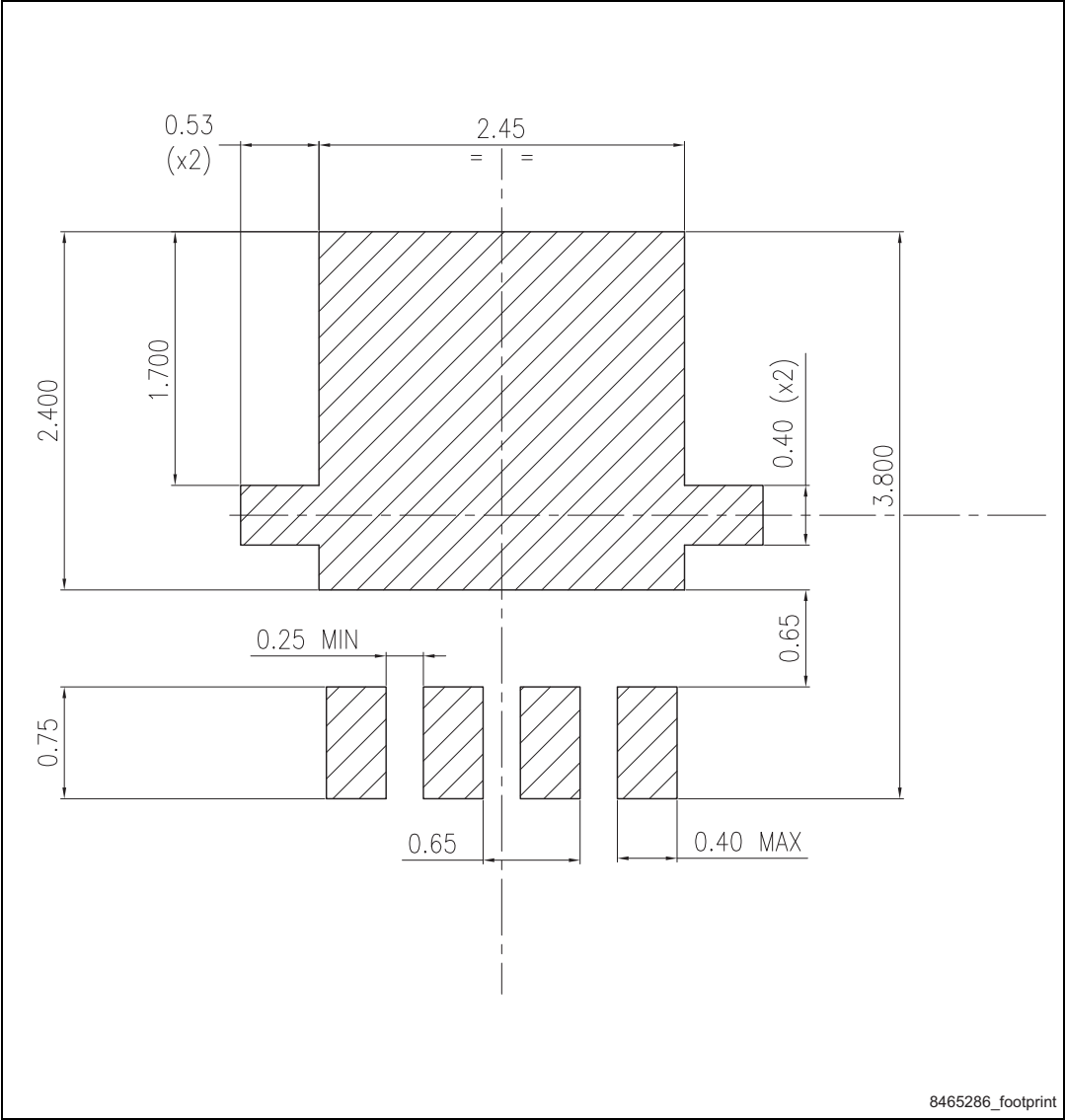


Table 8. PowerFLAT™ 3.3 x 3.3 mechanical data

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    | 0.70 | 0.80 | 0.90 |
| b    | 0.25 | 0.30 | 0.39 |
| c    | 0.14 | 0.15 | 0.20 |
| D    | 3.10 | 3.30 | 3.50 |
| D1   | 3.05 | 3.15 | 3.25 |
| D2   | 2.15 | 2.25 | 2.35 |
| e    | 0.55 | 0.65 | 0.75 |
| E    | 3.10 | 3.30 | 3.50 |
| E1   | 2.90 | 3.00 | 3.10 |
| E2   | 1.60 | 1.70 | 1.80 |
| H    | 0.25 | 0.40 | 0.55 |
| K    | 0.65 | 0.75 | 0.85 |
| L    | 0.30 | 0.45 | 0.60 |
| L1   | 0.05 | 0.15 | 0.25 |
| L2   |      |      | 0.15 |
| θ    | 8°   | 10°  | 12°  |

Figure 20. PowerFLAT™ 3.3 x 3.3 recommended footprint



## 5 Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes                                                      |
|-------------|----------|--------------------------------------------------------------|
| 24-Feb-2014 | 1        | First release.                                               |
| 29-Apr-2014 | 2        | Document status promoted from preliminary to production data |

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[STMicroelectronics:](#)

[STL7N10F7](#)