

Automotive-grade dual N-channel 30 V, 5.9 mΩ typ., 20 A STripFET™ H5 Power MOSFET in a PowerFLAT™ 5x6 double island package

Datasheet - production data

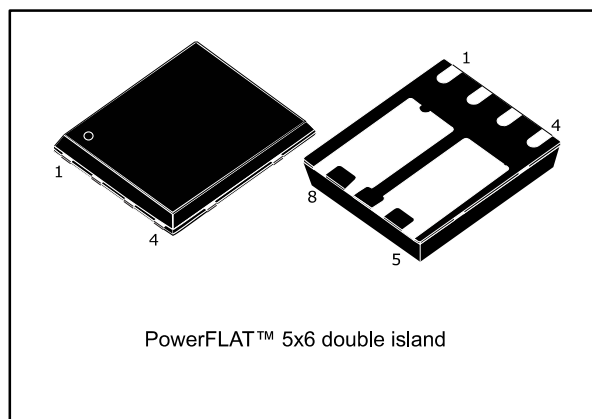
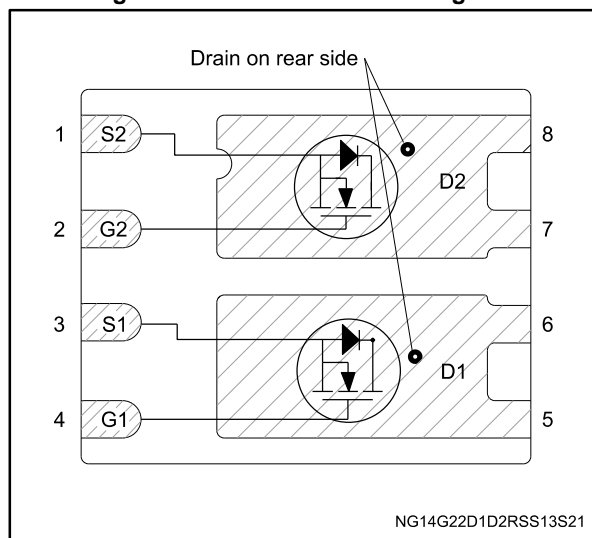


Figure 1: Internal schematic diagram



## Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STL66DN3LLH5	30 V	6.5 mΩ	20 A	4.7 W

- Designed for automotive applications and AEC-Q101 qualified
- Logic level V<sub>GS(th)</sub>
- 175 °C maximum junction temperature
- Wettable flanks package

## Applications

- Switching applications

## Description

This device is a dual N-channel Power MOSFET developed using STMicroelectronics' STripFET™ H5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Table 1: Device summary

Order code	Marking	Package	Packing
STL66DN3LLH5	66DN3LH5	PowerFLAT™ 5x6 double island	Tape and reel

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 22$	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ °C}$	78.5	A
	Drain current (continuous) at $T_{case} = 100\text{ °C}$	55.5	
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ °C}$	20	A
	Drain current (continuous) at $T_{pcb} = 100\text{ °C}$	14.2	
$I_{DM}^{(2)/(3)}$	Drain current (pulsed)	80	A
$P_{TOT}$	Total dissipation at $T_{case} = 25\text{ °C}$	72	W
$P_{TOT}^{(1)}$	Total dissipation at $T_{pcb} = 25\text{ °C}$	4.7	
$T_{stg}$	Storage temperature	-55 to 175	°C
$T_j$	Operating junction temperature		

**Notes:**

(1) This value is rated according to  $R_{thj-c}$

(2) When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board,  $t < 10\text{ s}$ .

(3) Pulse width is limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.08	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	32	

**Notes:**

(1) When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board,  $t < 10\text{ s}$ .

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AV}$	Avalanche current, not repetitive	18.5	A
$E_{AS}^{(1)}$	Single pulse avalanche energy	270	mJ

**Notes:**

(1) starting  $T_j = 25\text{ °C}$ ,  $I_D = 38\text{ A}$ ,  $V_{DD} = 24\text{ V}$ .

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

**Table 5: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 µA	30			V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 30 V			1	µA
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 30 V, T <sub>C</sub> = 125 °C			100	
I <sub>GSS</sub>	Gate-body leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±22 V			±10	µA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 µA	1		3	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		5.9	6.5	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		7.1	7.9	

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0 V	-	1500	-	pF
C <sub>oss</sub>	Output capacitance		-	230	-	
C <sub>rss</sub>	Reverse transfer capacitance		-	23	-	
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 19 A, V <sub>GS</sub> = 4.5 V (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	12	-	nC
Q <sub>gs</sub>	Gate-source charge		-	5	-	
Q <sub>gd</sub>	Gate-drain charge		-	4.4	-	

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 9.5 A R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	8.8	-	ns
t <sub>r</sub>	Rise time		-	18	-	
t <sub>d(off)</sub>	Turn-off delay time		-	26	-	
t <sub>f</sub>	Fall time		-	4	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		80	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 19\text{ A}$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 19\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 25\text{ V}$ , $T_j = 150\text{ °C}$ (see <i>Figure 15: "Test circuit for inductive load switching and diode recovery times")</i> )	-	24		ns
$Q_{rr}$	Reverse recovery charge		-	12		nC
$I_{RRM}$	Reverse recovery current		-	1.8		A

**Notes:**

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

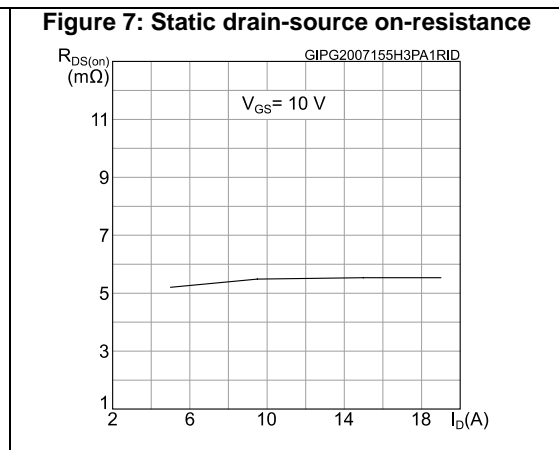
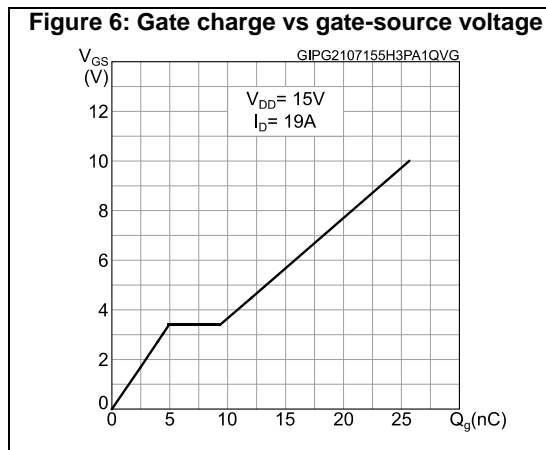
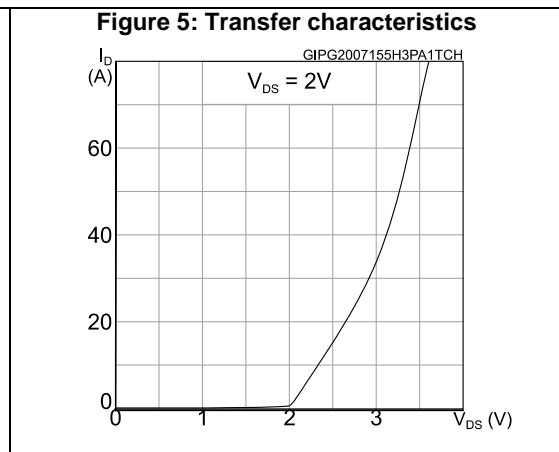
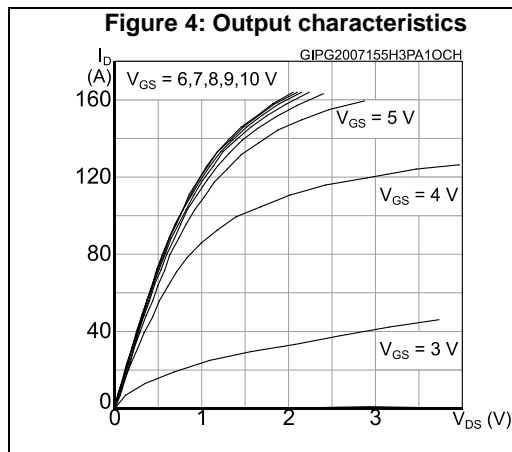
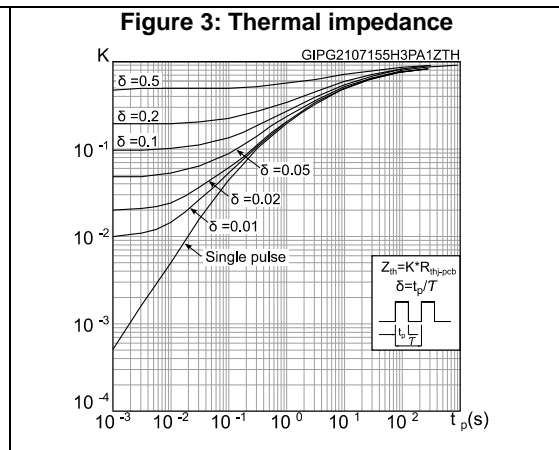
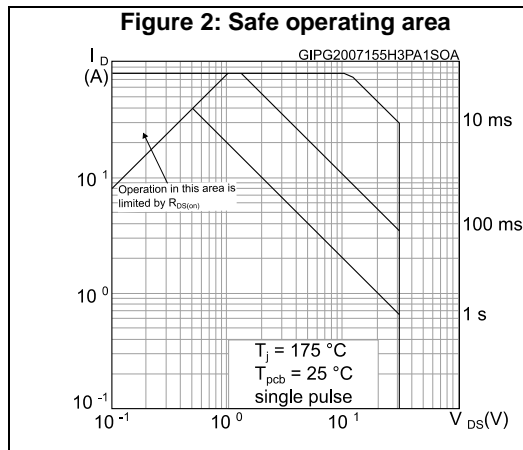


Figure 8: Capacitance variations

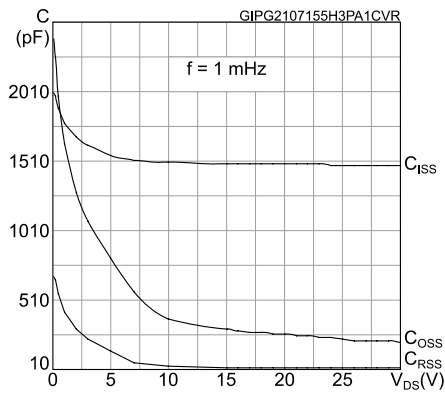


Figure 9: Normalized gate threshold voltage vs temperature

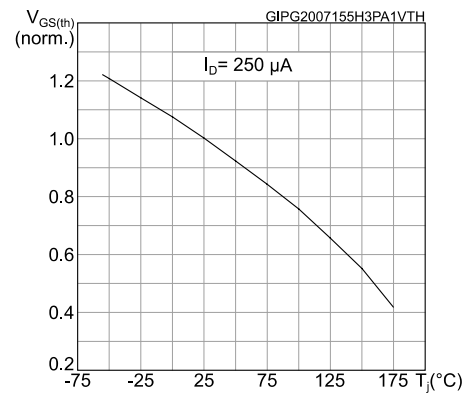


Figure 10: Normalized on-resistance vs temperature

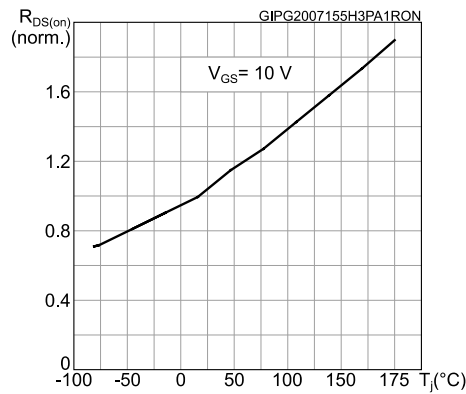


Figure 11: Normalized V(BR)DSS vs temperature

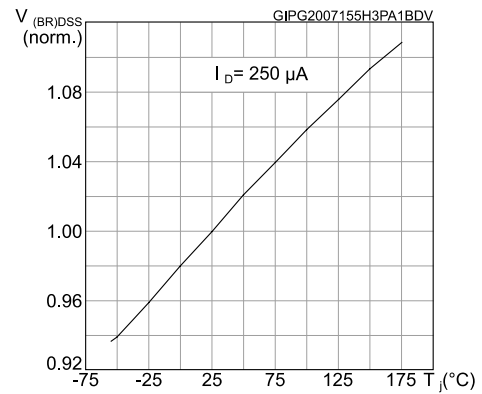
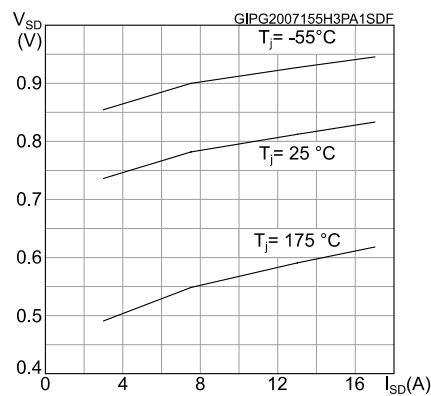
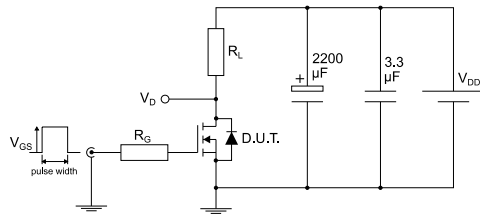


Figure 12: Source-drain diode forward characteristics



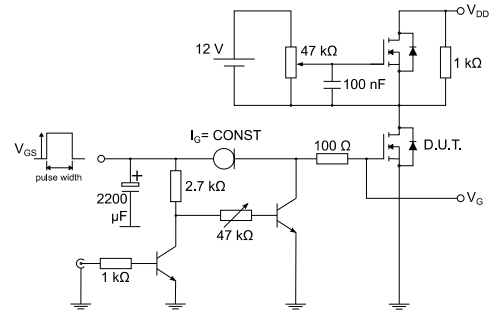
### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



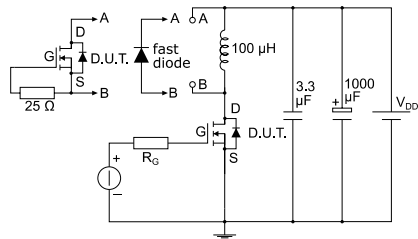
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**Figure 14: Test circuit for gate charge behavior**



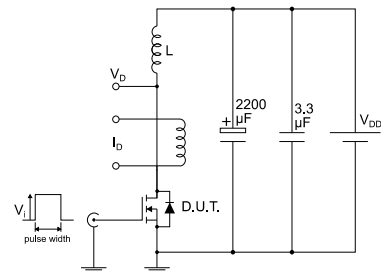
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**Figure 15: Test circuit for inductive load switching and diode recovery times**



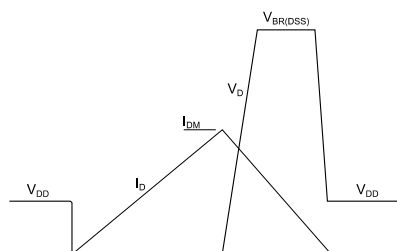
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**Figure 16: Unclamped inductive load test circuit**



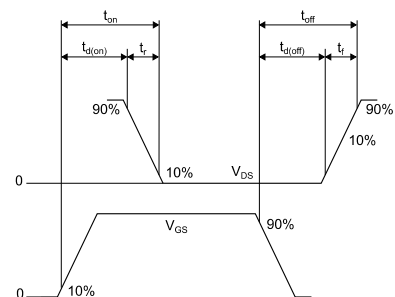
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**Figure 17: Unclamped inductive waveform**



AM01472v1

**Figure 18: Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT™ 5x6 double island WF type C package information

Figure 19: PowerFLAT™ 5x6 double island WF type C package outline

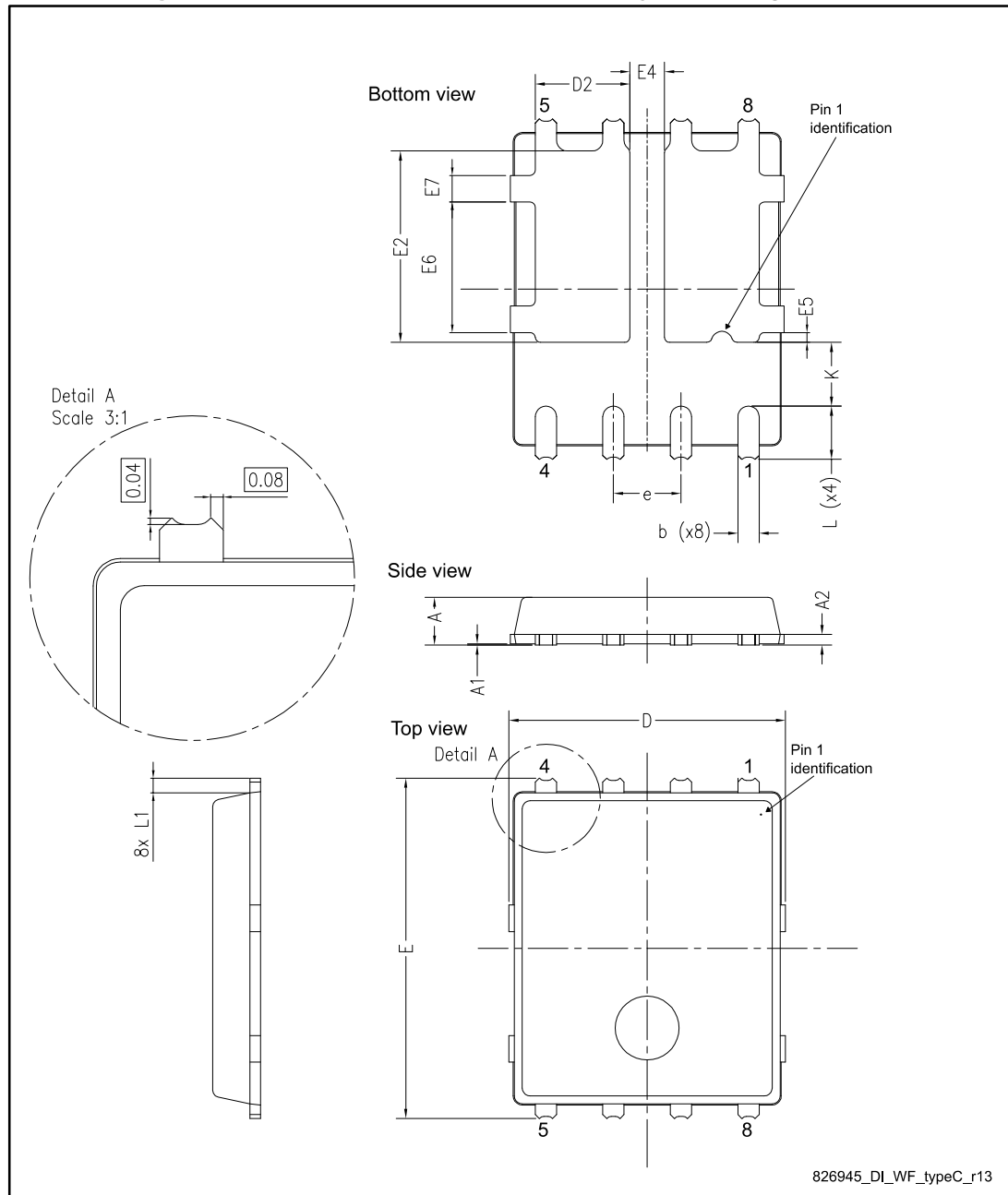
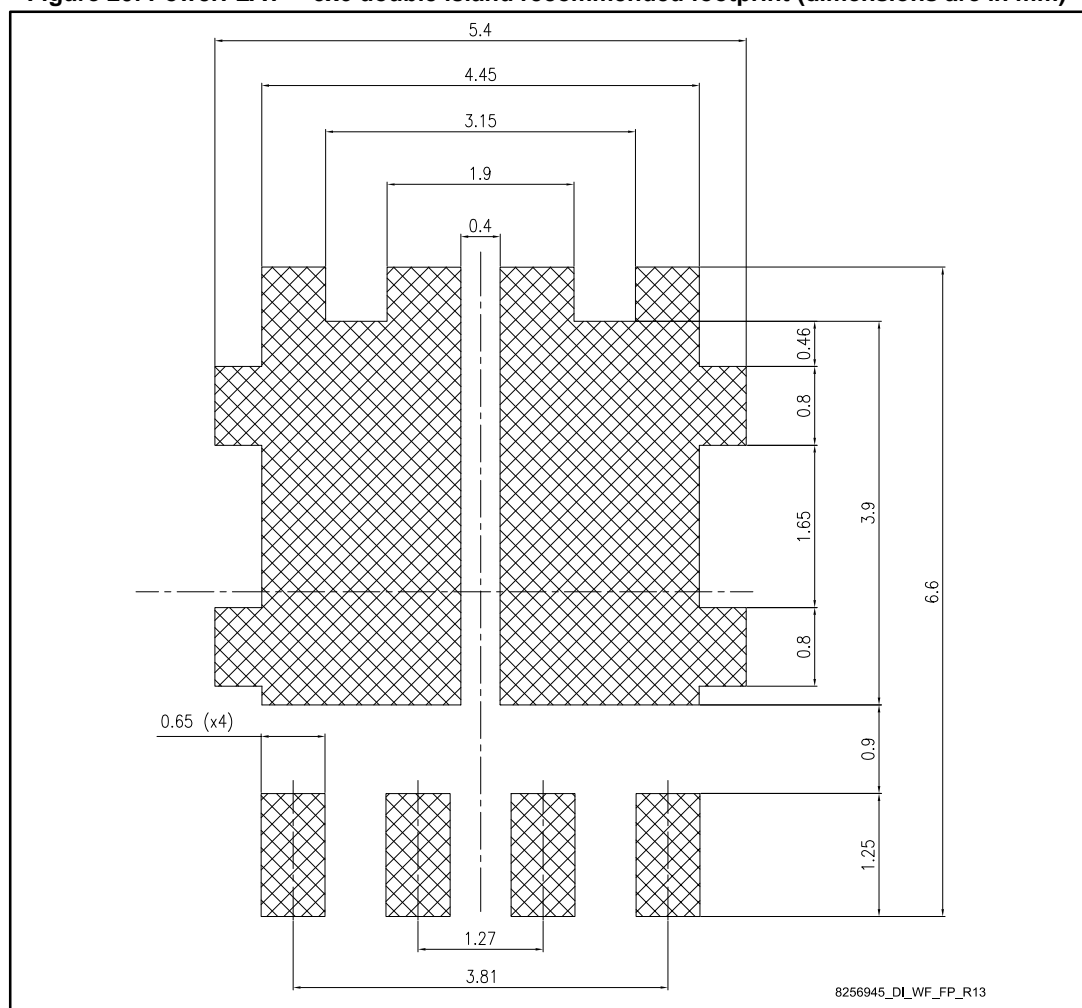


Table 9: PowerFLAT™ 5x6 double island WF type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
D2	1.68		1.88
E	6.20	6.40	6.60
E2	3.50		3.70
E4	0.55		0.75
E5	0.08		0.28
E6	2.35		2.55
E7	0.40		0.60
e		1.27	
L	0.90		1.10
L1		0.275	
K	1.05		1.35

Figure 20: PowerFLAT™ 5x6 double island recommended footprint (dimensions are in mm)



## 4.2 PowerFLAT™ 5x6 WF packing information

Figure 21: PowerFLAT™ 5x6 WF tape

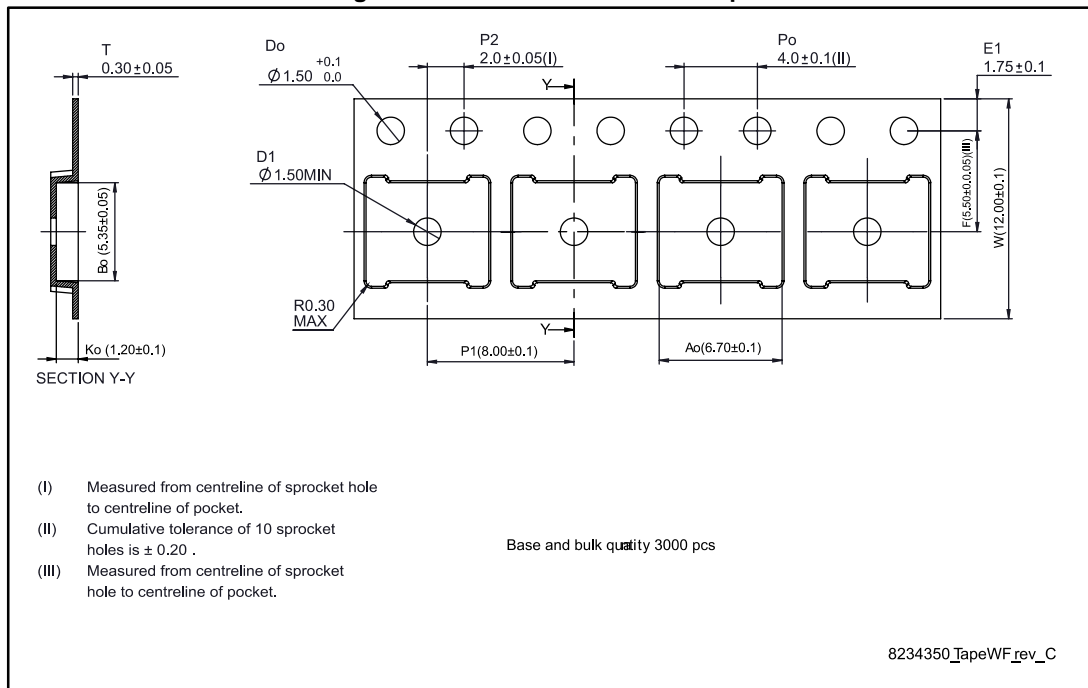


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

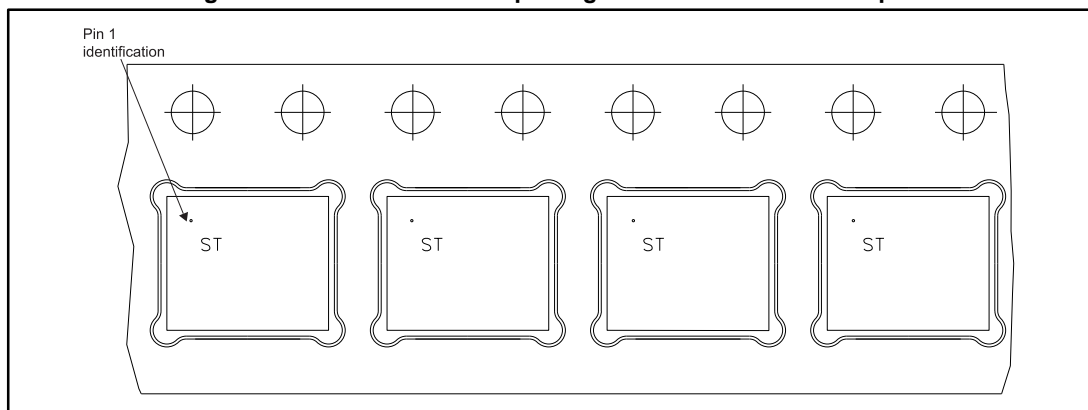
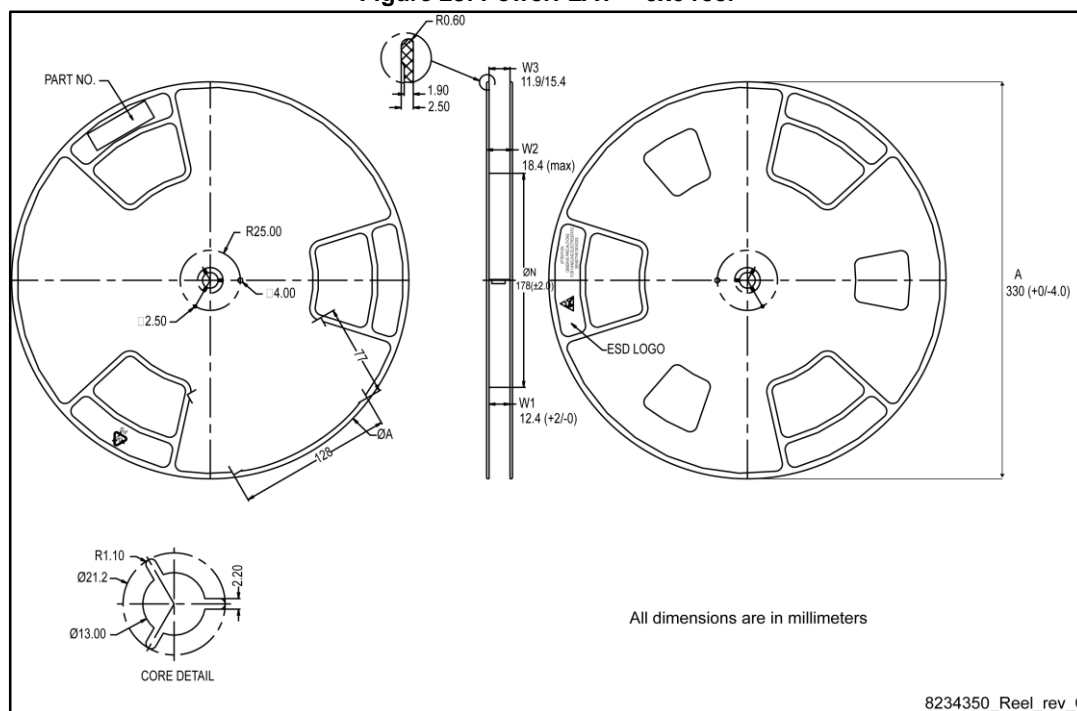


Figure 23: PowerFLAT™ 5x6 reel



## 5 Revision history

**Table 10: Document revision history**

Date	Revision	Changes
12-Oct-2011	1	First release.
14-Mar-2012	2	Document status changed from preliminary data to production data. Inserted Section 5: Packaging mechanical data. Minor text changes.
28-Aug-2015	3	Text and formatting changes throughout document Updated device marking information. Updated device package information.

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