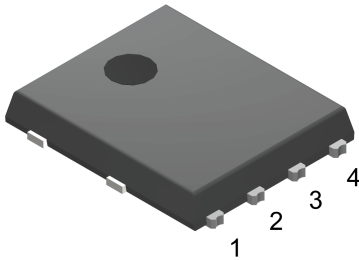
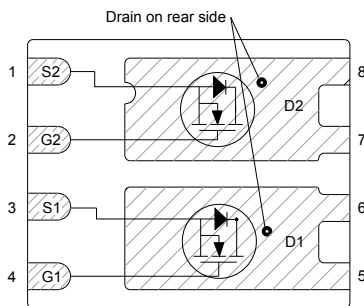


## Automotive-grade dual N-channel, 40 V, 7.0 mΩ typ., 40 A, STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 double island package



**PowerFLAT™ 5x6  
double island**



NG14G22D1D2RSS13S21

### Product status link

[STL64DN4F7AG](#)

### Product summary

|            |                              |
|------------|------------------------------|
| Order code | STL64DN4F7AG                 |
| Marking    | 64DN4F7                      |
| Package    | PowerFLAT™ 5x6 double island |
| Packing    | Tape and reel                |

## Features

| Order code   | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|--------------|-----------------|--------------------------|----------------|
| STL64DN4F7AG | 40 V            | 8.5 mΩ                   | 40 A           |

- AEC-Q101 qualified 
- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent FoM (figure of merit)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness
- Wettable flank package

## Applications

- Switching applications

## Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

## 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter                                                       | Value      | Unit             |
|----------------|-----------------------------------------------------------------|------------|------------------|
| $V_{DS}$       | Drain-source voltage                                            | 40         | V                |
| $V_{GS}$       | Gate-source voltage                                             | $\pm 20$   | V                |
| $I_D^{(1)}$    | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$  | 40         | A                |
|                | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 40         | A                |
| $I_{DM}^{(2)}$ | Drain current (pulsed at 10 $\mu\text{s}$ )                     | 240        | A                |
| $P_{TOT}$      | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$           | 57         | W                |
| $T_j$          | Operating junction temperature range                            | -55 to 175 | $^\circ\text{C}$ |
| $T_{stg}$      | Storage temperature range                                       |            |                  |

1. Drain current is limited by package, the current capability of the silicon is 64 A at 25  $^\circ\text{C}$ .

2. Pulse width limited by safe operating area

**Table 2. Thermal data**

| Symbol              | Parameter                        | Value | Unit               |
|---------------------|----------------------------------|-------|--------------------|
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb  | 32    | $^\circ\text{C/W}$ |
| $R_{thj-case}$      | Thermal resistance junction-case | 2.6   | $^\circ\text{C/W}$ |

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ s}$ .

## 2 Electrical characteristics

( $T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified).

**Table 3. On-/off-states**

| Symbol        | Parameter                         | Test conditions                                    | Min. | Typ. | Max. | Unit          |
|---------------|-----------------------------------|----------------------------------------------------|------|------|------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$        | 40   |      |      | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 40\text{ V}$     |      |      | 1    | $\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage current         | $V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$     |      |      | 100  | nA            |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$ | 2    |      | 4    | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$       |      | 7.0  | 8.5  | m $\Omega$    |

**Table 4. Dynamic**

| Symbol    | Parameter                    | Test conditions                                                     | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|---------------------------------------------------------------------|------|------|------|------|
| $C_{iss}$ | Input capacitance            | $V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$ | -    | 637  | -    | pF   |
| $C_{oss}$ | Output capacitance           |                                                                     | -    | 240  | -    | pF   |
| $C_{rss}$ | Reverse transfer capacitance |                                                                     | -    | 26   | -    | pF   |
| $Q_g$     | Total gate charge            | $V_{DD} = 20\text{ V}$ , $I_D = 40\text{ A}$ ,                      | -    | 9.8  | -    | nC   |
| $Q_{gs}$  | Gate-source charge           | $V_{GS} = 0\text{ to }10\text{ V}$                                  | -    | 3.8  | -    | nC   |
| $Q_{gd}$  | Gate-drain charge            | (see Figure 13. Test circuit for gate charge behavior)              | -    | 3.1  | -    | nC   |

**Table 5. Switching times**

| Symbol       | Parameter           | Test conditions                                                                                                                                                                                                 | Min. | Typ.  | Max. | Unit |
|--------------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 20\text{ V}$ , $I_D = 20\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br>(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform) | -    | 18.8  | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                                                                                                 | -    | 102.6 | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |                                                                                                                                                                                                                 | -    | 21.4  | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                                                                                                                 | -    | 13.3  | -    | ns   |

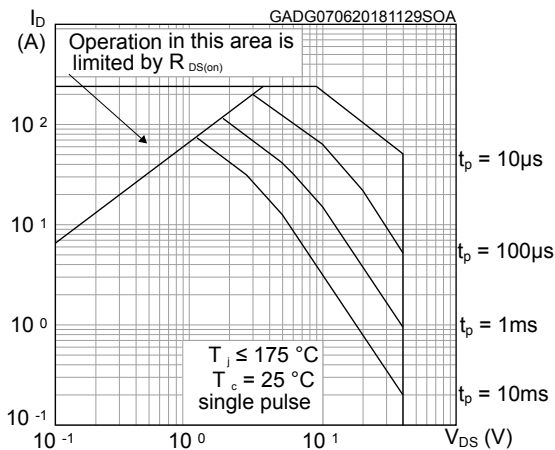
**Table 6. Source-drain diode**

| Symbol         | Parameter                | Test conditions                                                                     | Min. | Typ. | Max. | Unit |
|----------------|--------------------------|-------------------------------------------------------------------------------------|------|------|------|------|
| $V_{SD}^{(1)}$ | Forward on voltage       | $I_{SD} = 40\text{ A}$ , $V_{GS} = 0\text{ V}$                                      | -    |      | 1.3  | V    |
| $t_{rr}$       | Reverse recovery time    | $I_D = 40\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$                            | -    | 27.5 |      | ns   |
| $Q_{rr}$       | Reverse recovery charge  | $V_{DD} = 32\text{ V}$                                                              | -    | 17.3 |      | nC   |
| $I_{RRM}$      | Reverse recovery current | (see Figure 14. Test circuit for inductive load switching and diode recovery times) | -    | 1.4  |      | A    |

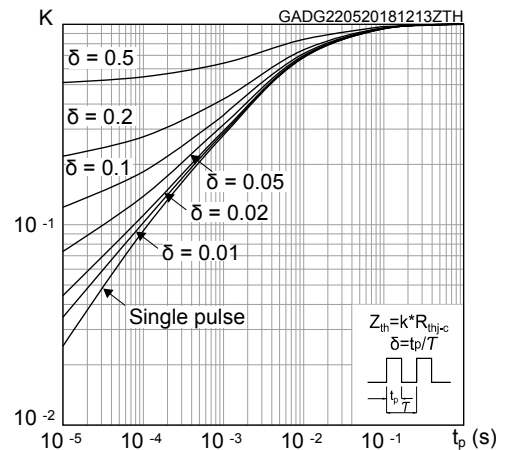
1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

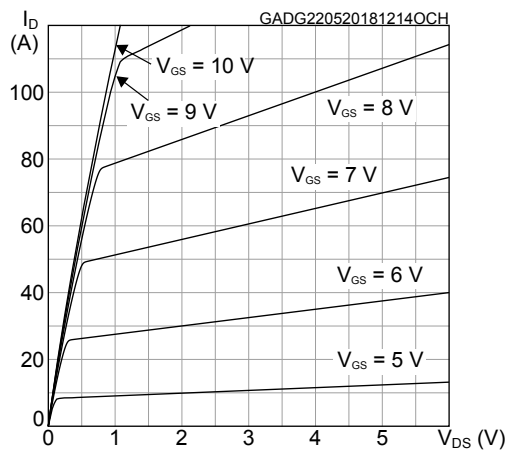
**Figure 1. Safe operating area**



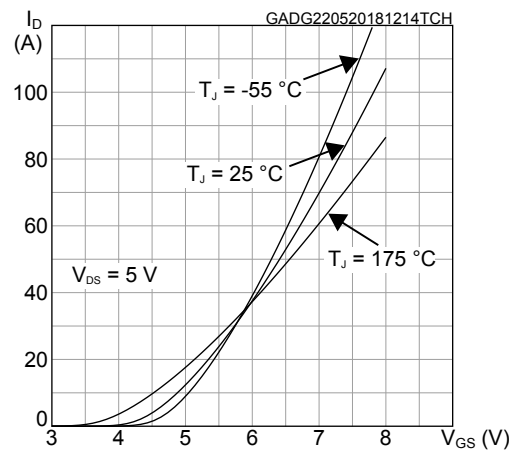
**Figure 2. Thermal impedance**



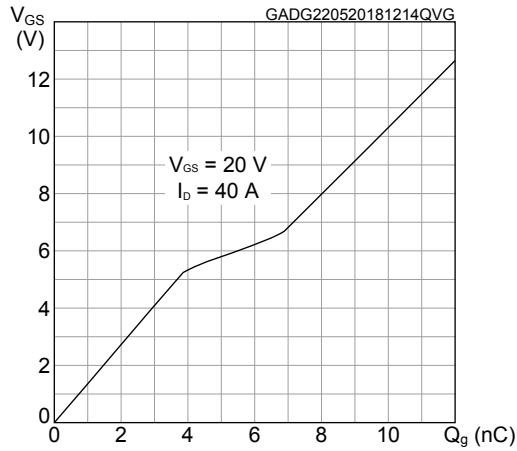
**Figure 3. Output characteristics**



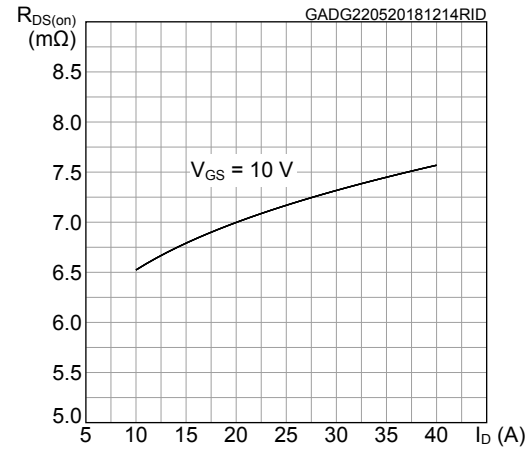
**Figure 4. Transfer characteristics**



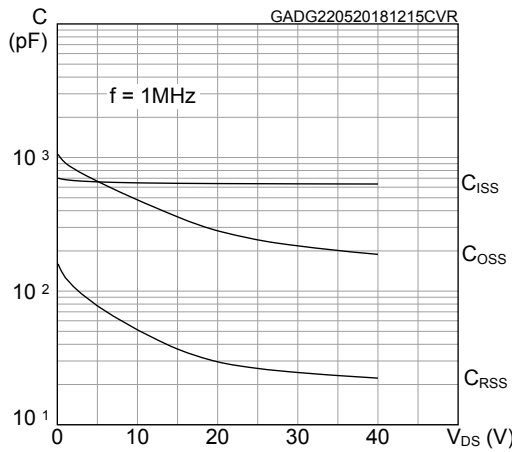
**Figure 5. Gate charge vs gate-source voltage**



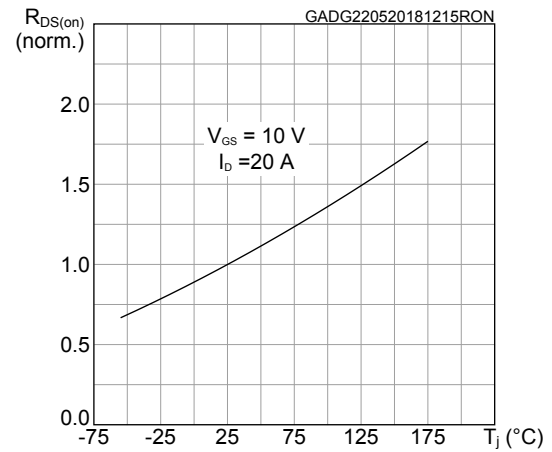
**Figure 6. Static drain-source on-resistance**



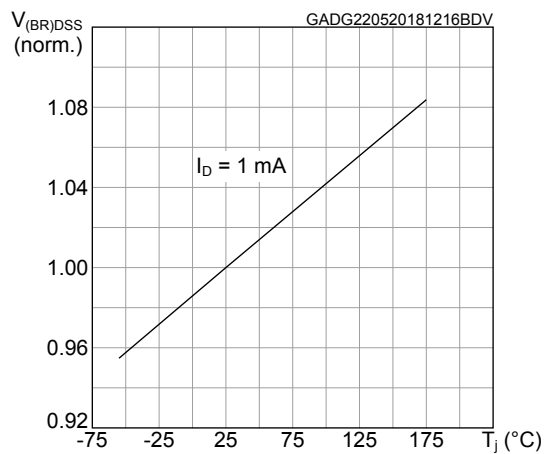
**Figure 7. Capacitance variations**



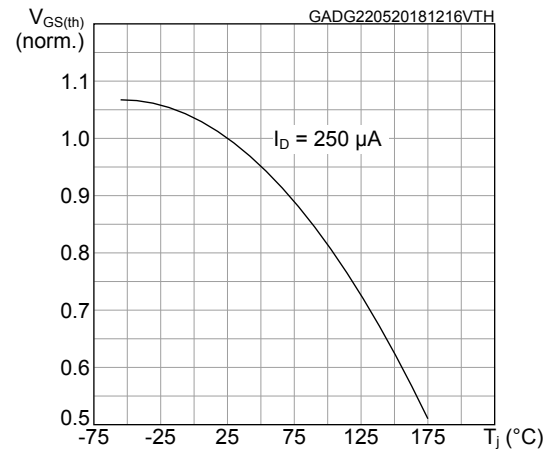
**Figure 8. Normalized on-resistance vs temperature**



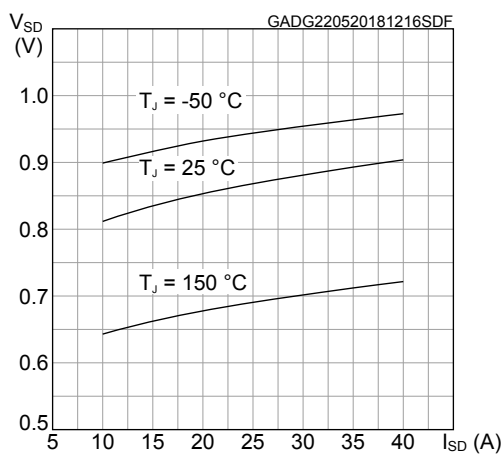
**Figure 9. Normalized  $V_{(BR)DSS}$  vs temperature**



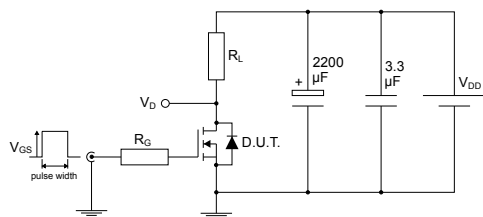
**Figure 10. Normalized gate-threshold voltage vs temperature**



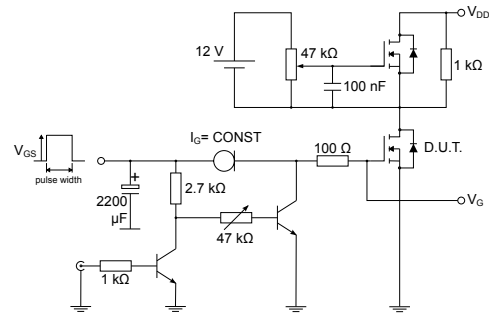
**Figure 11. Source-drain diode forward characteristics**



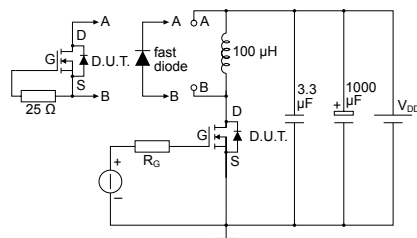
### 3 Test circuits

**Figure 12. Test circuit for resistive load switching times**


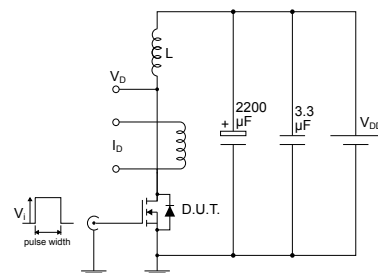
AM01468v1

**Figure 13. Test circuit for gate charge behavior**


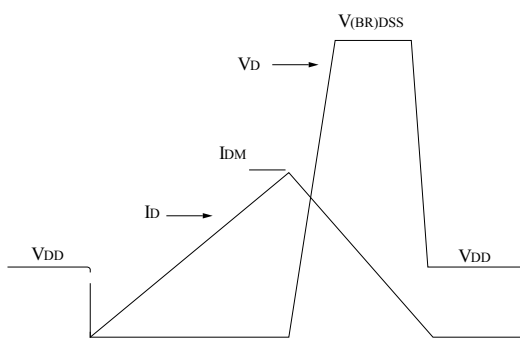
AM01469v1

**Figure 14. Test circuit for inductive load switching and diode recovery times**


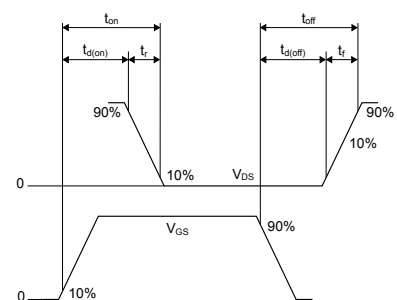
AM01470v1

**Figure 15. Unclamped inductive load test circuit**


AM01471v1

**Figure 16. Unclamped inductive waveform**


AM01472v1

**Figure 17. Switching time waveform**


AM01473v1

## **4 Package information**

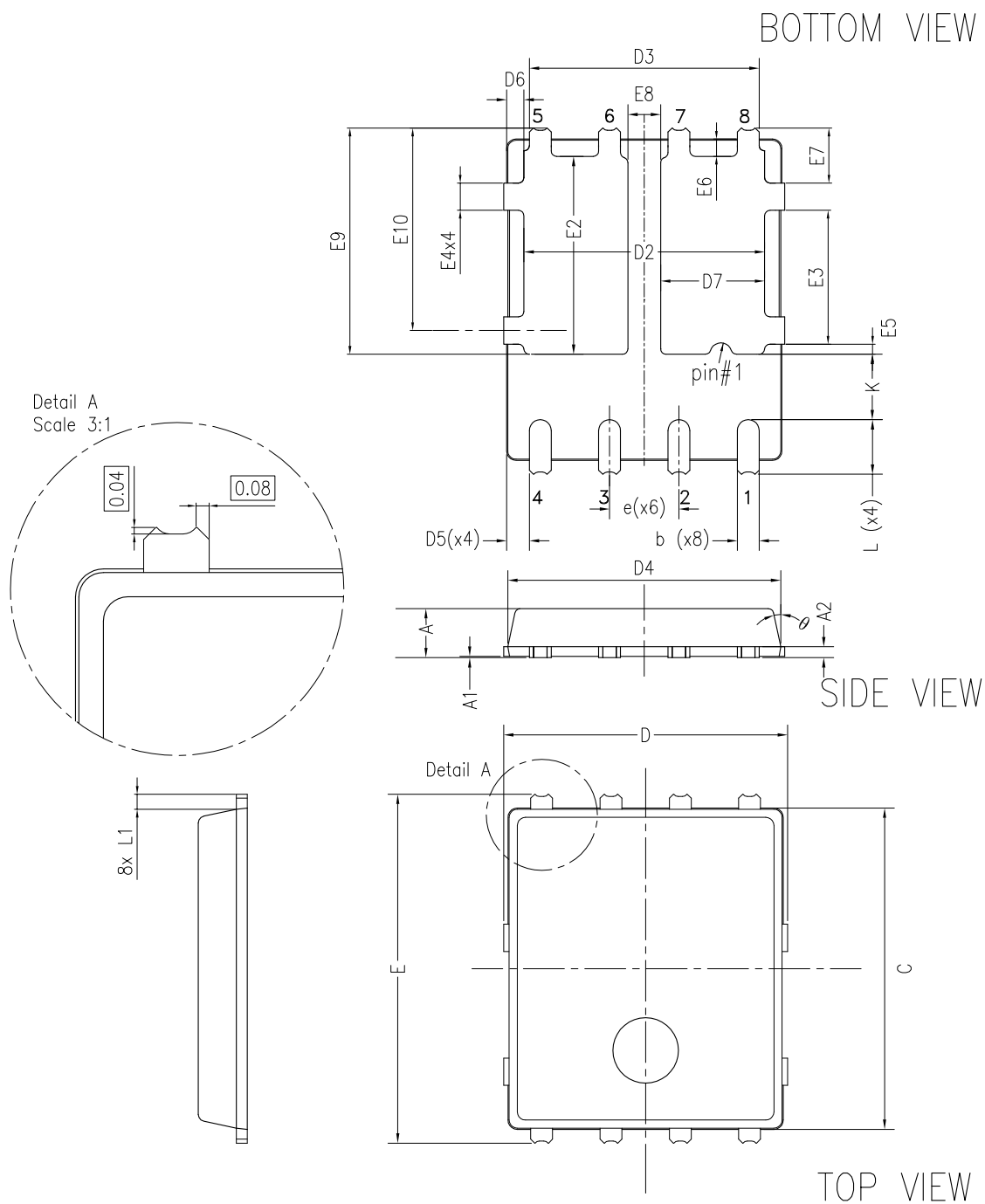
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## 4.1 PowerFLAT™ 5x6 double island WF type C package information

**Figure 18. PowerFLAT™ 5x6 double island WF type C package outline**

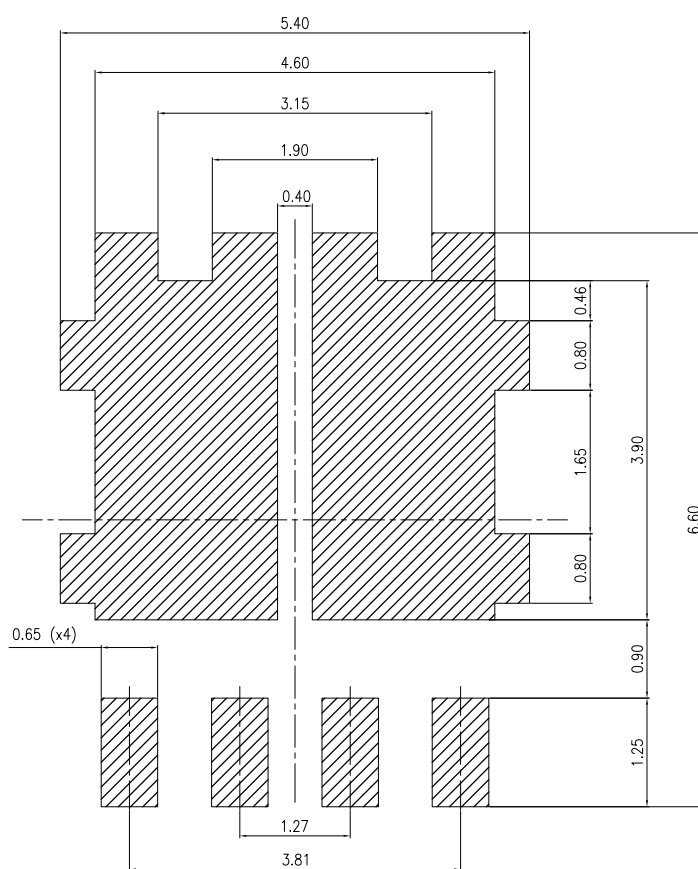


8256945\_DI\_WF\_typeC\_r18

**Table 7. PowerFLAT™ 5x6 double island WF type C mechanical data**

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 0.80  |       | 1.00  |
| A1   | 0.02  |       | 0.05  |
| A2   |       | 0.25  |       |
| b    | 0.30  |       | 0.50  |
| C    | 5.80  | 6.00  | 6.10  |
| D    | 5.00  | 5.20  | 5.40  |
| D2   | 4.15  |       | 4.45  |
| D3   | 4.05  | 4.20  | 4.35  |
| D4   | 4.80  | 5.00  | 5.10  |
| D5   | 0.25  | 0.40  | 0.55  |
| D6   | 0.15  | 0.30  | 0.45  |
| D7   | 1.68  |       | 1.98  |
| e    |       | 1.27  |       |
| E    | 6.20  | 6.40  | 6.60  |
| E2   | 3.50  |       | 3.70  |
| E3   | 2.35  |       | 2.55  |
| E4   | 0.40  |       | 0.60  |
| E5   | 0.08  |       | 0.28  |
| E6   | 0.20  | 0.325 | 0.45  |
| E7   | 0.85  | 1.00  | 1.15  |
| E8   | 0.55  |       | 0.75  |
| E9   | 4.00  | 4.20  | 4.40  |
| E10  | 3.55  | 3.70  | 3.85  |
| K    | 1.05  |       | 1.35  |
| L    | 0.90  | 1.00  | 1.10  |
| L1   | 0.175 | 0.275 | 0.375 |
| Θ    | 0°    |       | 12°   |

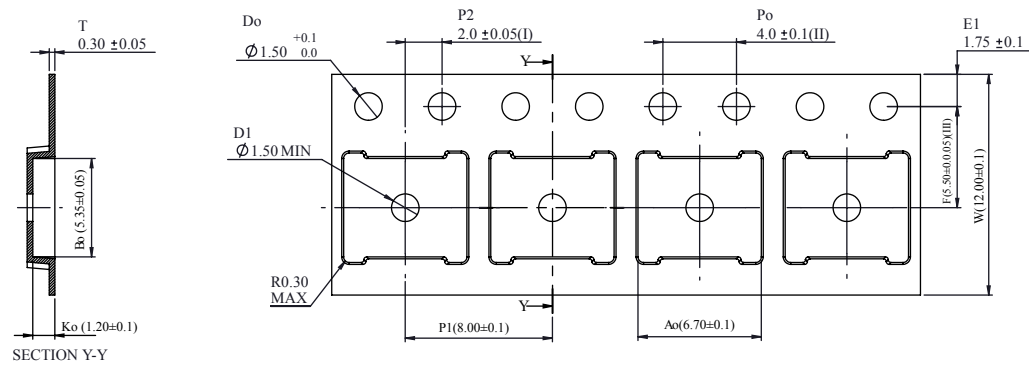
**Figure 19. PowerFLAT™ 5x6 double island recommended footprint (dimensions are in mm)**



8256945\_FP\_std\_R18

## 4.2 PowerFLAT™ 5x6 WF packing information

**Figure 20. PowerFLAT™ 5x6 WF tape (dimensions are in mm)**

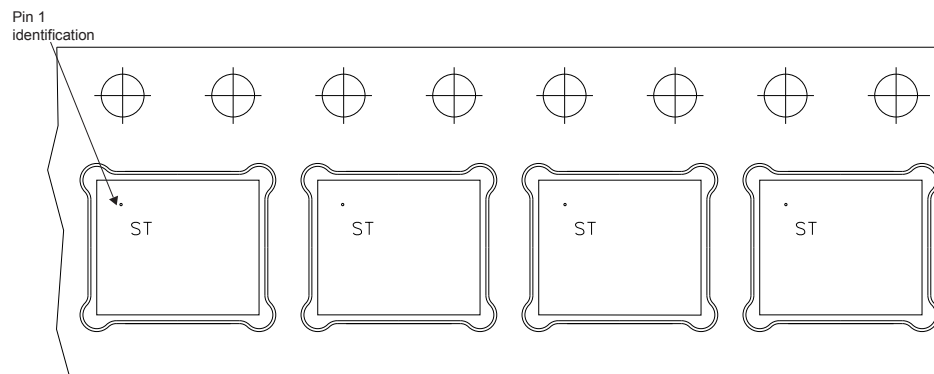


- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .
- (III) Measured from centreline of sprocket hole to centreline of pocket.

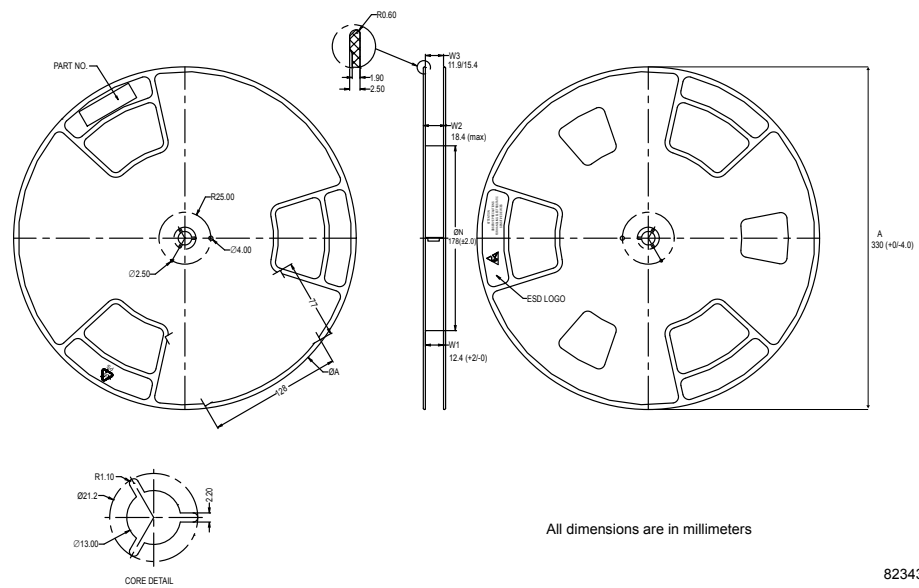
Base and bulk quantity 3000 pcs

8234350\_TapeWF\_rev\_C

**Figure 21. PowerFLAT™ 5x6 package orientation in carrier tape**



**Figure 22. PowerFLAT™ 5x6 reel (dimensions are in mm)**



## Revision history

**Table 8. Document revision history**

| Date        | Version | Changes                                                                                             |
|-------------|---------|-----------------------------------------------------------------------------------------------------|
| 28-May-2018 | 1       | Initial release                                                                                     |
| 07-Jun-2018 | 2       | Updated title and features in cover page.<br>Updated <a href="#">Figure 1. Safe operating area.</a> |
| 08-Jun-2018 | 3       | Updated <a href="#">Section 4.1 PowerFLAT™ 5x6 double island WF type C package information.</a>     |

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