

## Automotive-grade N-channel 40 V, 2.9 mΩ typ., 55 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

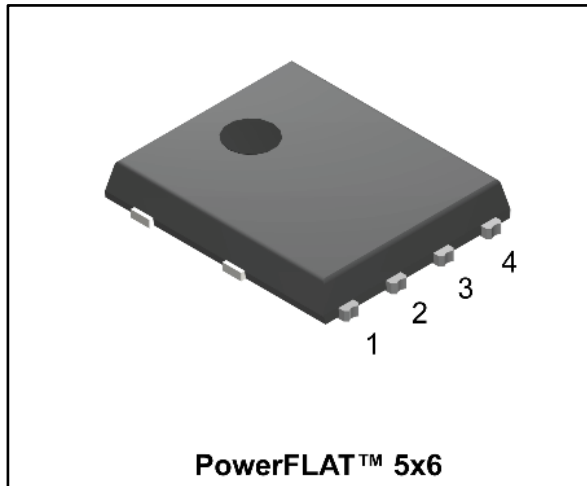
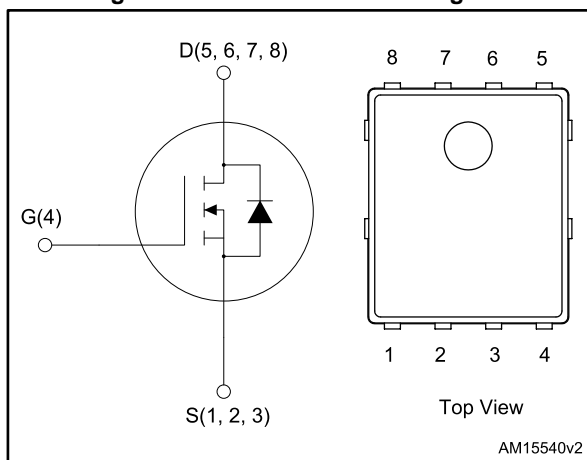


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL120N4F6AG	40 V	3.6 mΩ	55 A



- AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL120N4F6AG	120N4F6	PowerFLAT™ 5x6	Tape and reel

---

## Contents

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
	2.1 Electrical characteristics (curves).....	6
<b>3</b>	<b>Test circuits .....</b>	<b>8</b>
<b>4</b>	<b>Package information .....</b>	<b>9</b>
	4.1 PowerFLAT™ 5x6 WF type R package information .....	9
	4.2 PowerFLAT™ 5x6 WF packing information .....	12
<b>5</b>	<b>Revision history .....</b>	<b>14</b>

# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$V_{DS}$	Drain-source voltage	40	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	55	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	55	A
$I_{DM}^{(2)}$	Drain current (pulsed)	220	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	115	W
$T_{stg}$	Storage temperature range	-55 to 175	$^{\circ}\text{C}$
$T_j$	Operating junction temperature range		$^{\circ}\text{C}$

**Notes:**

<sup>(1)</sup>Drain current is limited by package, the current capability of the silicon is 120 A at 25  $^{\circ}\text{C}$ .

<sup>(2)</sup>Pulse width is limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.3	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

**Notes:**

<sup>(1)</sup>When mounted on 1 inch<sup>2</sup> 2 Oz. Cu board,  $t \leq 10\text{ s}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AV}$	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	20	A
$E_{AS}$	Single pulse avalanche energy ( $T_j = 25\text{ }^{\circ}\text{C}$ , $I_C = I_{AV}$ , $V_{DD} = 25\text{ V}$ )	200	mJ

## 2 Electrical characteristics

(T<sub>C</sub> = 25 °C unless otherwise specified)

**Table 5: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40			V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 40 V			1	μA
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C <sup>(1)</sup>			10	μA
I <sub>GSS</sub>	Gate-body leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2		4	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 13 A		2.9	3.6	mΩ

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0 V	-	3700	-	pF
C <sub>oss</sub>	Output capacitance		-	625	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	295	-	pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 26 A, V <sub>GS</sub> = 0 to 10 V (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	63	-	nC
Q <sub>gs</sub>	Gate-source charge		-	19	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	15	-	nC
R <sub>G</sub>	Intrinsic gate resistance	f = 1 MHz, I <sub>D</sub> = 0 A	-	1.5	-	Ω

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 13 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	20	-	ns
t <sub>r</sub>	Rise time		-	70	-	ns
t <sub>d(off)</sub>	Turn-off-delay time		-	40	-	ns
t <sub>f</sub>	Fall time		-	20	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		55	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		220	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 13\text{ A}$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 26\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 25\text{ V}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	40		ns
$Q_{rr}$	Reverse recovery charge		-	5.6		nC
$I_{RRM}$	Reverse recovery current		-	2.8		A

**Notes:**

<sup>(1)</sup>Pulse width is limited by safe operating area.

<sup>(2)</sup>Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

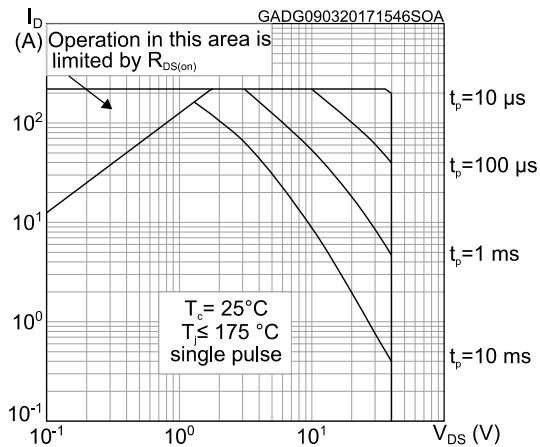


Figure 3: Thermal impedance

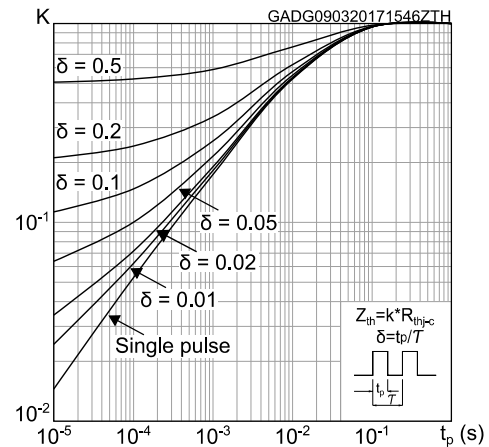


Figure 4: Output characteristics

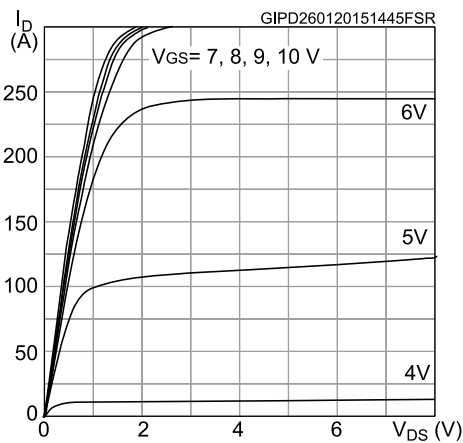


Figure 5: Transfer characteristics

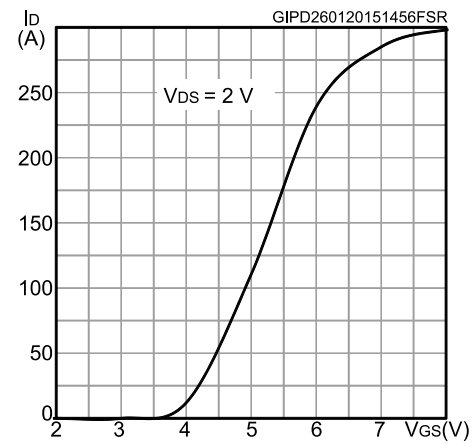


Figure 6: Gate charge vs gate-source voltage

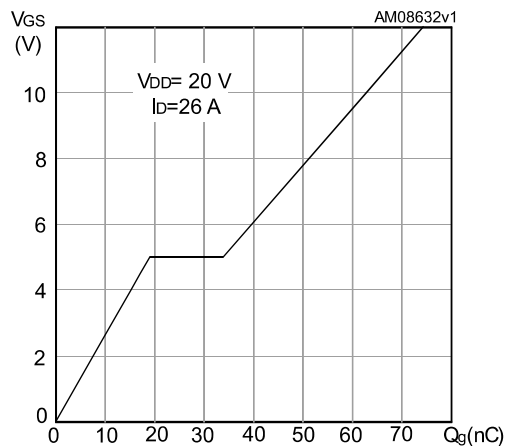


Figure 7: Static drain-source on-resistance

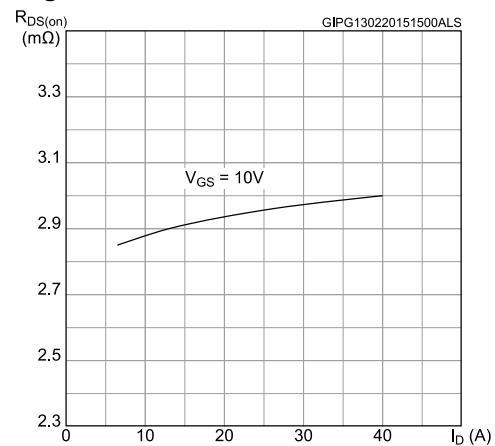


Figure 8: Capacitance variations

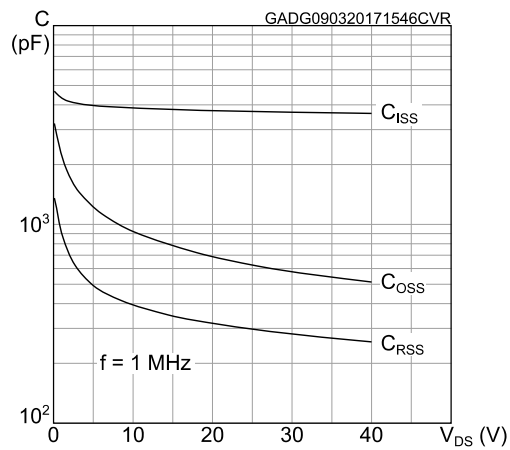
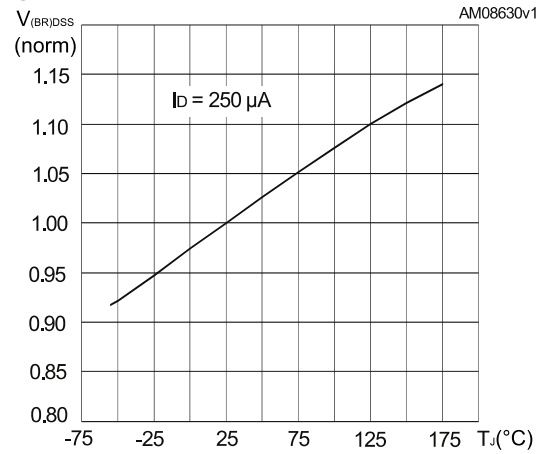
Figure 9: Normalized  $V_{(BR)DSS}$  vs temperature

Figure 10: Normalized gate threshold voltage vs temperature

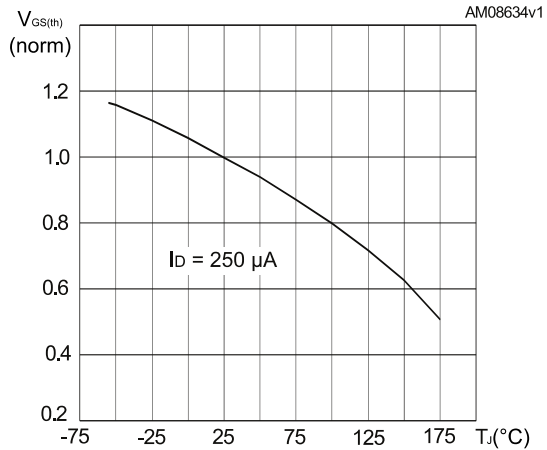


Figure 11: Normalized on-resistance vs. temperature

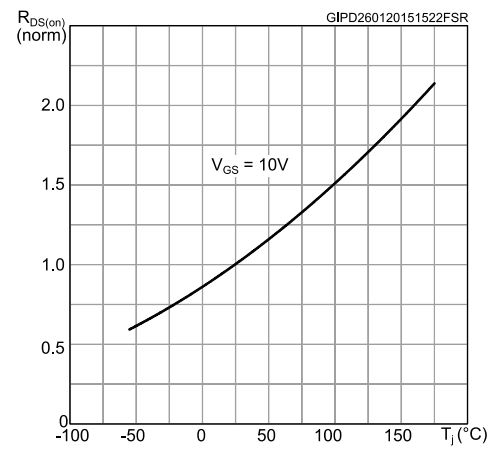
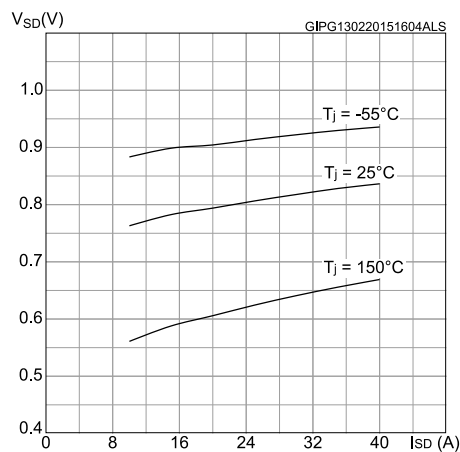
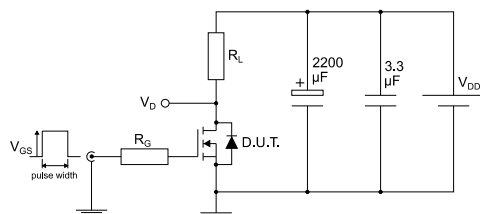


Figure 12: Source-drain diode forward characteristics



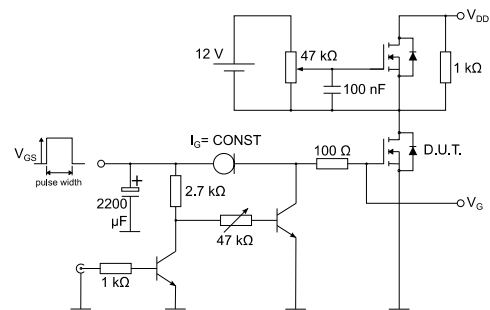
### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



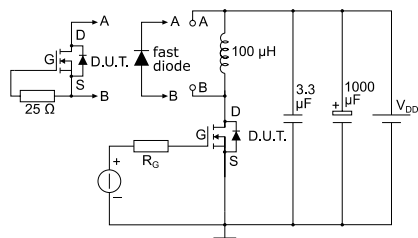
AM01468v1

**Figure 14: Test circuit for gate charge behavior**



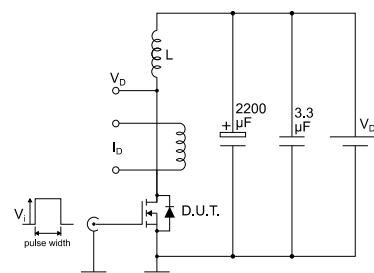
AM01469v1

**Figure 15: Test circuit for inductive load switching and diode recovery times**



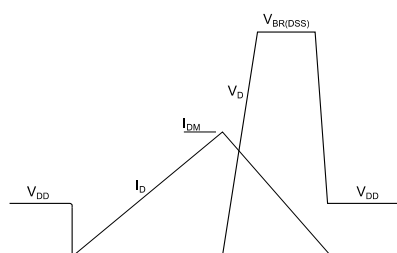
AM01470v1

**Figure 16: Unclamped inductive load test circuit**



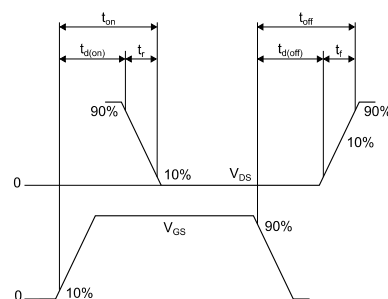
AM01471v1

**Figure 17: Unclamped inductive waveform**



AM01472v1

**Figure 18: Switching time waveform**



AM01473v1

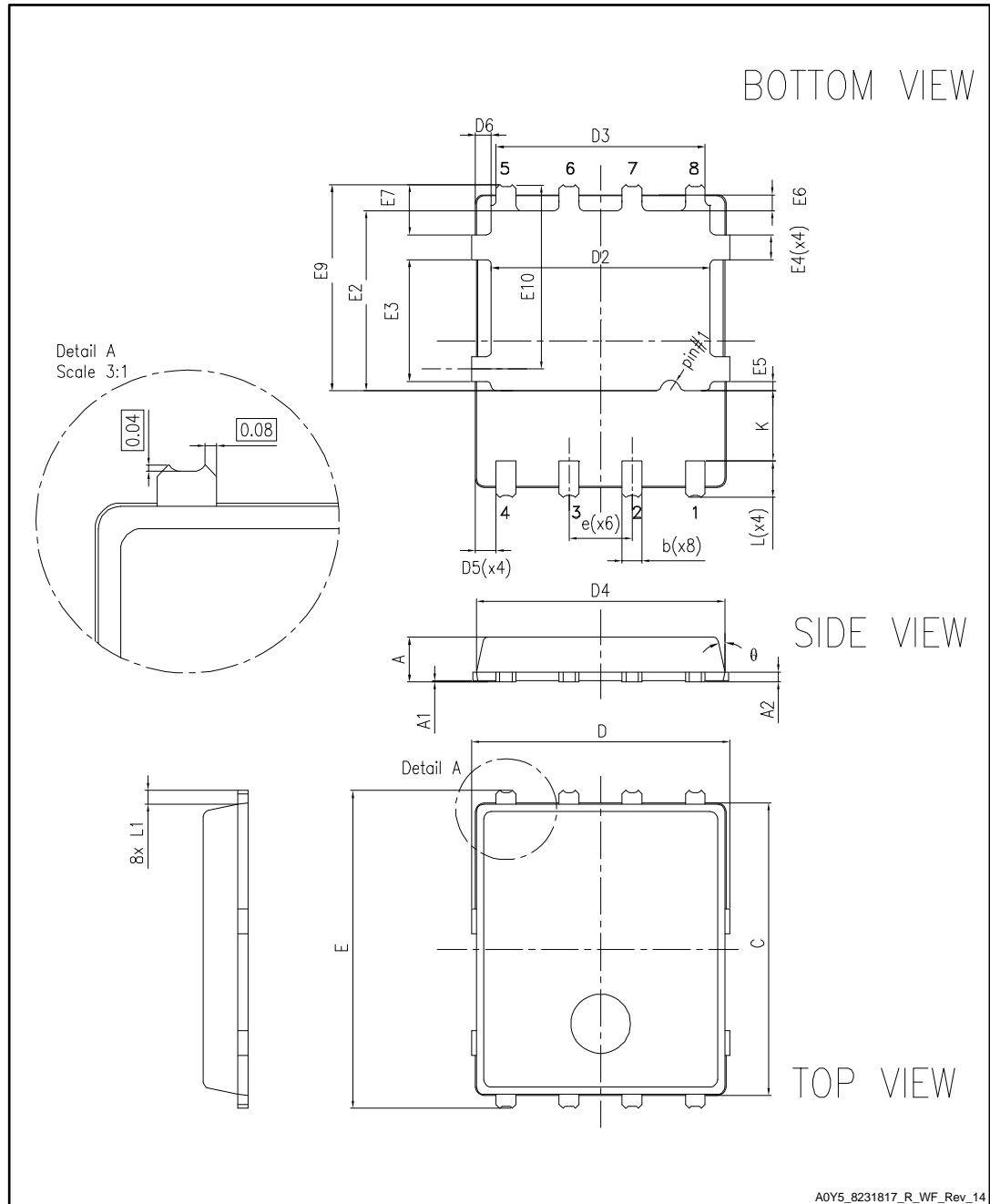


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT™ 5x6 WF type R package information

Figure 19: PowerFLAT™ 5x6 WF type R package outline

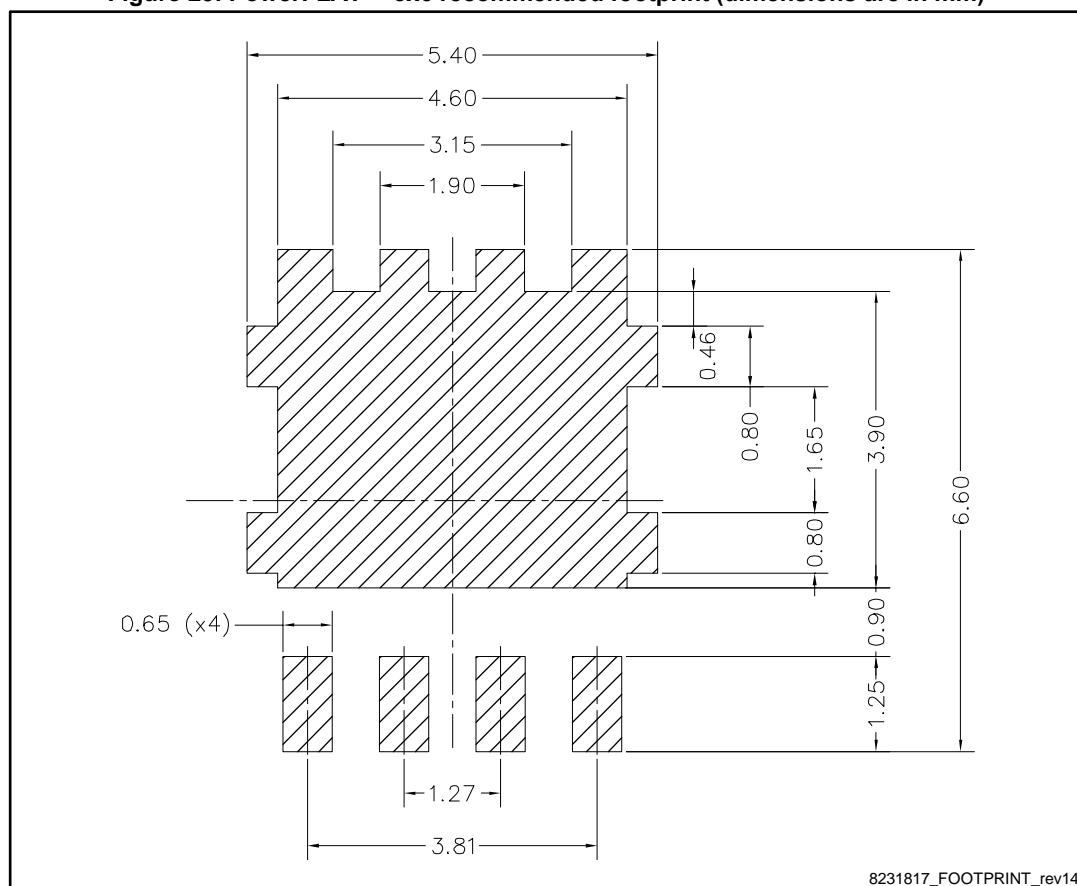


A0V5\_8231817\_R\_WF\_Rev\_14

Table 9: PowerFLAT™ 5x6 WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
Θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



## 4.2 PowerFLAT™ 5x6 WF packing information

Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

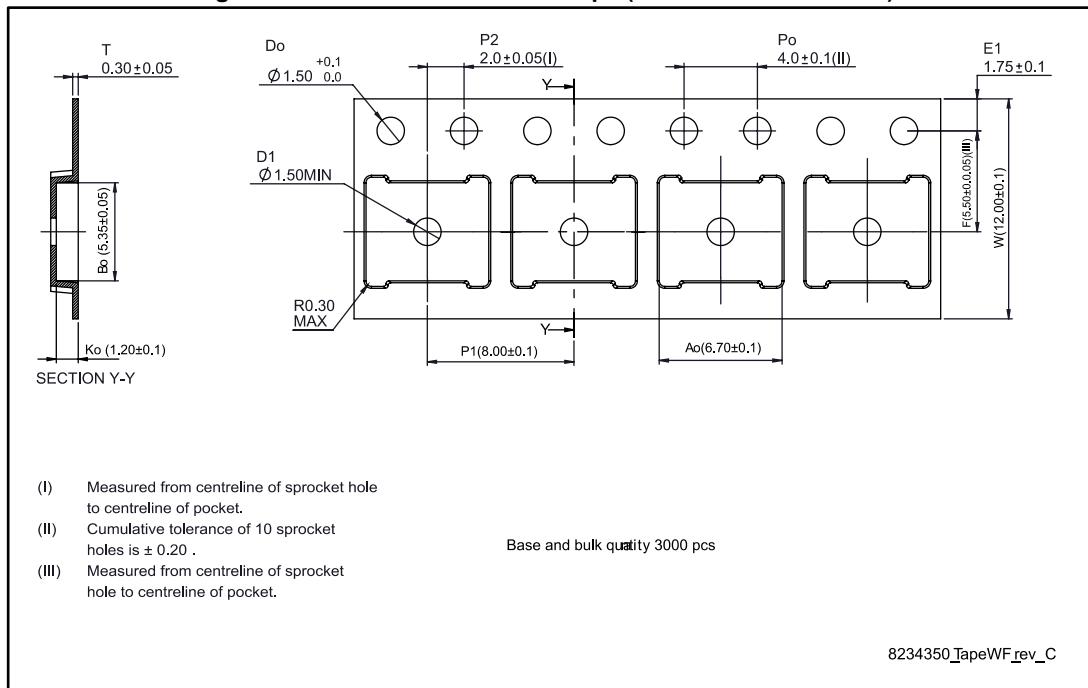
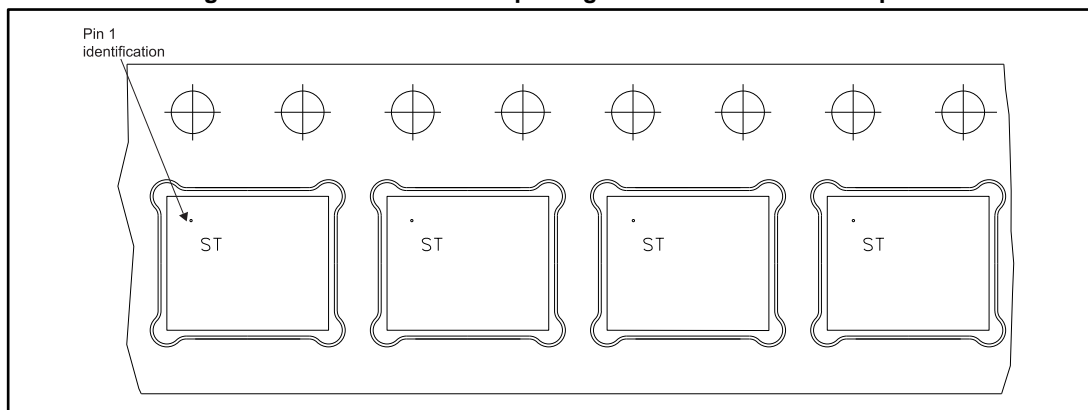
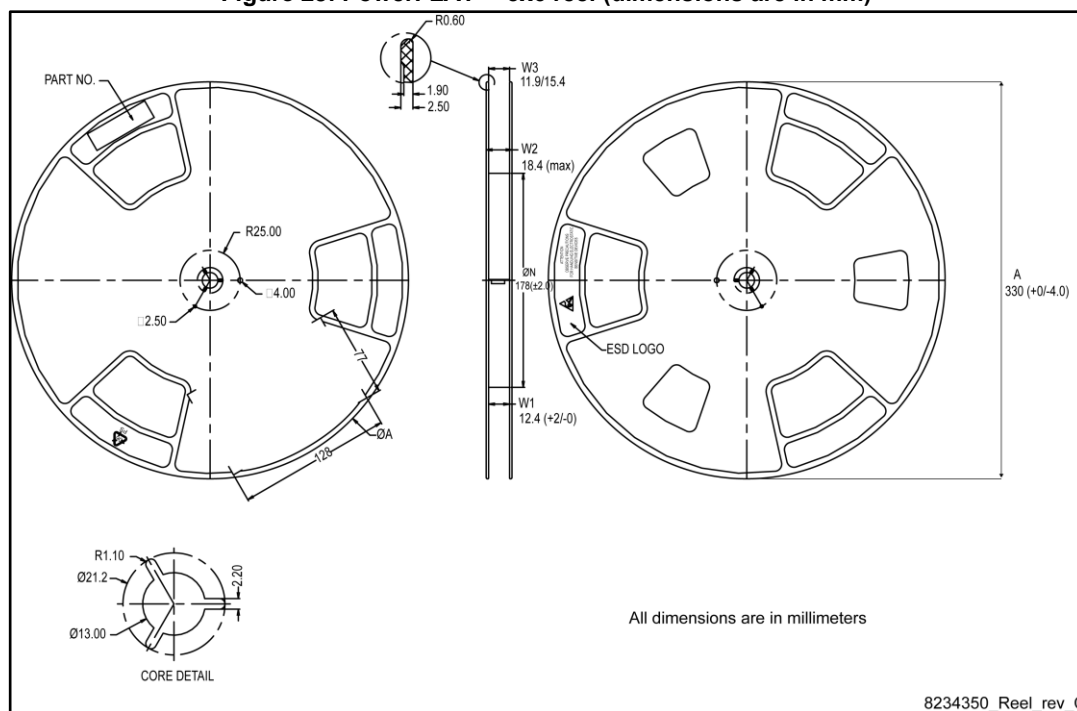


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape



**Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)**



## 5 Revision history

**Table 10: Document revision history**

Date	Revision	Changes
19-Feb-2015	1	First release.
11-Apr-2016	2	Updated <i>Table 2: "Absolute maximum ratings"</i> Minor text changes.
10-Jan-2017	3	Updated <i>Table 2: "Absolute maximum ratings"</i> and <i>Table 8: "Source drain diode"</i> . Updated <i>Figure 6: "Gate charge vs gate-source voltage"</i> and <i>Figure 8: "Capacitance variations"</i> . Minor text changes
09-Mar-2017	4	Updated <i>Table 2: "Absolute maximum ratings"</i> and <i>Table 3: "Thermal data"</i> . Updated <i>Figure 2: "Safe operating area"</i> , <i>Figure 3: "Thermal impedance"</i> and <i>Figure 8: "Capacitance variations"</i> . Added <i>Figure 9: "Normalized V(BR)DSS vs temperature"</i> and <i>Figure 10: "Normalized gate threshold voltage vs temperature"</i> . Minor text changes

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[STMicroelectronics:](#)

[STL120N4F6AG](#)