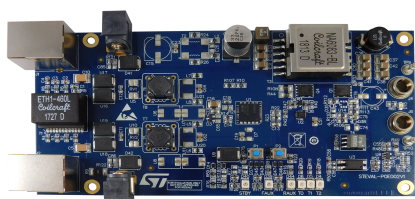


5V/8A, synchronous flyback converter, Power over Ethernet (PoE) IEEE 802.3bt compliant reference design



Features

- **PM8805** 4-pair IEEE 802.3bt compliant PD interface
- Works with power supplied from Ethernet LAN cables or local auxiliary sources
- Line input voltage range: 40 to 60 V_{DC}
- Output stage managed by configurable **PM8804** controller
- Output voltage: 5 V_{DC} ±2.5%
- Output current: 8 A
- Peak-to-peak output ripple: <50 mV
- DC-DC full load efficiency: >91%
- Overall full load efficiency: >90%
- Transient response ΔV pk-pk 100% to 50% load step ≈ 700 mV
- Switching frequency ≈ 280 KHz

Description

The **STEVAL-POE002V1** reference design is a two-stage converter for a powered device (PD), and is able to deliver up to 40 W (5 V/8 A) DC from appropriate 4-pair PoE power sourcing equipment (PSE), or an external auxiliary supply.

The first stage is the Ethernet interface is based on the **PM8805** controller with integrated full active bridge rectification. The PoE controller is compliant with the third generation IEEE 802.3bt specification (as well as the preceding 802.3af/at standards), with improved features and increased power capacity that allow new application possibilities for PoE networks, including point of sales and retail logistics devices.

The second stage is the DC-DC converter designed around a fixed frequency flyback topology managed by the configurable **PM8804** PWM controller, with secondary synchronous rectification via a gate driver transformer.

Product summary	
PoE-PD converter based on PM8804 and PM8805	STEVAL-POE002V1
PWM peak current mode controller for PoE and telecom systems	PM8804
IEEE802.3bt PoE-PD interface with integrated dual-active bridge	PM8805

1 STEVAL-POE002V1 schematic diagrams

Figure 1. STEVAL-POE002V1 circuit schematic (1 of 4)

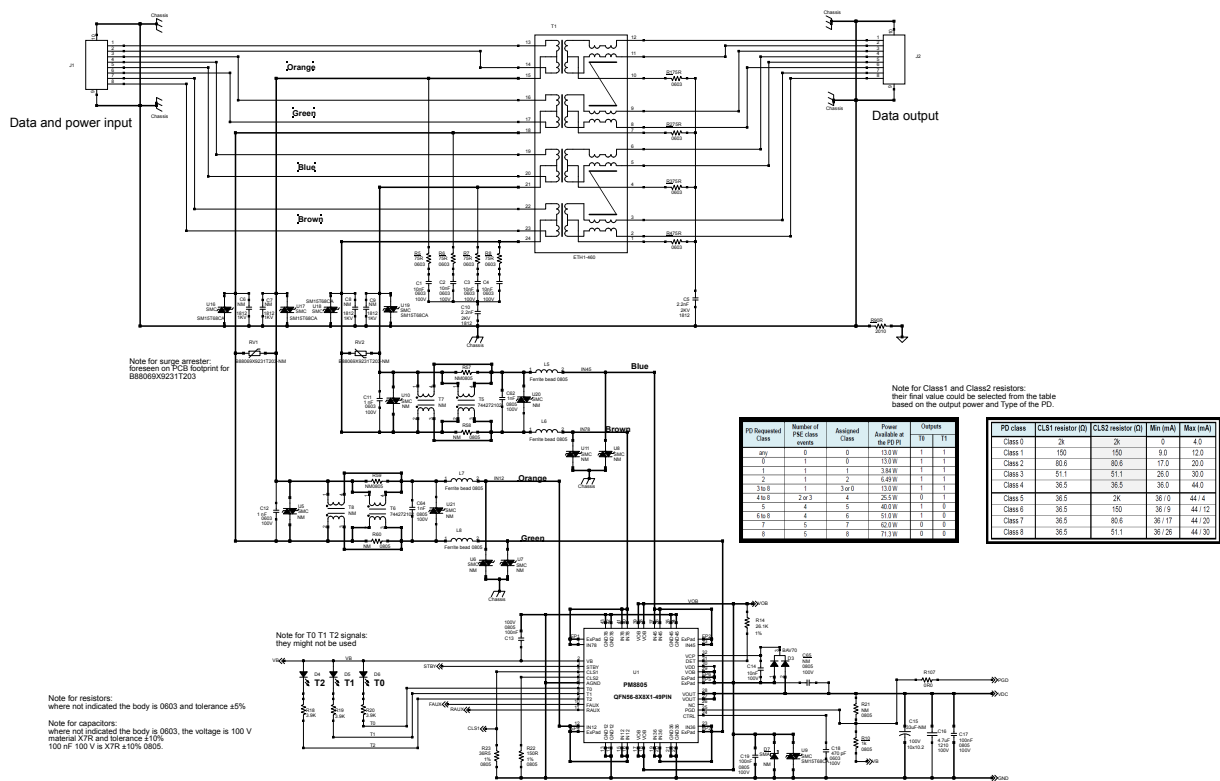


Figure 2. STEVAL-POE002V1 circuit schematic (2 of 4)

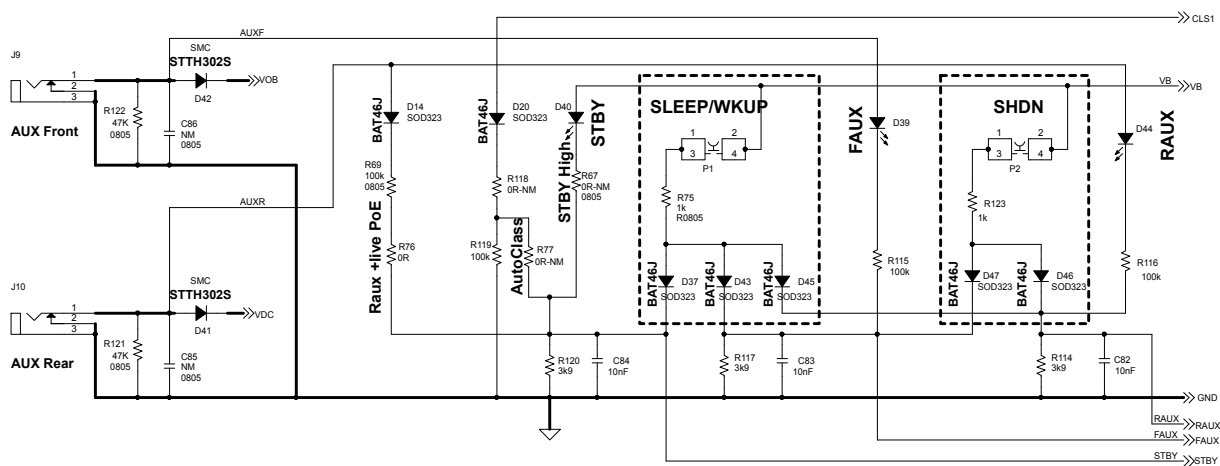


Figure 3. STEVAL-POE002V1 circuit schematic (3 of 4)

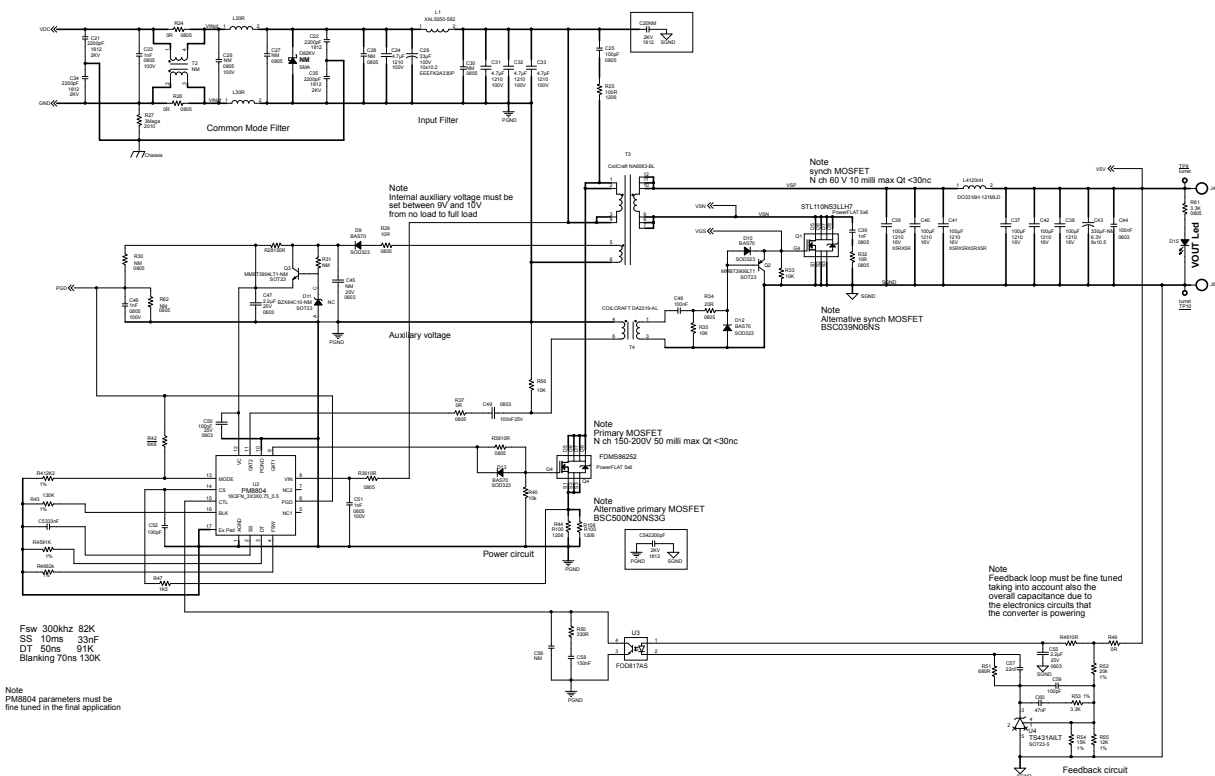
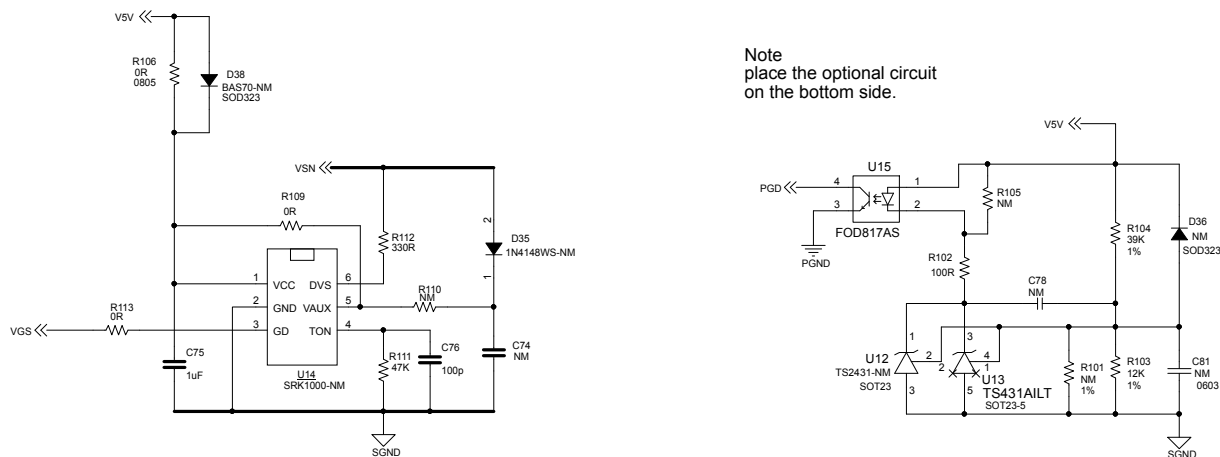


Figure 4. STEVAL-POE002V1 circuit schematic (4 of 4)



Revision history

Table 1. Document revision history

Date	Version	Changes
16-Oct-2018	1	Initial release.
02-May-2019	2	Updated cover page title and Description

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