



## STEVAL-ISA044V5

3 A synchronous 900 kHz step-down DC-DC converter with inhibit function based on the ST1S10 (Power SO-8)

Data brief

### Features

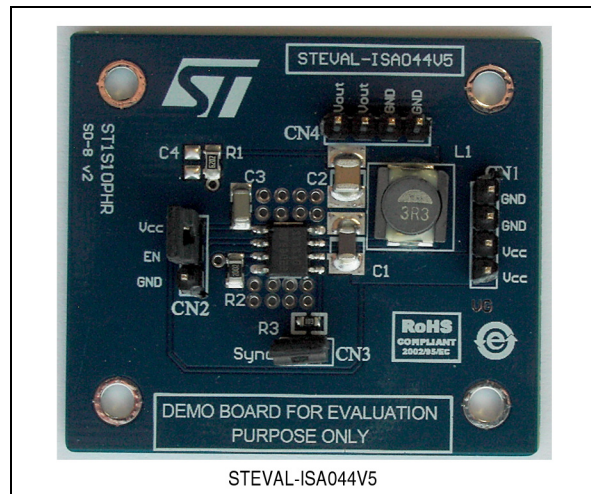
- Input voltage range: 2.5 V to 18.0 V
- Max  $I_{OUT}$  : 3 A
- High internal switching frequency : 900 kHz
- PWM mode operation with a fixed frequency or synchronized to an external frequency between 400 kHz and 1.2 MHz
- Inhibit pin available
- Quiescent current : < 6  $\mu$ A in inhibit state
- RoHS compliant

### Description

The STEVAL-ISA044V5 is a demonstration board based on the ST1S10 device assembled in a Power SO-8 ePad package. The ST1S10 is a step-down DC-DC converter with the inhibit function optimized for powering high voltages in LCD applications and low voltages in digital-core HDD applications. It replaces the high-current linear solution when high power dissipation is an issue.

It provides up to 3 A over an input voltage range of 2.5 V to 18.0 V, and synchronous rectification removes the need for an external Schottky diode. A high internal switching frequency (900 kHz) allows for the use of tiny surface-mount components, as well as a resistor divider to set the output voltage value. Only an inductor and 3 capacitors are required.

The current-mode PWM architecture and stable operation with low-ESR SMD ceramic capacitors result in low output ripple. To maximize power conversion efficiency in light load, the regulator can work in burst mode automatically. The device can operate in PWM mode with a fixed frequency or synchronized to an external frequency. It switches at a frequency of 900 kHz when the SYNC pin is connected to ground or a fixed voltage (less than 5.5 V), and can synchronize the

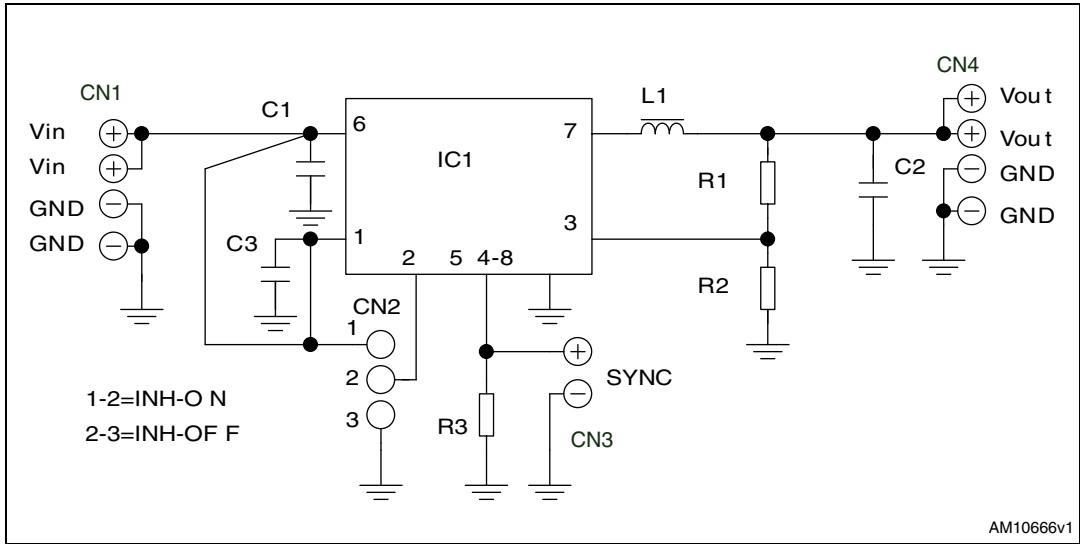


switching frequency between 400 kHz to 1.2 MHz from an external clock applied to the SYNC pin.

A thermal shutdown circuit is integrated and activates at 150 °C. Cycle-by-cycle current limitation provides protection against shorted outputs. The quiescent current is less than 6  $\mu$ A in the inhibit state.

# 1 Schematic

Figure 1. Schematic



## 2 Revision history

Table 1. Document revision history

Date	Revision	Changes
11-Oct-2011	1	Initial release.

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