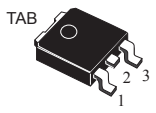
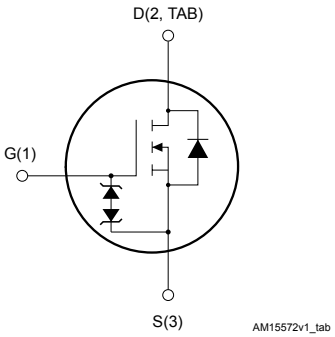
STD70R1K3S

Datasheet

N-channel 700 V, 1.3 Ω typ., 5 A Power MOSFET in a DPAK package



DPAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD70R1K3S	700 V	1.4 Ω	5 A

- Reduced switching losses
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an high voltage N-channel Power MOSFET. This product offers improved on-resistance, low gate charge, high dv/dt capability and excellent avalanche characteristics.

Product status link
STD70R1K3S

Product summary	
Order code	STD70R1K3S
Marking	70R1K3S
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	5	A
	Drain current (continuous) at T_C = 100 °C	3.15	
I_{DM} (1)	Drain current (pulsed)	8.5	A
P_{TOT}	Total power dissipation at T_C = 25 °C	77	W
dv/dt(2)	Peak diode recovery voltage slope	5	V/ns
di/dt(2)	Peak diode recovery current slope	100	A/µs
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 5 A, V_{DS} peak < $V_{(BR)DSS}$, V_{DD} = 100 V.*
3. *V_{DS} ≤ 560 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.62	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-ambient	50	°C/W

1. *When mounted on an 1-inch² FR-4, 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max)	1	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25°C, I_D = I_{AR}, V_{DD} = 50 V)	90	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0 V, I_D = 1 mA	700			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 700 V			1	µA
		V_{GS} = 0 V, V_{DS} = 700 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.25	3.00	3.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1.75 A		1.3	1.4	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	175	-	pF
C_{oss}	Output capacitance		-	13	-	pF
C_{rss}	Reverse transfer capacitance		-	0.43	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 560 V, V_{GS} = 0 V	-	70	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	5	-	Ω
Q_g	Total gate charge	V_{DD} = 560 V, I_D = 3.5 A, V_{GS} = 0 to 10 V (See Figure 14. Test circuit for gate charge behavior)	-	4.1	-	nC
Q_{gs}	Gate-source charge		-	0.9	-	nC
Q_{gd}	Gate-drain charge		-	1.6	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 350 V, I_D = 1.75 A, R_G = 4.7 Ω, V_{GS} = 10 V (See Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	7	-	ns
t_r	Rise time		-	6.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	18	-	ns
t_f	Fall time		-	20	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		8.5	A
V_{SD} (2)	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 3.5 A, di/dt = 100 A/µs, V_{DD} = 60 V (See Figure 15. Test circuit for inductive load switching and diode recovery times)	-	267		ns
Q_{rr}	Reverse recovery charge		-	1.78		µC
I_{RRM}	Reverse recovery current		-	9.8		A
t_{rr}	Reverse recovery time	I_{SD} = 3.5 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (See Figure 15. Test circuit for inductive load switching and diode recovery times)	-	400		ns
Q_{rr}	Reverse recovery charge		-	2.52		µC
I_{RRM}	Reverse recovery current		-	8.5		A

1. *Pulse width limited by safe operating area*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

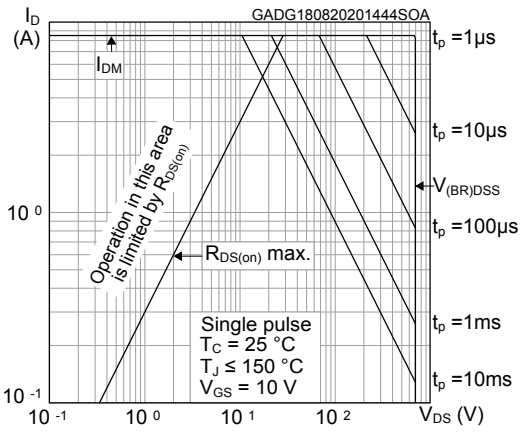


Figure 2. Maximum transient thermal impedance

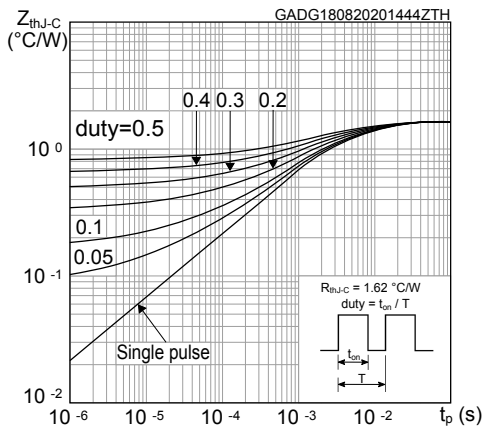


Figure 3. Typical output characteristics

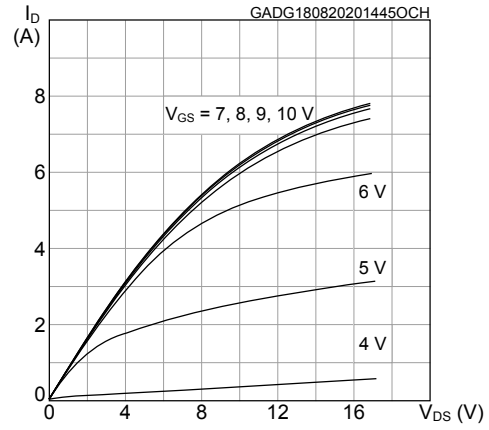


Figure 4. Typical transfer characteristics

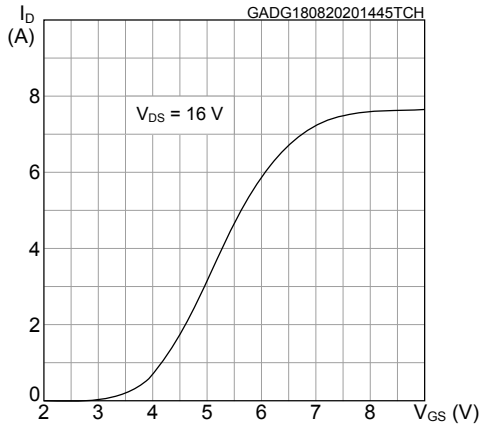


Figure 5. Typical gate charge characteristics

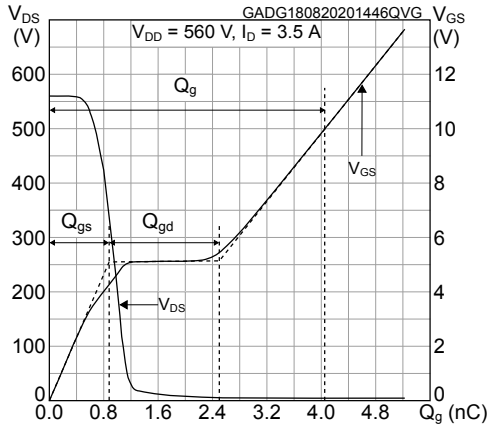


Figure 6. Typical drain-source on-resistance

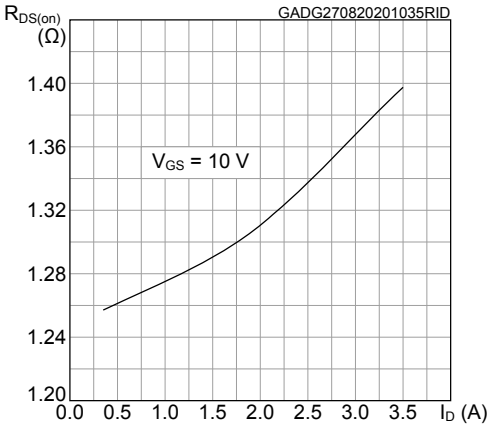


Figure 7. Typical capacitance characteristics

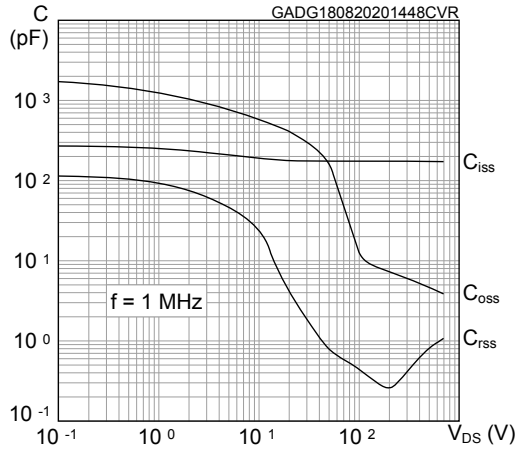


Figure 8. Normalized gate threshold vs temperature

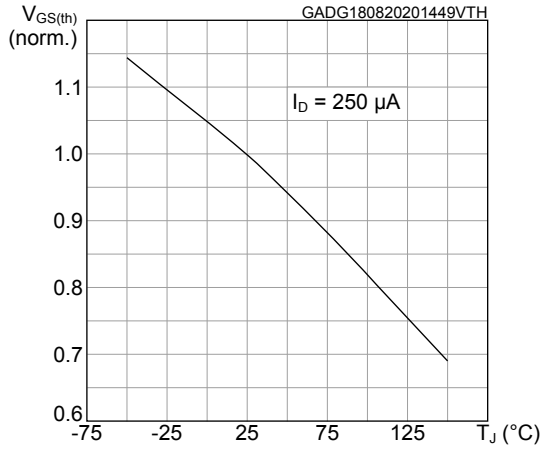


Figure 9. Normalized on-resistance vs temperature

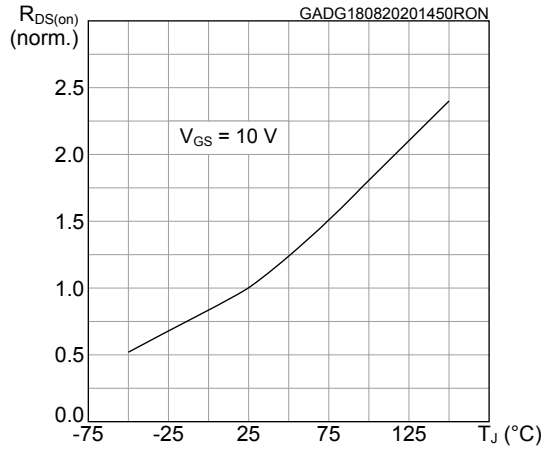


Figure 10. Normalized breakdown voltage vs temperature

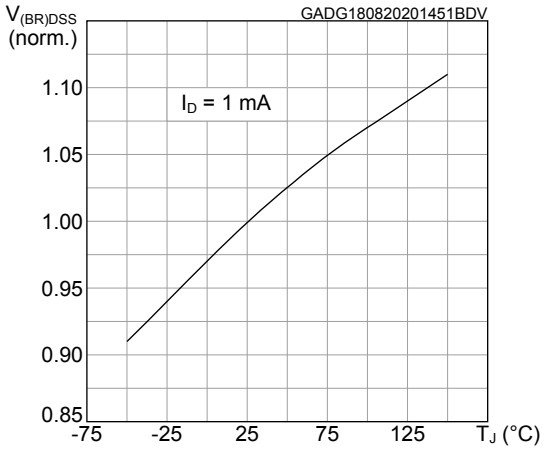


Figure 11. Typical output capacitance stored energy

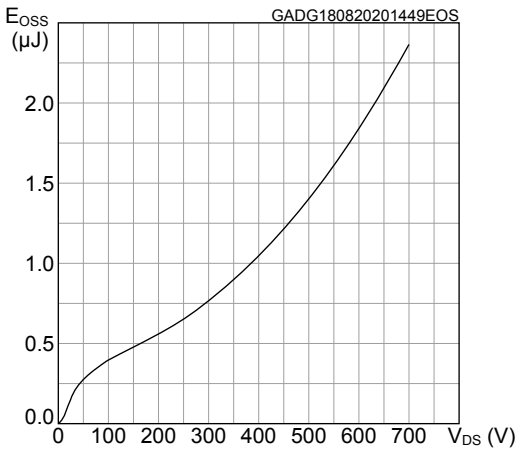
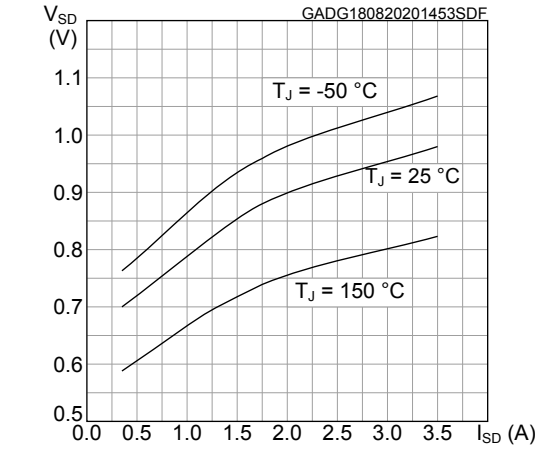


Figure 12. Typical reverse diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times

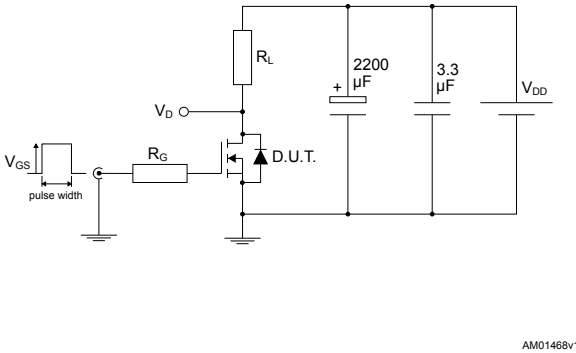


Figure 14. Test circuit for gate charge behavior

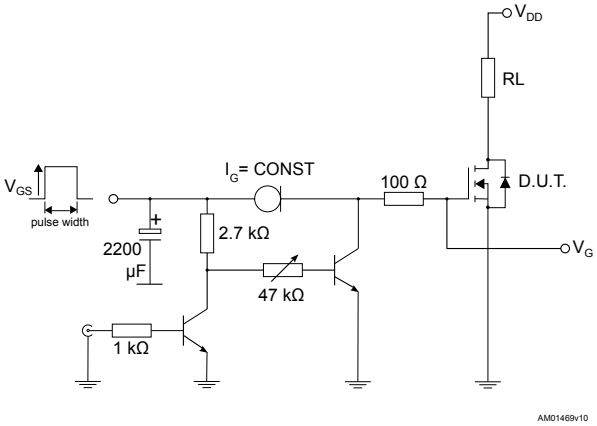


Figure 15. Test circuit for inductive load switching and diode recovery times

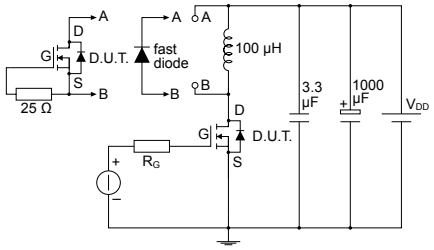


Figure 16. Unclamped inductive load test circuit

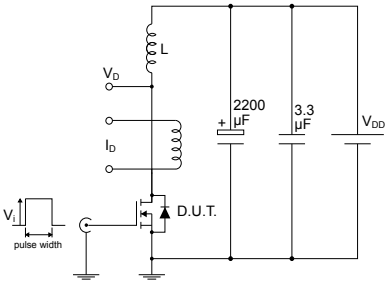


Figure 17. Unclamped inductive waveform

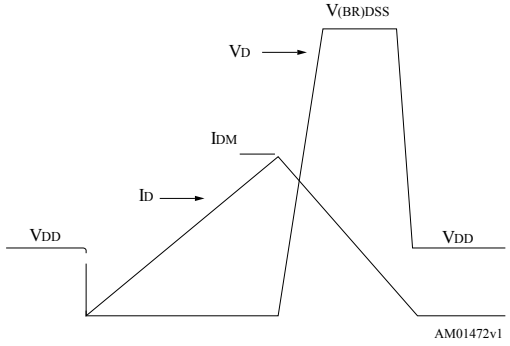
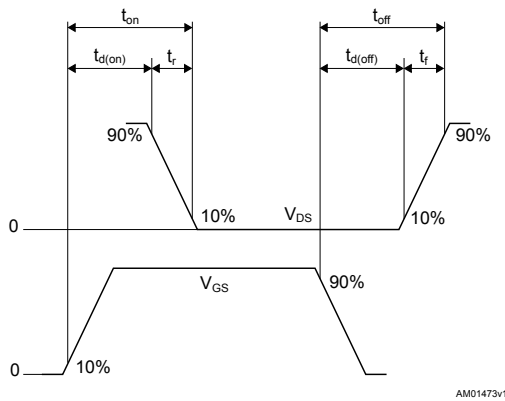


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type C package information

Figure 19. DPAK (TO-252) type C package outline

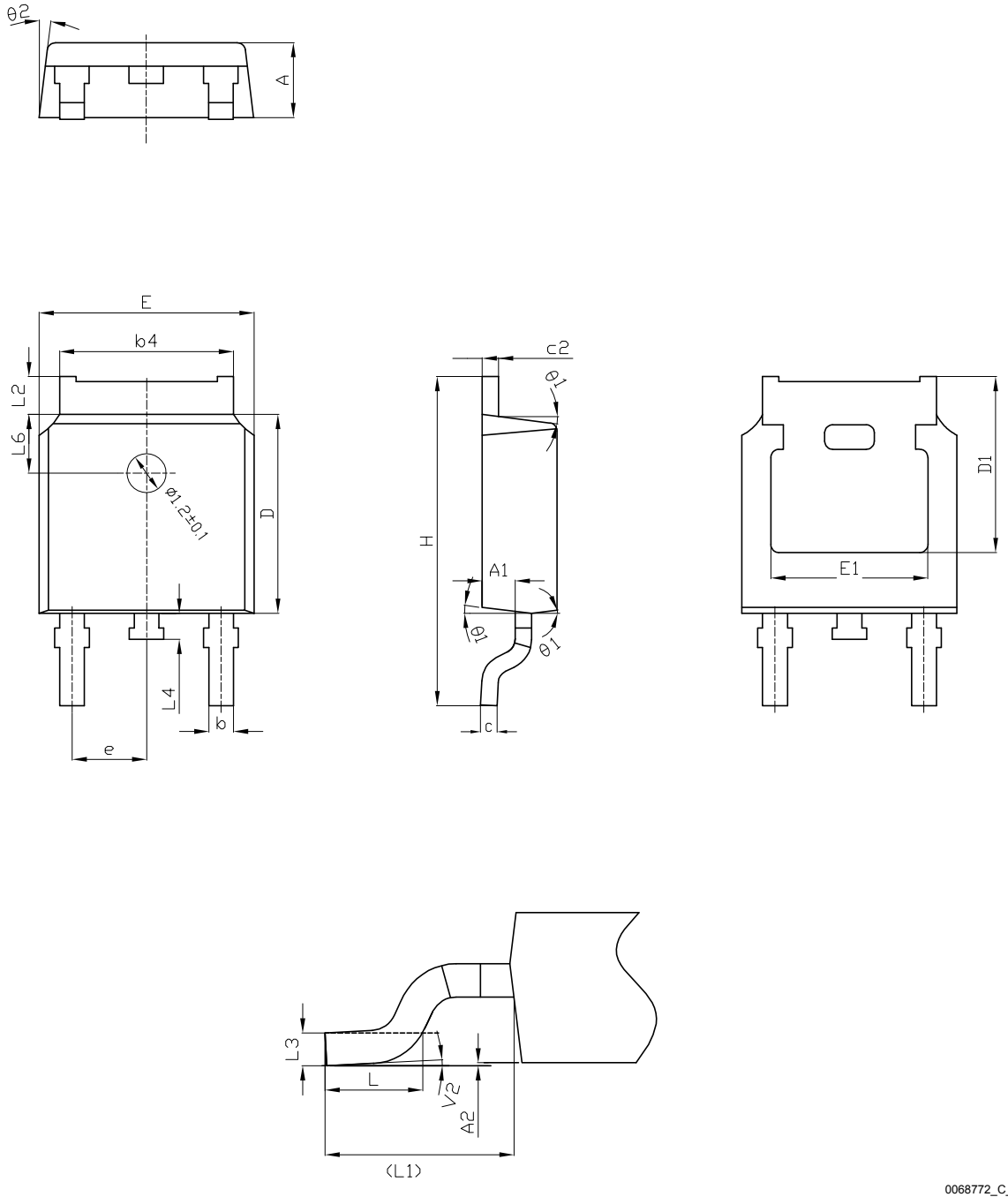
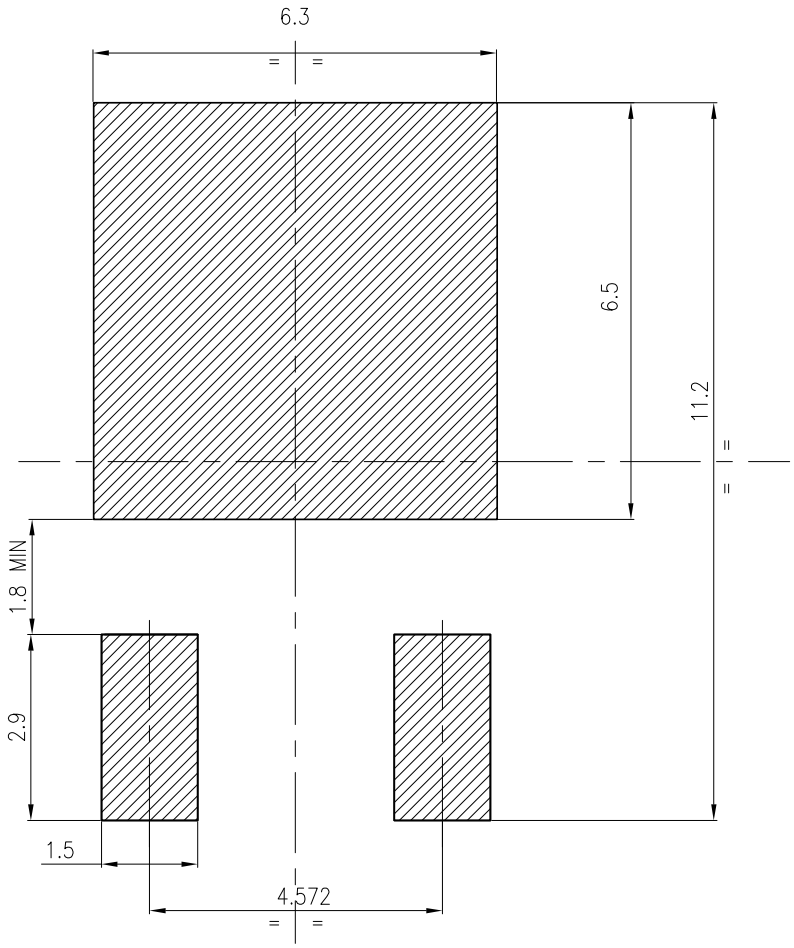


Table 8. **DPAK (TO-252) type C mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60	0.80	1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 20. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



4.2 DPAK (TO-252) packing information

Figure 21. **DPAK (TO-252) tape outline**

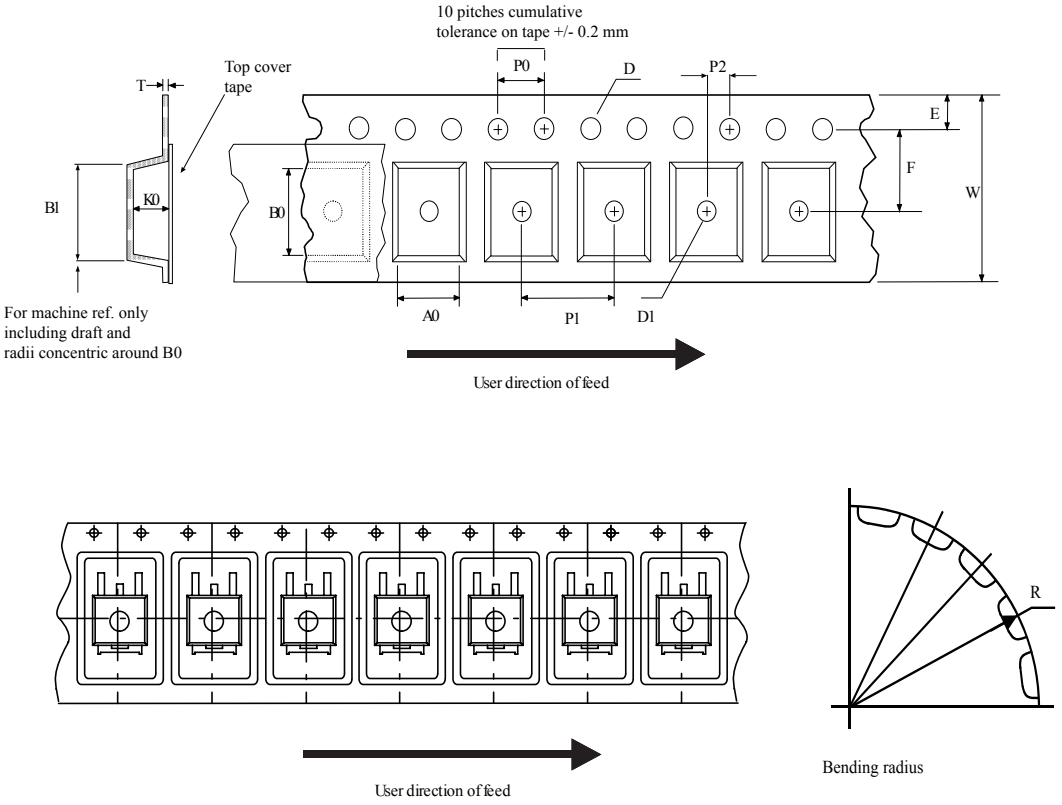
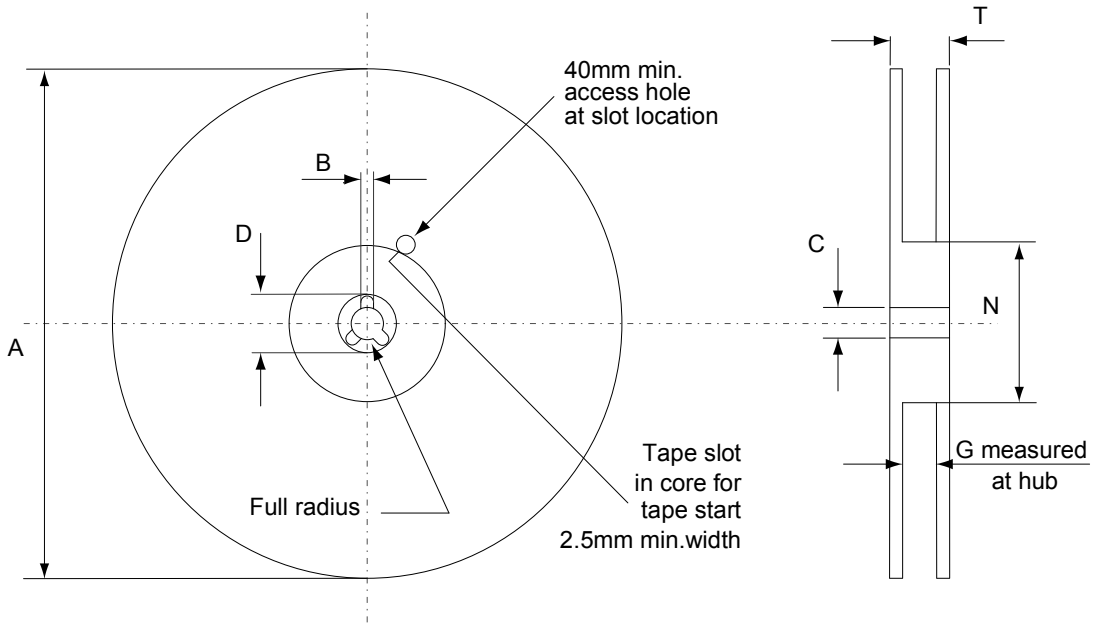


Figure 22. **DPAK (TO-252) reel outline**



AM06038v1

Table 9. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 10. **Document revision history**

Date	Version	Changes
17-Dec-2019	1	Initial release.
03-Sep-2020	2	Updated Title and Features in cover page. Updated Section 1 Electrical ratings. Updated Section 2 Electrical characteristics. Added Section 2.1 Electrical characteristics (curves). Updated Figure 14. Test circuit for gate charge behavior. Updated Section 4 Package information.

Contents

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