



STD70N6F3

N-channel 60 V, 8.0 mΩ, 70 A DPAK
STripFET™ III Power MOSFET

Preliminary data

Features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STD70N6F3	60 V	< 10.5 mΩ	70 A	110 W

- Standard threshold drive
- 100% avalanche tested

Application

- Switching applications

Description

This STripFET™ III Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance providing superior switching performance.

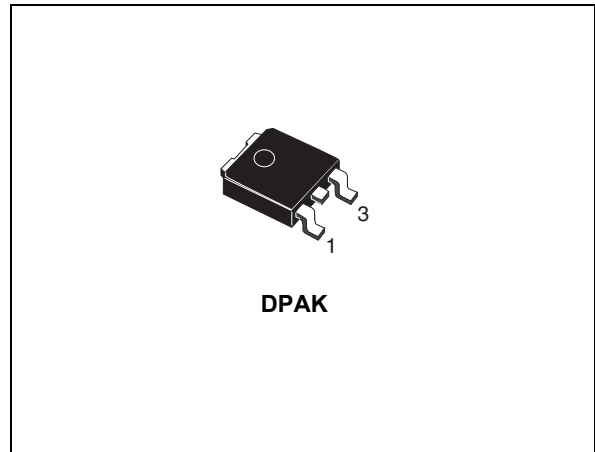
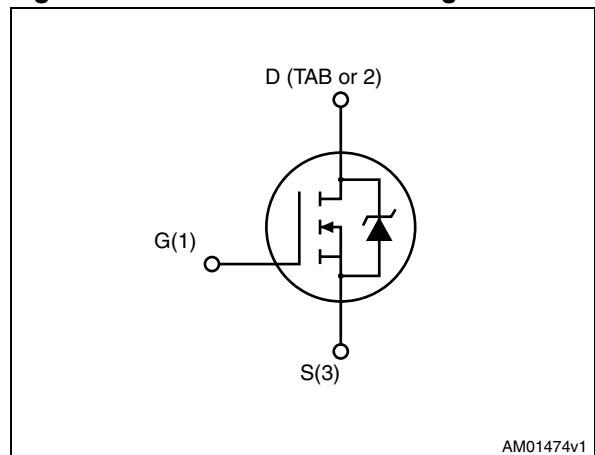


Figure 1. Internal schematic diagram



AM01474v1

Table 1. Device summary

Order code	Marking	Package	Packaging
STD70N6F3	70N6F3	DPAK	Tape & reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	60	V
V_{GS}	Gate-Source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	70	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	50	A
$I_{DM}^{(1)}$	Drain current (pulsed)	280	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	110	W
	Derating factor	0.73	W/ $^{\circ}\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	TBD	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	TBD	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 70\text{ A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{jmax}$
3. Starting $T_j = 25^{\circ}\text{C}$, $I_d = 35\text{ A}$, $V_{dd} = 40\text{ V}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.36	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	50	$^{\circ}\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu.

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	60			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating}$, $T_c = 125\ ^{\circ}\text{C}$			10 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\ \text{V}$			± 200	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}$, $I_D = 35\ \text{A}$		8.0	10.5	$\text{m}\Omega$

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 25\ \text{V}$, $I_D = 35\ \text{A}$	-	Tbd		S
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$	-	2200		pF
C_{oss}	Output capacitance			500		pF
C_{rss}	Reverse transfer capacitance			25		pF
Q_g	Total gate charge	$V_{DD} = 48\ \text{V}$, $I_D = 70\ \text{A}$	-	35	TBD	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\ \text{V}$		15		nC
Q_{gd}	Gate-drain charge	(see Figure 5)		10		nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=30\text{ V}$, $I_D=35\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ (see Figure 4), (see Figure 7)	-	TBD TBD	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=30\text{ V}$, $I_D=35\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ (see Figure 4), (see Figure 7)	-	TBD TBD	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed) ⁽¹⁾		-		70 280	A A
V_{SD}	Forward on voltage	$I_{SD}=70\text{ A}$, $V_{GS}=0$	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=70\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$, $V_{DD}=30\text{ V}$, $T_J=150\text{ }^\circ\text{C}$ (see Figure 6)	-	TBD TBD TBD		ns nC A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

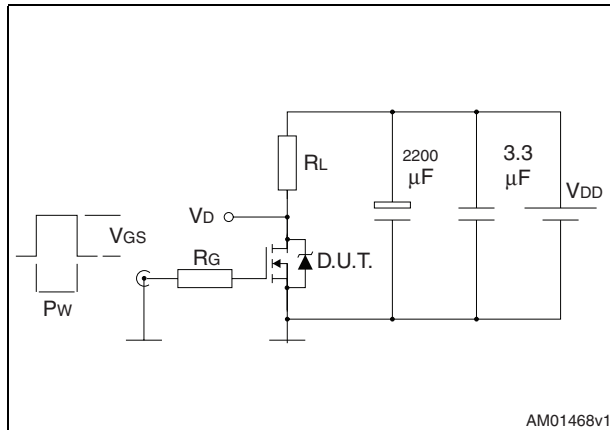


Figure 3. Gate charge test circuit

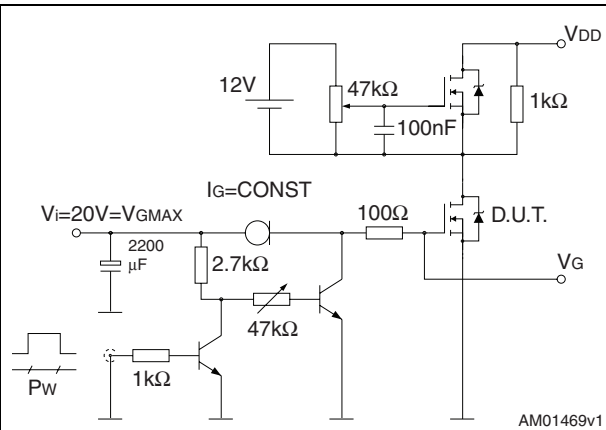


Figure 4. Test circuit for inductive load switching and diode recovery times

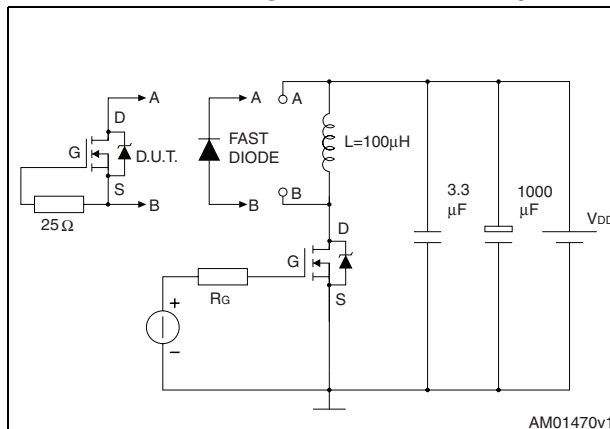


Figure 5. Unclamped inductive load test circuit

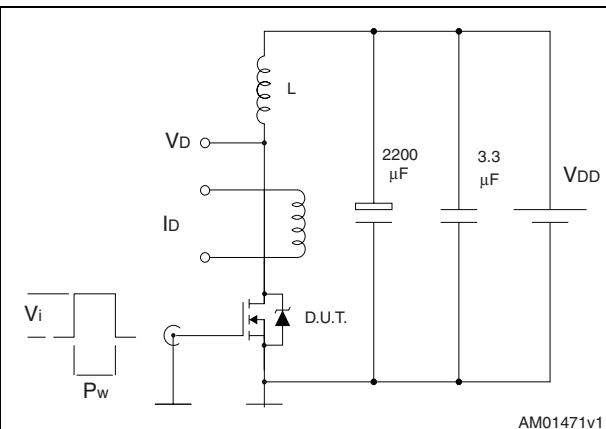


Figure 6. Unclamped inductive waveform

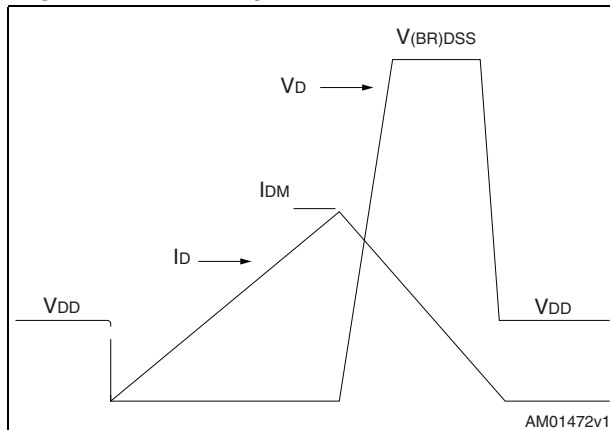
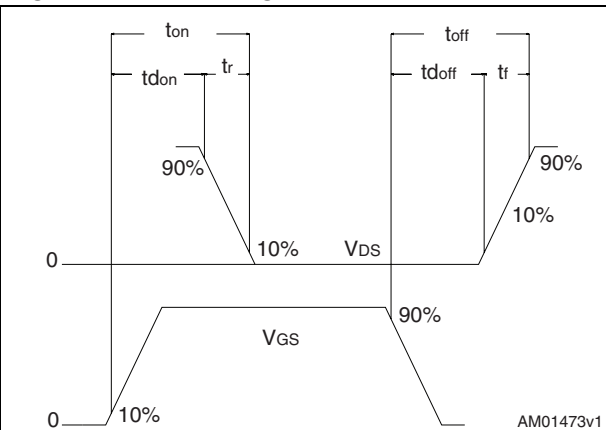
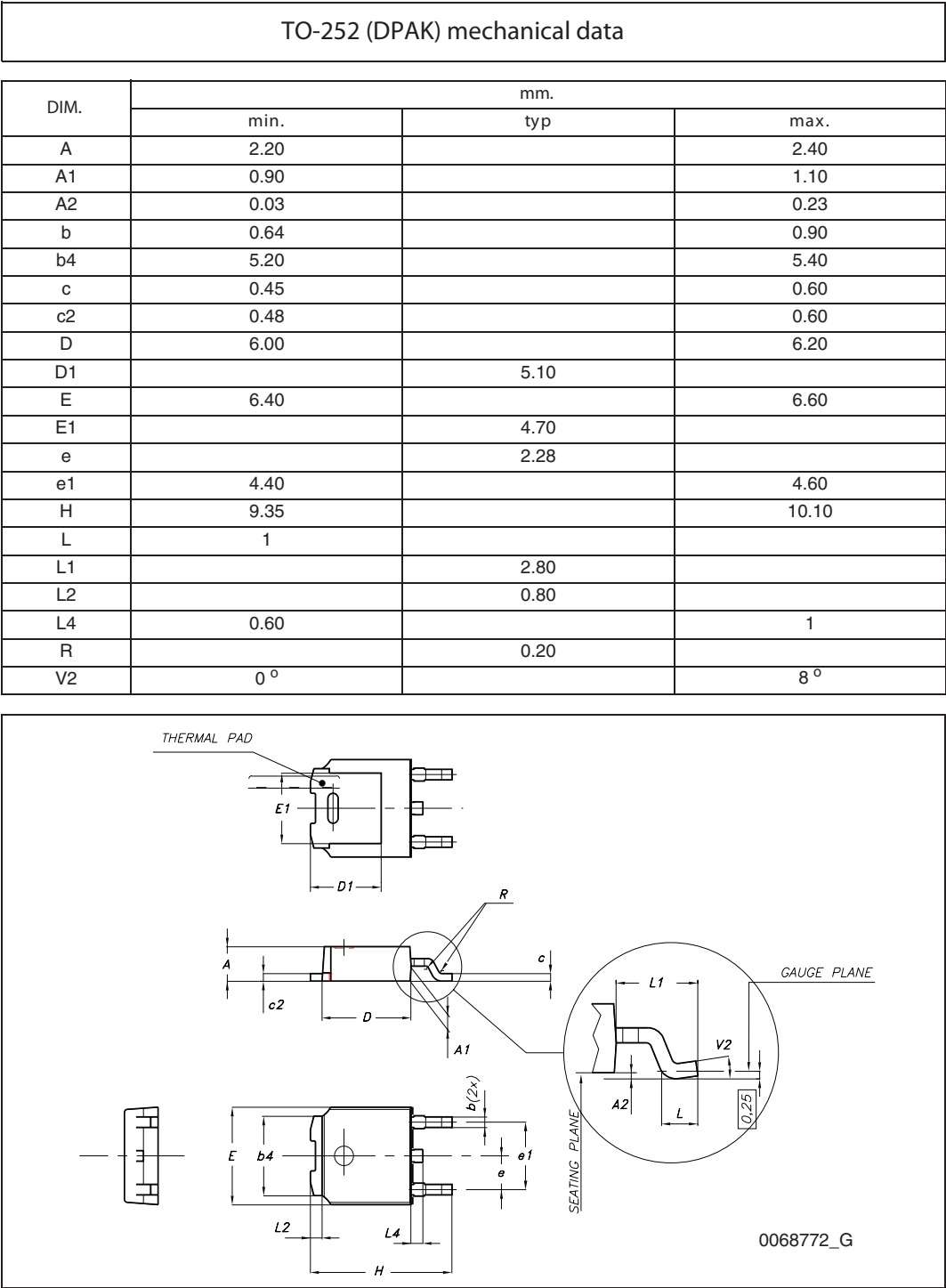


Figure 7. Switching time waveform



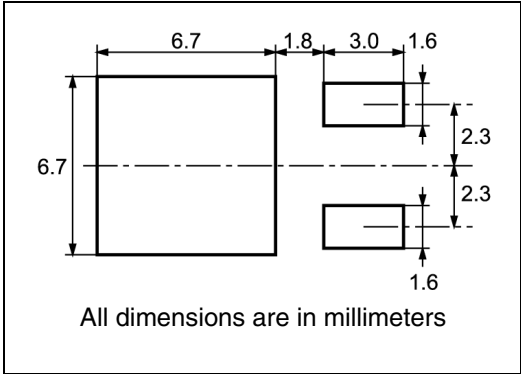
4 Package mechanical data

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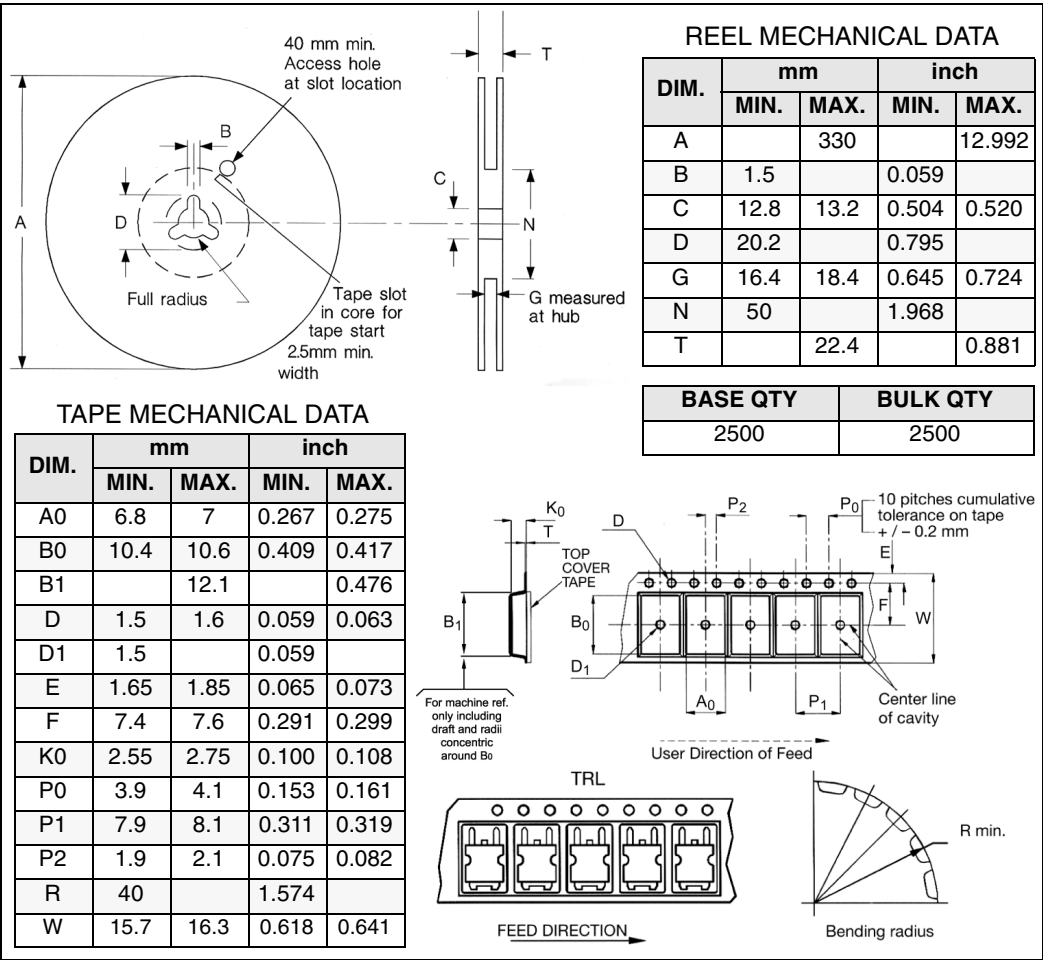


5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 8. Revision history

Date	Revision	Changes
11-Dec-2009	1	First release

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