



# STD5N20L

N-CHANNEL 200V - 0.65Ω - 5A DPAK

STripFET™ MOSFET

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STD5N20L	200 V	< 0.7 Ω	5 A	33 W

- TYPICAL R<sub>DS(on)</sub> = 0.65 Ω @ 5V
- CONDUCTION LOSSES REDUCED
- LOW INPUT CAPACITANCE
- LOW THRESHOLD DEVICE

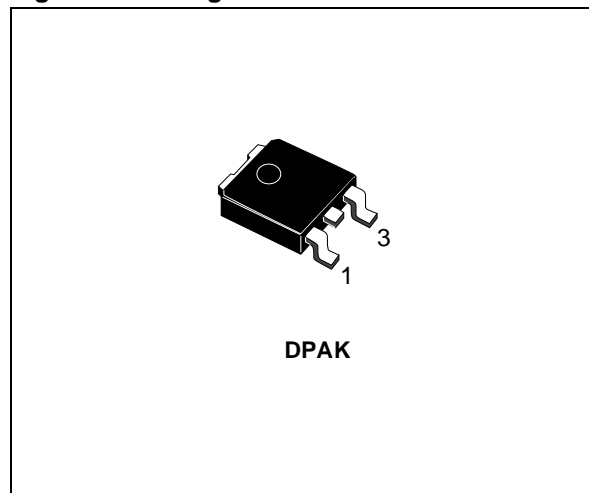
## DESCRIPTION

The STD5N20L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC Motor Control and lighting application.

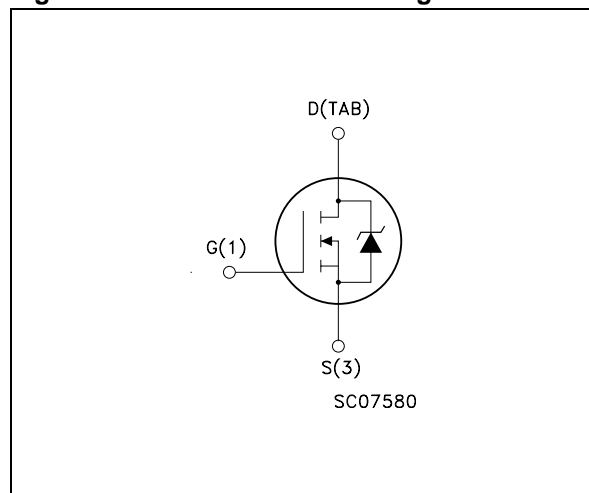
## APPLICATIONS

- UPS AND MOTOR CONTROL
- LIGHTING

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STD5N20LT4	D5N20L	DPAK	TAPE & REEL

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	200	V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20\text{ k}\Omega$ )	200	V
$V_{GS}$	Gate- source Voltage	$\pm 20$	V
$I_D$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	5	A
$I_D$	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	3.6	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	20	A
$P_{TOT}$	Total Dissipation at $T_C = 25^\circ\text{C}$	33	W
	Derating Factor	0.27	W/ $^\circ\text{C}$
$T_{stg}$	Storage Temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Operating Junction Temperature		

( $\bullet$ ) Pulse width limited by safe operating area

**Table 4: Thermal Data**

$R_{thj-case}$	Thermal Resistance Junction-case Max	3.75	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	100	$^\circ\text{C/W}$
$T_l$	Maximum Lead Temperature For Soldering Purpose	275	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^\circ\text{C}$  UNLESS OTHERWISE SPECIFIED)**Table 5: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$	200			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$			1	$\mu\text{A}$
		$V_{DS} = \text{Max Rating}$ , $T_C = 125^\circ\text{C}$			10	$\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 5\text{ V}$ , $I_D = 2.5\text{ A}$		0.65	0.7	$\Omega$

Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (2)	Forward Transconductance	$V_{DS} = 15\text{ V}$ , $I_D = 5\text{ A}$		6.5		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		242 44 6		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 100\text{ V}$ , $I_D = 2.5\text{ A}$ $R_G = 4.7\Omega$ , $V_{GS} = 5\text{ V}$ (Resistive Load see Figure 14)		11.5 21.5 14 15.5		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 160\text{ V}$ , $I_D = 5\text{ A}$ , $V_{GS} = 5\text{ V}$		5 1.5 3	6	nC nC nC

Table 7: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				5	A
$I_{SDM}$ (*)	Source-drain Current (pulsed)				20	A
$V_{SD}$ (1)	Forward On Voltage	$I_{SD} = 5\text{ A}$ , $V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$ , $T_j = 25^\circ\text{C}$ (see test circuit, see Figure 15)		93 237 5.1		ns nC A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$ , $T_j = 150^\circ\text{C}$ (see test circuit, see Figure 15)		97 286 5.9		ns nC A

(1) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.(2) Starting  $T_j = 25^\circ\text{C}$ ,  $I_d = 5\text{ A}$ ,  $V_{DD} = 50\text{ V}$ 

(\*) Pulse width limited by safe operating area

Figure 3: Safe Operating Area

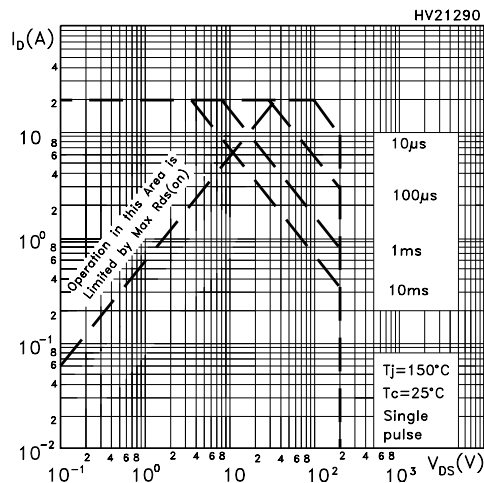


Figure 4: Output Characteristics

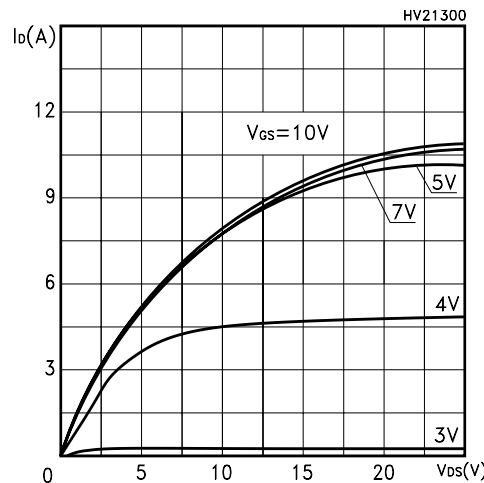


Figure 5: Transconductance

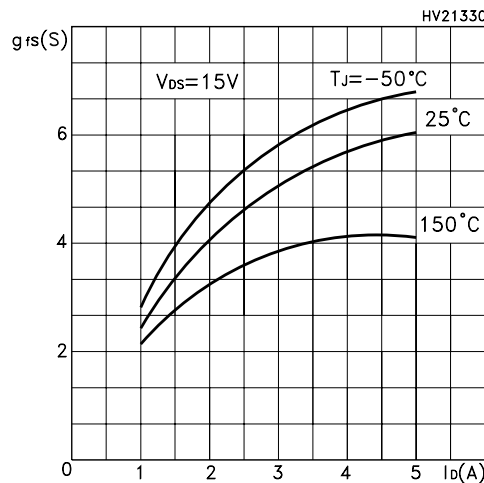


Figure 6: Thermal Impedance

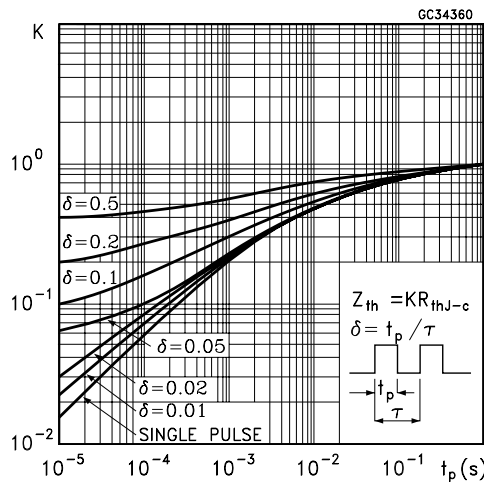


Figure 7: Transfer Characteristics

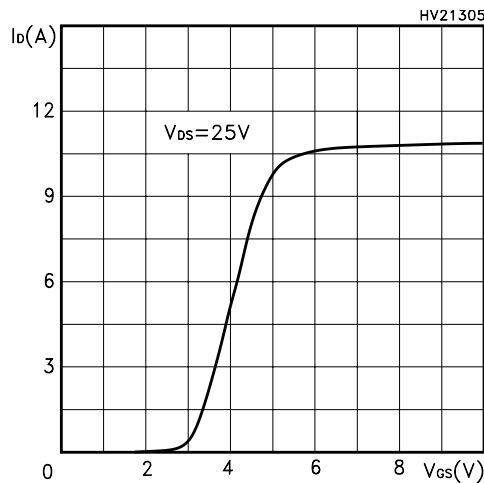


Figure 8: Static Drain-source On Resistance

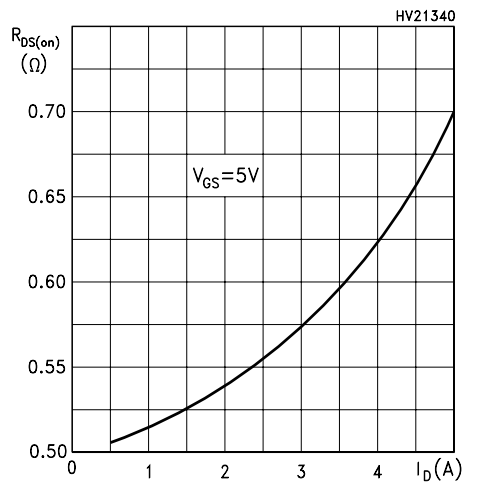


Figure 9: Gate Charge vs Gate-source Voltage

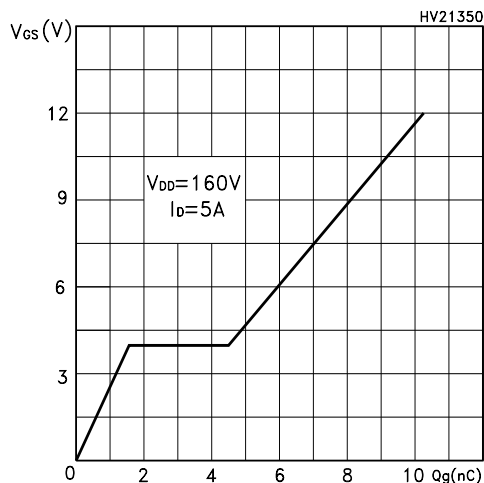


Figure 10: Normalized Gate Threshold Voltage vs Temperature

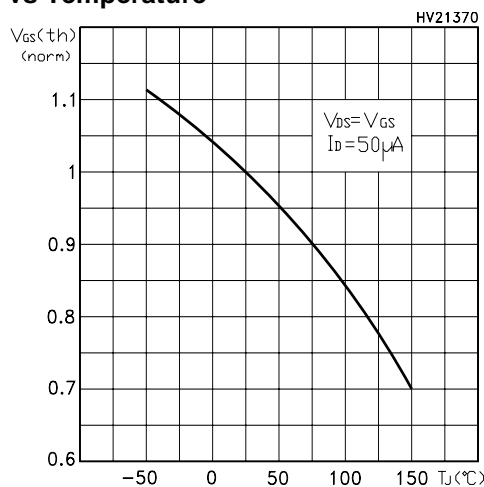


Figure 11: Source-Drain Diode Forward Characteristics

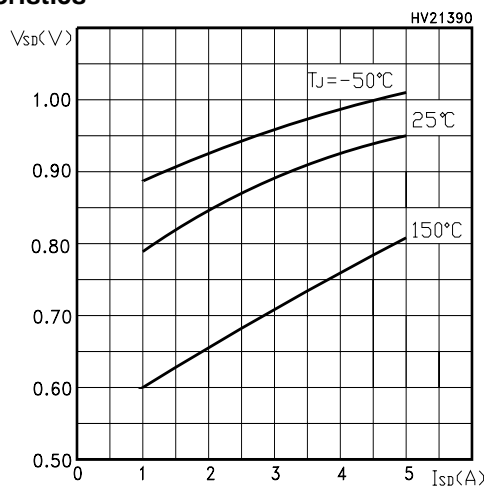


Figure 12: Capacitance Variations

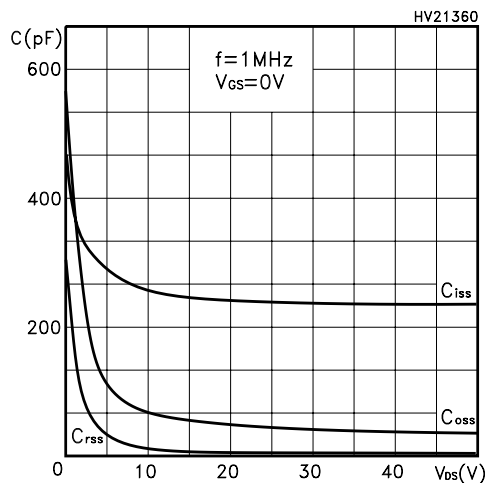


Figure 13: Normalized On Resistance vs Temperature

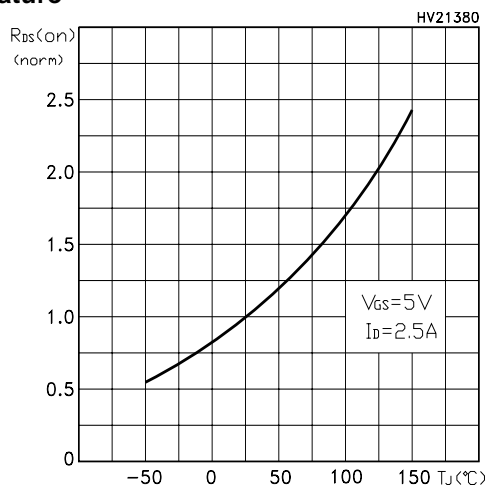


Figure 14: Switching Times Test Circuit For Resistive Load

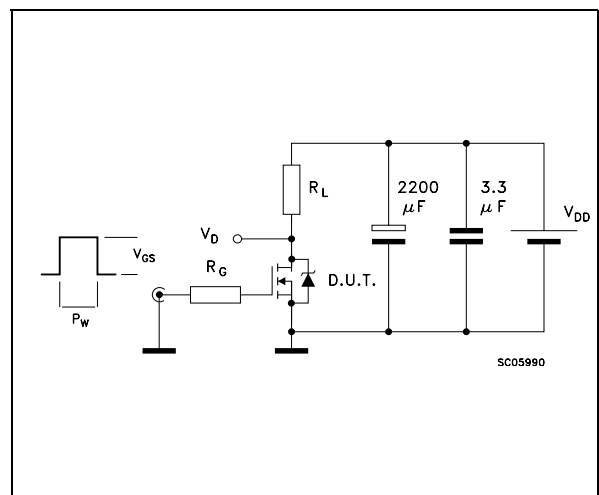


Figure 15: Test Circuit For Inductive Load Switching and Diode Recovery Times

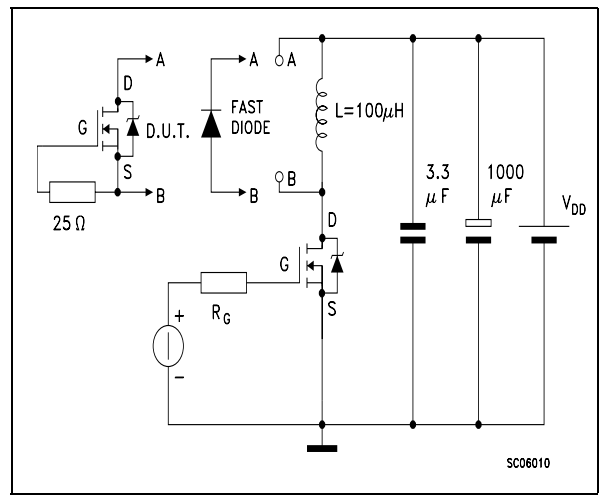
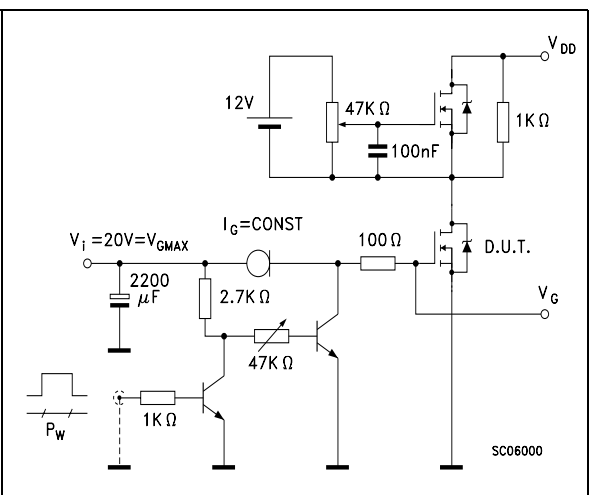
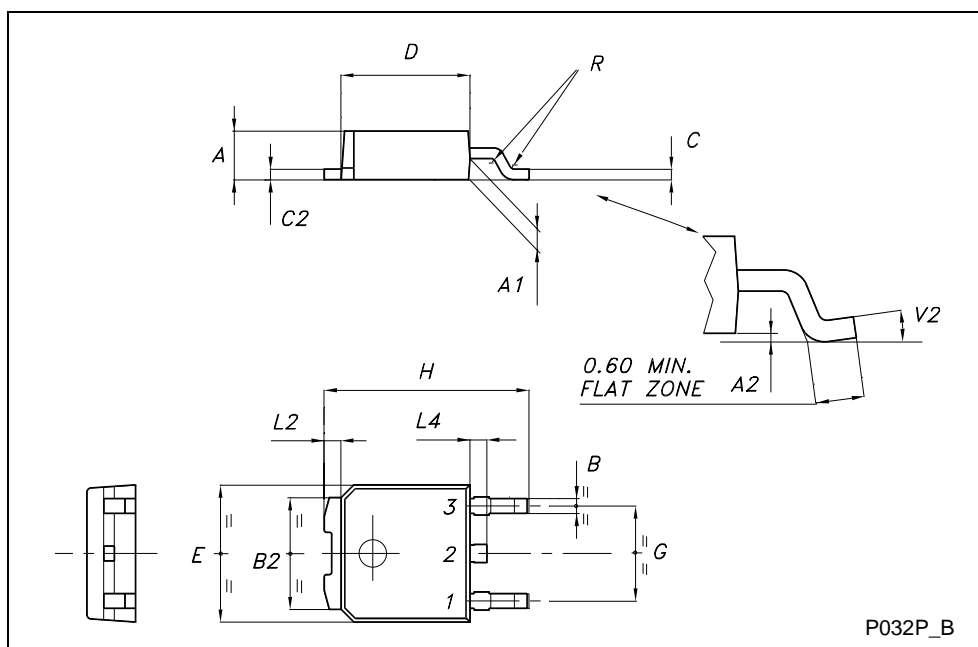


Figure 16: Gate Charge Test Circuit

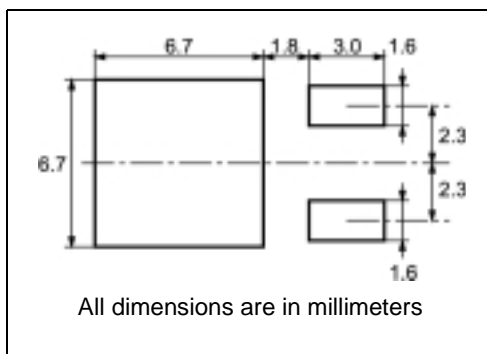


## TO-252 (DPAK) MECHANICAL DATA

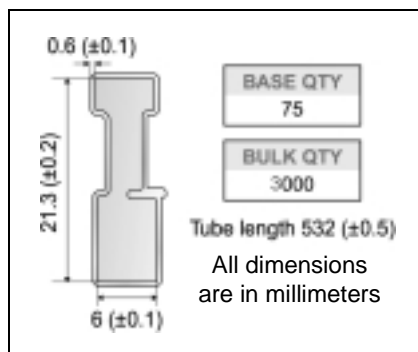
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



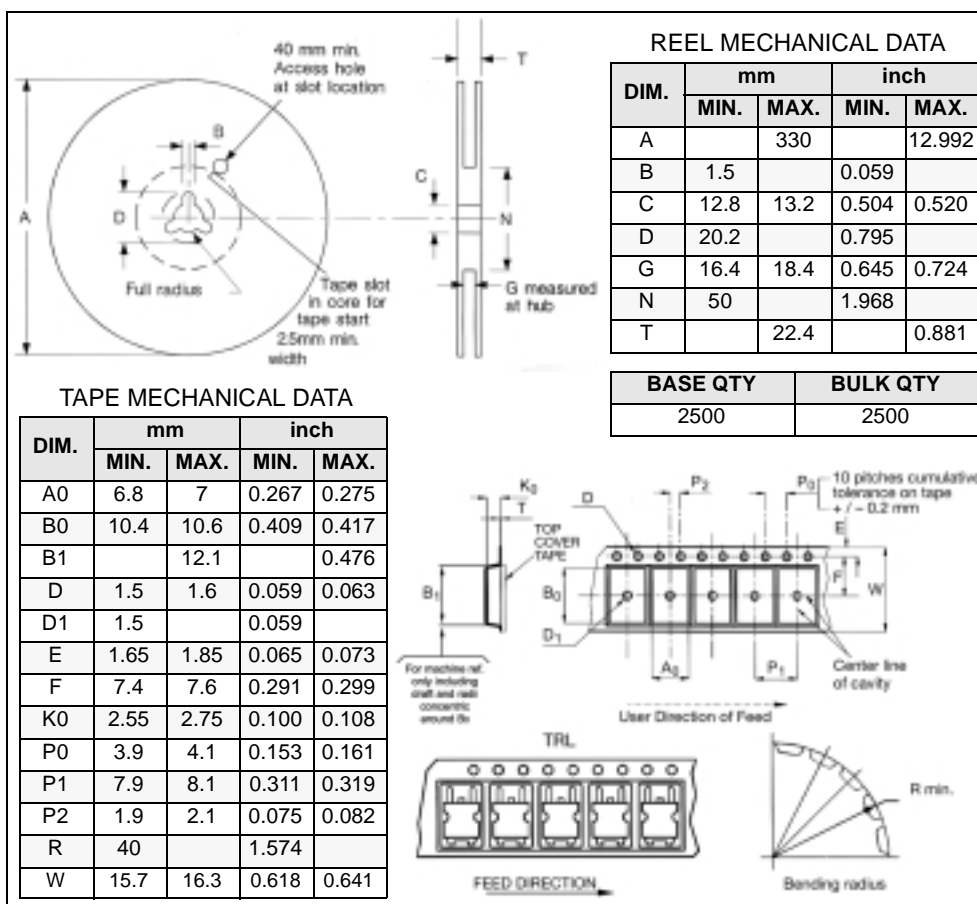
## DPAK FOOTPRINT



## TUBE SHIPMENT (no suffix)\*



## TAPE AND REEL SHIPMENT (suffix "T4")\*



\* on sales type



**Table 8: Revision History**

Date	Revision	Description of Changes
08-June-2004	2	New Stylesheet. Datasheet according to PCN DSG-TRA/04/532
20-Sep-2004	3	Changes on Table 3, and on Figure 3.

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