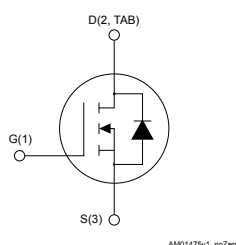
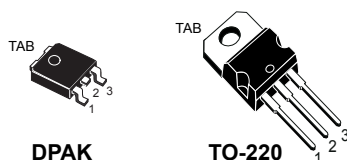


N-channel 550 V, 0.150 Ω typ., 16 A MDmesh M5 Power MOSFETs in a DPAK and TO-220 packages



Features

Order code	V_{DS} @ $T_{jmax.}$	$R_{DS(on)max.}$	Package
STD18N55M5	600 V	0.192 Ω	DPAK
STP18N55M5			TO-220

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Product status link

[STD18N55M5](#)

[STP18N55M5](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	16	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	10	A
$I_{DM}^{(1)}$	Drain current (pulsed)	64	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_j	Operating junction temperature range	-55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 16\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$; $V_{DD} = 340\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		DPAK	TO-220	
R_{thJC}	Thermal resistance, junction-to-case	1.14		$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient		62.5	$^{\circ}\text{C}/\text{W}$
$R_{thJB}^{(1)}$	Thermal resistance, junction-to-board	50		$^{\circ}\text{C}/\text{W}$

1. When mounted on an 1-inch² FR-4, 2oz Cu board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	4	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	210	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	550			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 550 V			1	μA
		V _{GS} = 0 V, V _{DS} = 550 V, T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	4	5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 8 A		0.150	0.192	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	1260	-	pF
C _{oss}	Output capacitance			42		
C _{rss}	Reverse transfer capacitance			3.6		
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{DS} = 0 to 440 V, V _{GS} = 0 V	-	103	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related		-	35	-	pF
R _g	Gate input resistance	f = 1 MHz open drain	-	2.8	-	Ω
Q _g	Total gate charge	V _{DD} = 440 V, I _D = 8 A,	-	31	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 0 to 10 V		8.3		
Q _{gd}	Gate-drain charge	(see Figure 18. Test circuit for gate charge behavior)		14.2		

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t _{d(v)}	Voltage delay time	V _{DD} = 400 V, I _D = 10.5 A,	-	37	-	ns
t _{r(v)}	Voltage rise time	R _G = 4.7 Ω, V _{GS} = 10 V		7		
t _{c(off)}	Crossing time	(see Figure 19. Test circuit for inductive load switching and diode recovery times and Figure 22. Switching time waveform)		10.3		
t _{f(i)}	Current fall time			8.3		

Table 7. Source drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		16	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				64	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 16\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	244		ns
Q_{rr}	Reverse recovery charge			2.8		μC
I_{RRM}	Reverse recovery current			23		A
t_{rr}	Reverse recovery time	$I_{SD} = 16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	295		ns
Q_{rr}	Reverse recovery charge			3.7		μC
I_{RRM}	Reverse recovery current			25		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

Figure 1. Safe operating area for DPAK

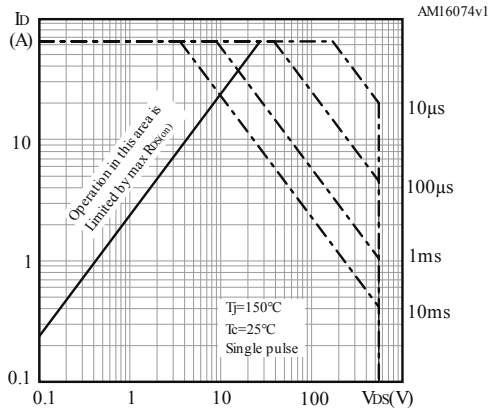


Figure 2. Thermal impedance for DPAK

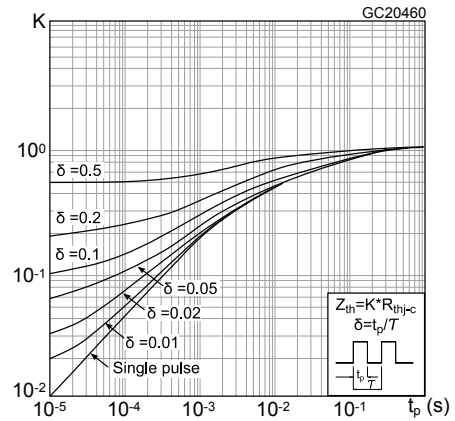


Figure 3. Safe operating area for TO-220

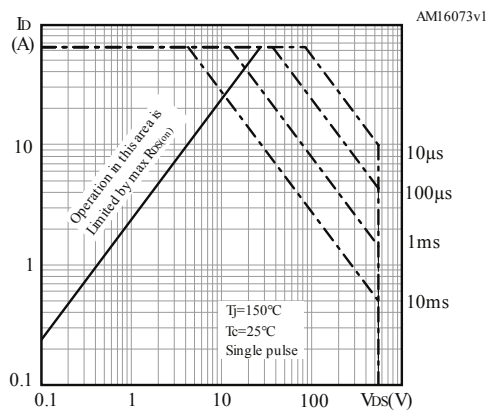


Figure 4. Thermal impedance for TO-220

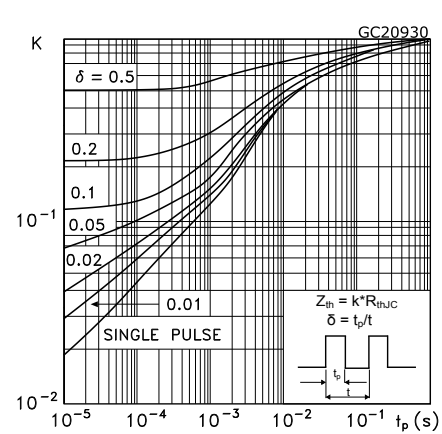


Figure 5. Output characteristics

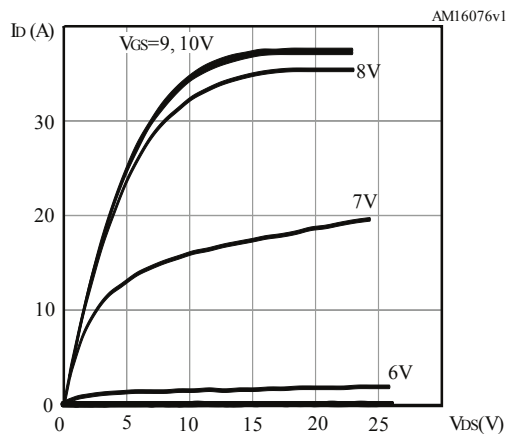


Figure 6. Transfer characteristics

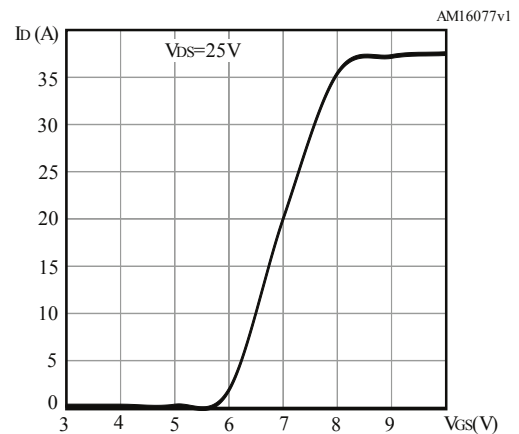


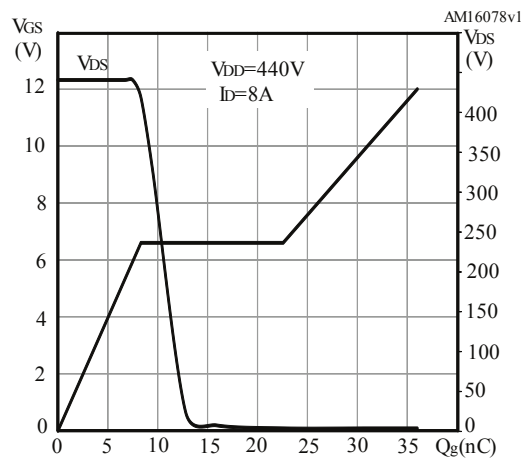
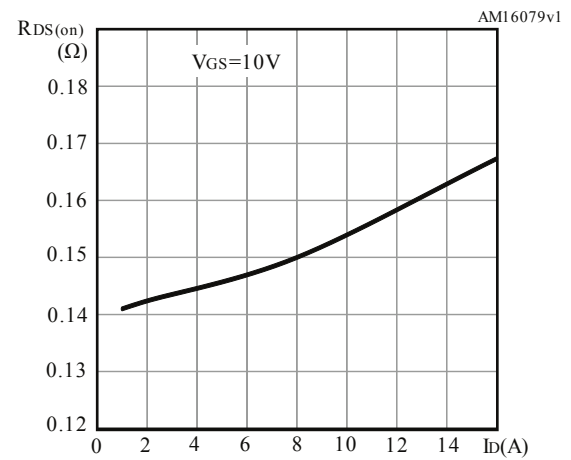
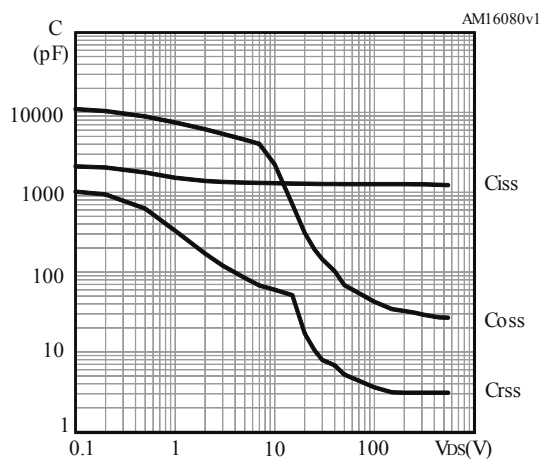
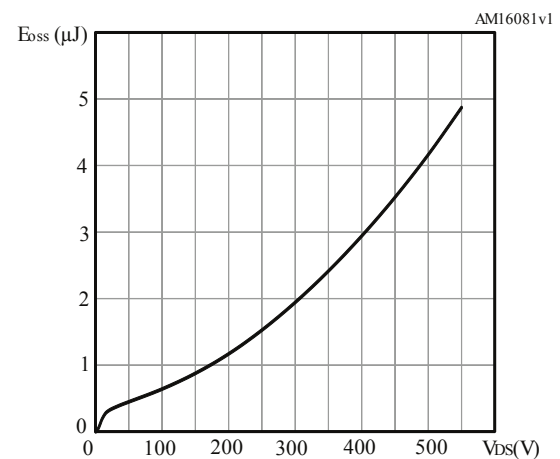
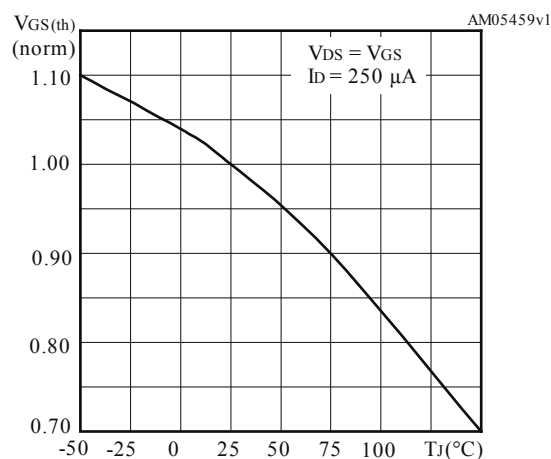
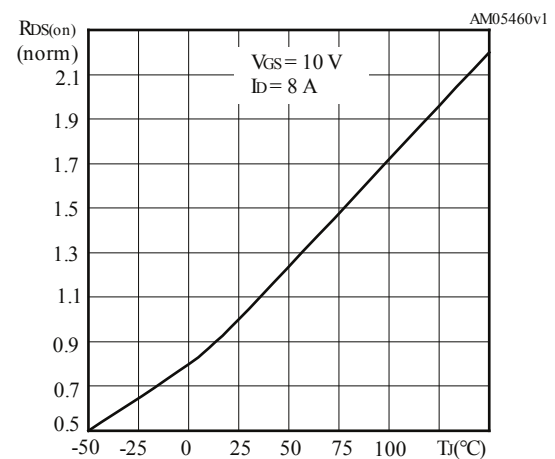
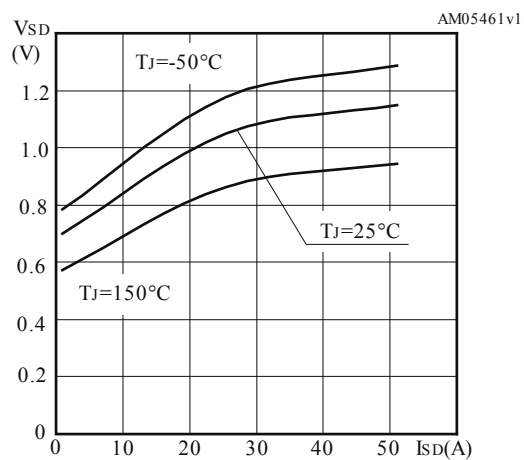
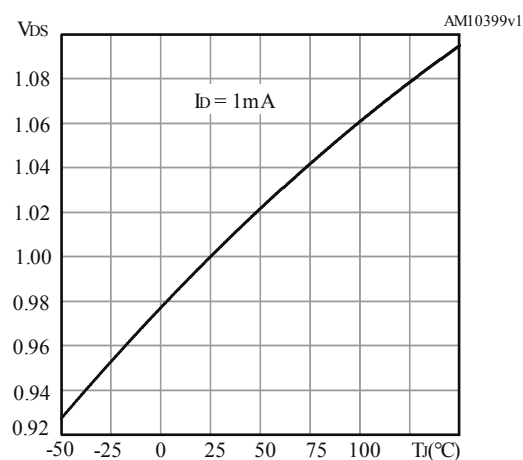
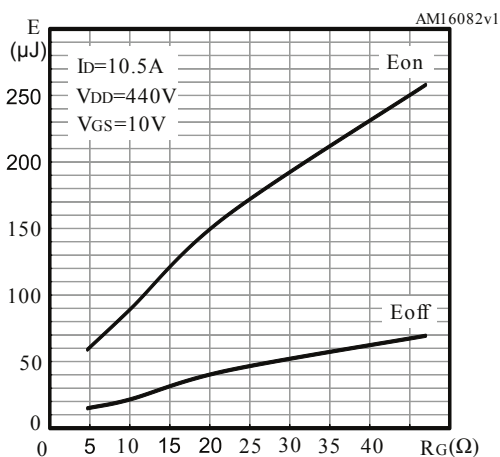
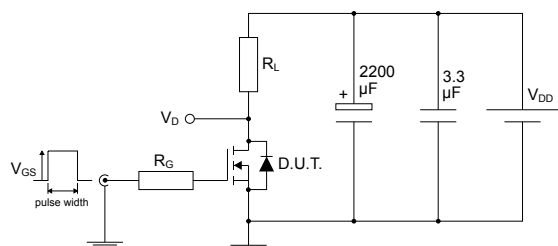
Figure 7. Gate charge vs gate-source voltage

Figure 8. Static drain-source on resistance

Figure 9. Capacitance variations

Figure 10. Output capacitance stored energy

Figure 11. Normalized gate threshold voltage vs temperature

Figure 12. Normalized on-resistance vs temperature


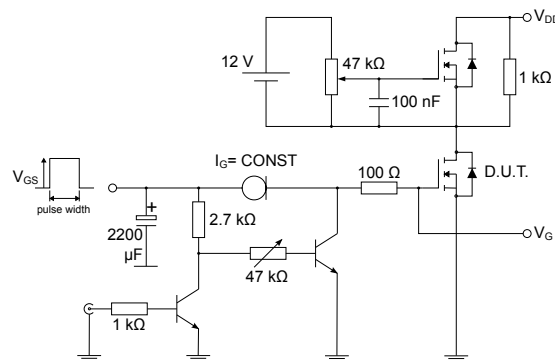
Figure 13. Drain-source diode forward characteristics

Figure 14. Normalized $V_{(BR)DSS}$ vs temperature

Figure 15. Switching energy vs gate resistance


* Eon including reverse recovery of a SiC diode

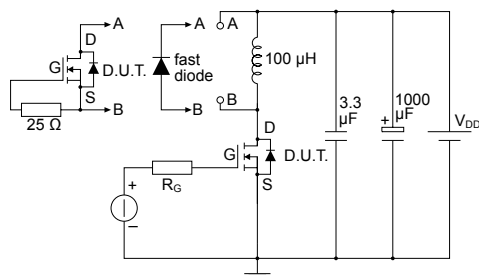
3 Test circuits

Figure 16. Test circuit for resistive load switching times


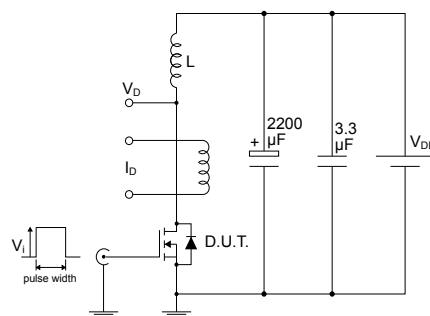
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Figure 17. Test circuit for gate charge behavior


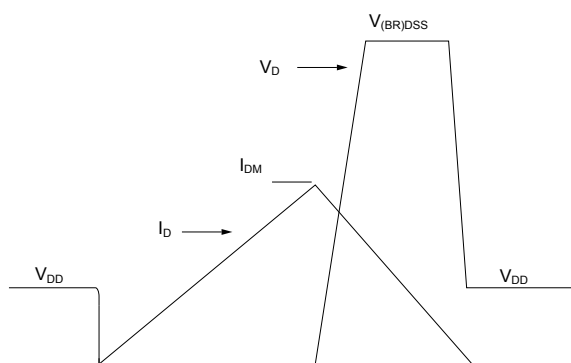
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Figure 18. Test circuit for inductive load switching and diode recovery times


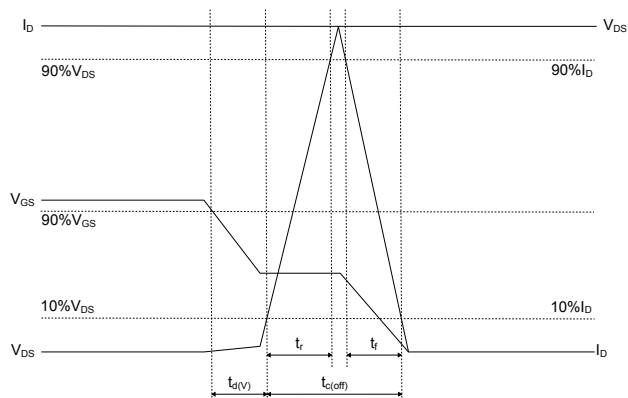
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Figure 19. Unclamped inductive load test circuit


AM01471v1

Figure 20. Unclamped inductive waveform


AM01472v1

Figure 21. Switching time waveform


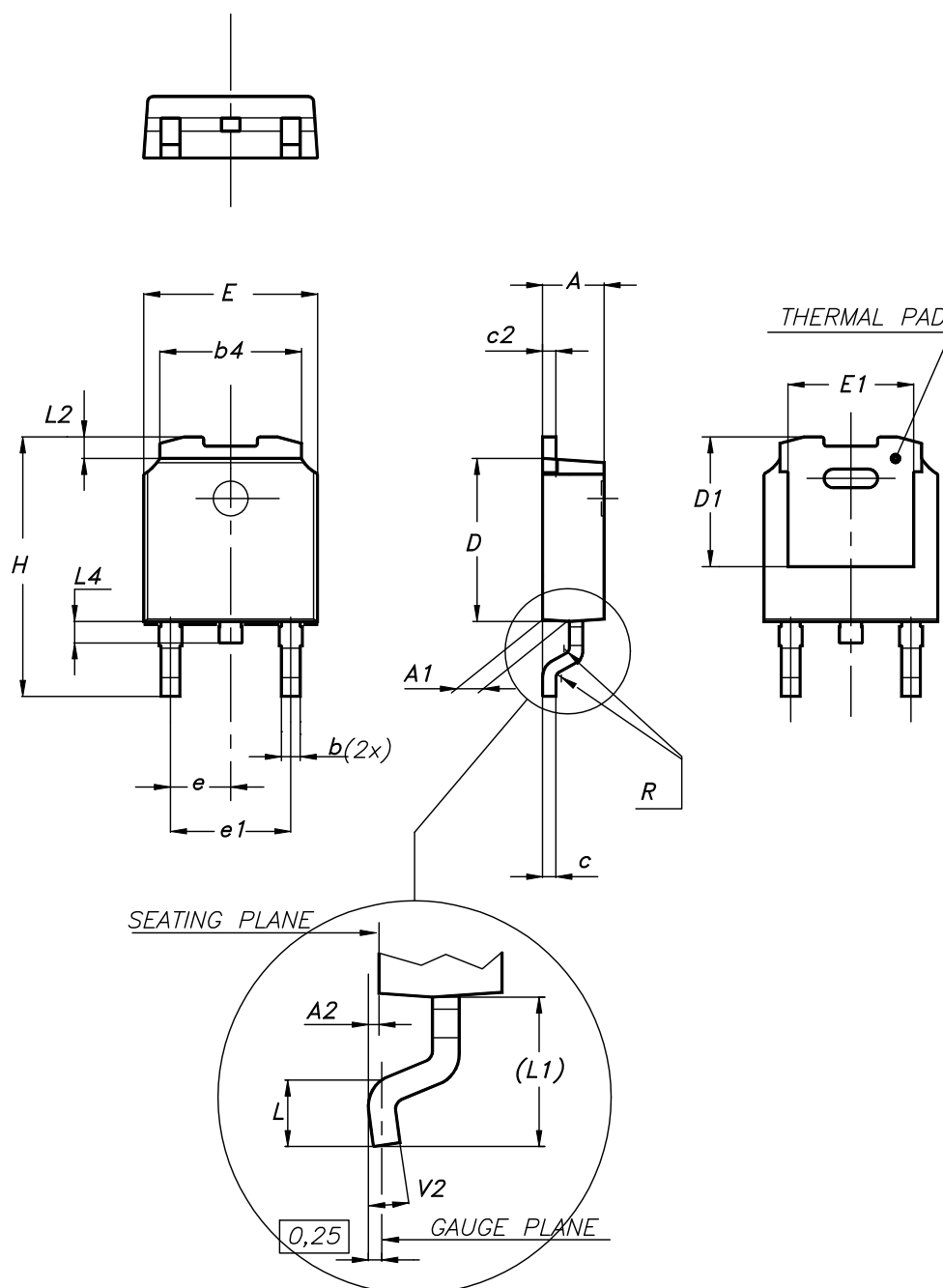
AM05540v2

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 22. DPAK (TO-252) type A2 package outline



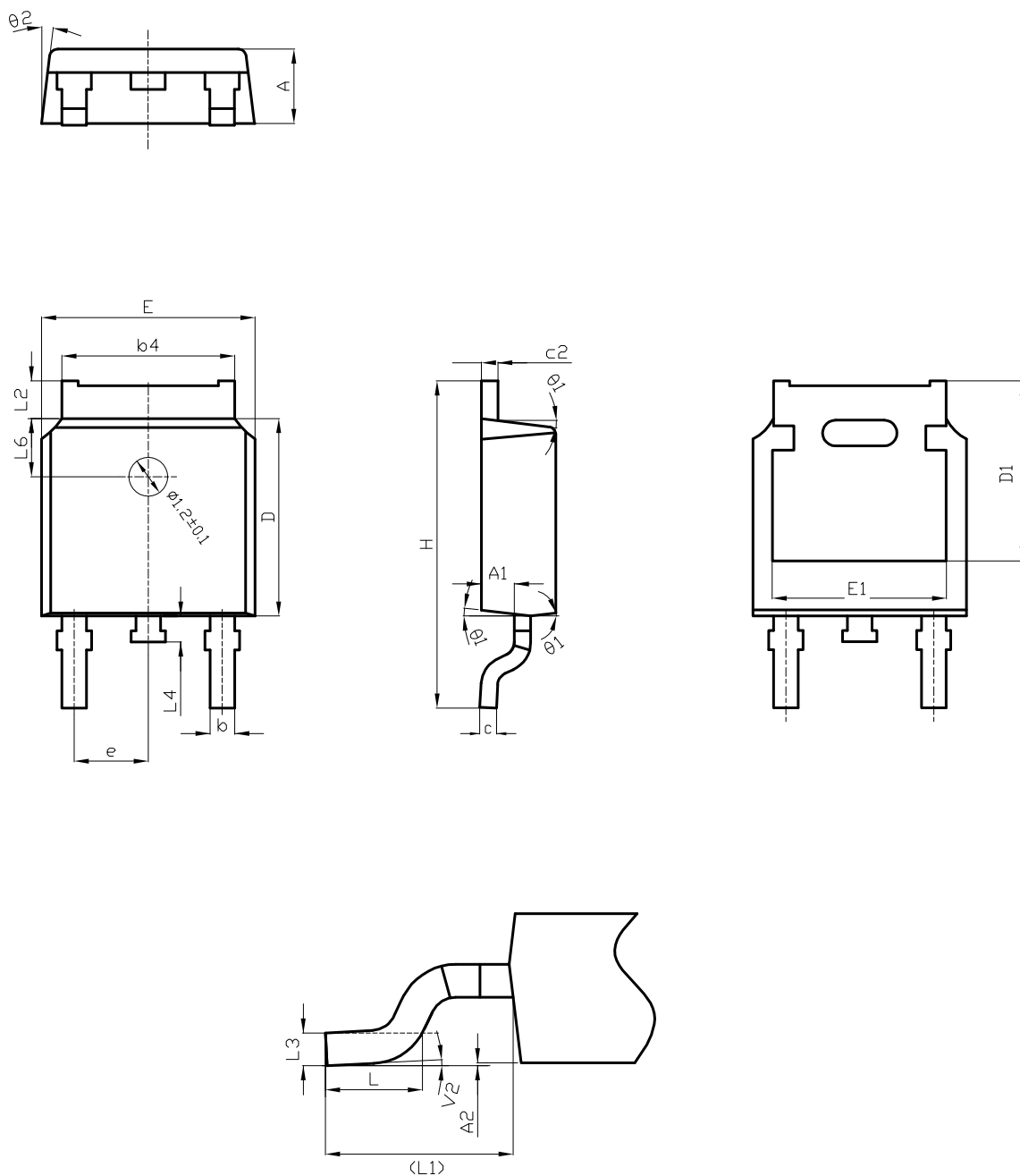
0068772_type-A2_rev30

Table 8. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C2 package information

Figure 23. DPAK (TO-252) type C2 package outline

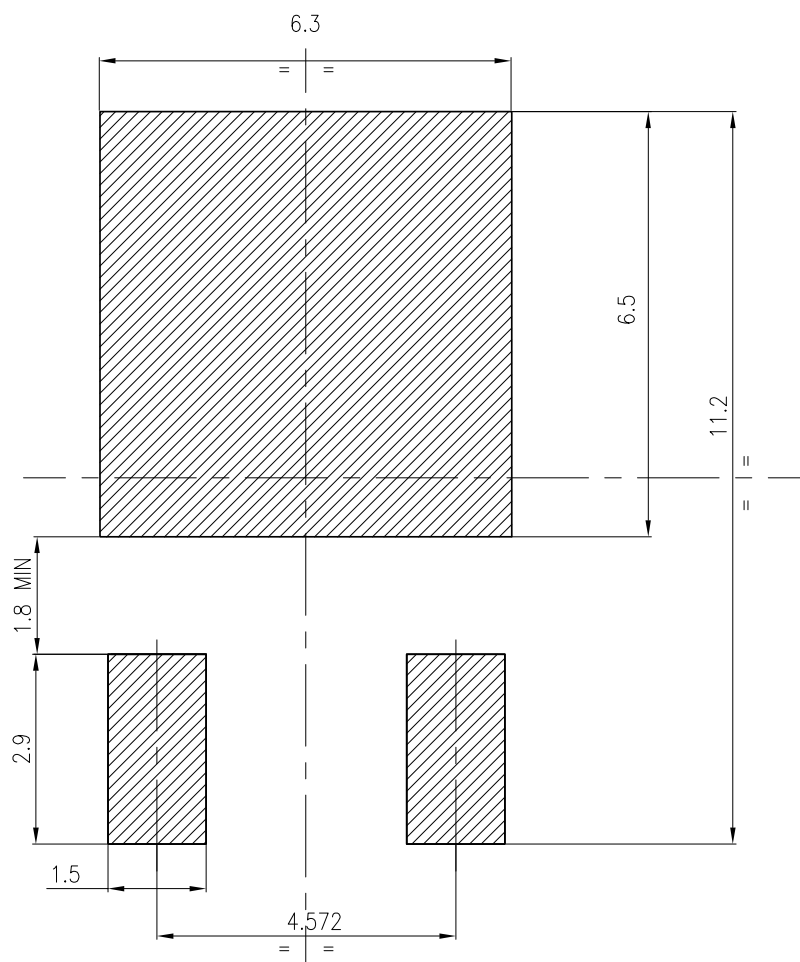


0068772_type-C2_rev30

Table 9. DPAK (TO-252) type C2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

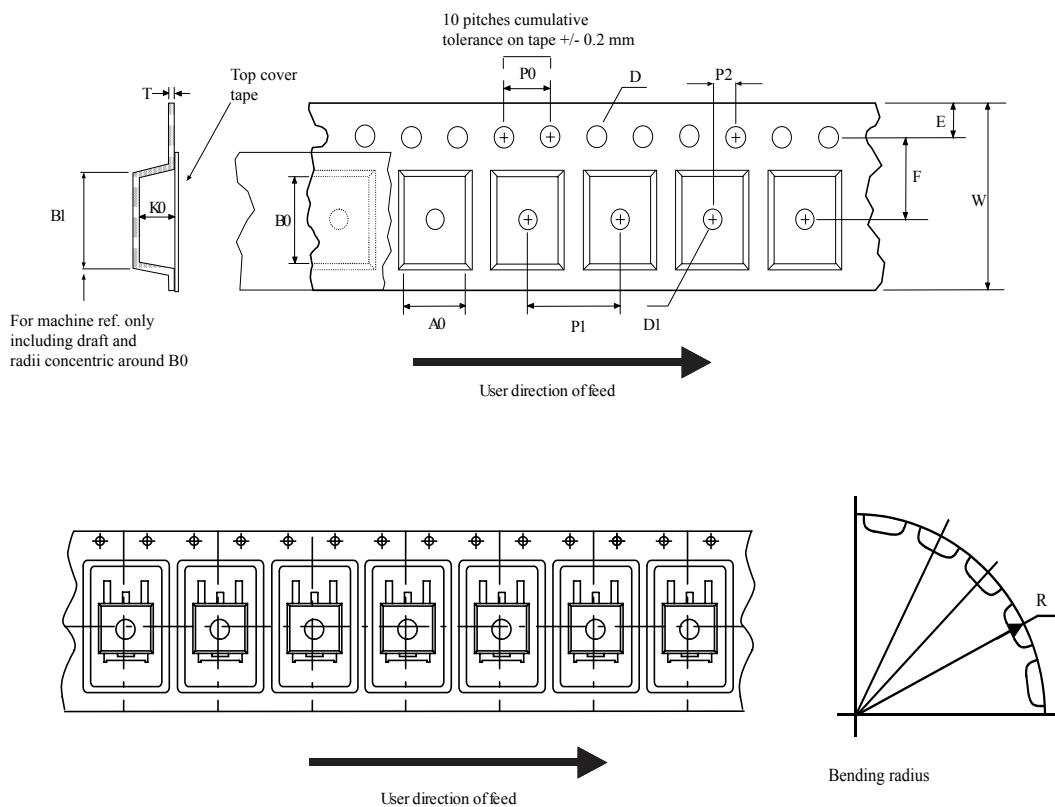
Figure 24. DPAK (TO-252) recommended footprint (dimensions are in mm)



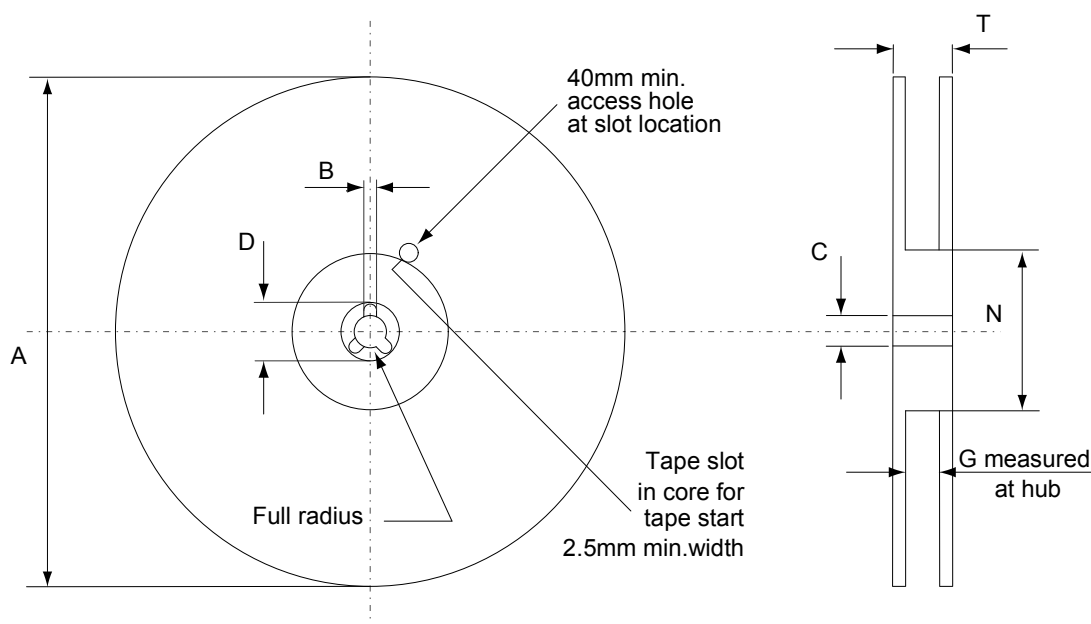
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4.3 DPAK (TO-252) packing information

Figure 25. DPAK (TO-252) tape outline



AM08852v1

Figure 26. DPAK (TO-252) reel outline


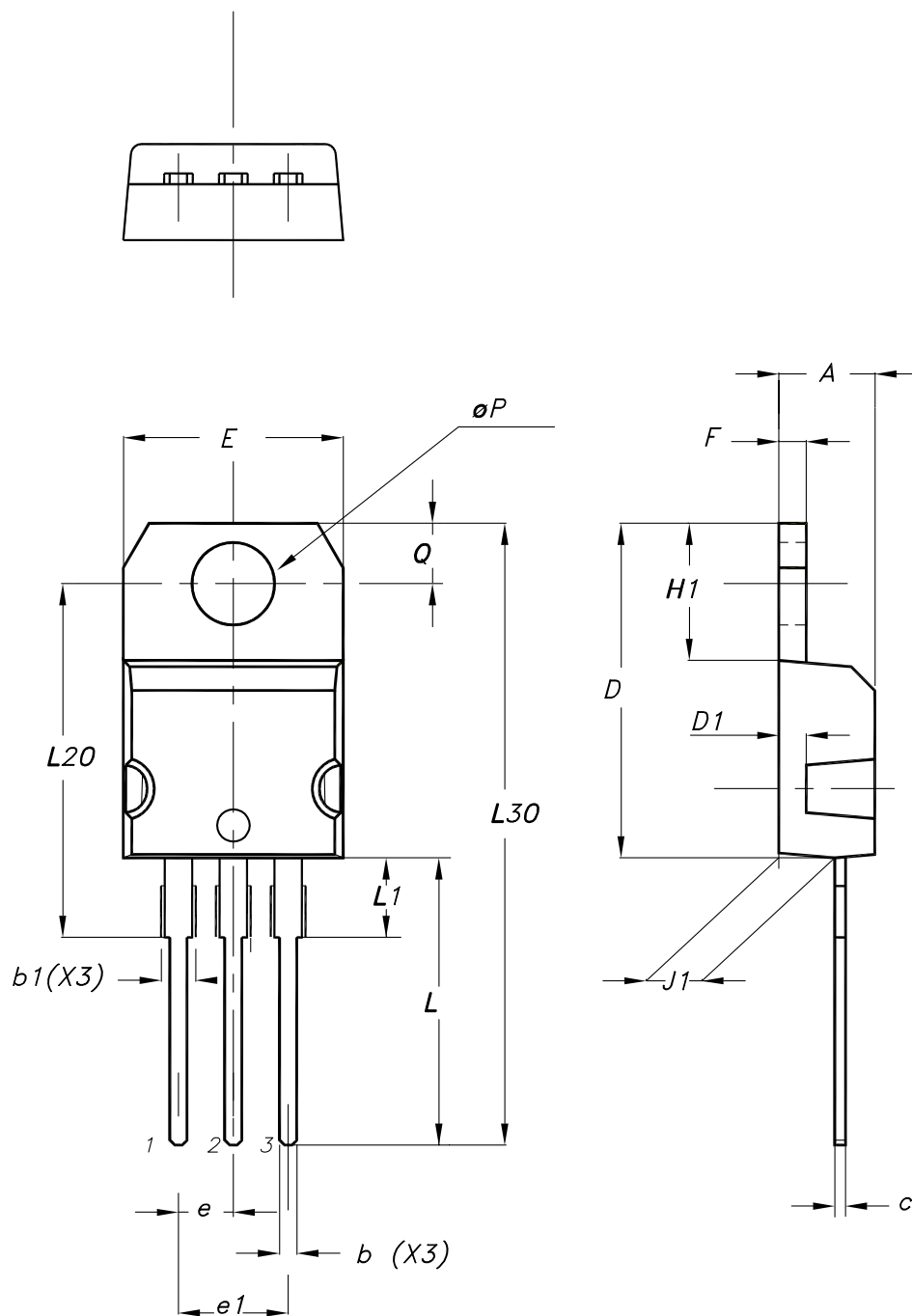
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Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.4 TO-220 type A package information

Figure 27. TO-220 type A package outline



0015988_typeA_Rev_23

Table 11. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

5 Ordering information

Table 12. Order codes

Order code	Marking	Package	Packing
STD18N55M5	18N55M5	DPAK	Tape and reel
STP18N55M5		TO-220	Tube

Revision history

Table 13. Document revision history

Date	Version	Changes
09-Feb-2010	1	First release.
04-Mar-2011	2	– Document status promoted from preliminary data to datasheet; – Added new package, mechanical data: D²PAK.
22-Nov-2013	3	– Updated: title on the cover page and RDS(on) values. – Modified: EAS value and note 3 in Table 2 – Modified: RDS(on) value in Table 4, typical values in Table 5 and 7 – Updated: the entire Table 5 – Added: Section 2.1: Electrical characteristics (curves) – Updated: Section 4: Package mechanical data and Section 5: Packaging mechanical data – Updated: Figure 11 and 18 – Minor text changes.
03-Aug-2018	4	The part numbers STB18N55M5 and STF18N55M5 have been moved to a separate datasheet. Removed maturity status indication from cover page. The document status is production data. Updated title in cover page, Section 1 Electrical ratings, Section 2 Electrical characteristics and Section 4 Package information. Minor text changes.
24-Mar-2020	5	Updated title on Figure 12. Normalized gate threshold voltage vs temperature and Figure 13. Normalized on-resistance vs temperature. Updated Section 4 Package information. Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics curves	5
3	Test circuits	8
4	Package information	9
4.1	DPAK (TO-252) type A2 package information	9
4.2	DPAK (TO-252) type C2 package information	11
4.3	DPAK (TO-252) packing information	14
4.4	TO-220 type A package information	16
5	Ordering information	18
	Revision history	19

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