

P-channel 100 V, 0.136 Ω typ., 10 A STripFET™ F6 Power MOSFET in a DPAK package

Datasheet - production data

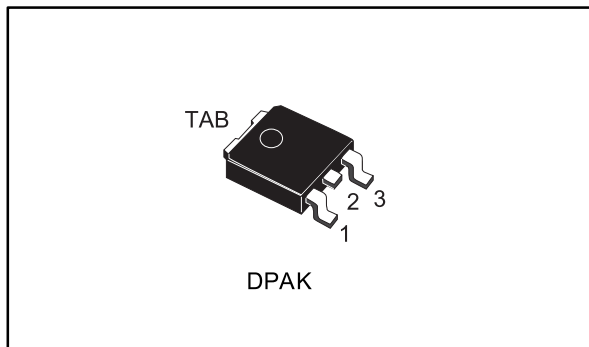
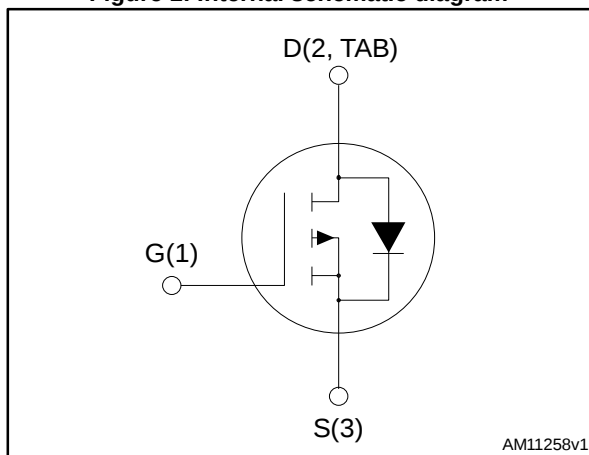


Figure 1: Internal schematic diagram



Features

Order code	V _{DSS}	R _{DS(on)} max	I _D
STD10P10F6	100 V	0.18 Ω	10 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STD10P10F6	10P10F6	DPAK	Tape and reel



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	10	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	7.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	40	W
T_{stg}	Storage temperature	-55 to 175	$^{\circ}\text{C}$
T_j	Max. operating junction temperature	175	$^{\circ}\text{C}$

Notes:

⁽¹⁾Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	3.75	$^{\circ}\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	50	$^{\circ}\text{C/W}$

Notes:

⁽¹⁾When mounted on 1 inch² FR-4, 2 Oz copper board



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown Voltage	V _{GS} = 0, I _D = 250 μA	100			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0, V _{DS} = 100 V			1	μA
		V _{GS} = 0, V _{DS} = 100 V, T _C = 125 °C			10	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0, V _{GS} = ± 20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 5 A		0.136	0.18	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 80 V, f = 1 MHz, V _{GS} = 0	-	864	-	pF
C _{oss}	Output capacitance		-	45	-	pF
C _{rss}	Reverse transfer capacitance		-	25	-	pF
Q _g	Total gate charge	V _{DD} = 80 V, I _D = 10 A V _{GS} = 10 V	-	16.5	-	nC
Q _{gs}	Gate-source charge		-	3.5	-	nC
Q _{gd}	Gate-drain charge		-	3.8	-	nC

Table 6: Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 80 V, I _D = 5 A, R _G = 4.7 Ω, V _{GS} = 10 V	-	10.5	-	ns
t _r	Rise time		-	4.8	-	ns
t _{d(off)}	Turn-off delay time		-	24	-	ns
t _f	Fall time		-	4.5	-	ns



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 5\text{ A}$, $V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 80\text{ V}$	-	26.5		ns
Q_{rr}	Reverse recovery charge		-	36.5		nC
I_{RRM}	Reverse recovery current		-	2.7		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

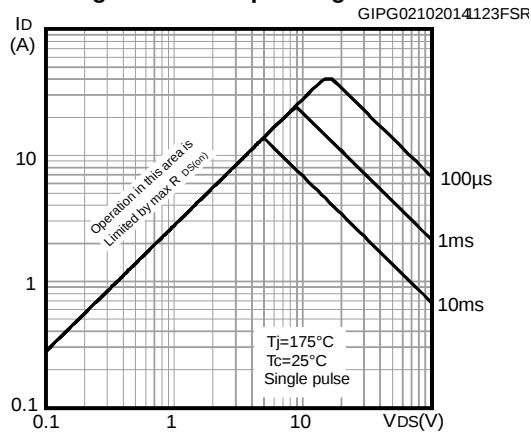


Figure 3: Thermal impedance

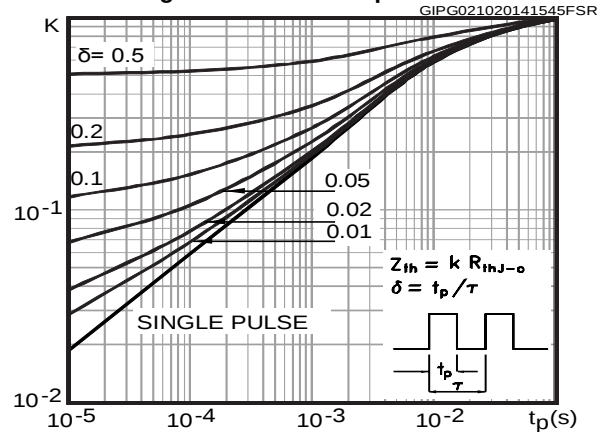


Figure 4: Output characteristics

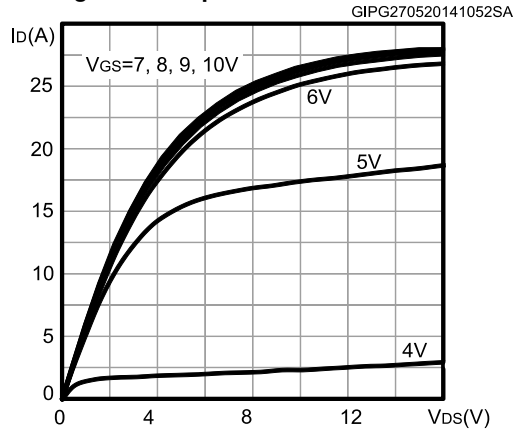


Figure 5: Transfer characteristics

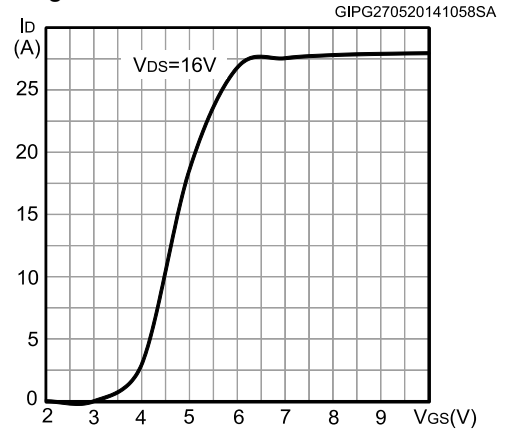


Figure 6: Gate charge vs gate-source voltage



Figure 7: Static drain-source on-resistance

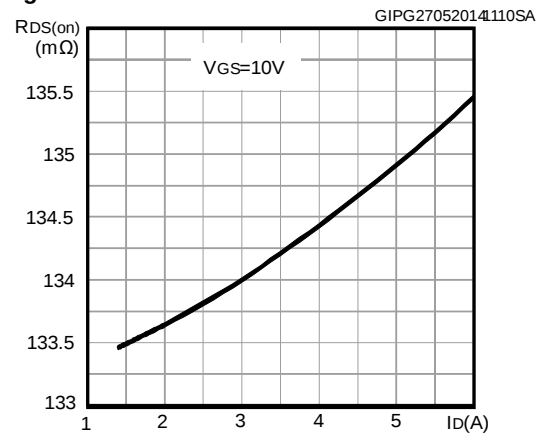


Figure 8: Capacitance variations

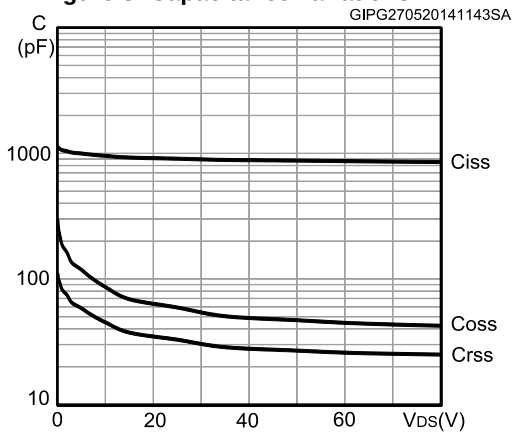


Figure 9: Normalized gate threshold voltage vs temperature

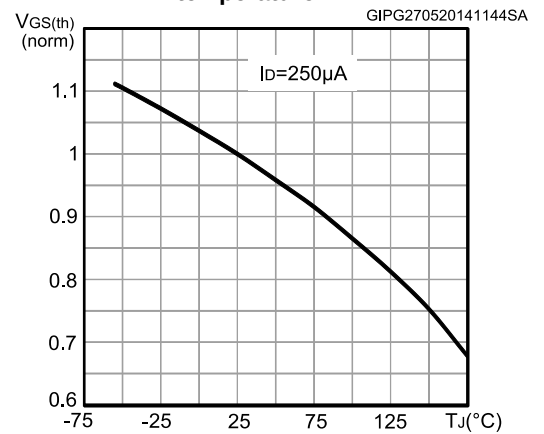


Figure 10: Normalized on-resistance

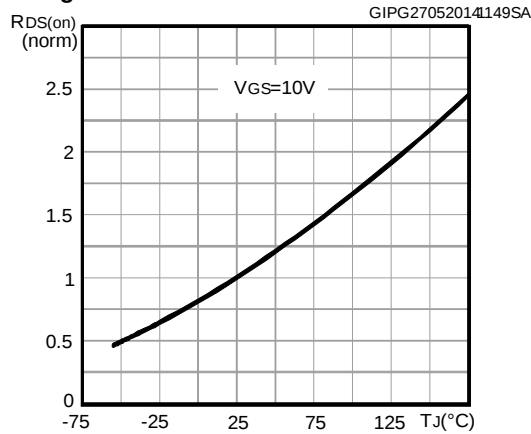


Figure 11: Normalized V(BR)DSS vs temperature

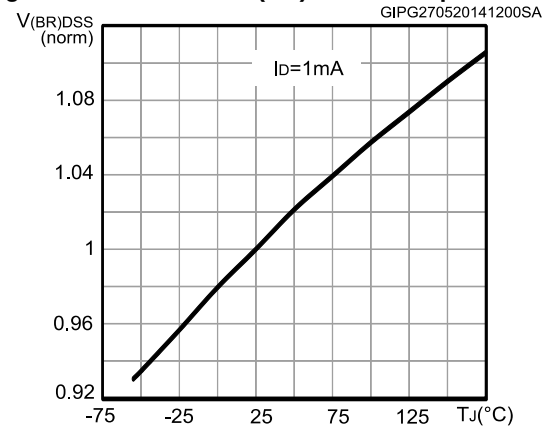
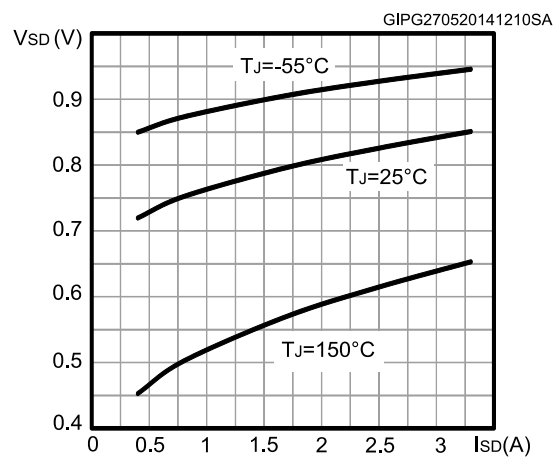


Figure 12: Source-drain diode forward characteristics

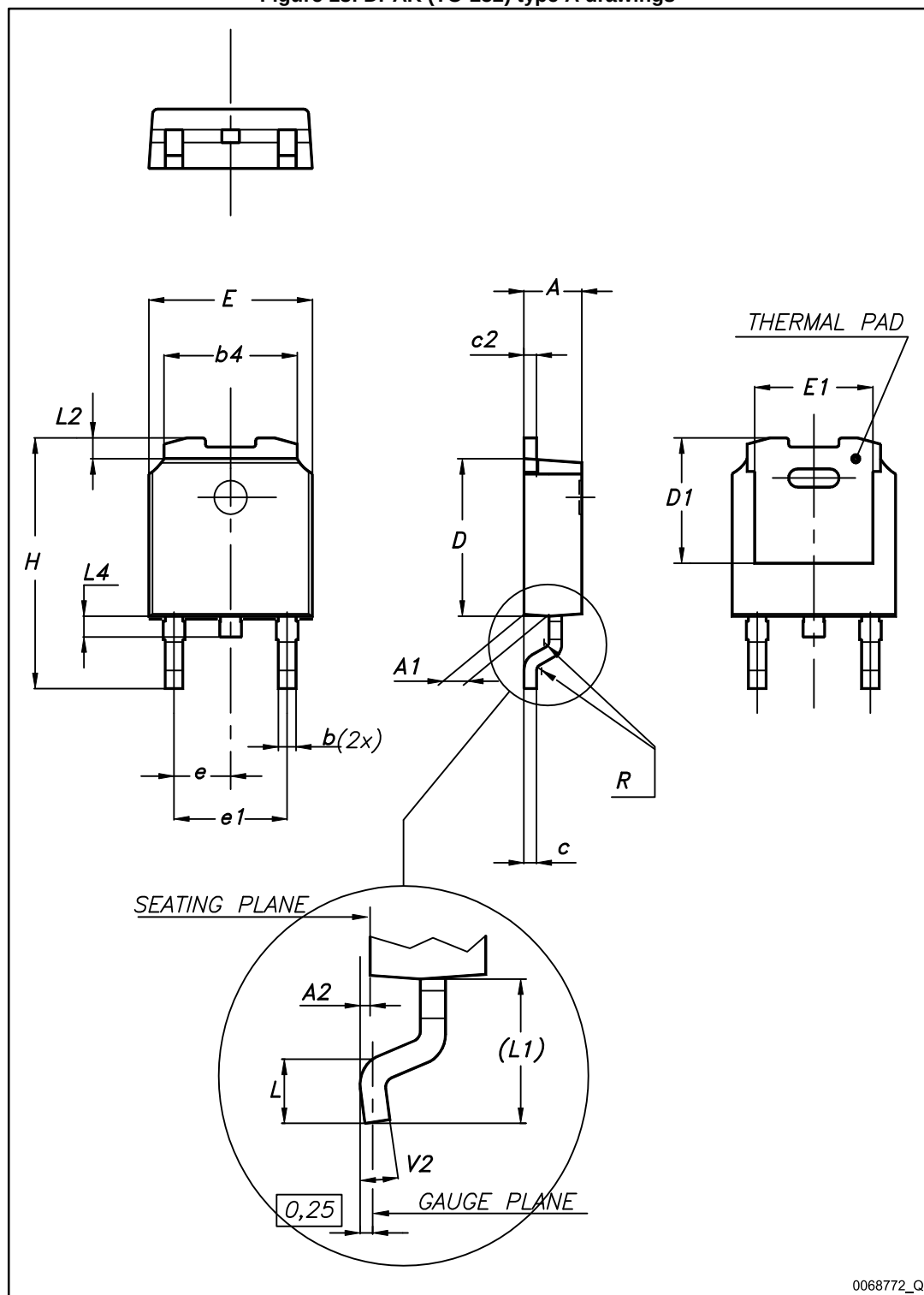


3 **Package mechanical data**

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**.
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3.1 DPAK (TO-252) type A mechanical data

Figure 13: DPAK (TO-252) type A drawings

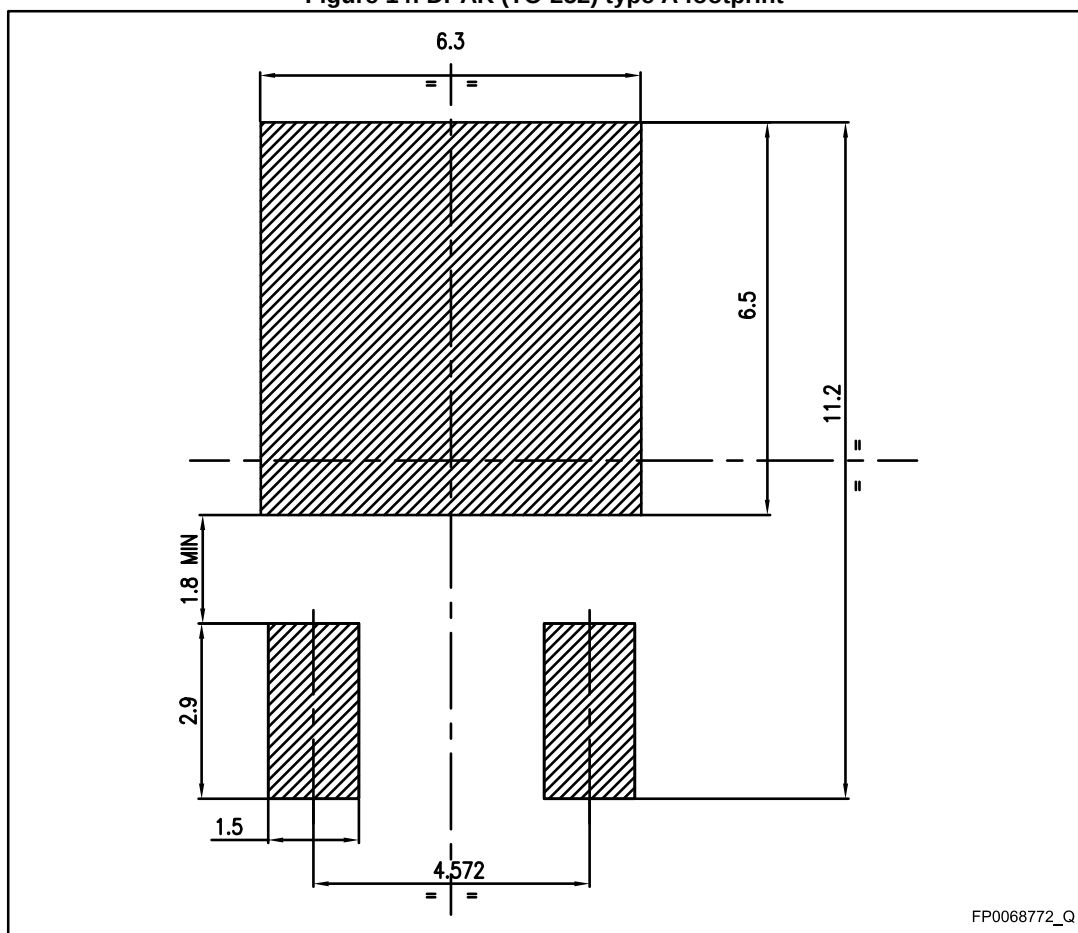


0068772_Q

Table 8: DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 14: DPAK (TO-252) type A footprint



All dimensions are in mm

4 DPAK (TO-252) tape and reel mechanical data

Figure 15: Tape for DPAK (TO-252)

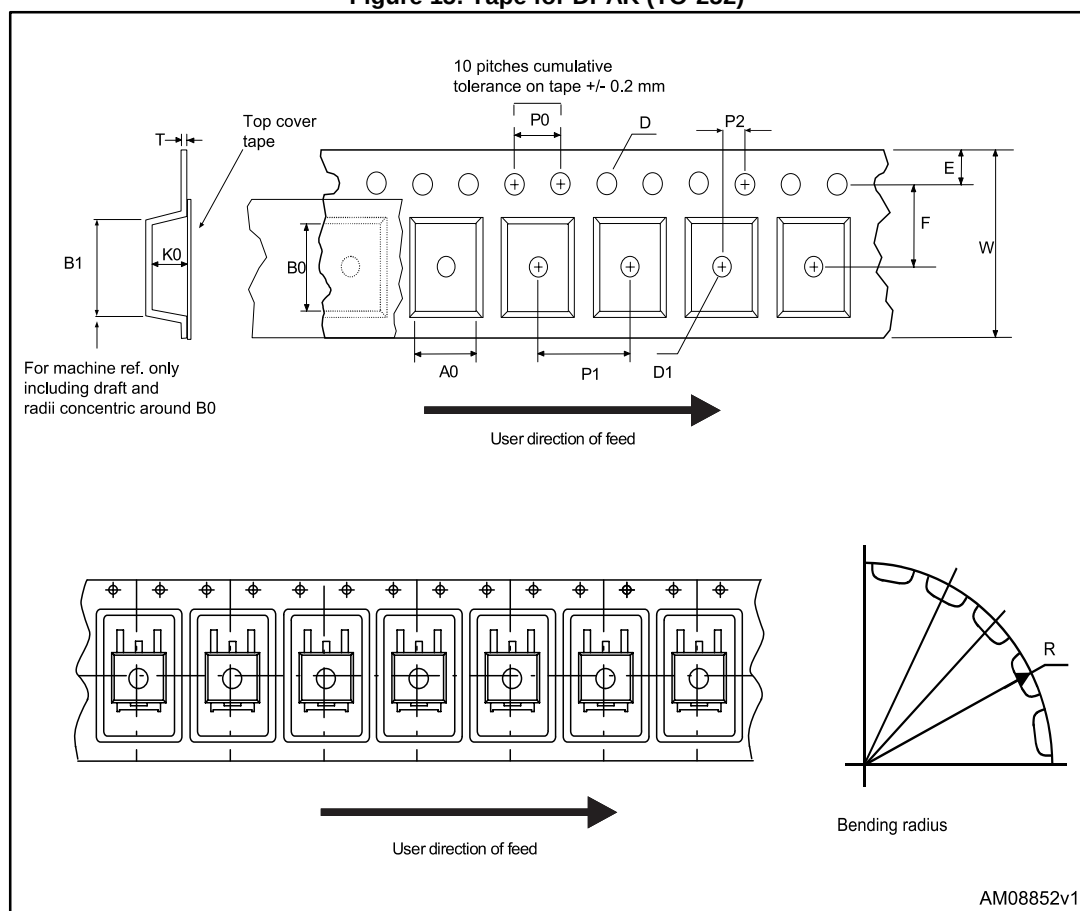


Figure 16: Reel for DPAK (TO-252)

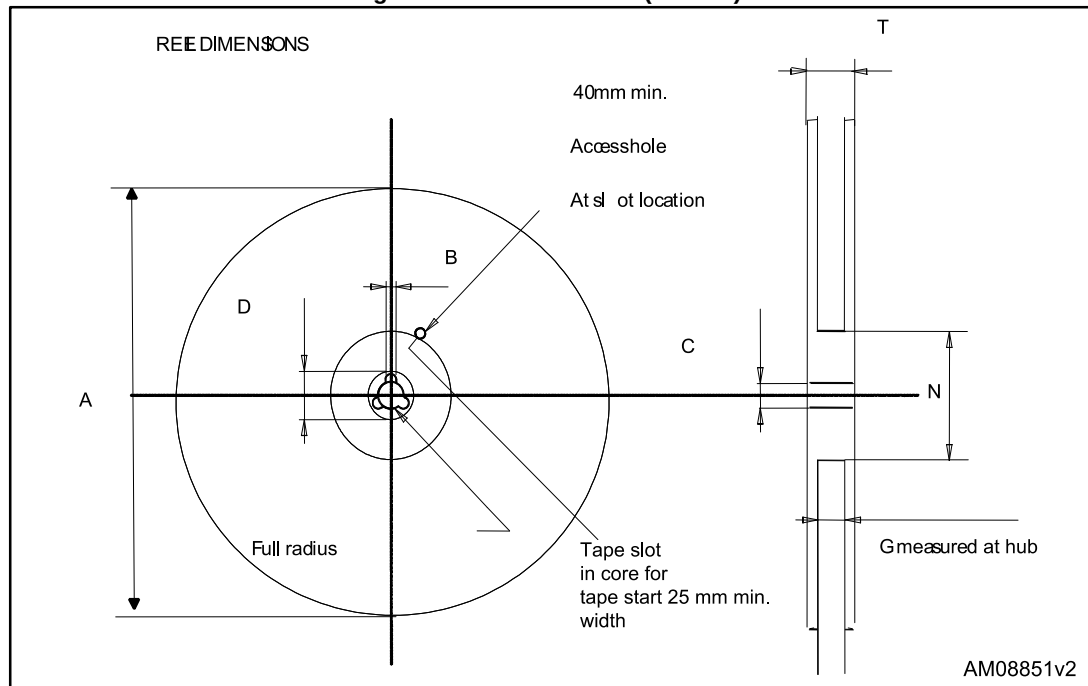


Table 9: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
20-May-2014	1	First release.
02-Oct-2014	2	Document status promoted from preliminary to production data Added Section 2.1: "Electrical characteristics (curves)" .

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