

N-channel 800 V, 0.23 Ω typ., 16 A MDmesh™ K5 Power MOSFET in a D²PAK package

Datasheet - production data

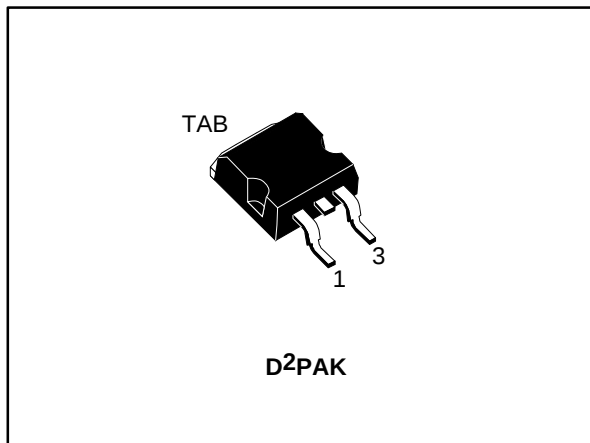
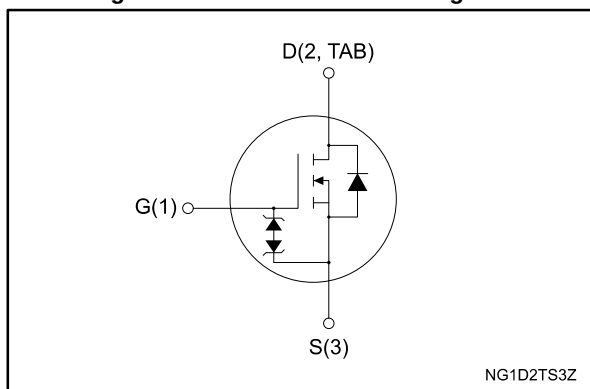


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STB23N80K5	800 V	0.28 Ω	16 A	190 W

- Industry's lowest R_{DS(on)} x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STB23N80K5	23N80K5	D ² PAK	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	16	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	10	
$I_{DM}^{(1)}$	Drain current (pulsed)	64	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	190	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature		

Notes:

(1) Pulse width is limited by safe operating area.

(2) $I_{SD} \leq 16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

(3) $V_{DS} \leq 640\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.66	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient	30	

Notes:

(1) When mounted on a 1-inch² FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	5	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	400	mJ

Notes:

(1) Pulse width limited by T_{jmax} .

(2) starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	800			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 800\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 800\text{ V}$, $T_{\text{case}} = 125\text{ }^{\circ}\text{C}$			50	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 20\text{ V}$			± 10	μA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 8\text{ A}$		0.23	0.28	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	1000	-	pF
C_{oss}	Output capacitance		-	65	-	
C_{rss}	Reverse transfer capacitance		-	1.5	-	
$C_{\text{O(tr)}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }640\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	165	-	pF
$C_{\text{O(er)}}^{(2)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }640\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	59	-	
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	4.7	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 640\text{ V}$, $I_{\text{D}} = 16\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	33	-	nC
Q_{gs}	Gate-source charge		-	6	-	
Q_{gd}	Gate-drain charge		-	25	-	

Notes:

⁽¹⁾ Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

⁽²⁾ Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 400\text{ V}$, $I_{\text{D}} = 8\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	14	-	ns
t_{r}	Rise time		-	9	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	48	-	
t_{f}	Fall time		-	9	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		16	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		64	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 16\text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15 : "Test circuit for inductive load switching and diode recovery times")	-	410		ns
Q_{rr}	Reverse recovery charge		-	7		μC
I_{RRM}	Reverse recovery current		-	34		A
t_{rr}	Reverse recovery time	$I_{SD} = 16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15 : "Test circuit for inductive load switching and diode recovery times")	-	650		ns
Q_{rr}	Reverse recovery charge		-	10		μC
I_{RRM}	Reverse recovery current		-	32		A

Notes:

⁽¹⁾ Pulse width is limited by safe operating area.

⁽²⁾ Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	± 30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

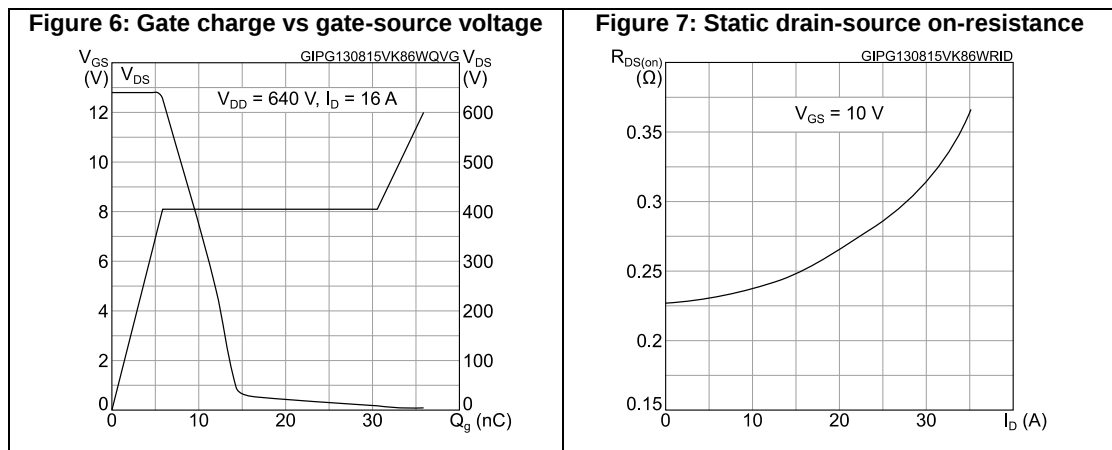
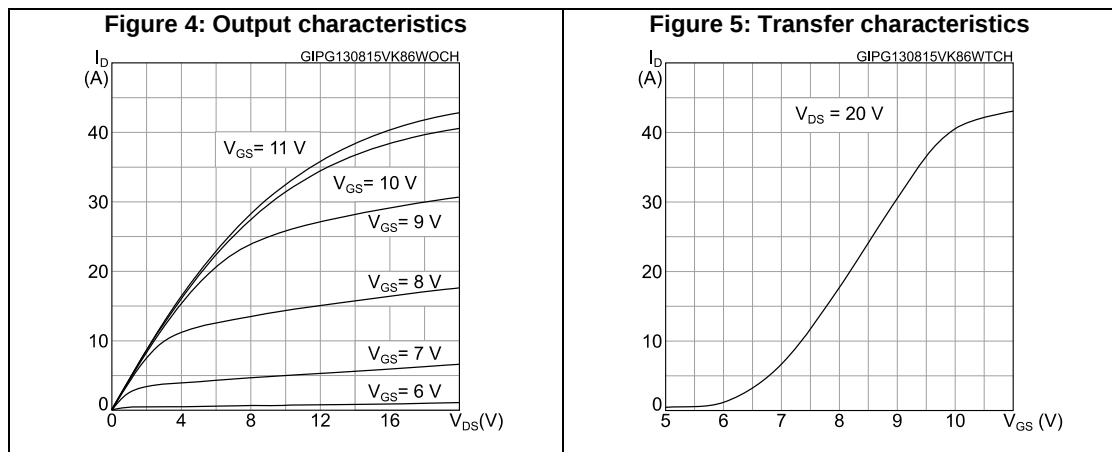
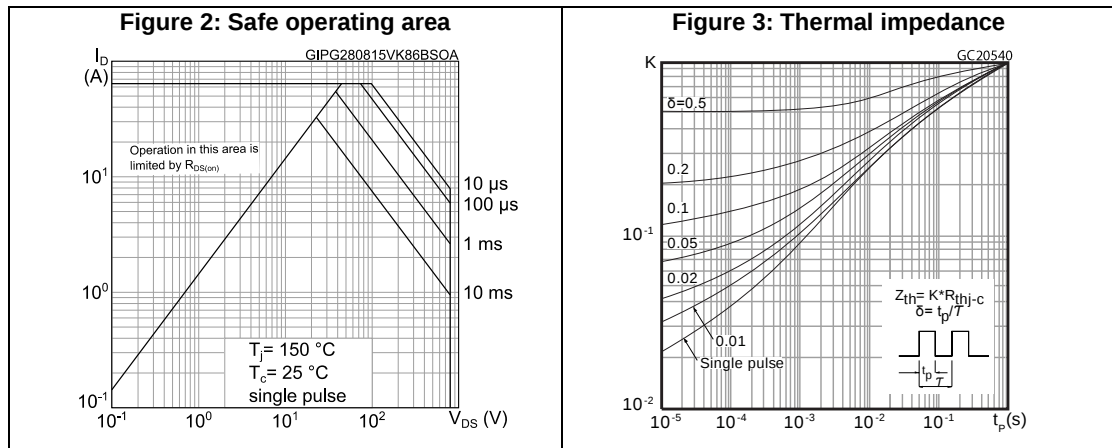


Figure 8: Capacitance variations

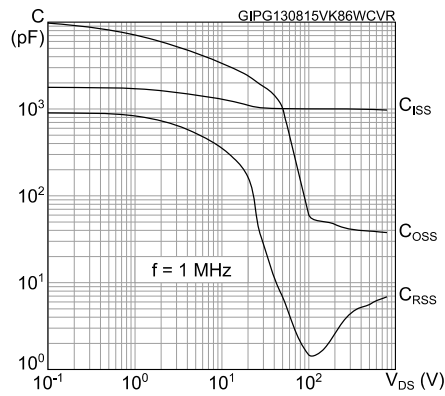


Figure 9: Normalized gate threshold voltage vs temperature

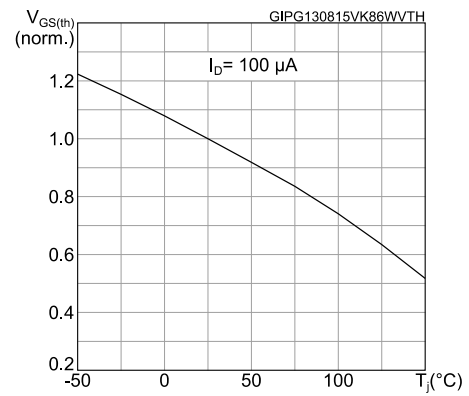


Figure 10: Normalized on-resistance vs temperature

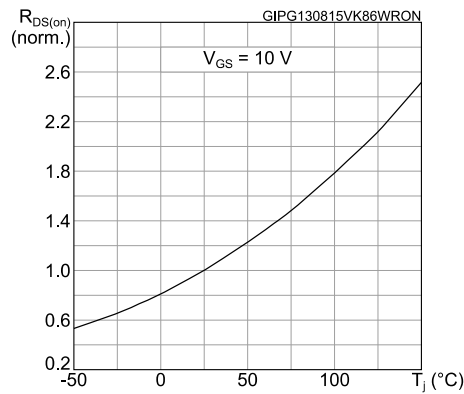


Figure 11: Normalized V(BR)DSS vs temperature

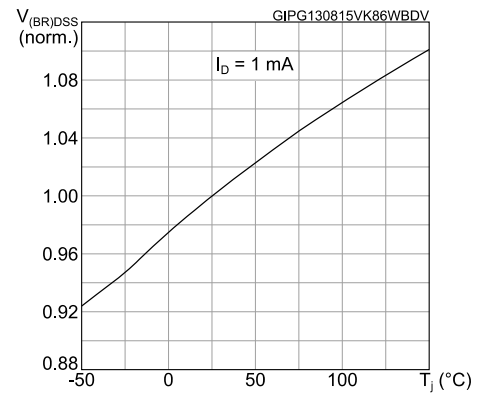
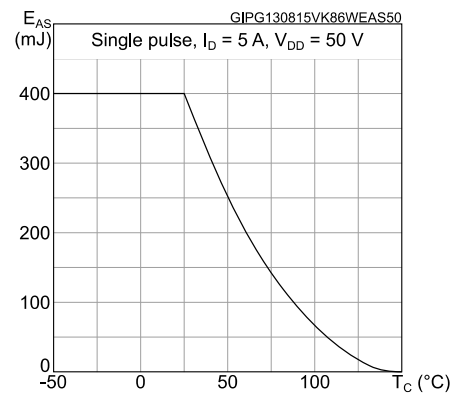


Figure 12: Maximum avalanche energy vs temperature



3 Test circuits

Figure 13: Test circuit for resistive load switching times

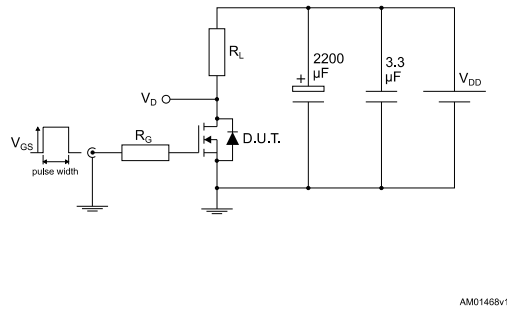


Figure 14: Test circuit for gate charge behavior

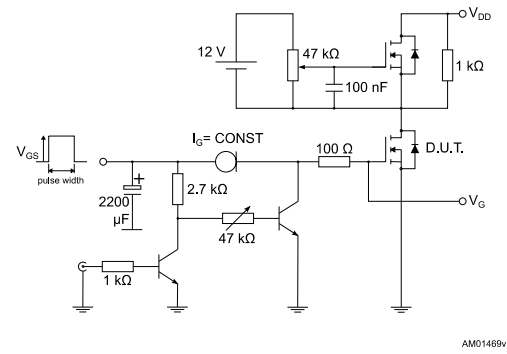


Figure 15: Test circuit for inductive load switching and diode recovery times

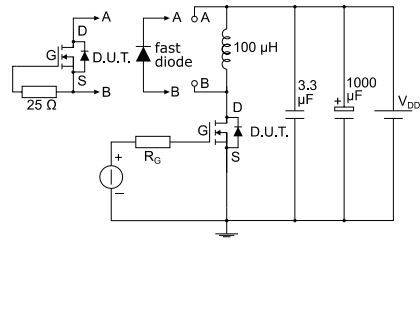


Figure 16: Unclamped inductive load test circuit

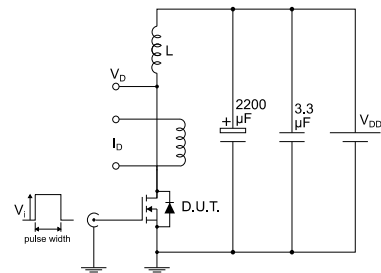


Figure 17: Unclamped inductive waveform

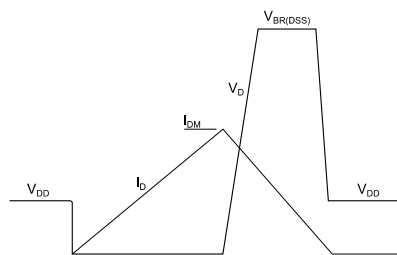
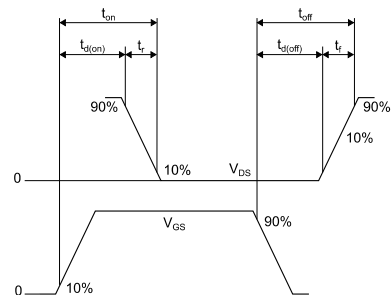


Figure 18: Switching time waveform

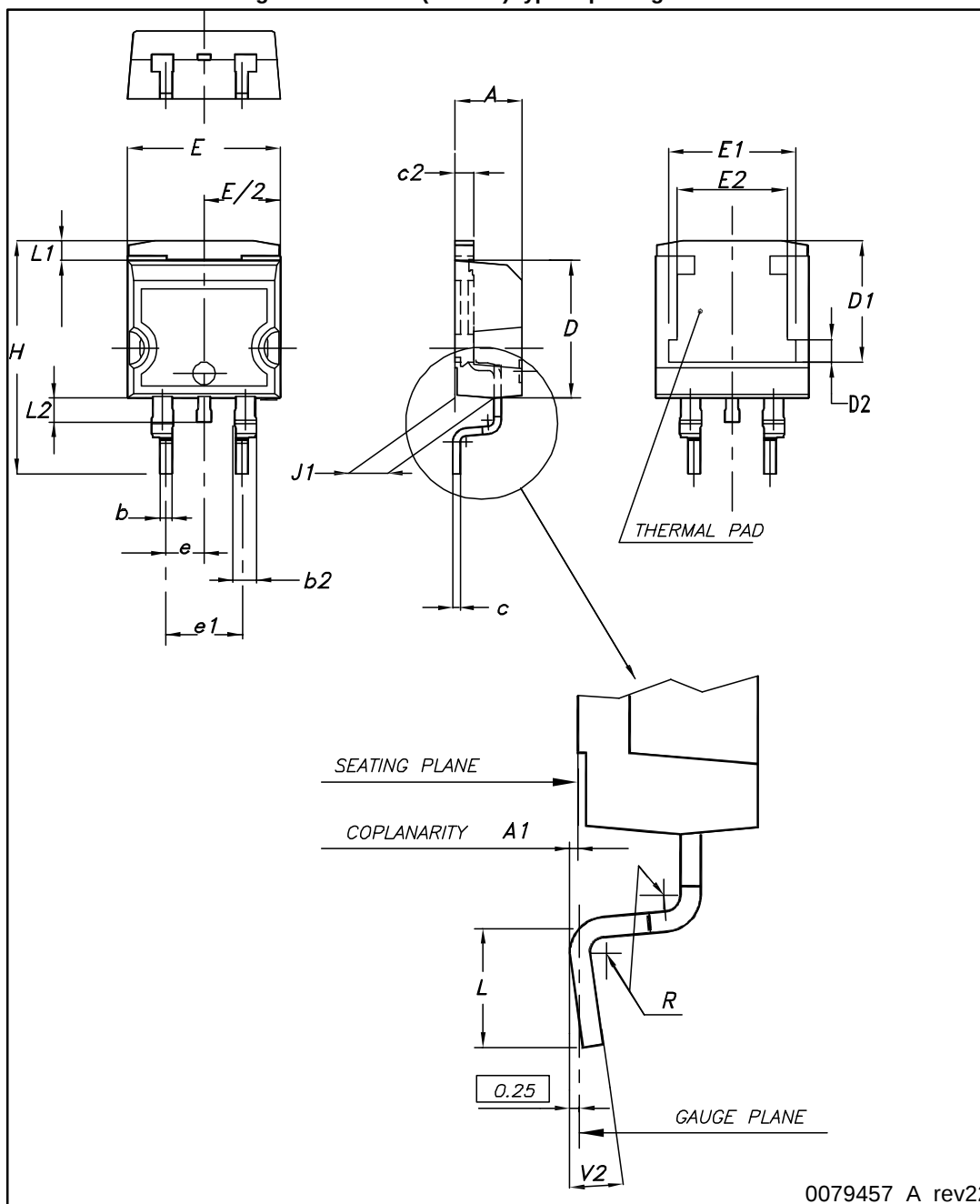


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A package information

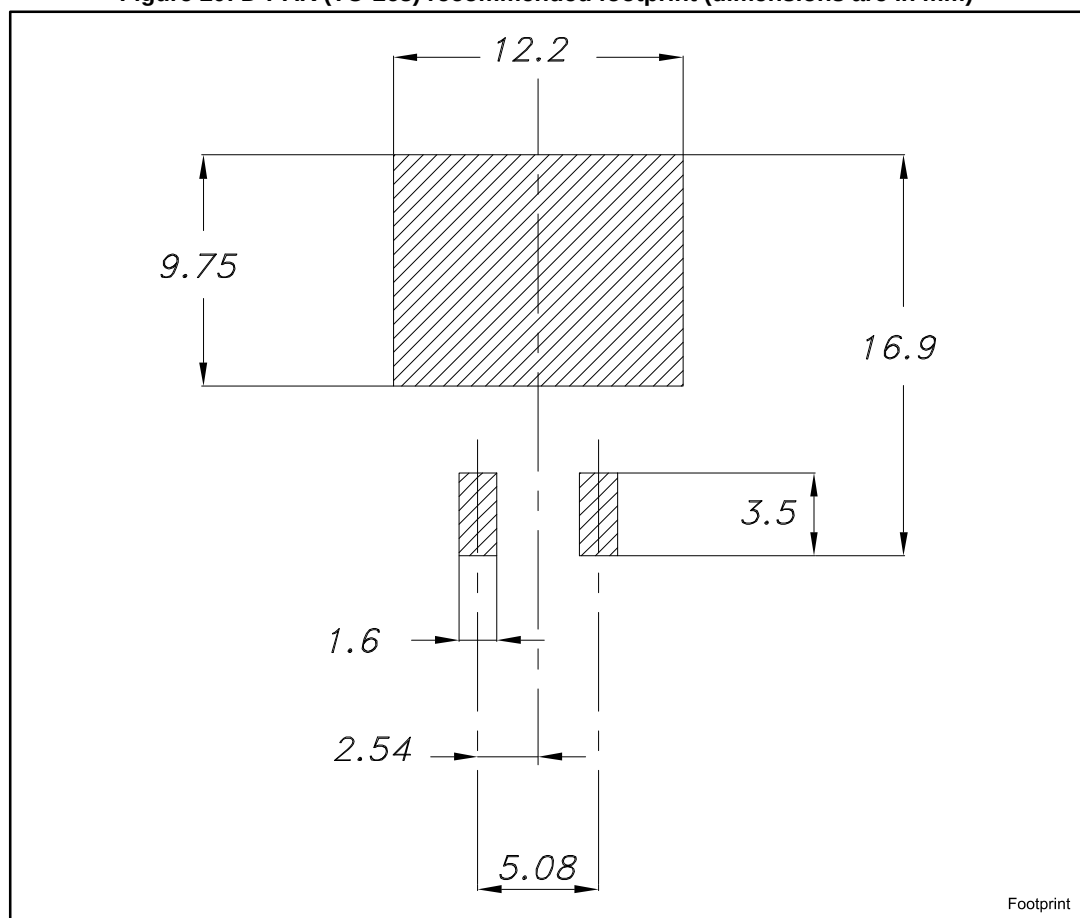
Figure 19: D²PAK (TO-263) type A package outline



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Table 10: D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 20: D²PAK (TO-263) recommended footprint (dimensions are in mm)

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10 pitches cumulative
tolerance on tape +/- 0.2 mm

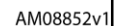
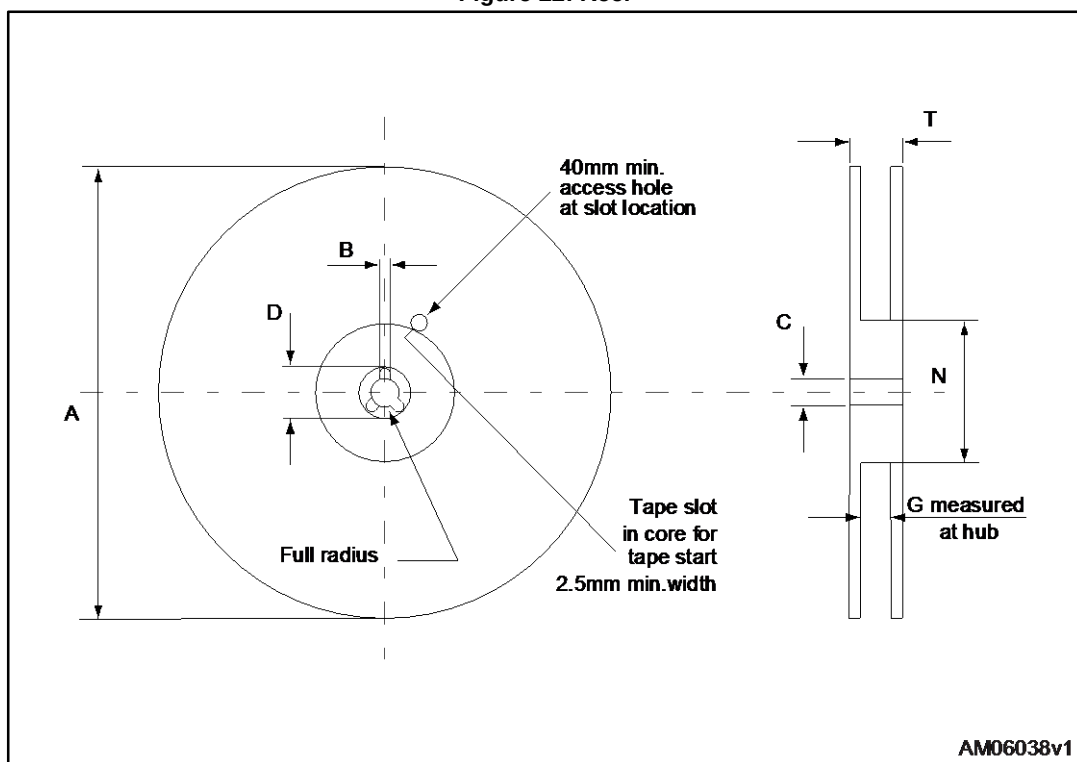


Figure 22: Reel

Table 11: D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 12: Document revision history

Date	Revision	Changes
28-Aug-2015	1	First release.

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