

N-channel 60 V, 4.2 mΩ typ., 80 A STripFET™ F7 Power MOSFET in a D²PAK package

Datasheet - production data

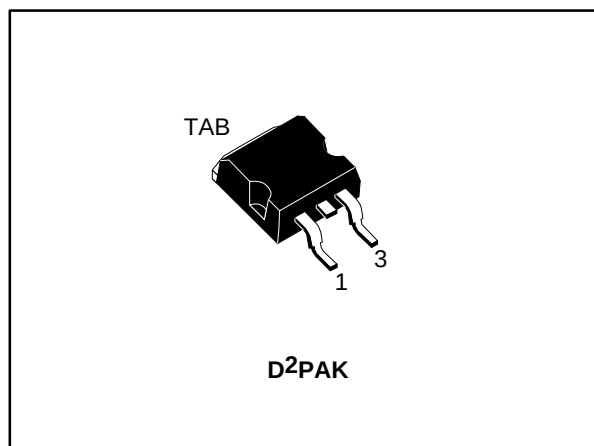
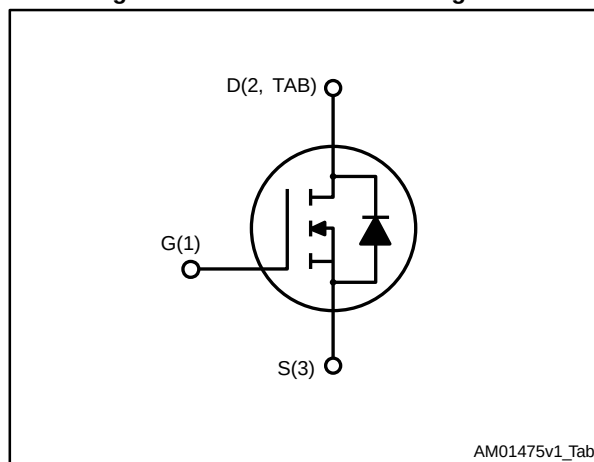


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STB130N6F7	60 V	5.0 mΩ	80 A	160 W

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STB130N6F7	130N6F7	D ² PAK	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	80	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	80	
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	160	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	200	mJ
T_{stg}	Storage temperature	-55 to 175	$^{\circ}\text{C}$
T_j	Operating junction temperature		

Notes:

⁽¹⁾ Current is limited by package.

⁽²⁾ Pulse width is limited by safe operating area.

⁽³⁾ starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = 20\text{ A}$, $V_{DD} = 40\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.94	$^{\circ}\text{C/W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient	35	

Notes:

⁽¹⁾ When mounted on a 1-inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	60			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 60\text{ V}$			1	μA
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = 20\text{ V}$			100	nA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	2		4	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 40\text{ A}$		4.2	5.0	m Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	2600	-	pF
C_{oss}	Output capacitance		-	1200	-	
C_{rss}	Reverse transfer capacitance		-	115	-	
Q_{g}	Total gate charge	$V_{\text{DD}} = 30\text{ V}$, $I_{\text{D}} = 80\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	42	-	nC
Q_{gs}	Gate-source charge		-	13.6	-	
Q_{gd}	Gate-drain charge		-	13	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 30\text{ V}$, $I_{\text{D}} = 40\text{ A}$, $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	24	-	ns
t_{r}	Rise time		-	44	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	62	-	
t_{f}	Fall time		-	24	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{\text{SD}}^{(1)}$	Forward on voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{SD}} = 80\text{ A}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{\text{SD}} = 80\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{\text{DD}} = 48\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	50		ns
Q_{rr}	Reverse recovery charge		-	56		nC
I_{RRM}	Reverse recovery current		-	2.2		A

Notes:

(1) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

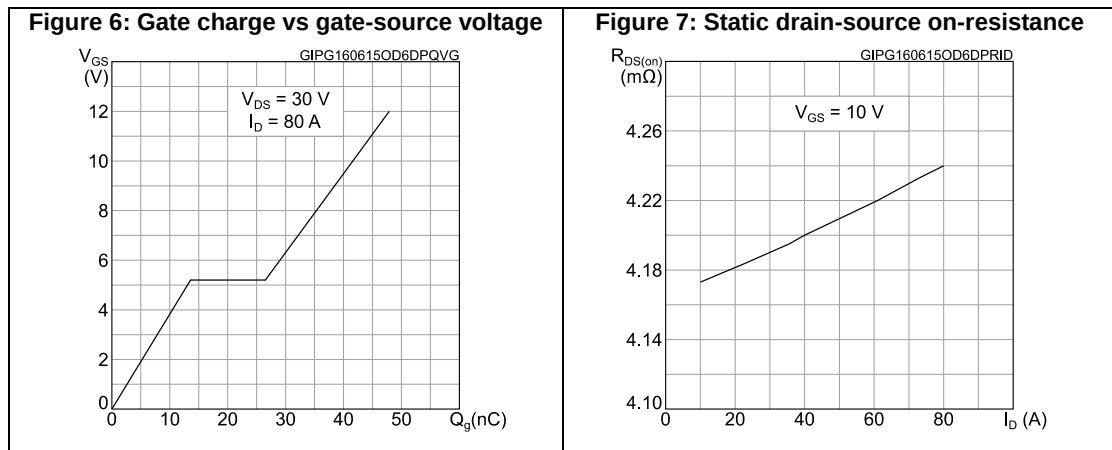
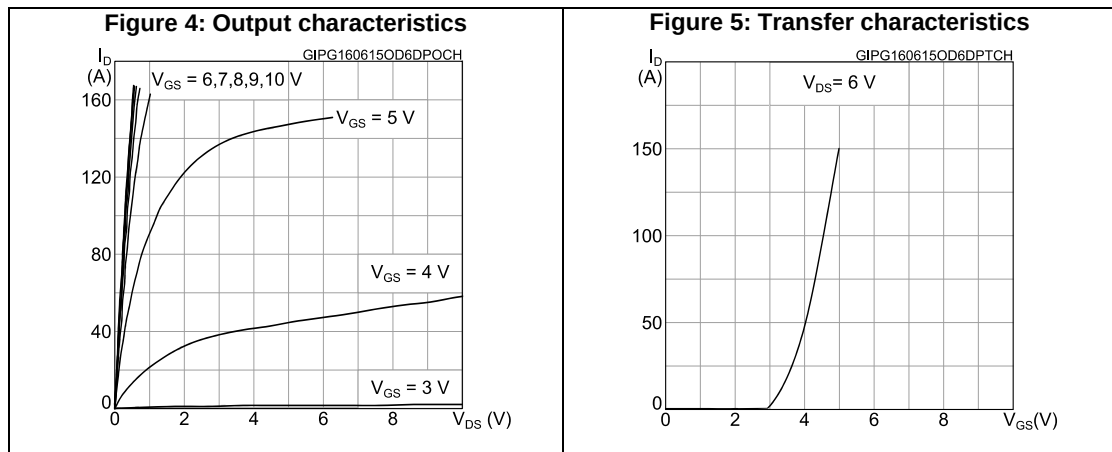
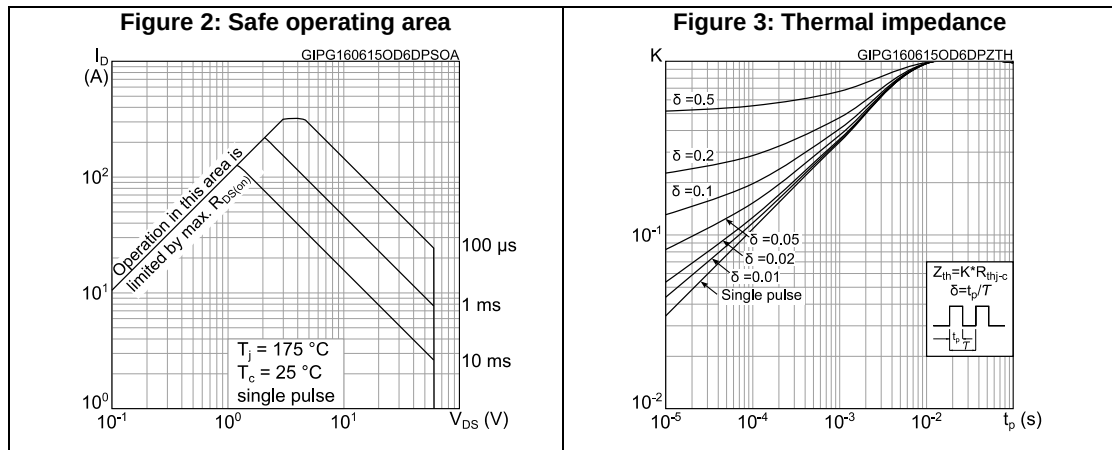


Figure 8: Capacitance variations

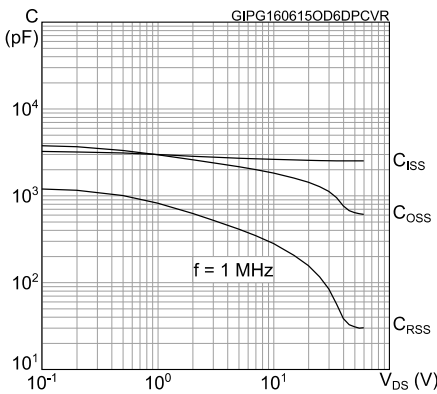


Figure 9: Normalized gate threshold voltage vs temperature

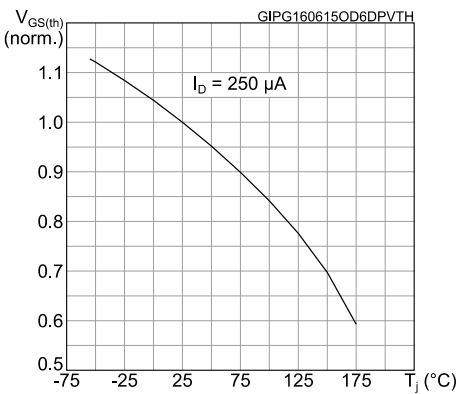


Figure 10: Normalized on-resistance vs temperature

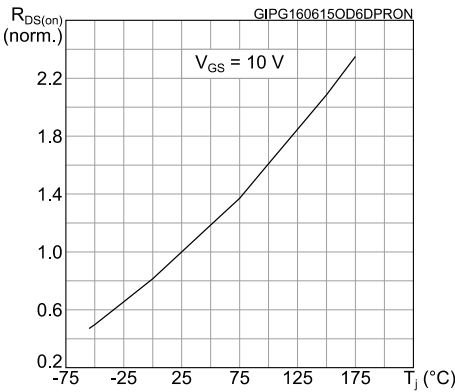


Figure 11: Normalized V(BR)DSS vs temperature

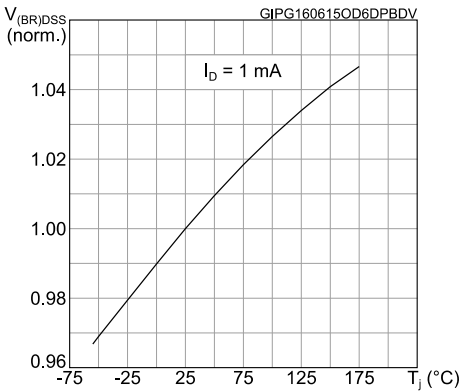
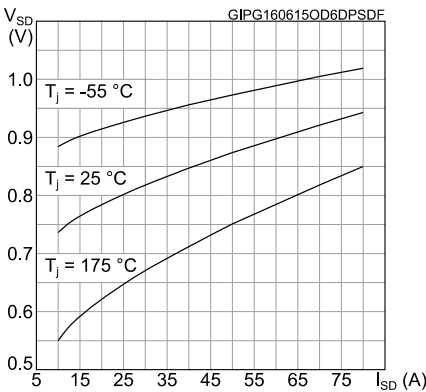
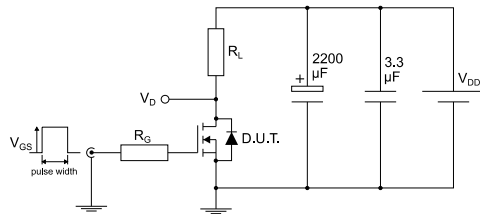


Figure 12: Source-drain diode forward characteristics



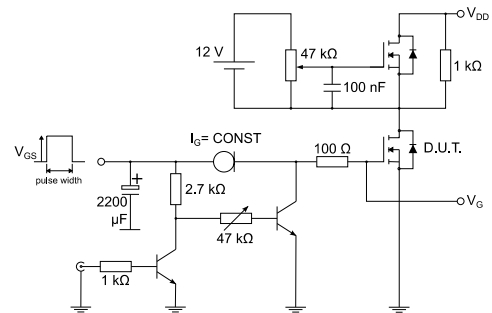
3 Test circuits

Figure 13: Test circuit for resistive load switching times



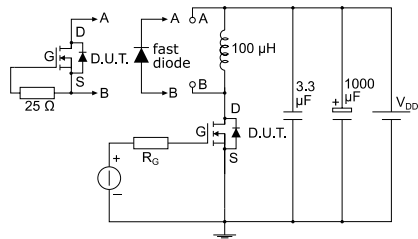
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Figure 14: Test circuit for gate charge behavior



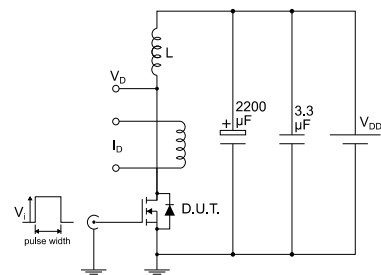
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Figure 15: Test circuit for inductive load switching and diode recovery times



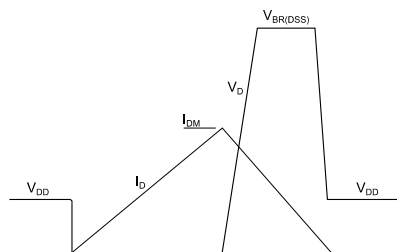
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Figure 16: Unclamped inductive load test circuit



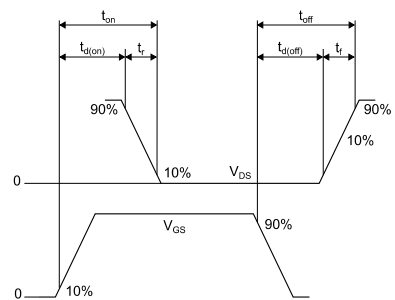
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



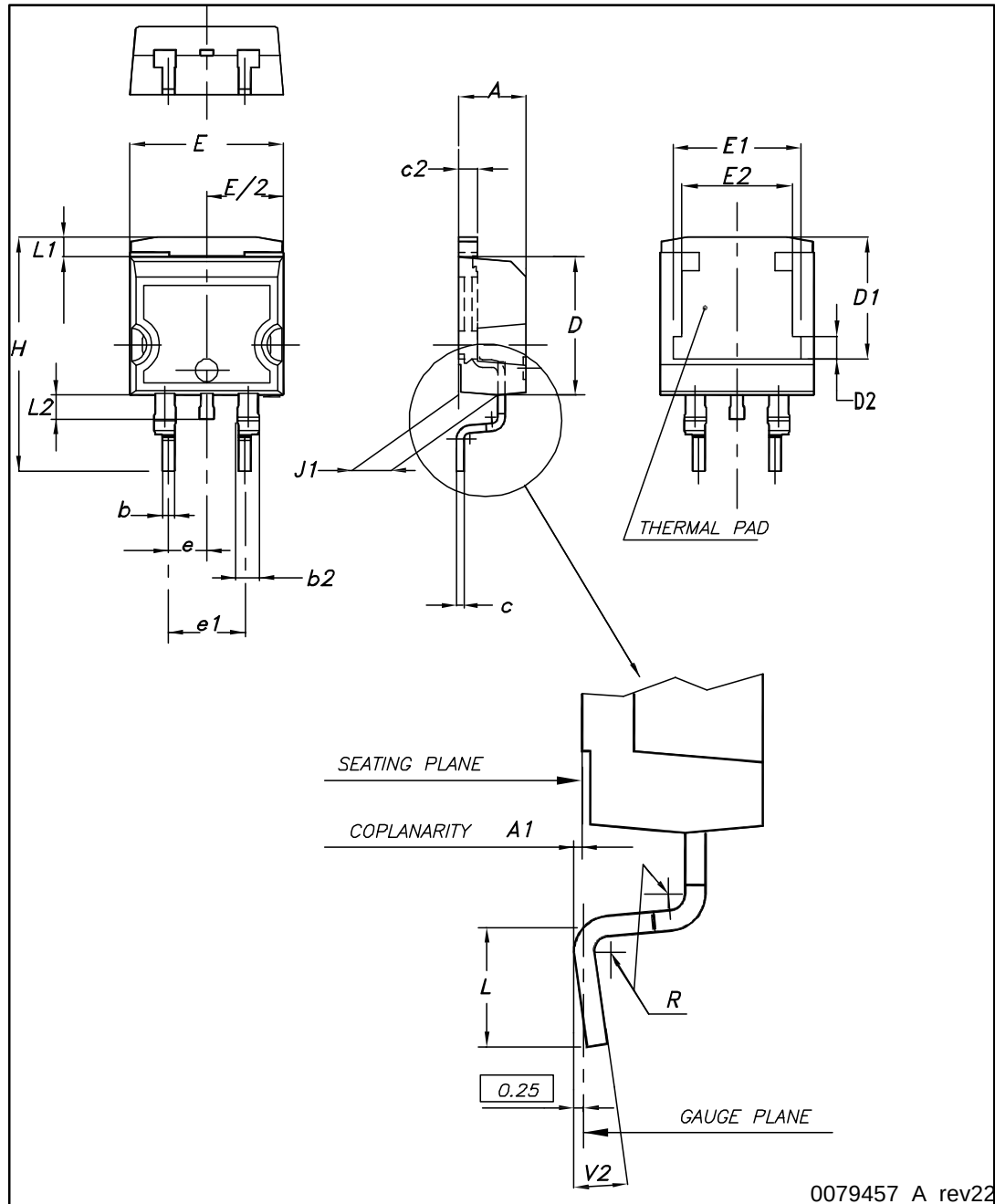
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A package information

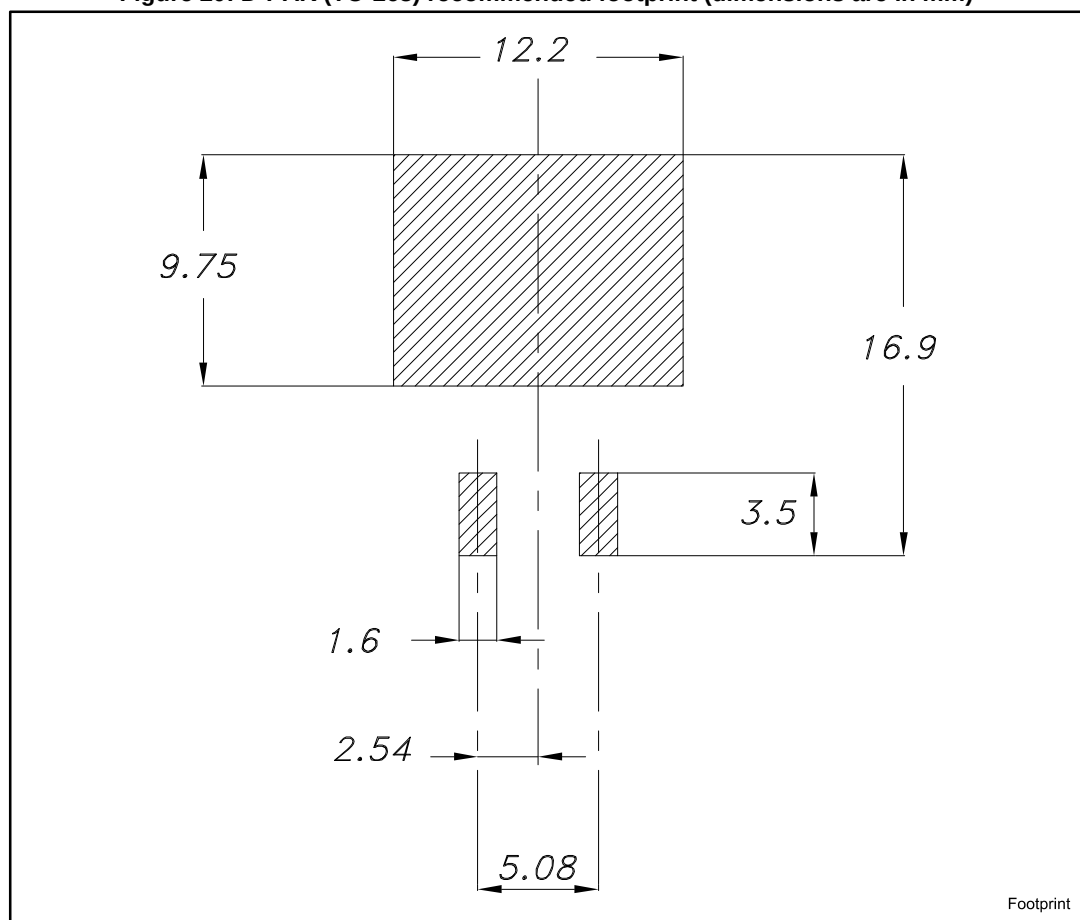
Figure 19: D²PAK (TO-263) type A package outline



0079457_A_rev22

Table 8: D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 20: D²PAK (TO-263) recommended footprint (dimensions are in mm)

4.2 D²PAK packing information

Figure 21: Tape outline

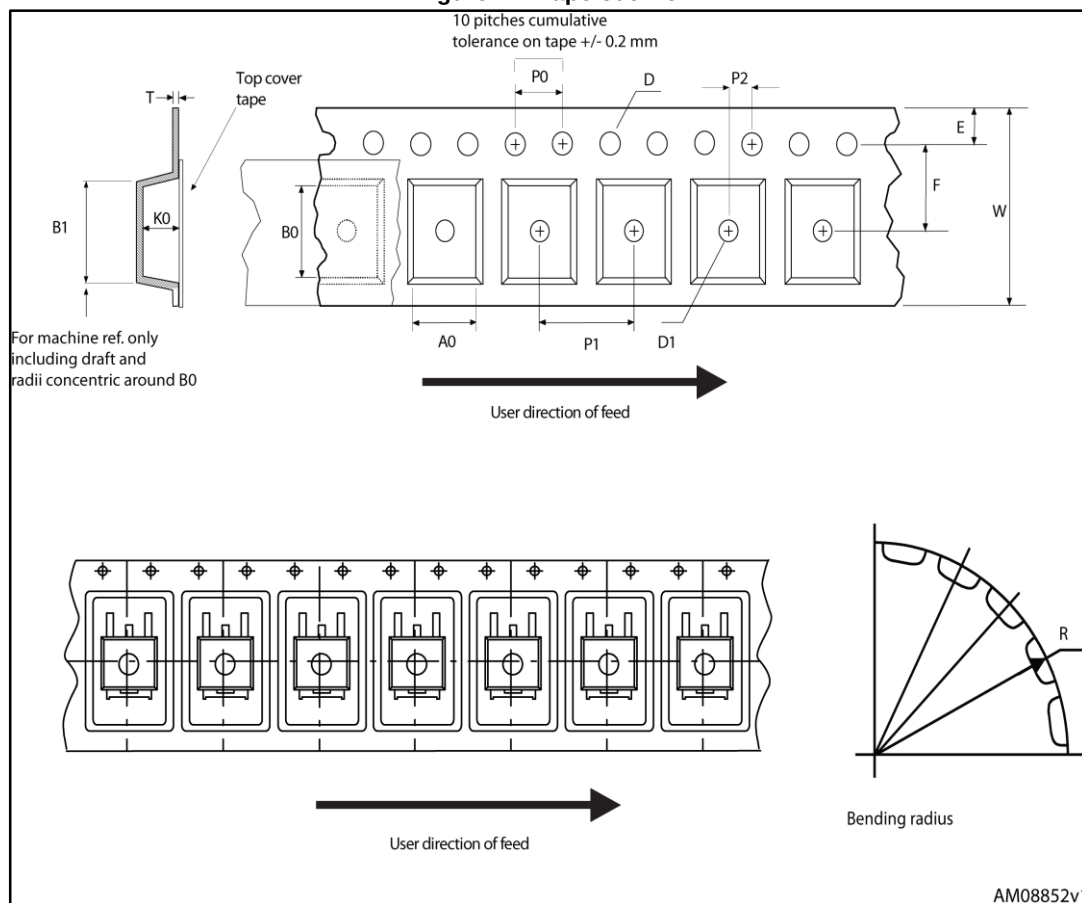
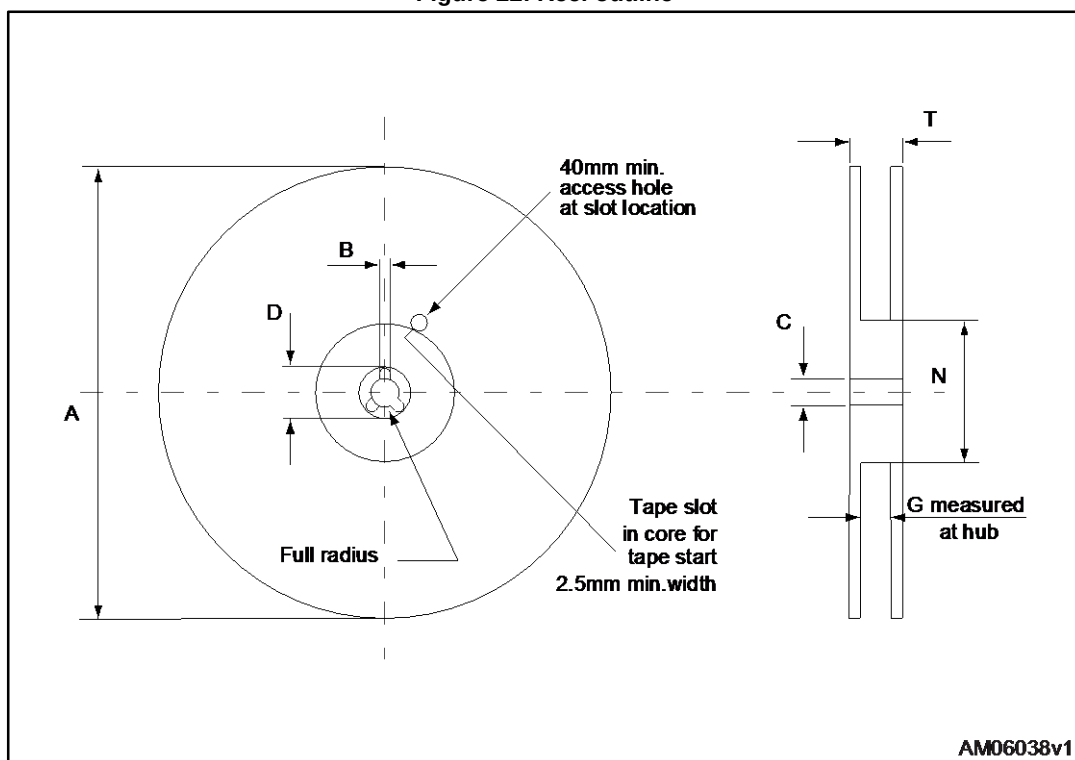


Figure 22: Reel outline

Table 9: D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
23-Jan-2015	1	First release.
16-Jun-2015	2	Datasheet promoted from preliminary data to production data Text and formatting edits throughout document In Section Electrical ratings: - updated Table Absolute maximum ratings In Section Electrical characteristics: - updated and renamed Table Static (was On/off states) - updated Table Switching times - updated Table Source drain diode Added Section Electrical characteristics (curves)
08-Jul-2015	3	In Section Electrical characteristics (curves): - updated Figures Output characteristics and Transfer characteristics
26-Jul-2015	4	In Section Electrical characteristics (curves): - updated Figures Output characteristics
15-Dec-2015	5	Updated Table 3: "Thermal data" .

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