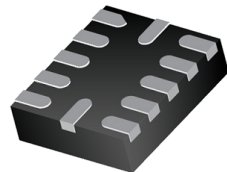


400 mA nano-quiescent synchronous step-down converter with digital voltage selection, Power Good and AUX switch



TQFN12 (2.0x1.7 mm)

Features

- 500 nA input quiescent current at $V_{IN} = 3.6$ V (not switching)
- 92% typical efficiency at 10 mA load ($V_{IN} = 3.6$ V, $V_{OUT} = 2.5$ V)
- 100% duty cycle
- 1.8 V to 5.5 V input operating range
- Undervoltage lockout: 1.57 V (V_{IN} falling, typ.)
- Up to 400 mA output current capability
- Low power control operation for the best efficiency
- Embedded soft-start circuit
- Tiny external components: $L = 2.2$ μ H typ.
- Settable inductor current limitation
- Selectable output voltages: 1.0 V to 3.3 V
- Output voltage Power Good
- $\pm 1.5\%$ output voltage accuracy (V_{OUT} , $T_A = 25$ °C)
- Dynamic output voltage selection (D0, D1 and D2)
- Auxiliary load switch Vout2 (AUX control input)
- Available in TQFN12 package

Applications

- Wearable applications
- Personal tracking monitors
- Smart watches, sport bands
- Energy harvesting, wireless sensors
- Wearable and fitness accessories
- Industrial sensors, portable low power devices
- Single cell Li-Ion battery applications
- Bluetooth® low energy
- Zigbee

Description

The **ST1PS02** is a nano-quiescent miniaturized synchronous step-down converter, which is able to provide up to 400 mA output current with an input voltage ranging from 1.8 V to 5.5 V. This converter is specifically designed for applications where high efficiency, PCB size and thickness are the key factors. The output voltage can be set using three digital control inputs, a V_{OUT} from 1.0 V to 3.3 V can be dynamically selected. Thanks to the enhanced PCC (peak current control) the **ST1PS02** reaches very high efficiency conversion using just a 2.2 μ H inductor and two small capacitors. The device embeds a controlled load switch to supply a subsystem with same voltage rail. Advanced design circuitry is implemented to minimize the quiescent current. The device is available in thin plastic package.

Product status link

[ST1PS02](#)

1 Application schematic

Figure 1. ST1PS02 application schematic

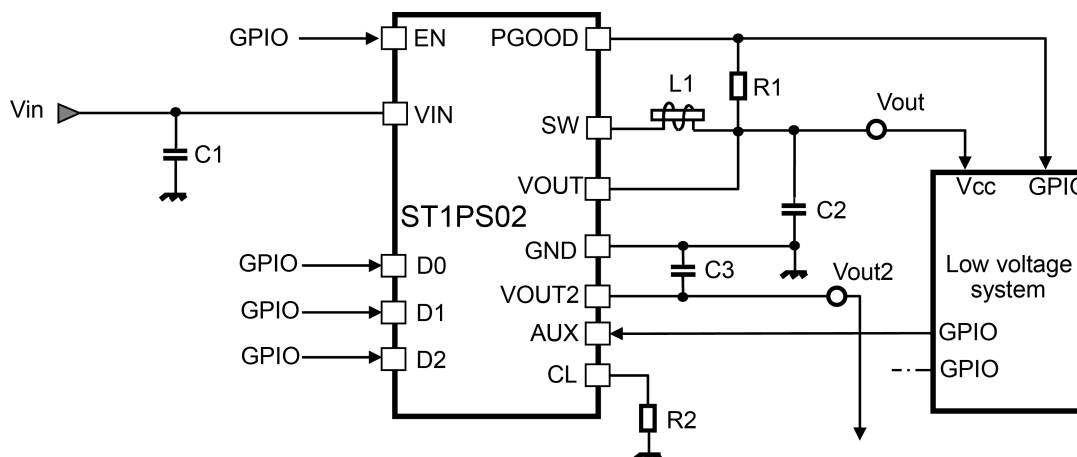


Table 1. Typical external components

Component	Description	Value	Size - imperial (metric)
C ₁	Ceramic capacitor with low ESR values	10 μ F	0603 (1608)
C ₂ , C ₃	Ceramic capacitor with low ESR values		
L1	Inductor	2.2 μ H	0806 (2016)
R ₁	Pull-up resistor	1 M Ω	0402 (1005)
R ₂	Current limit resistor	0 Ω	

2 Pin configuration

Figure 2. TQFN12 package (top through view)

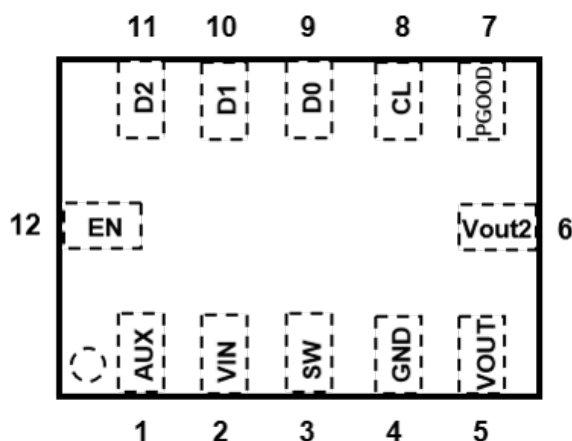


Table 2. Pin description

Name	Bump name	Description
AUX	1	Enable for the auxiliary output voltage
VIN	2	Input supply voltage. Bypass this pin to ground with a 10 μ F capacitor
SW	3	Switching output. Inductor connection
GND	4	Ground
VOUT	5	Sense pin used to monitor output voltage
Vout2	6	Auxiliary output pin with OCP (100 mA max. load)
PGOOD	7	Open drain output. It is in high impedance when the output voltage reaches 97.5% of the target V_{OUT}
CL	8	Current limit set. Connect to GND sets the default value (750 mA min.). An external resistor connected to GND can be used to adjust this parameter with a lower value (resistor values are reported on Table 6. Electrical characteristics)
D0	9	Output voltage selection inputs (refer to Table 7. Output voltage settings)
D1	10	
D2	11	
EN	12	Enable pin. High logic level turns on the IC

3 Functional pin description

GND

Device ground pin.

VIN

Supply voltage. This pin supplies power to the internal analog and digital circuitries when voltage is higher than V_{UVLO} . Bypass this pin to GND with a 10 μ F ceramic capacitor. Input capacitor C_1 must be chosen with low ESR to reduce the input voltage ripple.

SW

Inductor connection to internal PMOS and NMOS switches.

VOUT

Output voltage sense input. It provides the feedback voltage level to the regulation circuitry. 10 μ F output capacitor C_2 must be connected close to the pin or through a short trace and should have low ESR to reduce the output voltage ripple.

EN

Enable pin. A logic low level on this pin disables the device. High level enables the device. Do not leave this pin floating.

D0, D1, D2

Output voltage selection pins. See [Table 7. Output voltage settings](#) for V_{OUT} selection. Do not leave these pins floating. These pins can be dynamically changed during operation.

PGOOD

Power Good open drain output. If used it requires a pull-up resistor to hold a high level signal. High impedance indicates that V_{OUT} is above proper good threshold.

AUX

Load switch selection pins. Vout2 output is activated when this pin is at high level. Held to ground if auxiliary output (Vout2) is not used or if it should be disabled.

Vout2

Auxiliary output. It provides the same regulated voltage level as main output (VOUT) less drop on the load switch circuitry. 10 μ F output capacitor C_3 must be connected close to the pin or through a short trace and should have low ESR to reduce the output voltage ripple. This output is controlled from a soft-start circuit, if unused can be left open.

CL

Current limit threshold input. Held to ground if not used and default current limitation is the proper value. For smaller current values a pull-down resistor must be used.

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Power and signal supply voltage	- 0.3 to + 6.5	V
EN, D0, D1, D2, AUX	Logic input pins	- 0.3 to + 6.5	V
CL	Current limitation input pin	- 0.3 to + 6.5	V
V_{OUT} , SW	Output signal monitoring and switching pins	-0.3 to $V_{IN} + 0.3$	V
Vout2	Load switch output pin	- 0.3 to + 6.5	V
PGOOD	Power Good open drain output pin	- 0.3 to + 6.5	V
T_{AMB}	Operating ambient temperature	-40 to 85	°C
T_J	Junction temperature	-40 to 125	°C
T_{STG}	Storage temperature	-55 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 4. Thermal data

Symbol	Parameter	TQFN12	Unit
R_{thJA}	Thermal resistance junction-ambient	75	°C/W

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input supply voltage	1.8		5.5	V

5 Electrical characteristics

$C_1 = 10 \mu\text{F}$, $C_2 = 10 \mu\text{F}$, $C_3 = 10 \mu\text{F}$, $L1 = 2.2 \mu\text{H}$, $R_1 = 1 \text{ MOhm}$, $R_2 = 0 \text{ Ohm}$, $V_{\text{IN}} = 3.6 \text{ V}$, $V_{\text{EN}} = V_{\text{IN}}$, $V_{\text{OUT}} = 1.8 \text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
IQ	Quiescent current	EN=V _{IN} , AUX=GND, I _{OUT} =0 A, V _{OUT} =1.8 V, device does not switch, V _{IN} =2.5 V to 5.5 V		500	1000	nA
		EN=V _{IN} , AUX=V _{IN} , I _{OUT} =0 A, V _{OUT} =1.8 V, device not switching		2	4	μA
ISD	Shutdown current	EN=GND, shutdown current into V _{IN}		10	200	nA
V _{UVLO}	Undervoltage lockout threshold	V _{IN} rising		1.63	1.72	V
		V _{IN} falling	1.51	1.57		V
		Hysteresis		65		mV
V _{th100%+}	100% mode leave threshold	V _{IN} rising, 100% mode is disabled with V _{IN} = V _{OUTnom} + V _{th100%+}		300		mV
V _{th100%-}	100% mode enter threshold	V _{IN} falling, 100% mode is entered with V _{IN} = V _{OUTnom} + V _{th100%-}		200		
Output voltage						
V _{OUT}	Output voltage range	Output voltages are selected with pins D0, D1, D2	1.0		3.3	V
	Output voltage accuracy	V _{IN} = 3.6 V, whole V _{OUT} range, I _{OUT} =100 mA	-1.5		1.5	%
t _{ONmin}	Minimum on-time	V _{IN} = 3.6 V, V _{OUT} = 2 V, I _{OUT} = 0 A		225		ns
t _{OFFmin}	Minimum off-time	V _{IN} =2.3V		50		ns
t _{startupd}	Start-up delay time	V _{EN} from low to high, V _{IN} = 3.6 V, V _{OUT} = 1.8 V	1		5	ms
R _{OUTDIS}	Output discharge MOSFET on-resistance	V _{EN} = GND		30		Ω
Logic inputs (EN, D0, D1, D2)						
V _{IL}	Low level input voltage threshold	V _{IN} =1.8 V to 5.5 V			0.3	V
V _{IH}	High level input voltage threshold		1			
Power switch						
R _{DS(on)}	High-side MOSFET on-resistance	V _{IN} = 3.6 V, I _{sw} = 400 mA		0.38	0.45	Ω
	Low-side MOSFET on-resistance			0.14	0.2	
I _{LIM1}	High-side MOSFET switch current limit	1.8 V ≤ V _{IN} ≤ 5.5 V, CL=GND	750		1000	mA
I _{LIM2}	High-side MOSFET switch current limit	1.8 V ≤ V _{IN} ≤ 5.5 V, CL=1 MΩ	500		800	
I _{LIM3}	High-side MOSFET switch current limit	1.8 V ≤ V _{IN} ≤ 5.5 V, CL=2.2 MΩ		250		mA

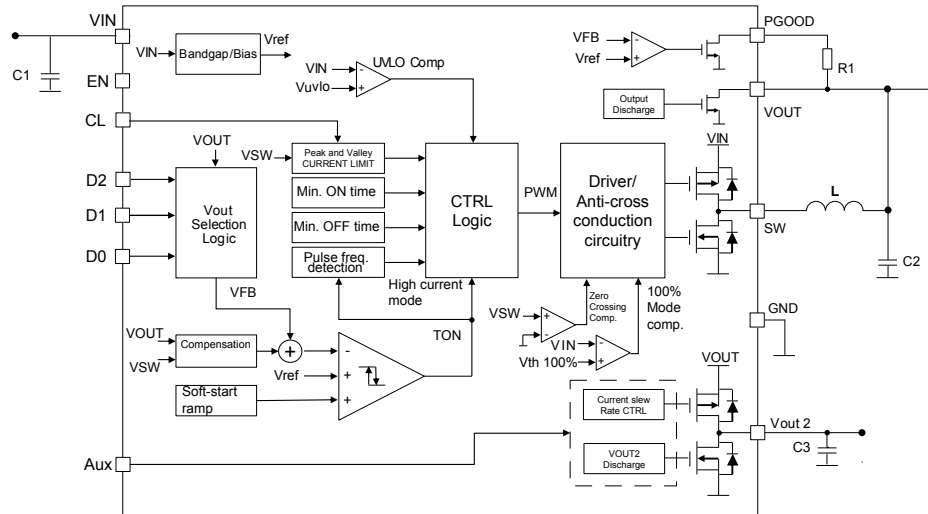
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LIMSS}	High-side MOSFET switch current limit during soft-start	Reduced switch current limit during soft-start period (typ. 400 μ s)	200	280	360	mA
Power Good output (PGOOD)						
V_{thpg}	Power Good threshold voltage	Rising output voltage on V_{OUT} pin, referred to V_{OUT} selected (D0, D1, D2)	95	97.5		%
V_{thpgH}		Hysteresis	-4	-3.5	-2.5	
V_{OL}	Low level output voltage	$1.8\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $E_N = \text{GND}$, current into PGOOD pin, $I_{PGOOD} = 4\text{ mA}$			0.23	V
Auxiliary output (Vout2)						
R_{AUX}	Load switch on-resistance	$I_{Load} = 100\text{ mA}$, $Aux = V_{IN}$		0.6	0.8	Ω
R_{disc2}	Auxiliary output discharge MOSFET on-resistance (discharger)	$I_{Load} = 100\text{ mA}$, $Aux = \text{GND}$		30	50	
tr_{aux}	Vaux rise time	Starting with AUX low-to-high transition, time to ramp V_{LOAD} from 0 V to 95% $V_{OUT} = 1.8\text{ V}$, $2.2\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $I_{LOAD} = 1\text{ mA}$		315	600	μ s

Table 7. Output voltage settings

Device	D2	D1	D0	V _{OUT}
ST1PS02AQTR	0	0	0	1.40 V
	0	0	1	1.45 V
	0	1	0	1.50 V
	0	1	1	1.55 V
	1	0	0	1.60 V
	1	0	1	1.65 V
	1	1	0	1.70 V
	1	1	1	1.75 V
ST1PS02BQTR	0	0	0	1.8 V
	0	0	1	1.9 V
	0	1	0	2.0 V
	0	1	1	2.1 V
	1	0	0	2.2 V
	1	0	1	2.3 V
	1	1	0	2.4 V
	1	1	1	2.5 V
ST1PS02CQTR	0	0	0	2.6 V
	0	0	1	2.7 V
	0	1	0	2.8 V
	0	1	1	2.9 V
	1	0	0	3.0 V
	1	0	1	3.1 V
	1	1	0	3.2 V
	1	1	1	3.3 V
ST1PS02DQTR	0	0	0	1.10 V
	0	0	1	1.15 V
	0	1	0	1.20 V
	0	1	1	1.25 V
	1	0	0	1.30 V
	1	0	1	1.35 V
	1	1	0	1.00 V
	1	1	1	1.05 V

6 ST1PS02 block diagram

Figure 3. Block diagram



7 Operation description

The ST1PS02 is an ultra-low quiescent new generation buck converter. It targets a very small quiescent current consumption (typical 500 nA) and it guarantees high efficiency operation even down to few microampere loads. It is based on a hysteretic comparator that senses the coil ripple current that is held constant in all operation modes. The device has seamless transition between PFM (pulse frequency modulation) and PWM (pulse width modulation) mode with low ripple and good load transient response.

In order to maintain constant ripple current on the selected coil, the device changes switching frequency, which also depends on input supply voltage. During PWM mode (heavy load), the device operates in continuous conduction up to 400 mA and switching frequency can reach 2 MHz maximum.

7.1 Power save mode

At light load the device enters automatically power save mode with total current consumption from the input power supply of 500 nA typical; during this condition most of the internal blocks are turned off in order to reach ultra-low power consumption. During this time, the load current is supported by the output capacitor.

7.2 Output voltage

The device allows the output voltage selection without an external resistor divider. Standard digital inputs are used to configure the device to supply a fixed output voltage according to [Table 7. Output voltage settings](#). The V_{OUT} pin must be connected directly and as close as possible to the inductor terminal to obtain the best performance and get the best output voltage regulation. The output voltage can be dynamically changed to implement voltage scaling.

7.3 Output discharge and UVLO

The device embeds a fast output discharge circuitry active when the enable pin is held to ground ($EN=gnd$) or when the input supply voltage reaches the minimum voltage level set by the UVLO protection circuit (undervoltage lock-out protection circuit). The UVLO rising threshold at 1.63 V (typ.) guarantees a proper device supply voltage operation. The output discharge function is available for the ST1PS02xQTR versions.

7.4 Soft-start and current limitation

The device embeds a fixed soft-start circuit active during a limited time period (few ms). This feature allows the inrush current to be minimized from the power supply in case of weak source. During this period internal circuit reduces to 280 mA the typical switch current limit.

7.5 100% duty cycle operation

The device enters 100% duty cycle operation if the input voltage comes close to the selected output voltage. During this mode, the regulator is turned off and output pin is directly connected to the input pin through the high-side MOSFET. The output voltage follows the input level minus the voltage drop across the internal MOSFET and the inductor. Once the input voltage exceeds the 100% duty cycle leave threshold, the device restarts to switch and regulates the select output voltage again.

7.6 Auxiliary output (Vout2)

The Aux pin controls Vout2 output. It provides the same regulated voltage level as the main output (V_{OUT}) less drop on the load switch circuitry, when Aux pin tied high. The Vout2 pin allows connecting/disconnecting the other system load to the output of the ST1PS02.

7.7 Power Good flag

The Power Good comparator monitors the selected V_{OUT} voltage. The Power Good open drain output is in high impedance when the V_{OUT} reaches the correct voltage level while it switches to low level when V_{OUT} falls below the normal voltage level.

8 Typical performance characteristics

Figure 4. Efficiency vs load, $V_{OUT} = 1.8\text{ V}$

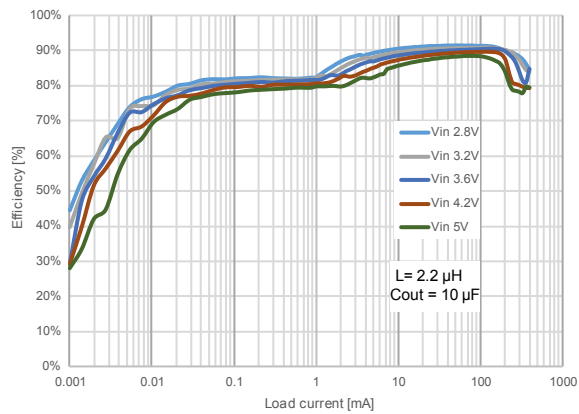


Figure 5. Efficiency vs V_{IN} , $V_{OUT} = 1.8\text{ V}$

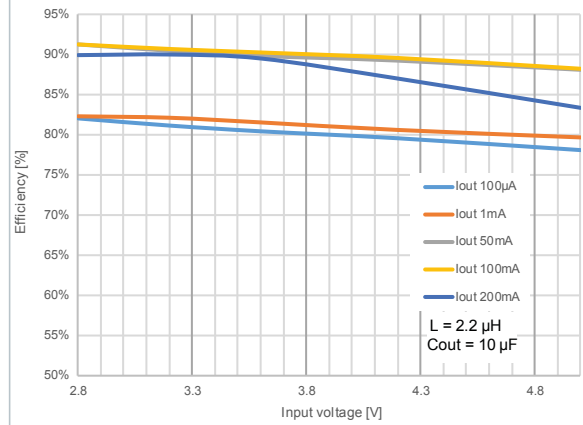


Figure 6. Efficiency vs load, $V_{OUT} = 2.5\text{ V}$

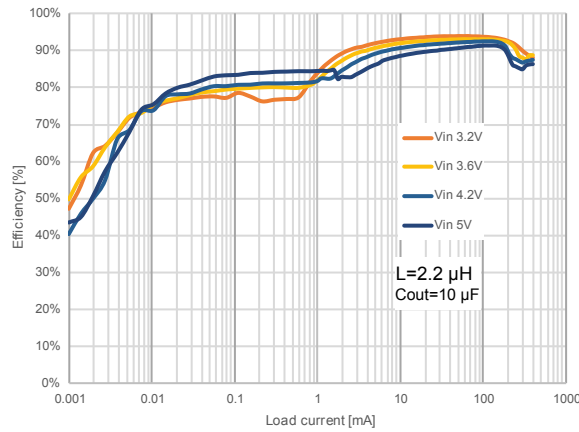


Figure 7. Efficiency vs V_{IN} , $V_{OUT} = 2.5\text{ V}$

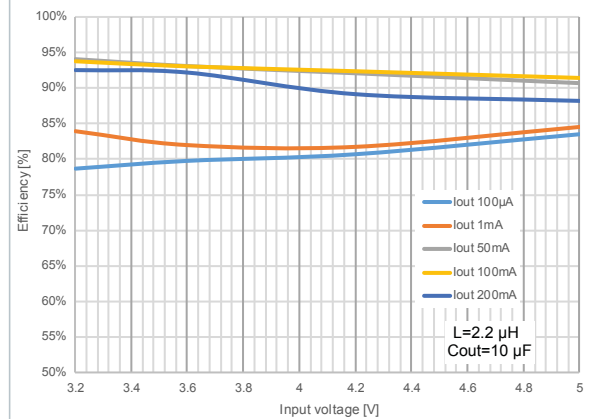


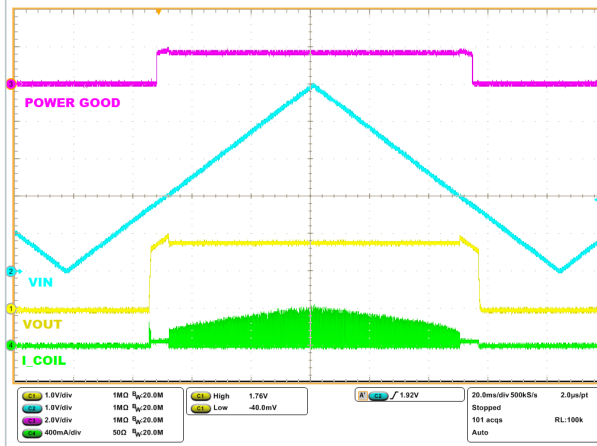
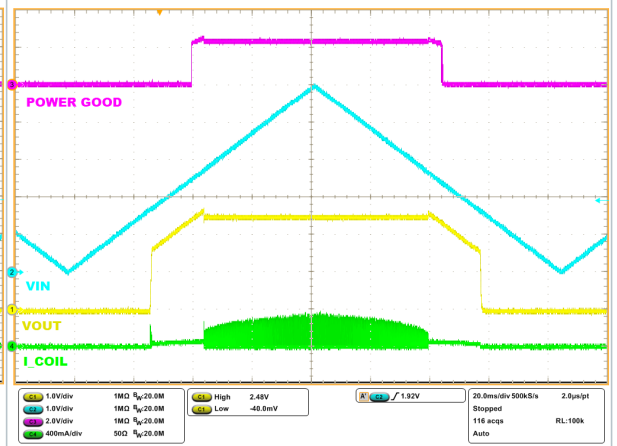
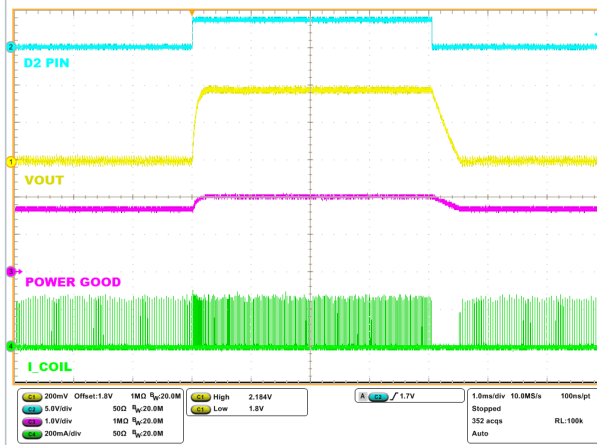
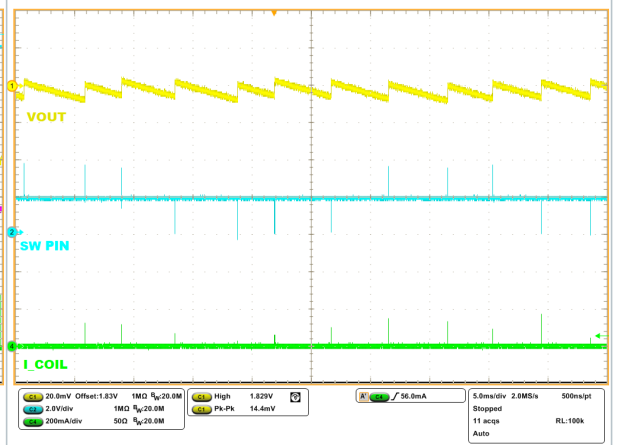
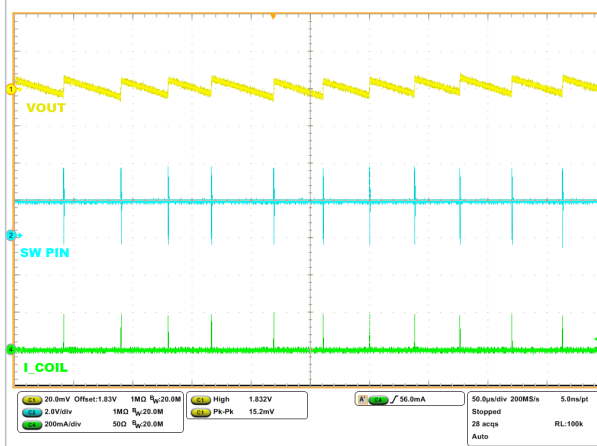
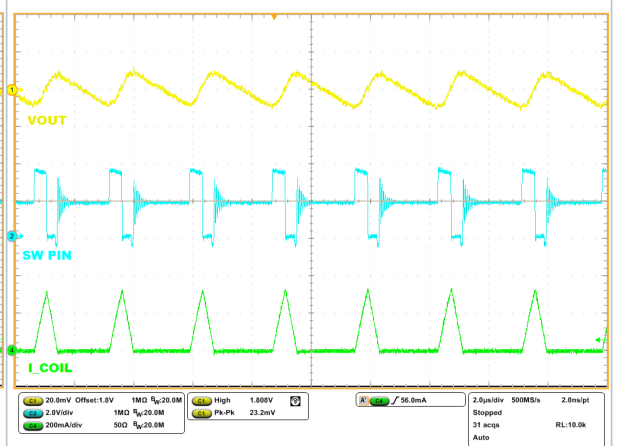
Figure 8. 100% mode, $V_{OUT} = 1.8\text{ V}$, 50 mA load

Figure 9. 100% mode, $V_{OUT} = 2.5\text{ V}$, 50 mA load

Figure 10. V_{OUT} change, 1.8 V to 2.5 V to 1.8 V, $I_{OUT} = 5\text{ mA}$, $V_{IN} = 3.6\text{ V}$

Figure 11. Output ripple, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 10\text{ }\mu\text{A}$

Figure 12. Output ripple, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 1\text{ mA}$

Figure 13. Output ripple, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 50\text{ mA}$


Figure 14. Output ripple, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=150\text{ mA}$

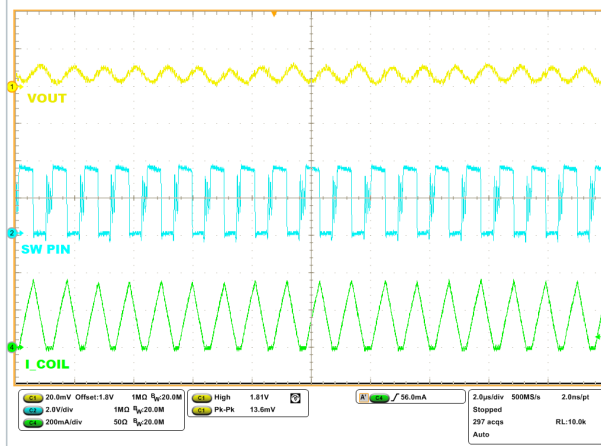


Figure 15. Output ripple, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=250\text{ mA}$

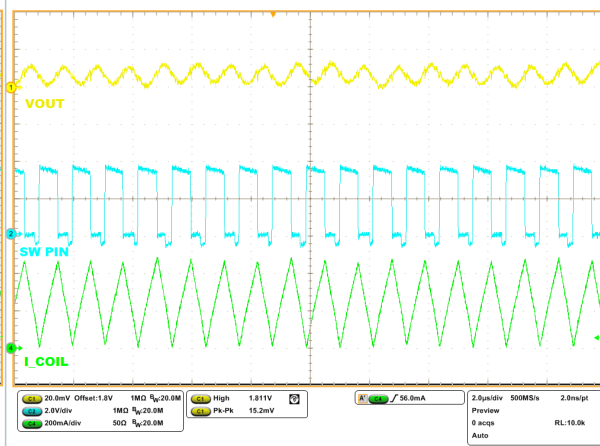


Figure 16. Start-up, $V_{IN}=3.6$ V, $V_{OUT}=1.8$ V, no load

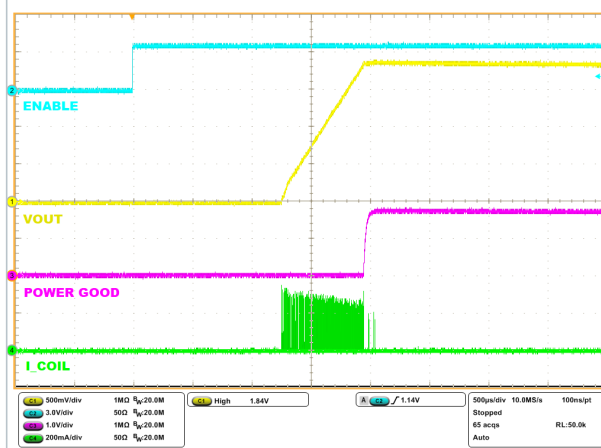


Figure 17. Disable, $V_{IN}=3.6$ V, $V_{OUT}=1.8$ V, no load

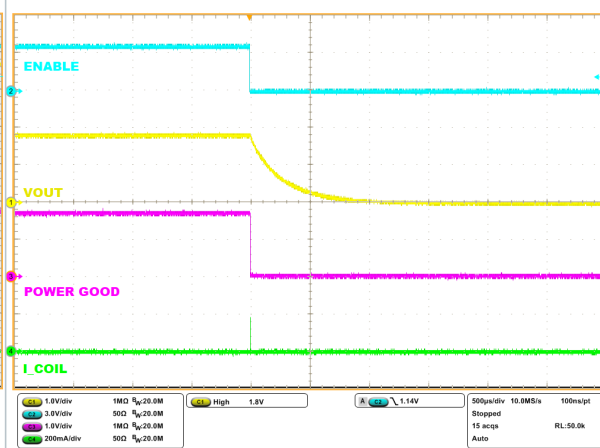


Figure 18. Start-up, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT} = 100\text{ mA}$

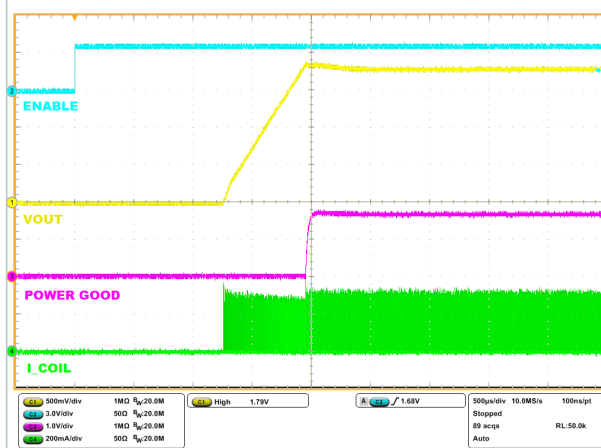


Figure 19. Disable, $V_{IN}=3.6\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 100\text{ mA}$

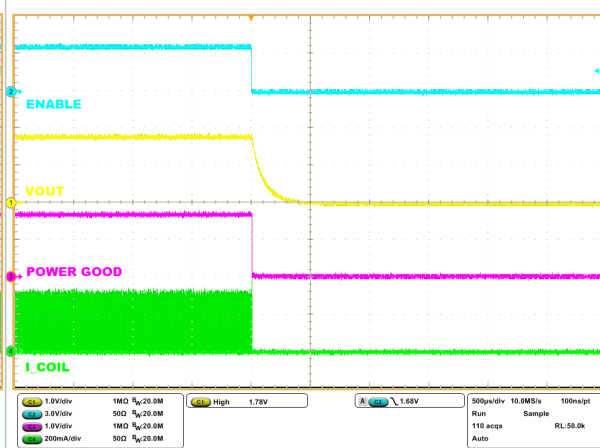


Figure 20. Load transient, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=50\text{ }\mu\text{A}$ to 10 mA

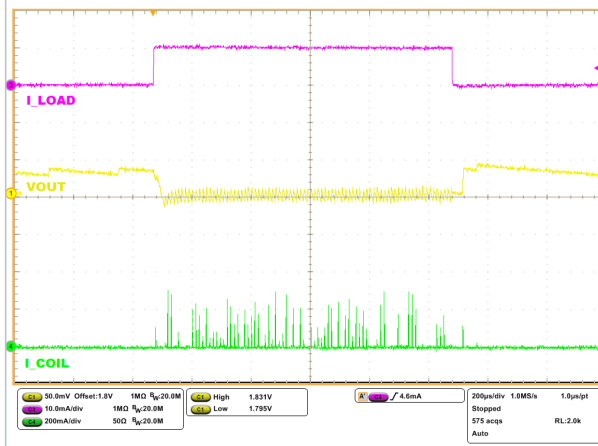


Figure 21. Load transient, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=0$ to 100 mA

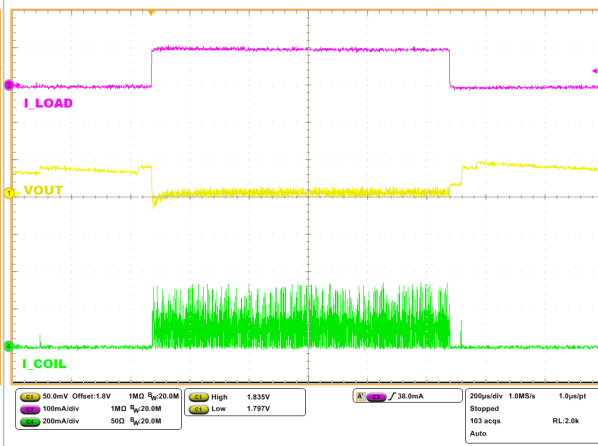


Figure 22. Load transient, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=10$ to 100 mA

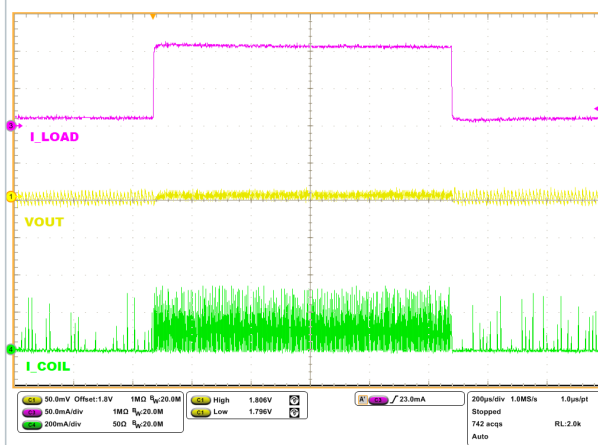


Figure 23. Start-up, $V_{IN}=3.6\text{ V}$, $V_{OUT2}=1.8\text{ V}$, no load

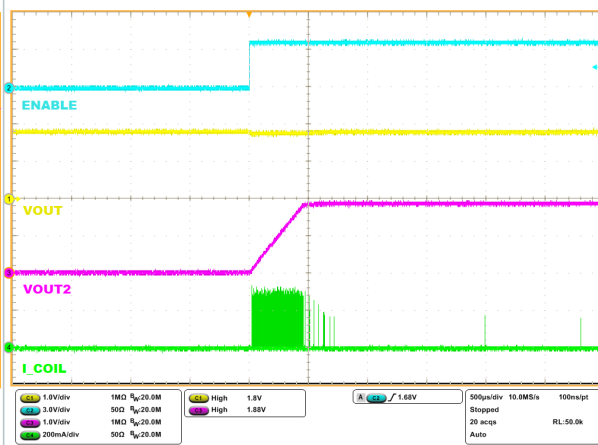


Figure 24. Disable, $V_{IN}=3.6\text{ V}$, $V_{OUT2}=1.8\text{ V}$, no load

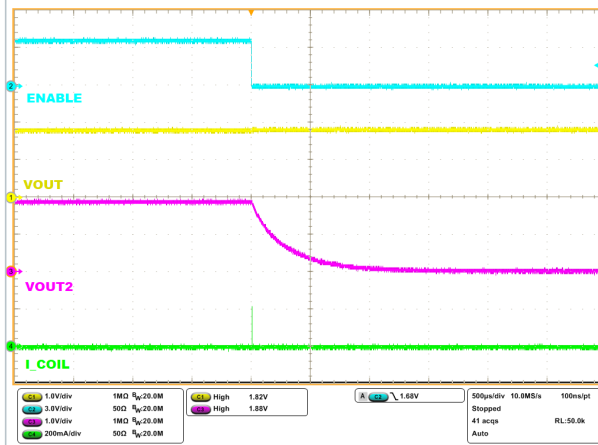


Figure 25. Start-up, $V_{IN}=3.6\text{ V}$, $V_{OUT2}=1.8\text{ V}$, $I_{OUT}=100\text{ mA}$

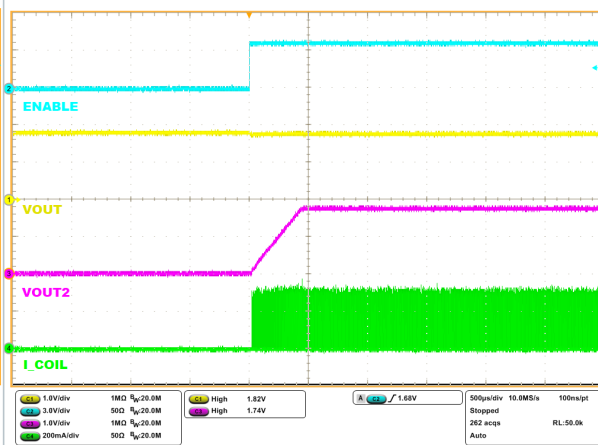
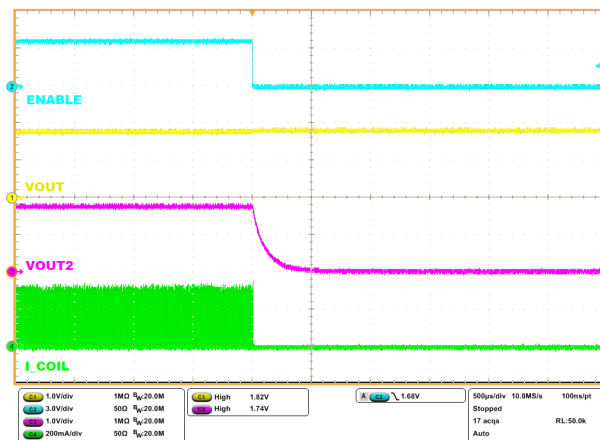


Figure 26. Disable, $V_{IN} = 3.6\text{ V}$, $V_{out2} = 1.8\text{ V}$, $I_{OUT} = 100\text{ mA}$



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 TQFN12 (2.0x1.7x0.55 mm) package information

Figure 27. TQFN12 (2.0x1.7x0.55 mm) package outline

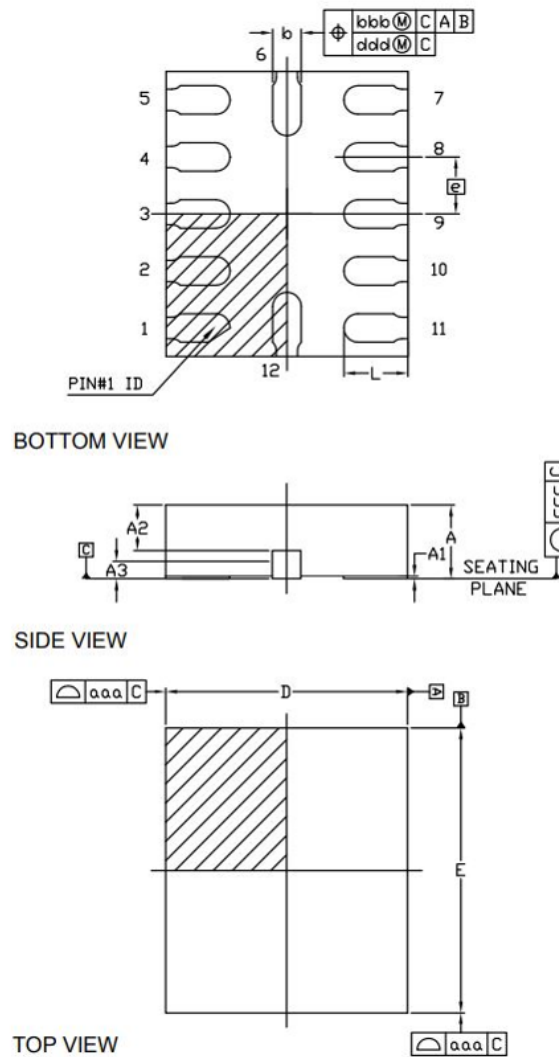
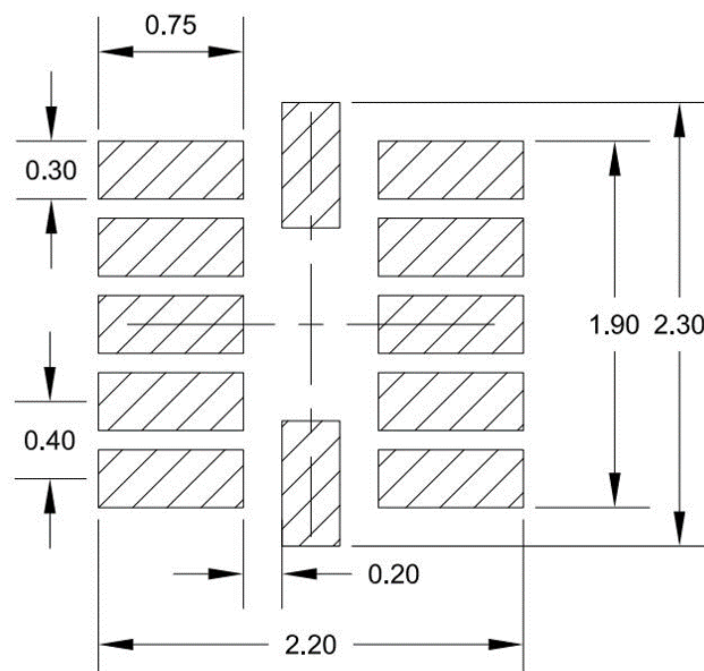


Table 8. TQFN12 (2.0x1.7x0.55 mm) mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	0.40	0.50	0.55
A1	0.00	0.03	0.05
A2	0.28	0.38	0.48
A3		0.125	
b	0.15	0.20	0.25
D	1.60	1.70	1.80
E	1.90	2.00	2.10
e		0.40	
L	0.35	0.45	0.55
aaa		0.15	
bbb		0.10	
ccc		0.08	
ddd		0.05	
eee		0.10	

Figure 28. TQFN12 (2.0x1.7x0.55 mm) recommended footprint


10 Ordering information

Table 9. Ordering information

Order codes	Output voltages	Output discharge	Package	Packing
ST1PS02AQTR	1.40 V to 1.75 V, 50 mV steps	Yes	TQFN12 (2.0x1.7 mm) 400 µm pitch	Tape and reel
ST1PS02A1QTR		No		
ST1PS02BQTR	1.8 V to 2.5 V, 100 mV steps	Yes		
ST1PS02B1QTR		No		
ST1PS02CQTR	2.6 V to 3.3 V, 100 mV steps	Yes		
ST1PS02C1QTR		No		
ST1PS02DQTR	1.0 V to 1.35 V, 50 mV steps	Yes		
ST1PS02D1QTR		No		

Revision history

Table 10. Document revision history

Date	Version	Changes
17-Feb-2020	1	Initial release.
17-Mar-2020	2	Updated Section 5 Electrical characteristics. Minor text changes throughout the document.
20-Mar-2020	3	Updated PGOOD an EN description in Table 2 , IQ test condition in Table 6 and Block diagram .

Contents

1	Application schematic	2
2	Pin configuration	3
3	Functional pin description	4
4	Maximum ratings	5
5	Electrical characteristics	6
6	ST1PS02 block diagram	9
7	Operation description	10
7.1	Power save mode	10
7.2	Output voltage	10
7.3	Output discharge and UVLO	10
7.4	Soft-start and current limitation	10
7.5	100% duty cycle operation	10
7.6	Auxiliary output (Vout2)	10
7.7	Power Good flag	10
8	Typical performance characteristics	11
9	Package information	16
9.1	TQFN12 (2x1.7x0.55) package information	16
10	Ordering information	18
	Revision history	19

List of tables

Table 1.	Typical external components	2
Table 2.	Pin description.	3
Table 3.	Absolute maximum ratings	5
Table 4.	Thermal data.	5
Table 5.	Recommended operating conditions.	5
Table 6.	Electrical characteristics	6
Table 7.	Output voltage settings	8
Table 8.	TQFN12 (2.0x1.7x0.55 mm) mechanical data	17
Table 9.	Ordering information.	18
Table 10.	Document revision history	19

List of figures

Figure 1.	ST1PS02 application schematic	2
Figure 2.	TQFN12 package (top through view)	3
Figure 3.	Block diagram	9
Figure 4.	Efficiency vs load, $V_{OUT} = 1.8\text{ V}$	11
Figure 5.	Efficiency vs V_{IN} , $V_{OUT} = 1.8\text{ V}$	11
Figure 6.	Efficiency vs load, $V_{OUT} = 2.5\text{ V}$	11
Figure 7.	Efficiency vs V_{IN} , $V_{OUT} = 2.5\text{ V}$	11
Figure 8.	100% mode, $V_{OUT} = 1.8\text{ V}$, 50 mA load	12
Figure 9.	100% mode, $V_{OUT} = 2.5\text{ V}$, 50 mA load	12
Figure 10.	V_{OUT} change, 1.8 V to 2.5 V to 1.8 V, $I_{OUT} = 5\text{ mA}$, $V_{IN} = 3.6\text{ V}$	12
Figure 11.	Output ripple, $V_{IN}=3.6\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 10\text{ }\mu\text{A}$	12
Figure 12.	Output ripple, $V_{IN}=3.6\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 1\text{ mA}$	12
Figure 13.	Output ripple, $V_{IN}=3.6\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 50\text{ mA}$	12
Figure 14.	Output ripple, $V_{IN}=3.6\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 150\text{ mA}$	13
Figure 15.	Output ripple, $V_{IN}=3.6\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 250\text{ mA}$	13
Figure 16.	Start-up, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, no load	13
Figure 17.	Disable, $V_{IN}=3.6\text{ V}$, $V_{OUT} = 1.8\text{ V}$, no load	13
Figure 18.	Start-up, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT} = 100\text{ mA}$	13
Figure 19.	Disable, $V_{IN}=3.6\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 100\text{ mA}$	13
Figure 20.	Load transient, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT} = 50\text{ }\mu\text{A}$ to 10 mA	14
Figure 21.	Load transient, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT} = 0$ to 100 mA	14
Figure 22.	Load transient, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT} = 10$ to 100 mA	14
Figure 23.	Start-up, $V_{IN} = 3.6\text{ V}$, $V_{out2} = 1.8\text{ V}$, no load	14
Figure 24.	Disable, $V_{IN} = 3.6\text{ V}$, $V_{out2} = 1.8\text{ V}$, no load	14
Figure 25.	Start-up, $V_{IN} = 3.6$, $V_{out2} = 1.8\text{ V}$, $I_{OUT} = 100\text{ mA}$	14
Figure 26.	Disable, $V_{IN} = 3.6\text{ V}$, $V_{out2} = 1.8\text{ V}$, $I_{OUT} = 100\text{ mA}$	15
Figure 27.	TQFN12 (2.0x1.7x0.55 mm) package outline	16
Figure 28.	TQFN12 (2.0x1.7x0.55 mm) recommended footprint	17

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics – All rights reserved

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[STMicroelectronics:](#)

[ST1PS02DQTR](#) [ST1PS02AQTR](#) [ST1PS02CQTR](#) [ST1PS02A1QTR](#) [ST1PS02B1QTR](#) [ST1PS02C1QTR](#)