SPC58EHx, SPC58NHx

SPC58 H Line - 32 bit Power Architecture automotive MCU Triple z4 cores 200 MHz, 10 MBytes Flash, HSM, ASIL-D

Datasheet - production data

eTQFP144 (20 x 20 x 1.0 mm)

eLQFP176 (24 x 24 x 1.4 mm)

FPBGA302 (17 x 17 x 1.8 mm)

FPBGA386 (19 x 19 x 1.8 mm)

Features

- AEC-Q100 qualified
- High performance e200z4 triple core:
  - 32-bit Power Architecture technology CPU
  - Core frequency as high as 200 MHz
  - Variable Length Encoding (VLE)
  - Floating Point, End-to-End Error Correction
- 10496 KB (10240 KB code Flash + 256 KB data Flash) on-chip Flash memory:
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
  - Supports read while read between the two code Flash partitions
  - Hardware support for Flash context switching (for FOTA with multi software versions)
- 1088 KB on-chip general-purpose SRAM (in addition to 192 KB core local data RAM):
  - 64 KB in CPU_0, 64 KB in CPU_1 and 64 KB in CPU_2
- 224 KB HSM dedicated Flash memory (192 KB code + 32 KB data)
- Multi-channel direct memory access controller (eDMA):
  - One eDMA with 64 channels
  - One eDMA with 16 channels
- One interrupt controller (INTC)
- Comprehensive new generation ASIL-D safety concept:
  - ASIL-D of ISO 26262
  - One CPU channel in lockstep
  - Logic BIST
  - FCCU for collection and reaction to failure notifications
  - Memory BIST
  - Cyclic redundancy check (CRC) unit
  - Memory Error Management Unit (MEMU) for collection and reporting of error events in memories
- Crossbar switch architecture for concurrent access to peripherals, Flash, or RAM from multiple bus masters with end-to-end ECC
- Body cross triggering unit (BCTU):
  - Triggers ADC conversions from any eMIOS channel
  - Triggers ADC conversions from up to 2 dedicated PIT_RTIs
- Enhanced modular IO subsystem (eMIOS):
  - up to 96 timed IO channels with 16-bit counter resolution
- Enhanced analog-to-digital converter system with:
  - 4 independent fast 12-bit SAR analog converters
  - One supervisor 12-bit SAR analog converter
  - One standby 10-bit SAR analog converter
  - 100 ADC channels
- Communication interfaces:
  - 24 LINFlexD modules
  - 10 deserial serial peripheral interface (DSPI) modules
  - 1 deserial serial peripheral interface (DSPI_LP) module available in low power mode

- 16 MCAN interfaces with advanced shared memory scheme and ISO CAN-FD support
- Dual-channel FlexRay controller
- One SD/SDIO/eMMC module
- One OctalSPI module with double Chip Select
- Two independent Ethernet controllers, one 10/100Mbps and the other one 10/100Mbps or 1Gbps, compliant IEEE 802.3-2008 and OPEN RGMII EPL v2.3
- Four I2C modules
- Two PSI5 modules

- Low power capabilities:
  - Versatile low power modes
  - Ultra low power standby with RTC
  - Smart Wake-up Unit for contact monitoring
  - Fast wakeup schemes
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Boot assist Flash (BAF) supports factory programming using a serial bootload through the asynchronous CAN or LIN/UART
- Low power supply options:
  - Single internal linear regulator with external ballast
  - External low voltage supply (1.2V)
- Temperature range:
  - -40 °C to 105 °C
  - -40 °C to 125 °C

Table 1. Device summary

Package	Part number					
	6 MB		8 MB		10 MB	
	Dual core	Triple core	Dual core	Triple core	Dual core	Triple core
eTQFP144	SPC58EH84E5	SPC58NH84E5	SPC58EH90E5	SPC58NH90E5	SPC58EH92E5	SPC58NH92E5
eLQFP176	SPC58EH84E7	SPC58NH84E7	SPC58EH90E7	SPC58NH90E7	SPC58EH92E7	SPC58NH92E7
FPBGA302	SPC58EH84C3	SPC58NH84C3	SPC58EH90C3	SPC58NH90C3	SPC58EH92C3	SPC58NH92C3
FPBGA386	SPC58EH84C5	SPC58NH84C5	SPC58EH90C5	SPC58NH90C5	SPC58EH92C5	SPC58NH92C5

Contents

1 Introduction

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

2 Description

The SPC58EHx, SPC58NHx microcontroller belongs to a family of devices superseding the SPC58x family. SPC58EHx, SPC58NHx builds on the legacy of the SPC5x family, while introducing new features coupled with higher throughput to provide substantial reduction of cost per feature and significant power and performance improvement (MIPS per mW).

2.1 Device feature summary

Table 2 lists a summary of major features for the SPC58EHx, SPC58NHx device. The feature column represents a combination of module names and capabilities of certain modules. A detailed description of the functionality provided by each on-chip module is given later in this document.

Table 2. Features list

Feature	Description
SPC58 family	40 nm
Processing shell	
Number of Cores	2
Number of checker cores	1
Local RAM	32 KB Instruction
	64 KB Data
Single Precision Floating Point	Yes
SIMD (LSP)	Yes
VLE	Yes
Cache	16 KB Instruction
	8 KB Data
Streaming shell	
Number of Cores	1
Number of checker cores	0
Local RAM	32 KB Instruction
	64 KB Data
Single Precision Floating Point	Yes
SIMD (LSP)	Yes
VLE	Yes
Cache	16 KB Instruction
	8 KB Data
Other	
Security (HSM Module)	up to 1

Table 2. Features list (continued)

Feature	Description
MPU	Core MPU: 24 per CPU
	System MPU: 24 per XBAR
Semaphores	Yes
CRC Channels	2 x 4
Software Watchdog Timer (SWT)	4
Core Nexus Class	3+
Event Processor	4 x SCU
	4 x PMC
Run control Module	Yes
System SRAM	1088 KB (including 256 KB of standby RAM)
User Flash	up to 10240 KB code / 256 KB data
Security Flash	up to 192 KB code / 32 KB data
Flash fetch accelerator	2 x 2 x 4 x 256-bit
DMA channels	80
DMA Nexus Class	3
LINFlexD	24
M_CAN supporting CAN-FD according to ISO 11898-1 2015	16
DSPI	11
I2C	4
PSI5 / PSI5-S bus	2 / 1
FlexRay	1 x Dual channel
Ethernet	2 MAC with Time stamping, AVB and VLAN support
System Timers	8 PIT channels
	4 AUTOSAR® (STM)
	RTC/API
eMIOS	3 x 32 channels
OctalSPI	1 (2 Chip select)
SDMMC	1
GST	1
BCTU	96 channels
Interrupt controller	> 710 sources
ADC (SAR)	Five 12-bit (4+1 Supervisor); One 10-bit
Temp. sensor	Yes
Self Test Controller	Yes

Table 2. Features list (continued)

Feature	Description
PLL	Dual PLL with FM
External Power Supplies	1.2 V - 3.3 V - 5 V
Integrated linear voltage regulator	Yes
Low Power Modes	Stop Mode
	Halt Mode
	Smart Standby with output controller, analog and digital inputs
	Standby Mode

2.2 Block Diagram

The figures below show the top-level block diagrams.

Figure 1. Block Diagram

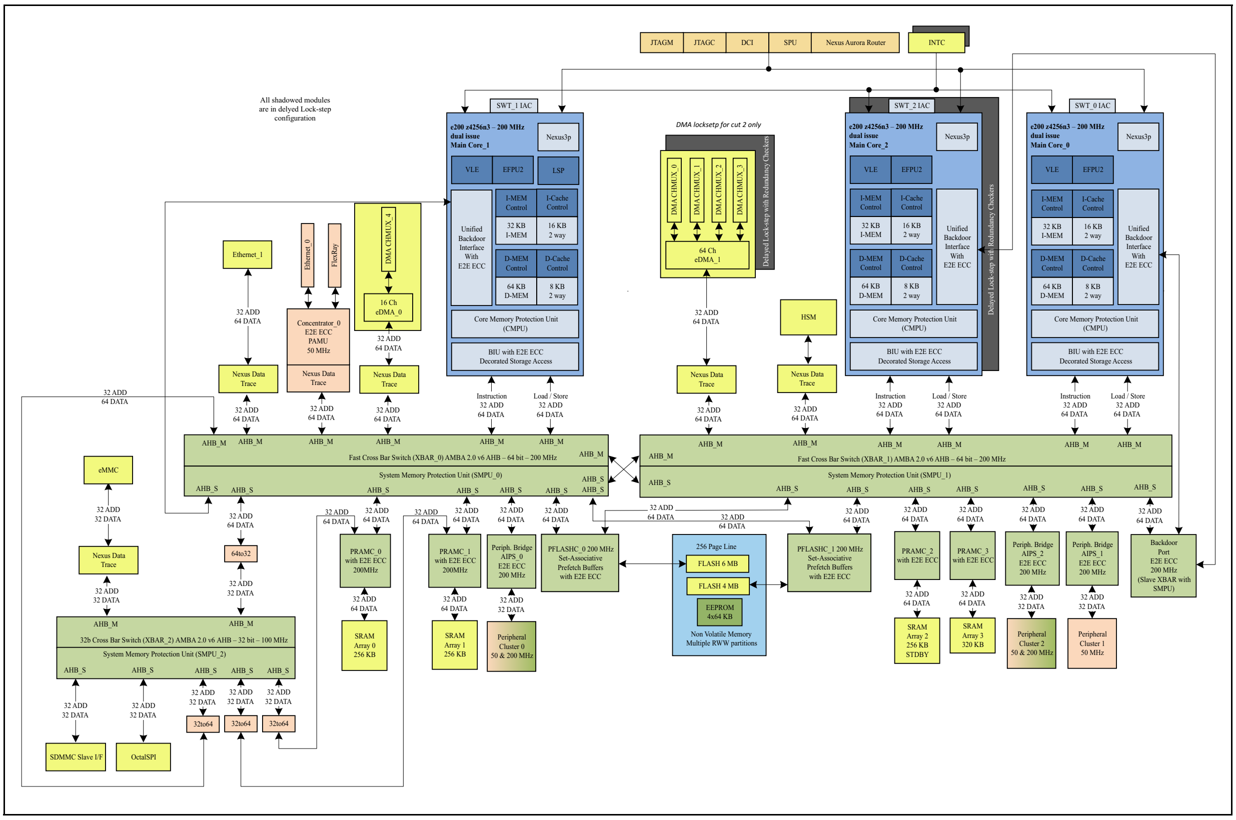
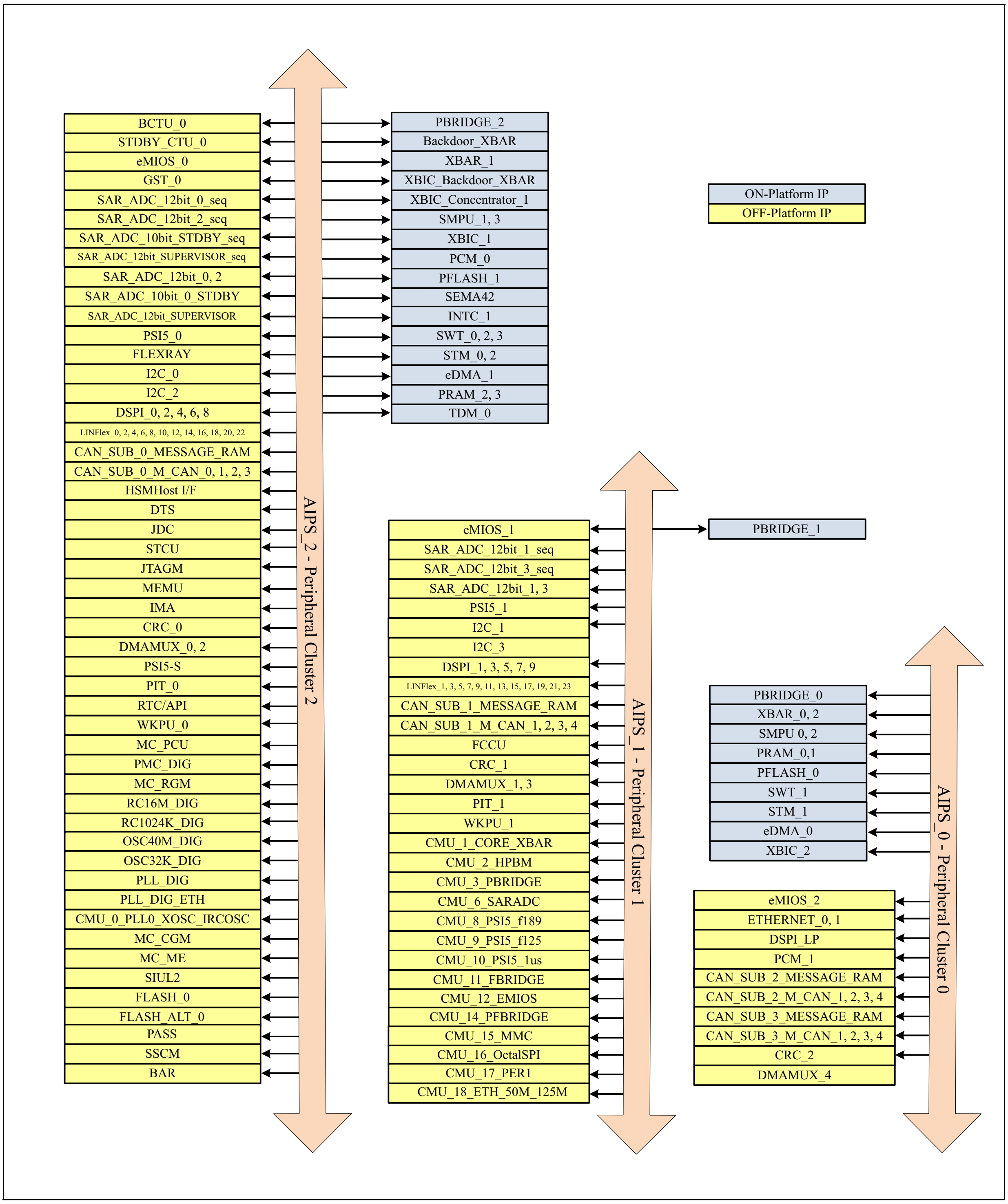


Figure 2. Periphery allocation



2.3 Features

On-chip modules within SPC58EHx, SPC58NHx include the following features:

- Three main CPUs, dual issue, 32-bit CPU core complexes (e200z4), one of them having a checker core in lock-step
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
  - Single-precision floating point operations
  - Lightweight signal processing auxiliary processing unit (LSP APU) instruction support for digital signal processing (DSP) on Core_0, Core_1, Core_2
  - 32 KB local instruction RAM and 64 KB local data RAM for Core_0, Core_1 and Core_2
  - 16 KB I-Cache and 8 KB D-Cache for Core_0, Core_1 and Core_2
  - 10 MB on-chip Flash
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
  - Supports read while read between the two code Flash partitions.
- 1088 KB on-chip general-purpose SRAM (+ 192 KB data RAM and 96 KB instruction RAM included in the CPUs)
- 224 KB HSM dedicated flash memory (192 KB code + 32 KB data)
- Multi channel direct memory access controllers (eDMA)
  - One eDMA with 64 channels
  - One eDMA with 16 channels
- One interrupt controller (INTC) in lock-step
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for processing and streaming shell
- Dual crossbar switch architecture for concurrent access to peripherals, Flash, or RAM from multiple bus masters with end-to-end ECC
- Hardware security module (HSM) compliant with EVITA full
- System integration unit lite (SIUL)
- Boot assist Flash (BAF) supports factory programming using a serial bootload through the asynchronous CAN or LIN/UART.
- Enhanced analog-to-digital converter system with
  - One supervisor 12-bit SAR analog converter
  - Four separate fast 12-bit SAR analog converters
  - One separate 10-bit SAR analog converter for standby mode
- Eleven deserial serial peripheral interface (DSPI) modules, one working even in low power mode
- Twenty four LIN and UART communication interface (LINFlexD) modules
  - LINFlexD_0 is a Master/Slave
  - All others are Masters
- Sixteen modular controller area network (MCAN) modules all supporting flexible data rate (CAN-FD)
- Dual-channel FlexRay controller

- On ethernet controller 10/100 Mbps (Ethernet 0)
  - Standard compliance

    Ethernet interface is compliant to following standards:
    - IEEE 802.3-2008 for Ethernet MAC, Media Independent Interface (MII), reduced Media Independent Interface (RMII)
    - IEEE 1588-2008 for precision networked clock synchronization
    - IEEE 802.1AS-2011 and 802.1-Qav-2009 for Audio Video (AV) traffic
    - IEEE 802.3az-2010 for Energy Efficient Ethernet (EEE) with MII interface
    - RMII specification version 1.2 from RMII consortium
    - Turbo MII, overclocked MII @200 Mbps
    - AMBA 2.0 for AHB master port and APB slave port
  - MAC Tx and Rx features:
    - Separate transmission, reception, and control interfaces to the application
    - 10, 100 Mbps data transfer rates with the following PHY interfaces:

      IEEE 802.3-compliant MII interface to communicate with an external Fast Ethernet PHY

      RMII interface to communicate with an external Fast Ethernet PHY
    - Half-duplex operation
    - Full-duplex flow control operations (IEEE 802.3x Pause packets and Priority flow control)
    - Network statistics with RMON or MIB Counters (RFC2819/RFC2665)
    - Support Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008. Both one-step and two-step timestamping is supported in TX direction
    - Flexibility to control the Pulse-Per-Second (PPS) output signal (ptp_pps_o)
    - MDIO (Clause 22 and Clause 45) master interface for PHY device configuration and management
  - MAC Tx features:
    - Source Address field insertion or replacement, VLAN insertion, replacement, and deletion in transmitted packets with per-packet or static-global control
  - MAC Rx features:
    - Automatic Pad and CRC Stripping options:
    - Option to disable Automatic CRC checking
    - Preamble and SFD deletion
    - Separate 112-bit or 128-bit status
    - Programmable watchdog timeout limit
    - Fixed address filtering modes:

      Up to 31 additional 48-bit perfect (DA) address filters with masks for each byte

      Up to 31 48-bit SA address comparison check with masks for each byte

      Option to pass all multi-cast addressed packets

      Promiscuous mode to pass all packets without any filtering for network monitoring

      Pass all incoming packets (as per filter) with a status report
    - Additional packet filtering:

VLAN tag-based: Perfect match and Hash-based filtering. Filtering based on either outer or inner VLAN tag is possible.

Layer 3 and Layer 4-based: TCP or UDP over IPv4 or IPv6

Extended VLAN tag based filtering with 16 filters

  - IEEE 802.1Q VLAN tag detection
- DMA block features:
  - 64-bit data transfers
  - 2-channel Transmit and Receive engines
  - Separate DMA channel in the Transmit path for each queue
  - Single or multiple DMA channels for any number of queues in Receive path
  - Optimization for packet-oriented DMA transfers with packet delimiters
  - Byte-aligned addressing for data buffer support
  - Dual-buffer (ring) descriptor support
  - Descriptor architecture to allow large blocks of data transfer with minimum CPU intervention (each descriptor can transfer up to 32 KB of data)
- Audio and video features:

  Ethernet0 can be used in Audio Video (AV) mode, and the supported features are compliant to the industry standards for AV traffic:
  - Separate channels or queues for AV data transfer in 100 Mbps
  - Up to 2- queues on the Receive paths for AV traffic and 1-queue on the Transmit path for AV traffic
  - IEEE 802.1-Qav specified credit-based shaper (CBS) algorithm for Transmit channels

• One ethernet controller 10/100/1000 Mbps (Ethernet 1)

  Features changes on top of Ethernet 0:
  - RGMII PHY interface with DoS on TX clock
  - Transaction layer supports 3-TX queues and 3 RX queues
  - DMA supports 3 TX and 3-RX channels
  - Checksum offload engine on TX Queue0 only
  - 16 KB each for both TX and RX FIFOs
  - 2 AV queues on TX and 3 AV queues on RX
  - MAC does not support half duplex operations
  - Flexible Receive Parsing based filtering mode:

    Programmable lookup table based flexible Parser for filtering all incoming packets as per the programmable instructions in the memory. partial/group DA/SA match (bit mask instead of byte mask). partial/group VLAN match (Only perfect match in fixed/register filter) link DA/SA filter with VLAN filter; fixed/register filter does not give that flexibility (sequential links) can do any of the fixed/register filter functions;

only difference is that, it can check for patterns sequentially (1 field at a time) unlike fixed/register filtering which can compare in parallel and at line rate.

- TSN features:

  IEEE 802.1Qbv (EST)

  IEEE 802.1AS-Rev/D2.0 (timing and synchronization)

  IEEE 802.3br/D3.1 (frame preemption)

  IEEE 802.1Qbu/D3.1 (frame preemption)

- SD/SDIO/MMC host interface that supports:
  - eMMC - MultiMedia Card Specification v4.51
    - 1-bit, 4-bit, 8-bit interface
    - Full backward compatibility with legacy MMC cards (0-25 MHz), 25 MB/s
    - Full High Speed SDR bus mode (0-50 MHz), 50 MB/s
    - Full High Speed DDR bus mode (0-50 MHz), 100 MB/s
    - 3.3 V IO voltage
  - SD Card Specification v3.01
    - Full support for Default Speed mode (0-25 MHz), 12.5 MB/s
    - Full support for High Speed (0-50 MHz) mode, 25 MB/s
    - 1-bit, 4-bit interface
    - 3.3 V IO voltage
  - SDIO Specification v3.0
    - Full support for Default Speed mode (0-25 MHz) mode, 12.5 MB/s
    - Full support for High Speed (0-50 MHz) mode, 25 MB/s
    - 1-bit or 4-bit interface
    - 3.3 V IO voltage

  The current version supports only one SD3.01/SDIO3.0/MMC4.51 card at any one time.
- OctalSPI host interface that supports:
  - SPI mode
    - 1-bit, 4-bit, 8-bit interface
    - SDR for 1 bit interface only (SPI mode)
    - SDR and DDR for 4 and 8 bits interface (quad and Octal SPI mode)
    - 3.3 V IO voltage
    - Clock up to 100 MHz
    - SPI NOR device with DQS mode compliant
  - Hyperbus(TM) bus mode
    - Compliant with “HyperBus™ Specification Low Signal Count, High Performance DDR Bus”, June 2017, revision F
    - DDR for 8-bit interface
    - 3.3 V IO voltage

  - Single-ended clock up to 100 MHz

  The current version supports up to two devices at any one time, which means it has to Chip selects sharing one 8 bits data bus.
- Low Power Supply options:
  - External Regulators (1.2 V core, 3.3 V–5 V IO)
  - Single internal Linear Regulator with external ballast
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard.
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- Standby power domain with smart wake-up sequence

3 Package pinouts and signal descriptions

Refer to the SPC58EHx, SPC58NHx IO_ Definition document.

It includes the following sections:

1. Package pinouts
2. Pin descriptions
   a) Power supply and reference voltage pins
   b) System pins
   c) Generic pins

4 Electrical characteristics

4.1 Introduction

The present document contains the target Electrical Specification for the 40 nm family 32-bit MCU SPC58EHx, SPC58NHx products.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” (Controller Characteristics) is included in the “Symbol” column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” (System Requirement) is included in the “Symbol” column.

The electrical parameters shown in this document are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 3* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 3. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design validation on a small sample size from typical devices.
D	Those parameters are derived mainly from simulations.

4.2 Absolute maximum ratings

Table 4 describes the maximum ratings for the device. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Stress beyond the listed maxima, even momentarily, may affect device reliability or cause permanent damage to the device.

Table 4. Absolute maximum ratings

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{DD_LV}	SR	D	Core voltage operating life range(1)	—	–0.3	—	1.4	V
$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_OSC}$ $V_{DD\_HV\_FLA}$ $V_{DD\_HV\_IO\_EMMC}$ $V_{DD\_HV\_IO\_ETH0}$ $V_{DD\_HV\_IO\_ETH1}$	SR	D	I/O supply voltage(2)	—	–0.3	—	6.0	V
$V_{SS\_HV\_ADV}$	SR	D	ADC ground voltage	Reference to digital ground	–0.3	—	0.3	V
$V_{DD\_HV\_ADV}$	SR	D	ADC Supply voltage(2)	Reference to $V_{SS\_HV\_ADV}$	–0.3	—	6.0	V
$V_{SS\_HV\_ADR\_S}$	SR	D	SAR ADC ground reference	—	–0.3	—	0.3	V
$V_{DD\_HV\_ADR\_S}$	SR	D	SAR ADC voltage reference(2)	Reference to $V_{SS\_HV\_ADR\_S}$	–0.3	—	6.0	V
V_{SS}-$V_{SS\_HV\_ADR\_S}$	SR	D	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–0.3	—	0.3	V
V_{SS}-$V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADV}$ differential voltage	—	–0.3	—	0.3	V
V_{IN}	SR	D	I/O input voltage range(2)(3) (4)	—	–0.3	—	6.0	V
				Relative to V_{SS}	–0.3	—	—	
				Relative to $V_{DD\_HV\_IO}$ and $V_{DD\_HV\_ADV}$	—	—	0.3	
T_{TRIN}	SR	D	Digital Input pad transition time(5)	—	—	—	1	ms

Table 4. Absolute maximum ratings (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{INJ}	SR	T	Maximum DC injection current for each analog/digital PAD[(6)]	—	–5	—	5	mA
T_{STG}	SR	T	Maximum non-operating Storage temperature range	—	–55	—	125	°C
T_{PAS}	SR	C	Maximum nonoperating temperature during passive lifetime	—	–55	—	150[(7)]	°C
$T_{STORAGE}$	SR	—	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 60 °C	—	—	20	years
T_{SDR}	SR	T	Maximum solder temperature Pb-free packaged[(8)]	—	—	—	260	°C
MSL	SR	T	Moisture sensitivity level[(9)]	—	—	—	3	—
T_{XRAY} dose	SR	T	Maximum cumulated XRAY dose	Typical range for X-rays source during inspection:80 ÷ 130 KV; 20 ÷ 50 µA	—	—	1	grey

1. V_{DD_LV}: allowed 1.335 V - 1.400 V for 60 seconds cumulative time at the given temperature profile. Remaining time allowed 1.260 V - 1.335 V for 10 hours cumulative time at the given temperature profile. Remaining time as defined in *Section 4.3: Operating conditions*.
2. V_{DD_HV}: allowed 5.5 V – 6.0 V for 60 seconds cumulative time at the given temperature profile, for 10 hours cumulative time with the device in reset at the given temperature profile. Remaining time as defined in *Section 4.3: Operating conditions*.
3. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3 V can be used for nominal calculations.
4. Relative value can be exceeded if design measures are taken to ensure injection current limitation (parameter IINJ).
5. This limitation applies to pads with digital input buffer enabled. If the digital input buffer is disabled, there are no maximum limits to the transition time.
6. The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in *Section 4.8.3: I/O pad current specifications*.

7. 175°C are allowed for limited time. Mission profile with passive lifetime temperature >150°C have to be evaluated by ST to confirm that are granted by product qualification.
8. Solder profile per IPC/JEDEC J-STD-020D.
9. Moisture sensitivity per JDEC test method A112.

4.3 Operating conditions

Table 5 describes the operating conditions for the device, and for which all the specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded or the functionality of the device is not guaranteed.

Table 5. Operating conditions

Symbol		C	Parameter	Conditions	Value[1] Min	Typ	Max	Unit
F_{SYS}[2]	SR	P	Operating system clock frequency[3]	—	—	—	200	MHz
$T_{A\_125\ Grade}$[4]	SR	D	Operating Ambient temperature	—	–40	—	125	°C
$T_{J\_125\ Grade}$[4]	SR	P	Junction temperature under bias	T_A = 125 °C	–40	—	150	°C
$T_{A\_105\ Grade}$[4]	SR	D	Ambient temperature under bias	—	–40	—	105	°C
$T_{J\_105\ Grade}$[4]	SR	D	Operating Junction temperature	T_A = 105 °C	–40	—	130	°C
V_{DD_LV}	SR	P	Core supply voltage[5]	—	1.14	1.20	1.26[6] [7]	V
$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_IO\_EMMC}$ $V_{DD\_HV\_IO\_ETH0}$ $V_{DD\_HV\_IO\_ETH1}$ $V_{DD\_HV\_FLA}$ $V_{DD\_HV\_OSC}$	SR	P	IO supply voltage	—	3.0	—	5.5	V
$V_{DD\_HV\_ADV}$	SR	P	ADC supply voltage	—	3.0	—	5.5	V
$V_{SS\_HV\_ADV}$-V_{SS}	SR	D	ADC ground differential voltage	—	–25	—	25	mV
$V_{DD\_HV\_ADR\_S}$	SR	P	SAR ADC reference voltage	—	3.0	—	5.5	V
$V_{DD\_HV\_ADR\_S}$-$V_{DD\_HV\_ADV}$	SR	D	SAR ADC reference differential voltage	—	—	—	25	mV
$V_{SS\_HV\_ADR\_S}$	SR	P	SAR ADC ground reference voltage	—	$V_{SS\_HV\_ADV}$			V

Table 5. Operating conditions (continued)

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
$V_{SS\_HV\_ADR\_S}$-$V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–25	—	25	mV
V_{RAMP_LV}	SR	D	Slew rate on core power supply pins	V_{DD_LV}	—	—	20	V/ms
V_{RAMP_HV}	SR	D	Slew rate on HV power supply	—	—	—	100	V/ms
V_{IN}	SR	P	I/O input voltage range	—	0	—	5.5	V
I_{INJ1}	SR	T	Injection current (per pin) without performance degradation(8) (9) (10)	Digital pins and analog pins	–3.0	—	3.0	mA
I_{INJ2}	SR	D	Dynamic Injection current (per pin) with performance degradation(10) (11)	Digital pins and analog pins	–10	—	10	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. The PRAM pipeline gasket has to be kept enabled through bit PCM*/BYP_GSKT_XBAR*_TO_PRAMC* to keep system work at maximum speed; The maximum frequency will go to half if the pipeline gasket is bypassed.
3. Maximum operating frequency is applicable to the cores and platform of the device. See the Clock Chapter in the Microcontroller Reference Manual for more information on the clock limitations for the various IP blocks on the device.
4. In order to evaluate the actual difference between ambient and junction temperatures in the application, refer to *Section 5.5: Package thermal characteristics*.
5. Core voltage as measured on device pin to guarantee published silicon performance.
6. Core voltage can exceed 1.26 V with the limitations provided in *Section 4.2: Absolute maximum ratings*, provided that HVD134_C monitor reset is disabled.
7. 1.260 V - 1.290 V range allowed periodically for supply with sinusoidal shape and average supply value below or equal to 1.236 V at the given temperature profile.
8. Full device lifetime. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See *Section 4.2: Absolute maximum ratings* for maximum input current for reliability requirements.
9. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pins is above the supply rail, current will be injected through the clamp diode to the supply rails. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
10. The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in *Section 4.8.3: I/O pad current specifications*.
11. Positive and negative Dynamic current injection pulses are allowed up to this limit. See the dedicated chapters for the different specification limits. See the Absolute Maximum Ratings table for maximum input current for reliability requirements. Refer to the following pulses definitions: Pulse1 (ISO 7637-2:2011), Pulse 2a (ISO 7637-2:2011 5.6.2), Pulse 3a (ISO 7637-2:2011 5.6.3), Pulse 3b (ISO 7637-2:2011 5.6.3).

4.3.1 Power domains and power up/down sequencing

The following table shows the constraints and relationships for the different power domains. Supply1 (on rows) can exceed Supply2 (on columns), only if the cell at the given row and column is reporting ‘ok’. This limitation is valid during power-up and power-down phases, as well as during normal device operation.

Table 6. Device supply relation during power-up/power-down sequence

		Supply2						
		V_{DD_LV}	$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_FLA}$ $V_{DD\_HV\_OSC}$	$V_{DD\_HV\_IO\_ETH0}$	$V_{DD\_HV\_IO\_ETH1}$	$V_{DD\_HV\_IO\_EMMC}$	$V_{DD\_HV\_ADV}$	$V_{DD\_HV\_ADR}$
Supply1	V_{DD_LV}(1)		ok	ok	ok	ok	ok	ok
	$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_FLA}$ $V_{DD\_HV\_OSC}$(2)	ok		ok	ok	ok	ok	ok
	$V_{DD\_HV\_IO\_ETH0}$	ok	not allowed		ok	ok	ok	ok
	$V_{DD\_HV\_IO\_ETH1}$	ok	not allowed	ok		ok	ok	ok
	$V_{DD\_HV\_IO\_EMMC}$	ok	not allowed	ok	ok		ok	ok
	$V_{DD\_HV\_ADV}$	ok	not allowed	ok	ok	not allowed		ok
	$V_{DD\_HV\_ADR}$	ok	not allowed	ok	ok	not allowed	not allowed	

1. V_{DD_LV} can be higher than V_{DD_HV} supplies only during power-up/down transient ramps, in case of external LV regulator and if V_{DD_HV} supply voltage level is lower than V_{DD_LV} allowed max operating condition.
2. The application shall grant that these supplies are always at the same voltage level.

During power-up, all functional terminals are maintained in a known state as described in the device pinout Microsoft Excel file attached to the IO_Definition document.

4.4 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device:

- All ESD testing are in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits,
- Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which include the complete DC parametric and functional testing at room temperature and hot temperature, maximum DC parametric variation within 10% of maximum specification”.

Table 7. ESD ratings

Parameter	C	Conditions	Value	Unit
ESD for Human Body Model (HBM)(1)	T	All pins	2000	V
ESD for field induced Charged Device Model (CDM)(2)	T	All pins	500	V
	T	Corner Pins	750	V

1. This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing.
2. This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level.

4.5 Electromagnetic compatibility characteristics

EMC measurements at IC-level IEC standards are available from STMicroelectronics on request.

4.6 Temperature profile

The device is qualified in accordance to AEC-Q100 Grade1 requirements, such as HTOL 1,000 h and HTDR 1,000 hrs, T_J = 150 °C.

Mission profile exceeding AEC-Q100 Grade 1, and with junction Temperature equal or lower than 150 °C have to be evaluated by ST to confirm that are covered by product qualification. Contact your STMicroelectronics Sales representative for validation.

4.7 Device consumption

Table 8. Device consumption

Symbol		C	Parameter	Conditions	Value[1] Min	Typ	Max	Unit
I_{DD_LKG}[2],[3]	CC	C	Leakage current on the V_{DD_LV} supply	T_J = 40 °C	—	—	24	mA
		D		T_J = 25 °C	—	—	16	
		D		T_J = 55 °C	—	—	36	
		D		T_J = 95 °C	—	—	110	
		D		T_J = 120 °C	—	—	220	
		P		T_J = 150 °C	—	—	500	
I_{DD_LV}[3]	CC	P	Dynamic current on the V_{DD_LV} supply, very high consumption profile[4]	—	—	—	550	mA
I_{DD_HV}	CC	P	Total current on the V_{DD_HV} supply[4]	f_{MAX}	—	—	100	mA
$I_{DD\_LV\_GW}$	CC	T	Dynamic current on the V_{DD_LV} supply, gateway profile[5]	—	—	—	350	mA
$I_{DD\_HV\_GW}$	CC	T	Dynamic current on the V_{DD_HV} supply, gateway profile[5],[6]	—	—	—	35	mA
$I_{DD\_LV\_BCM}$	CC	T	Dynamic current on the V_{DD_LV} supply, body profile[7]	—	—	—	285	mA
$I_{DD\_HV\_BCM}$	CC	T	Dynamic current on the V_{DD_HV} supply, body profile[7],[6]	—	—	—	40	mA
$I_{DD\_MAIN\_CORE\_AC}$	CC	T	Main Core dynamic current[8]	f_{MAX}	—	—	55	mA
$I_{DD\_CHKR\_CORE\_AC}$	CC	T	Checker Core dynamic operating current	f_{MAX}	—	—	35	mA
$I_{DD\_HSM\_AC}$	CC	T	HSM platform dynamic operating current[9]	$f_{MAX}/2$	—	—	30	mA
I_{DDHALT}[10]	CC	T	Dynamic current on the V_{DD_LV} supply +Total current on the V_{DD_HV} supply	—	—	106	150	mA
I_{DDSTOP}[11]	CC	T	Dynamic current on the V_{DD_LV} supply +Total current on the V_{DD_HV} supply	—	—	14.5	60	mA

Table 8. Device consumption (continued)

Symbol		C	Parameter	Conditions	Value[1] Min	Value[1] Typ	Value[1] Max	Unit
$I_{DDSTBY8}$[12]	CC	D	Total standby mode current on V_{DD_LV} and V_{DD_HV} supply, 8 KB RAM[13]	T_J = 25 °C	—	130	380	µA
		C		T_J = 40 °C	—	—	550	µA
		D		T_J = 55 °C	—	—	820	µA
		D		T_J = 120 °C	—	1.37	4	mA
		P		T_J = 150 °C	—	2.9	8	mA
$I_{DDSTBY128}$[12]	CC	D	Total standby mode current on V_{DD_LV} and V_{DD_HV} supply, 128 KB RAM[13]	T_J = 25 °C	—	150	530	µA
		C		T_J = 40 °C	—	—	790	µA
		D		T_J = 55 °C	—	—	1.2	mA
		D		T_J = 120 °C	—	—	5.5	mA
		P		T_J = 150 °C	—	—	11	mA
$I_{DDSTBY256}$[12]	CC	D	Total standby mode current on V_{DD_LV} and V_{DD_HV} supply, 256 KB RAM[13]	T_J = 25 °C	—	190	680	µA
		C		T_J = 40 °C	—	—	1	mA
		D		T_J = 55 °C	—	—	1.5	mA
		D		T_J = 120 °C	—	2.3	7	mA
		P		T_J = 150 °C	—	5	14	mA
$I_{DDSSWU1}$	CC	D	SSWU running over all STANDBY period with OPC/TU commands execution and keeping ADC off[14]	T_J = 40 °C	—	1	3.5	mA
$I_{DDSSWU2}$	CC	D	SSWU running over all STANDBY period with OPC/TU/ADC commands execution and keeping ADC on[15]	T_J = 40 °C	—	3.5	5	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. The leakage considered is the sum of core logic and RAM memories. The contribution of analog modules is not considered, and they are computed in the dynamic I_{DD_LV} and I_{DD_HV} parameters.
3. I_{DD_LKG} (leakage current) and I_{DD_LV} (dynamic current) are reported as separate parameters, to give an indication of the consumption contributors. The tests used in validation, characterization and production are verifying that the total consumption (leakage + dynamic) is lower or equal to the sum of the maximum values provided (I_{DD_LKG} + I_{DD_LV}). The two parameters, measured separately, may exceed the maximum reported for each, depending on the operative conditions and the software profile used.
4. Use case: 3 x e200Z4 @200 MHz with all locksteps on, HSM @100 MHz, all IPs clock enabled, Flash access with prefetch disabled, Flash consumption includes parallel read and program/erase, all SARADC in continuous conversion, DMA continuously triggered by ADC conversion, 4 DSPI / 8 CAN / 8 LINFlex / FlexRay / ENET0 / ENET1 / eMMC and OctoSPI transmitting, RTC and STM running, 2 x EMIOS running (8 channels in OPWMT mode), FIRC, SIRC, FXOSC, PLL0-1 running. The switching activity estimated for dynamic consumption does not include I/O toggling, which is highly dependent on the application. Details of the software configuration are available separately. The total device consumption is I_{DD_LV} + I_{DD_HV} + I_{DD_LKG} for the selected temperature.
5. GW use case: three cores running @200 MHz, no lockstep, HSM @100 MHz, INTC enabled, 1 EDMA triggered by ADC, PLL0 @200 MHz PLL1 @200 MHz, XOSC = 8/40 MHz, FLASH read only 25%, 12 x CAN running @40 MHz data 4 Mbps/1 Mbps/500 Kbps, 2 x SARADC running @15 MHz with 16 conversion channels, ETH 1 Gbps, OctoSPI @200 Mhz data 100 MB/sec, all other peripherals frozen.

6. $I_{DD\_HV\_BCM}$ and $I_{DD\_HV\_GW}$ consumption measured is averaged in time, by considering non-concurrent peaks from all the IP contributors (ADCs, FLASH, PADS, PMC, TSENS, Oscillators). Please consider IDD_HV parameter as peak value. IO consumption contribution may vary, depending on the application loads differences vs the validation board used.
7. BCM use case: two cores running @160 MHz, no lockstep, HSM @80 MHz, INTC enabled, 1 EDMA triggered by ADC, PLL0 @200 MHz PLL1 @160 MHz, XOSC = 8/40 MHz, FLASH read only 25%, 4 x CAN running @40 MHz data 4 Mbps, 5 x DSPI running @100 MHz data 4 Mbps, 2 EMIOS running @100 MHz - 12 PWM period=3 KHz, 5 x SARADC running @15 MHz with 23 conversion channels, 10 LIN/UART baud-rate 115200, all other peripherals frozen.
8. Dynamic consumption of one core, including the dedicated I/D-caches and I/D-MEMS contribution.
9. Dynamic consumption of the HSM module, including the dedicated memories, during the execution of Electronic Code Book crypto algorithm on 1 block of 16 byte of shared RAM.
10. Flash in Low Power. Sysclk at 160 MHz, PLL0_PHI at 160 MHz, XTAL at 40 MHz, FIRC 16 MHz ON, RCOSC1M off. MCAN: instances: 0, 1, 2, 3, 4, 5, 6 ON (configured but no reception or transmission), Ethernet ON (configured but no reception or transmission), ADC ON (continuously converting). All others IPs clock-gated.
11. Sysclk = RC16 MHz, RC16 MHz ON, RC1 MHz ON, PLL OFF. All possible peripherals off and clock gated. Flash in power down mode.
12. The consumption numbers shown here in IDD standby section are considering standby regulator specs, in case of external regulator mode, the consumption numbers can be higher.
13. STANDBY mode: device configured for minimum consumption, RC16 MHz off, RC1 MHz on.
14. SSWU1 mode adder: FIRC = ON, SSWU clocked at 8 MHz and running over all STANDBY period, ADC off. The total standby consumption can be obtained by adding this parameter to the IDDSTBY parameter for the selected memory size and temperature.
15. SSWU2 mode adder: FIRC = ON, SSWU clocked at 8 MHz and running over all STANDBY period, ADC on in continuous conversion. The total standby consumption can be obtained by adding this parameter to the I_{DDSTBY} parameter for the selected memory size and temperature.

4.8 I/O pad specification

The following table describes the different pad type configurations.

Table 9. I/O pad specification descriptions

Pad type	Description
Weak configuration	Provides a good compromise between transition time and low electromagnetic emission.
Medium configuration	Provides transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
Strong configuration	Provides fast transition speed; used for fast interface.
Very strong configuration	Provides maximum speed and controlled symmetric behavior for rise and fall transition. Used for fast interface including Ethernet, SDMMC, OctalSPI and FlexRay interfaces requiring fine control of rising/falling edge jitter.
Ultra strong configuration	Provides very high speed interfaces till 125 MHz. Used for fast interface including Ethernet, SDMMC, OctalSPI and FlexRay interfaces.
Input only pads	These low input leakage pads are associated with the ADC channels.
Standby pads	These pads (LP pads) are active during STANDBY. They are configured in CMOS level logic and this configuration cannot be changed. Moreover, when the device enters the STANDBY mode, the pad-keeper feature can be activated for LP pads. It means that: – if the pad voltage level is above the pad keeper high threshold, a weak pull-up resistor is automatically enabled – if the pad voltage level is below the pad keeper low threshold, a weak pull-down resistor is automatically enabled. For the pad-keeper high/low thresholds please consider (VDD_HV_IO_MAIN / 2) +/-20%.

Note: Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin. PMC_DIG_VSIO register has to be configured to select the voltage level (3.3 V or 5.0 V) for each IO segment.

Logic level is configurable in running mode while it is CMOS not-configurable in STANDBY for LP (low power) pads, so if a LP pad is used to wakeup from STANDBY, it should be configured as CMOS also in running mode in order to prevent device wrong behavior in STANDBY.

The SPC58EHx, SPC58NHx microcontroller has many GPIOs in double bonding; this feature is in place for all packages but FPBGA386. Indeed some IO PADS are bonded together within the package, in order to provide different alternative functions to the same pin/ball.

The application shall enable only one pad at a time for each pin/ball in double bonding, in order to avoid high current consumption, due to electrical contention, and reliability issues of the pad drivers.

Refer to the SPC58EHx, SPC58NHx IO_ definition document, where double bonded ball/pins are clearly identified, paying attention during software design to strictly avoid the above situation depicted of electrical contention.

4.8.1 I/O input DC characteristics

The following table provides input DC electrical characteristics, as described in *Figure 3*.

Figure 3. I/O input electrical characteristics

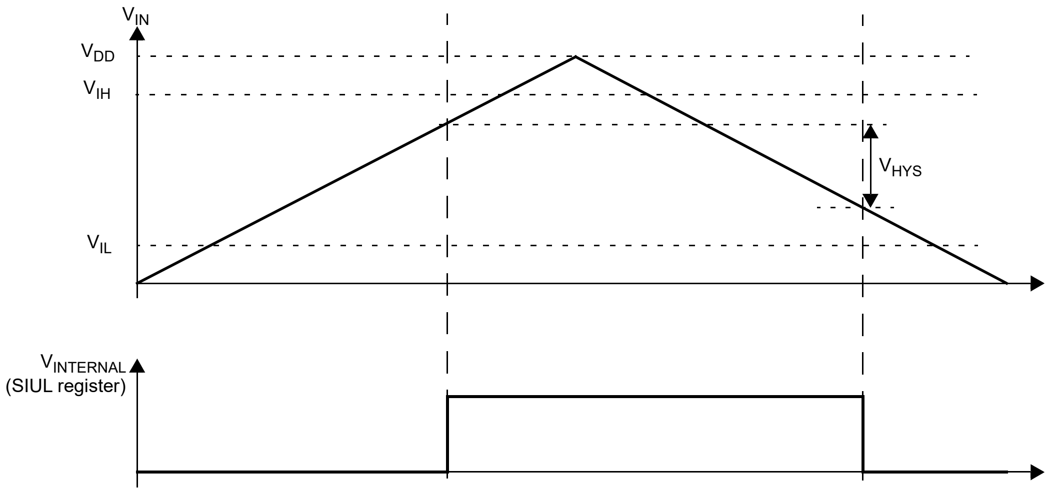


Table 10. I/O input electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
TTL								
V_{ihttl}	SR	P	Input high level TTL	—	2	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ilttl}	SR	P	Input low level TTL	—	–0.3	—	0.8	V
V_{hysttl}	CC	C	Input hysteresis TTL	—	0.3	—	—	V
CMOS								
V_{ihcmos}	SR	P	Input high level CMOS	—	0.65 * V_{DD}	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ilcmos}	SR	P	Input low level CMOS	—	–0.3	—	0.35 * V_{DD}	V
$V_{hyscmos}$	CC	C	Input hysteresis CMOS	—	0.10 * V_{DD}	—	—	V
COMMON								
I_{LKG}	CC	P	Pad input leakage	INPUT-ONLY pads T_J = 150 °C	—	—	200	nA
I_{LKG}	CC	P	Pad input leakage	MEDIUM pads T_J = 150 °C	—	—	360	nA
I_{LKG}	CC	P	Pad input leakage	STRONG pads T_J = 150 °C	—	—	1,000	nA

Table 10. I/O input electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{LKG}	CC	P	Pad input leakage	VERY STRONG pads, T_J = 150 °C	—	—	1,000	nA
I_{LKG}	CC	P	Pad input leakage	ULTRA STRONG pads, T_J = 150 °C	—	—	1,000	nA
C_{P1}	CC	D	Pad capacitance	—	—	—	10	pF
V_{drift}	CC	D	Input V_{il}/V_{ih} temperature drift	In a 1 ms period, with a temperature variation <30 °C	—	—	100	mV
W_{FI}	SR	C	Wakeup input filtered pulse(1)	—	—	—	20	ns
W_{NFI}	SR	C	Wakeup input not filtered pulse(1)	—	400	—	—	ns

1. In the range from W_{FI} (max) to W_{NFI} (min), pulses can be filtered or not filtered, according to operating temperature and voltage. Refer to the device pinout IO definition excel file for the list of pins supporting the wakeup filter feature.

Table 11. I/O pull-up/pull-down electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{WPU}	CC	T	Weak pull-up current absolute value	V_{IN} = 1.1 V(1)	—	—	130	µA
		P		V_{IN} = 0.69 * $V_{DD\_HV\_IO}$(2)	15	—	—	
R_{WPU}	CC	D	Weak Pull-up resistance	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	33	—	93	KΩ
R_{WPU}	CC	D	Weak Pull-up resistance	$V_{DD\_HV\_IO}$ = 3.3 V ± 10%	19	—	62	KΩ
I_{WPD}	CC	T	Weak pull-down current absolute value	V_{IN} = 0.69 * $V_{DD\_HV\_IO}$(1)	—	—	130	µA
		P		V_{IN} = 0.9 V(2)	15	—	—	
R_{WPD}	CC	D	Weak Pull-down resistance	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	29	—	60	KΩ
R_{WPD}	CC	D	Weak Pull-down resistance	$V_{DD\_HV\_IO}$ = 3.3 V ± 10%	19	—	60	KΩ

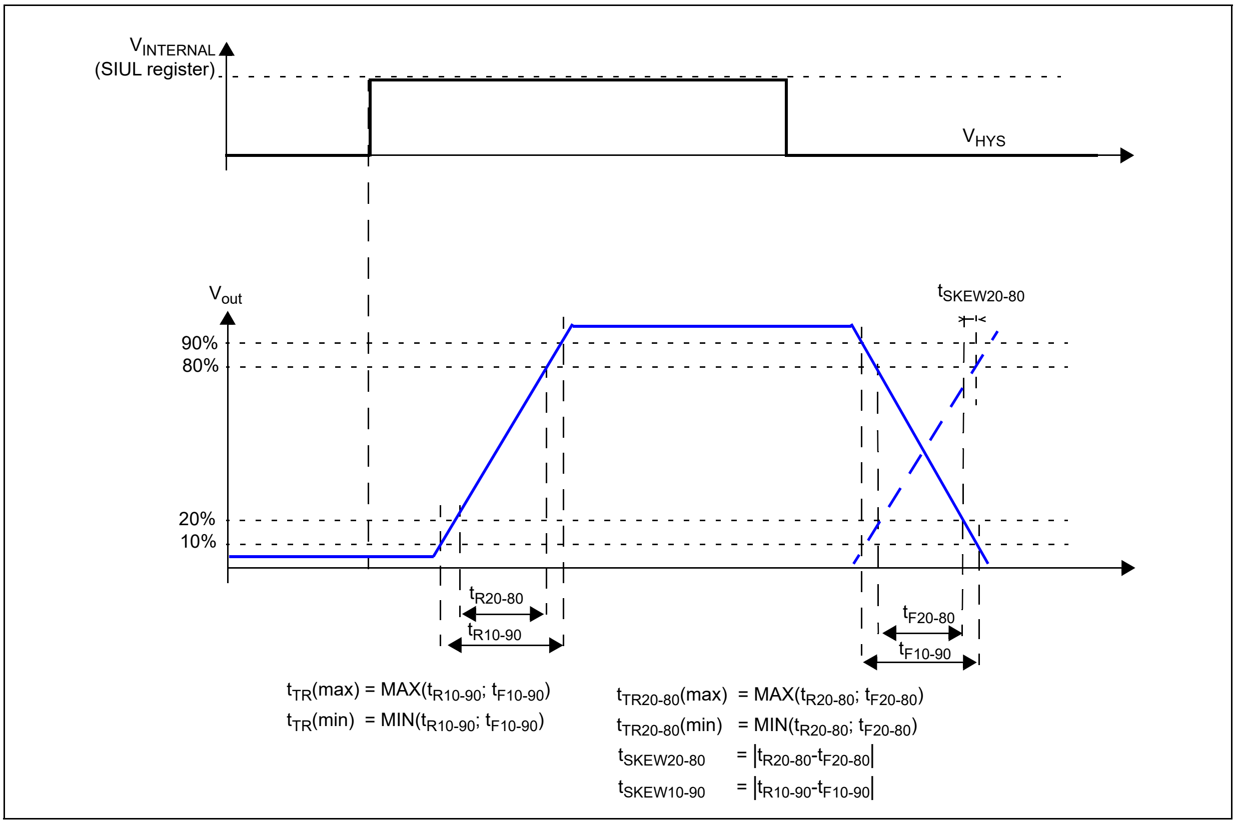
1. Maximum current when forcing a change in the pin level opposite to the pull configuration.
2. Minimum current when keeping the same pin level state than the pull configuration.

Note: When the device enters into standby mode, the LP pads have the input buffer switched-on. As a consequence, if the pad input voltage VIN is V_{SS}<V_{IN}<V_{DD_HV}, an additional consumption can be measured in the VDD_HV domain. The highest consumption can be seen around mid-range (VIN ~=VDD_HV/2), 2-3 mA depending on process, voltage and temperature.
This situation may occur if the PAD is used as a ADC input channel, and V_{SS}<V_{IN}<V_{DD_HV}. The applications should ensure that LP pads are always set to VDD_HV or VSS, to avoid the extra consumption. Please refer to the device pinout IO definition excel file to identify the low-power pads which also have an ADC function.

4.8.2 I/O output DC characteristics

Figure 4 provides description of output DC electrical characteristics.

Figure 4. I/O output DC electrical characteristics definition



The following tables provide DC characteristics for bidirectional pads:

- *Table 12* provides output driver characteristics for I/O pads when in WEAK/SLOW configuration.
- *Table 13* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 14* provides output driver characteristics for I/O pads when in STRONG/FAST configuration.
- *Table 15* provides output driver characteristics for I/O pads when in VERY STRONG/VERY FAST configuration.
- *Table 16* provides output driver characteristics for I/O pads when in ULTRA STRONG/ULTRA FAST configuration.

Note: 10%/90% is the default condition for any parameter if not explicitly mentioned differently.

Table 12. WEAK/SLOW I/O output characteristics

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
V_{ol_W}	CC	D	Output low voltage for Weak type PADs	I_{ol} = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	0.1*V_{DD}	V
V_{oh_W}	CC	D	Output high voltage for Weak type PADs	Ioh = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	0.9*V_{DD}	—	—	V
$R_{\_W}$	CC	P	Output impedance for Weak type PADs	V_{DD} = 5.0 V ± 10%	380	—	1040	Ω
				V_{DD} = 3.3 V ± 10%	250	—	700	
F_{max_W}	CC	T	Maximum output frequency for Weak type PADs	CL = 25 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	2	MHz
				CL = 50 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	1	MHz
t_{TR_W}	CC	T	Transition time output pin weak configuration, 10%-90%	CL = 25 pF V_{DD} = 5.0 V + 10% V_{DD} = 3.3 V + 10%	25	—	120	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10 % V_{DD} = 3.3 V ± 10 %	50	—	240	ns
$\|t_{SKEW\_W}\|$	CC	T	Difference between rise and fall time, 90%-10%	—	—	—	25	%
I_{DCMAX_W}	CC	D	Maximum DC current	V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	0.5	mA

Table 13. MEDIUM I/O output characteristics

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
V_{ol_M}	CC	D	Output low voltage for Medium type PADs	I_{ol} = 2.0 mA V_{DD} =5.0 V ± 10 % V_{DD} =3.3 V ± 10 %	—	—	0.1*V_{DD}	V
V_{oh_M}	CC	D	Output high voltage for Medium type PADs	I_{oh}=2.0 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	0.9*V_{DD}	—	—	V
$R_{\_M}$	CC	P	Output impedance for Medium type PADs	V_{DD} = 5.0 V ± 10%	90	—	260	Ω
				V_{DD} = 3.3 V ± 10%	60	—	170	
F_{max_M}	CC	T	Maximum output frequency for Medium type PADs	CL = 25 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	12	MHz
				CL = 50 pF V_{DD} = 5.0 V ± 10 % V_{DD} = 3.3 V ± 10 %	—	—	6	MHz
t_{TR_M}	CC	T	Transition time output pin MEDIUM configuration, 10%-90%	CL = 25 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	8	—	30	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	12	—	60	ns
$\|t_{SKEW\_M}\|$	CC	T	Difference between rise and fall time, 90%-10%	—	—	—	25	%
I_{DCMAX_M}	CC	D	Maximum DC current	V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	2	mA

Table 14. STRONG/FAST I/O output characteristics

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
V_{ol_S}	CC	D	Output low voltage for Strong type PADs	I_{ol} = 8.0 mA V_{DD} = 5.0 V ± 10%	—	—	0.1*V_{DD}	V
				I_{ol} = 5.5 mA V_{DD} =3 .3 V ± 10%	—	—	0.15*V_{DD}	V

Table 14. STRONG/FAST I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
V_{oh_S}	CC	D	Output high voltage for Strong type PADs	I_{oh} = 8.0 mA V_{DD} = 5.0 V ± 10%	0.9*V_{DD}	—	—	V
				I_{oh} = 5.5 mA V_{DD} = 3.3 V ± 10%	0.85*V_{DD}	—	—	V
$R_{\_S}$	CC	P	Output impedance for Strong type PADs	V_{DD} = 5.0 V ± 10%	20	—	65	Ω
				V_{DD} = 3.3 V ± 10%	28	—	90	
F_{max_S}	CC	T	Maximum output frequency for Strong type PADs	CL = 25 pF V_{DD}=5.0 V ± 10%	—	—	50	MHz
				CL = 50 pF V_{DD}=5.0 V ± 10%	—	—	25	MHz
				CL = 25 pF V_{DD} = 3.3 V ± 10%	—	—	25	MHz
				CL = 50 pF V_{DD} = 3.3 V ± 10%	—	—	12.5	MHz
t_{TR_S}	CC	T	Transition time output pin STRONG configuration, 10%-90%	CL = 25 pF V_{DD} = 5.0 V ± 10%	3	—	10	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10%	5	—	16	
				CL = 25 pF V_{DD} = 3.3 V ± 10%	1.5	—	15	
				CL = 50 pF V_{DD} = 3.3 V ± 10%	2.5	—	26	
I_{DCMAX_S}	CC	D	Maximum DC current	V_{DD} = 5 V ± 10%	—	—	8	mA
				V_{DD} = 3.3 V ± 10%	—	—	5.5	
$\lvert t_{SKEW\_S} \rvert$	CC	T	Difference between rise and fall time, 90%-10%	—	—	—	25	%

Table 15. VERY STRONG/VERY FAST I/O output characteristics

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
V_{ol_V}	CC	D	Output low voltage for Very Strong type PADs	I_{ol} = 9.0 mA V_{DD} =5.0 V ± 10%	—	—	0.1*V_{DD}	V
				I_{ol} = 9.0 mA V_{DD} =3.3 V ± 10%	—	—	0.15*V_{DD}	V

Table 15. VERY STRONG/VERY FAST I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{oh_V}	CC	D	Output high voltage for Very Strong type PADs	I_{oh} = 9.0 mA V_{DD} = 5.0 V ± 10%	0.9*V_{DD}	—	—	V
				I_{oh} = 9.0 mA V_{DD} = 3.3 V ± 10%	0.85*V_{DD}	—	—	V
$R_{\_V}$	CC	P	Output impedance for Very Strong type PADs	V_{DD} = 5.0 V ± 10%	20	—	60	Ω
				V_{DD} = 3.3 V ± 10%	18	—	50	
F_{max_V}	CC	T	Maximum output frequency for Very Strong type PADs	CL = 25 pF V_{DD} = 5.0 V ± 10%	—	—	50	MHz
				CL = 50 pF V_{DD} = 5.0 V ± 10%	—	—	25	MHz
				CL = 25 pF V_{DD} = 3.3 V ± 10%	—	—	50	MHz
				CL = 50 pF V_{DD} = 3.3 V ± 10%	—	—	25	MHz
t_{TR_V}	CC	T	10–90% threshold transition time output pin VERY STRONG configuration	CL = 25 pF V_{DD} = 5.0 V ± 10%	1	—	6	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10%	3	—	12	
				CL = 25 pF V_{DD} = 3.3 V ± 10%	1.5	—	6	
				CL = 50 pF V_{DD} = 3.3 V ± 10%	3	—	11	
$t_{TR20\text{-}80\_V}$	CC	T	20–80% threshold transition time output pin VERY STRONG configuration (Flexray Standard)	CL = 25 pF V_{DD} = 5.0 V ± 10%	0.8	—	4.5	ns
				CL = 15 pF V_{DD} = 3.3 V ± 10%	1	—	4.5	
t_{TRTTL_V}	CC	T	TTL threshold transition time for output pin in VERY STRONG configuration (Ethernet standard)	CL = 25 pF V_{DD} = 3.3 V ± 10%	0.88	—	5	ns

Table 15. VERY STRONG/VERY FAST I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\Sigma t_{TR20\text{-}80\_V}$	CC	T	Sum of transition time 20–80% output pin VERY STRONG configuration	CL = 25 pF V_{DD} = 5.0 V ± 10%	—	—	9	ns
				CL = 15 pF V_{DD} = 3.3 V ± 10%	—	—	9	
$\|t_{SKEW\_V}\|$	CC	T	Difference between rise and fall delay	CL = 25 pF V_{DD} = 5.0 V ± 10%	0	—	1.2	ns
I_{DCMAX_V}	CC	D	Maximum DC current	V_{DD} = 5.0 V±10% V_{DD} = 3.3 V ± 10%	—	—	9	mA

Table 16. ULTRA STRONG/ULTRA FAST I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_U}	CC	D	Output low voltage for ULTRA STRONG type PADs	I_{ol} = 9.0 mA V_{DD} =5.0 V ± 10%	—	—	0.1*V_{DD}	V
				I_{ol} = 9.0 mA V_{DD} =3.3 V ± 10%	—	—	0.15*V_{DD}	V
V_{oh_U}	CC	D	Output high voltage for ULTRA STRONG type PADs	I_{oh} = 9.0 mA V_{DD} = 5.0 V ± 10%	0.9*V_{DD}	—	—	V
				I_{oh} = 9.0 mA V_{DD} = 3.3 V ± 10%	0.85*V_{DD}	—	—	V
$R_{\_U}$	CC	P	Output impedance for ULTRA STRONG type PADs	V_{DD} = 5.0 V ± 10%	20	—	60	Ω
				V_{DD} = 3.3 V ± 10%	16	—	45	
F_{max_U}	CC	T	Maximum output frequency for ULTRA STRONG type PADs	CL = 8 pF V_{DD} = 3.3 V ± 10%	—	—	125	MHz
				CL = 25 pF V_{DD} = 5.5 V ± 10%	—	—	50	MHz
				CL = 50 pF V_{DD} = 5.5 V ± 10%	—	—	25	MHz

Table 16. ULTRA STRONG/ULTRA FAST I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
t_{TR_U}	CC	T	10–90% threshold transition time output pin ULTRA STRONG configuration	CL = 25 pF V_{DD} = 5.0 V ± 10%	1	—	6	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10%	2	—	12	
				CL = 25 pF V_{DD} = 3.3 V ± 10%	1	—	6	
				CL = 50 pF V_{DD} = 3.3 V ± 10%	2	—	11	
$t_{TR20\text{-}80\_U}$	CC	T	20–80% threshold transition time output pin ULTRA STRONG configuration	CL = 25 pF V_{DD} = 5.0 V ± 10%	0.8	—	4.5	ns
				CL = 8 pF Td = 0.25 ns Zo = 50 Ω V_{DD} = 3.3 V ± 10%	—	—	1	
t_{TRTTL_U}	CC	T	TTL threshold transition time for output pin in ULTRA STRONG configuration (Ethernet standard)	CL = 25 pF V_{DD} = 3.3 V ± 10%	0.88	—	5	ns
$\Sigma t_{TR20\text{-}80\_U}$	CC	T	Sum of transition time 20–80% output pin ULTRA STRONG configuration	CL = 25 pF V_{DD} = 5.0 V ± 10%	—	—	9	ns
				CL = 15 pF V_{DD} = 3.3 V ± 10%	—	—	9	
$\lvert t_{SKEW\_U} \rvert$	CC	T	Difference between rise and fall delay	CL = 25 pF V_{DD} = 5.0 V ± 10%	0	—	1.2	ns
I_{DCMAX_U}	CC	D	Maximum DC current	V_{DD} = 5.0 V±10% V_{DD} = 3.3 V ± 10%	—	—	9	mA

4.8.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in the device pinout Microsoft Excel file attached to the IO_Definition document.

Table 17 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{RMSSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Pad mapping on each segment can be optimized using the pad usage information provided on the I/O Signal Description table.

Table 17. I/O consumption

Symbol		C	Parameter	Conditions	Value[1]			Unit
					Min	Typ	Max	
Average consumption[2]								
I_{RMSSEG}	SR	D	Sum of all the DC I/O current within a supply segment	—	—	—	80	mA
I_{RMS_W}	CC	D	RMS I/O current for WEAK configuration	C_L = 25 pF, 2 MHz, V_{DD} = 5.0 V ± 10 %	—	—	1.1	mA
				C_L = 50 pF, 1 MHz, V_{DD} = 5.0 V ± 10 %	—	—	1.1	
				C_L = 25 pF, 2 MHz, V_{DD} = 3.3 V ± 10 %	—	—	1.0	
				C_L = 25 pF, 1 MHz, V_{DD} = 3.3 V ± 10%	—	—	1.0	
I_{RMS_M}	CC	D	RMS I/O current for MEDIUM configuration	C_L = 25 pF, 12 MHz, V_{DD} = 5.0 V ± 10%	—	—	5.5	mA
				C_L = 50 pF, 6 MHz, V_{DD} = 5.0 V ± 10%	—	—	5.5	
				C_L = 25 pF, 12 MHz, V_{DD} = 3.3 V ± 10%	—	—	4.2	
				C_L = 25 pF, 6 MHz, V_{DD} = 3.3 V ± 10%	—	—	4.2	
I_{RMS_S}	CC	D	RMS I/O current for STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0 V ± 10%	—	—	21	mA
				C_L = 50 pF, 25 MHz, V_{DD} = 5.0 V ± 10%	—	—	21	
				C_L = 25 pF, 25 MHz, V_{DD} = 3.3 V ± 10%	—	—	10	
				C_L = 25 pF, 12.5 MHz, V_{DD} = 3.3 V ± 10%	—	—	10	
I_{RMS_V}	CC	D	RMS I/O current for VERY STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0 V ± 10%	—	—	23	mA
				C_L = 50 pF, 25 MHz, V_{DD} = 5.0 V ± 10%	—	—	23	
				C_L = 25 pF, 50 MHz, V_{DD} = 3.3 V ± 10%	—	—	16	
				C_L = 25 pF, 25 MHz, V_{DD} = 3.3 V ± 10%	—	—	16	

Table 17. I/O consumption (continued)

Symbol		C	Parameter	Conditions	Value(1) Min	Typ	Max	Unit
I_{RMS_U}	CC	D	RMS I/O current for ULTRA STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0 V ± 10%	—	—	23	mA
				C_L = 50 pF, 25 MHz, V_{DD} = 5.0 V ± 10%	—	—	23	
				C_L = 12 pF (lumped), 125 MHz, V_{DD} = 3.3 V ± 10%	—	—	24	
Dynamic consumption(3)								
I_{DYN_SEG}	SR	D	Sum of all the dynamic and DC I/O current within a supply segment	V_{DD} = 5.0 V ± 10%	—	—	195	mA
				V_{DD} = 3.3 V ± 10%	—	—	150	
I_{DYN_W}	CC	D	Dynamic I/O current for WEAK configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	16.7	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	16.8	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	12.9	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	12.9	
I_{DYN_M}	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	18.2	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	18.4	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	14.3	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	16.4	
I_{DYN_S}	CC	D	Dynamic I/O current for STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	57	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	63.5	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	31	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	33.5	

Table 17. I/O consumption (continued)

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
I_{DYN_V}	CC	D	Dynamic I/O current for VERY STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	62	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	70	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	52	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	55	
I_{DYN_V}	CC	D	Dynamic I/O current for ULTRA STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	62	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	70	
				C_L = 12 pF (lumped), V_{DD} = 3.3 V ± 10%	—	—	67	

1. I/O current consumption specifications for the 4.5 V $\leq V_{DD\_HV\_IO} \leq$ 5.5 V range are valid for VSIO_[VSIO_xx] = 1, and VSIO[VSIO_xx] = 0 for 3.0 V $\leq V_{DD\_HV\_IO} \leq$ 3.6 V.
2. Average consumption in one pad toggling cycle.
3. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition. When possible (timed output) it is recommended to delay transition between pads by few cycles to reduce noise and consumption.

4.9 Reset pad (PORST) electrical characteristics

The device implements dedicated bidirectional reset pins as below specified. PORST pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 KΩ.

Figure 5. Startup Reset requirements

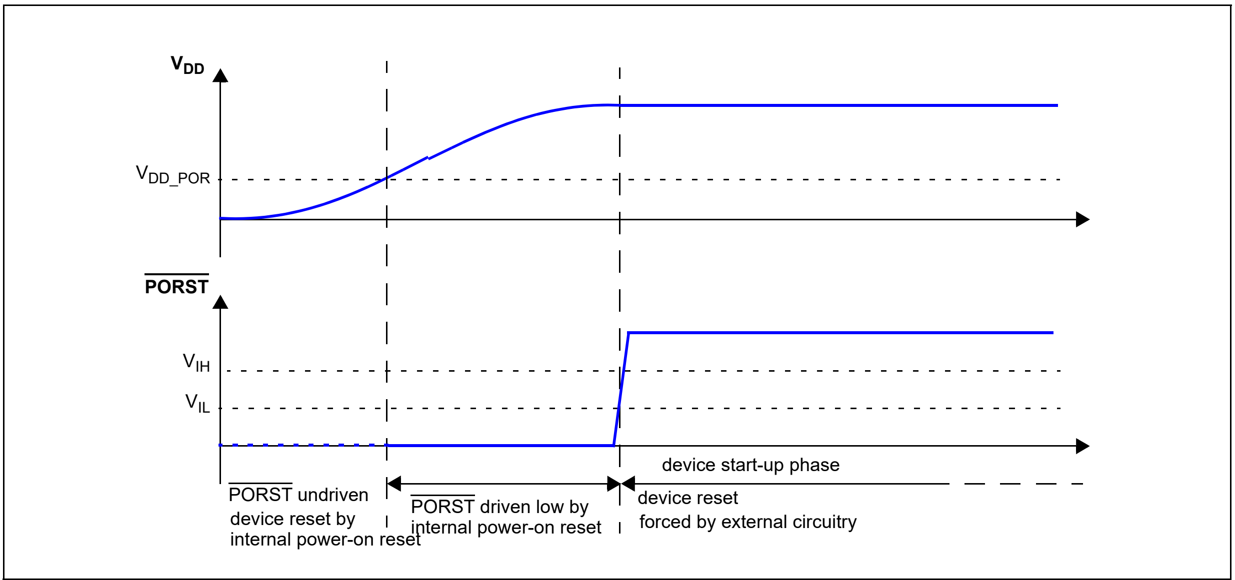


Figure 6 describes device behavior depending on supply signal on PORST:

1. PORST low pulse has too low amplitude: it is filtered by input buffer hysteresis. Device remains in current state.
2. PORST low pulse has too short duration: it is filtered by low pass filter. Device remains in current state.
3. PORST low pulse is generating a reset:
   a) PORST low but initially filtered during at least WFRST. Device remains initially in current state.
   b) PORST potentially filtered until WNFRST. Device state is unknown. It may either be reset or remains in current state depending on extra condition (temperature, voltage, device).
   c) PORST asserted for longer than WNFRST. Device is under reset.

Figure 6. Noise filtering on reset signal

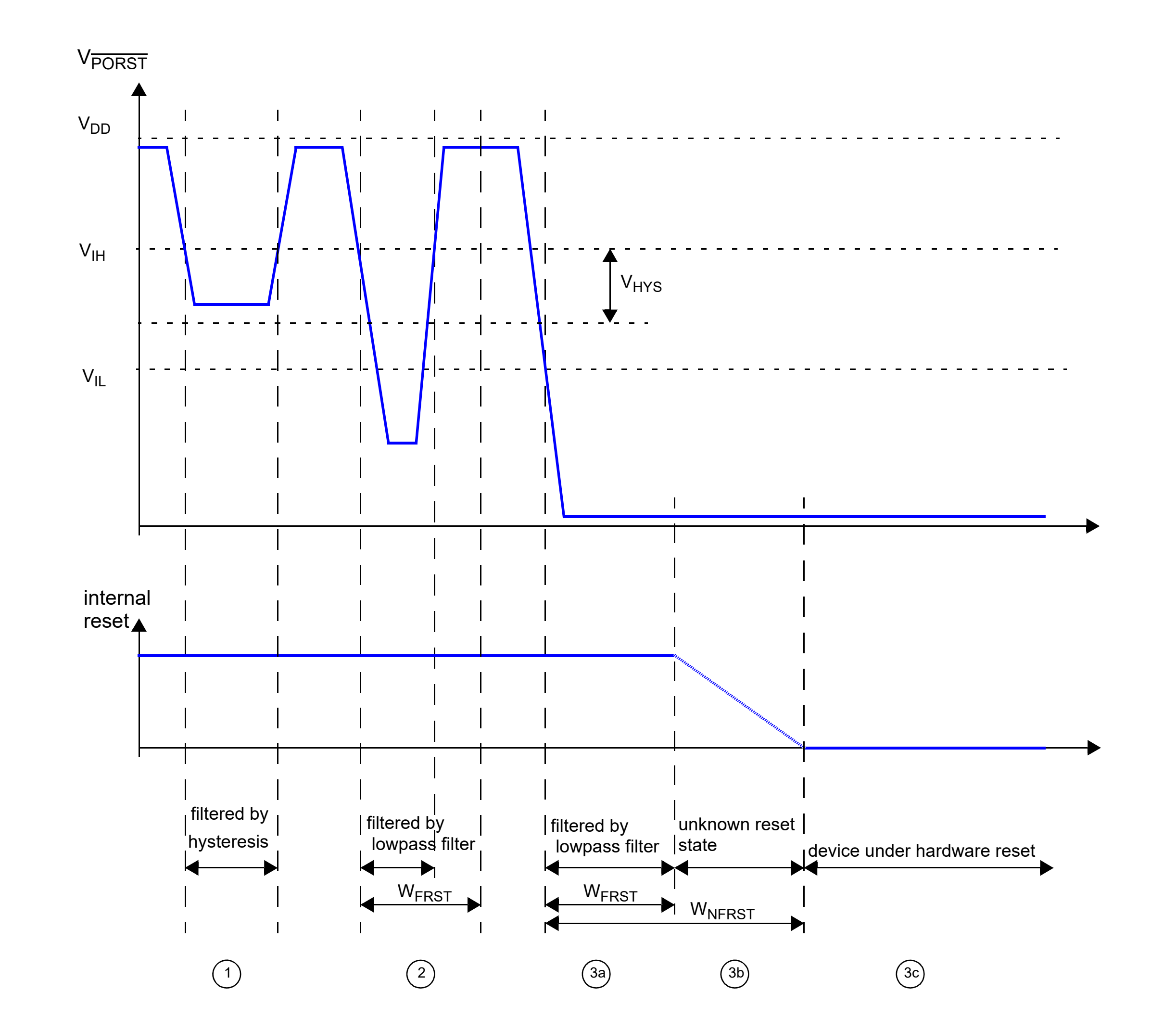


Table 18. Reset PAD electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IHRES}	SR	P	Input high level TTL	V_{DD_HV} = 5.0 V ± 10% V_{DD_HV} = 3.3 V ± 10%	2	—	$V_{DD\_HV\_IO}$ +0.3	V
V_{ILRES}	SR	P	Input low level TTL	V_{DD_HV} = 5.0 V ± 10%	-0.3	—	0.8	V
				V_{DD_HV} = 3.3 V ± 10%	-0.3	—	0.6	
V_{HYSRES}	CC	C	Input hysteresis TTL	V_{DD_HV} = 5.0 V ± 10%	0.3	—	—	V
				V_{DD_HV} = 3.3 V ± 10%	0.2	—	—	
V_{DD_POR}	CC	D	Minimum supply for strong pull-down activation	V_{DD_HV} = 5.0 V ± 10%	—	—	1.6	V
				V_{DD_HV} = 3.3 V ± 10%	—	—	1.05	

Table 18. Reset PAD electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
I_{OL_R}	CC	P	Strong pull-down current [1]	V_{DD_HV} = 5.0 V ± 10%	12	—	—	mA
				V_{DD_HV} = 3.3 V ± 10%	8	—	—	
I_{WPU}	CC	P	Weak pull-up current absolute value	V_{IN} = 1.1 V[2] V_{DD_HV} = 5.0 V ± 10%	—	—	130	µA
		P		V_{IN} = 1.1 V V_{DD_HV} = 3.3 V ± 10%	—	—	70	
		P		V_{IN} = 0.69 * $V_{DD\_HV\_IO}$[3] V_{DD_HV} = 5.0 V ± 10%	15	—	—	
		P		V_{IN} = 0.69 * $V_{DD\_HV\_IO}$ V_{DD_HV} = 3.3 V ± 10%	15	—	—	
I_{WPD}	CC	P	Weak pull-down current absolute value	V_{IN} = 0.69 * $V_{DD\_HV\_IO}$[2] V_{DD_HV} = 5.0 V ± 10%	—	—	130	µA
		P		V_{IN} = 0.69 * $V_{DD\_HV\_IO}$[2] V_{DD_HV} = 3.3 V ± 10%	—	—	80	
		P		V_{IN} = 0.9 V V_{DD_HV} = 5.0 V ± 10%	15	—	—	
		P		V_{IN} = 0.9 V $V_{DD\_HVDD\_HV}$ = 3.3 V ± 10%	15	—	—	
W_{FRST}	CC	P	Input filtered pulse	V_{DD_HV} = 5.0 V ± 10%	—	—	500	ns
		P		V_{DD_HV} = 3.3 V ± 10%	—	—	600	
W_{NFRST}	CC	P	Input not filtered pulse	V_{DD_HV} = 5.0 V ± 10%	2000	—	—	ns
		P		V_{DD_HV} = 3.3 V ± 10%	3000	—	—	

1. I_{ol_r} applies to PORST: Strong Pull-down is active on PHASE0 for PORST. Refer to the device pinout IO definition excel file for details regarding pin usage.
2. Maximum current when forcing a change in the pin level opposite to the pull configuration.
3. Minimum current when keeping the same pin level state than the pull configuration.

Table 19. Reset Pad state during power-up and reset

PAD	POWER-UP State	RESET state	DEFAULT state[1]	STANDBY state
PORST	Strong pull-down	Weak pull-down	Weak pull-down	Weak pull-up

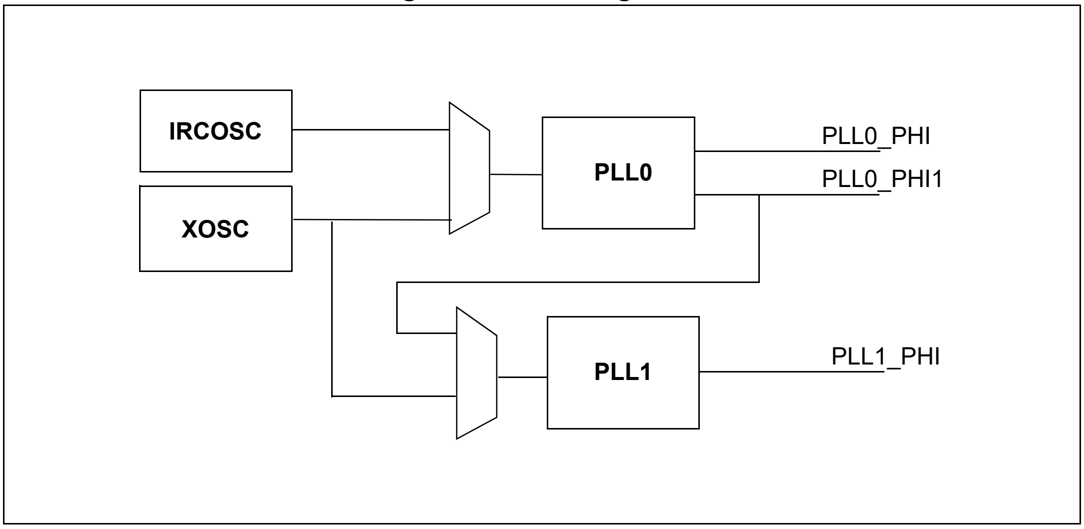
1. Before SW Configuration. Please refer to the Device Reference Manual, Reset Generation Module (MC_RGM) Functional Description chapter for the details of the power-up phases.

4.10 PLLs

Three phase-locked loop (PLL) modules are implemented to generate system, ethernet and auxiliary clocks on the device.

Figure 7 depicts the integration of the system and auxiliary PLLs. Refer to device Reference Manual for more detailed schematic.

Figure 7. PLLs integration



4.10.1 PLL0

Table 20. PLL0 electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{PLL0IN}	SR	—	PLL0 input clock(1)	—	8	—	44	MHz
Δ_{PLL0IN}	SR	—	PLL0 input clock duty cycle(1)	—	40	—	60	%
f_{INFIN}	SR	—	PLL0 PFD (Phase Frequency Detector) input clock frequency	—	8	—	20	MHz
$f_{PLL0VCO}$	CC	P	PLL0 VCO frequency	—	600	—	1400	MHz
$f_{PLL0PHI0}$	CC	D	PLL0 output frequency	—	4.762	—	400	MHz
$f_{PLL0PHI1}$	CC	D	PLL0 output clock PHI1	—	20	—	175(2)	MHz
$t_{PLL0LOCK}$	CC	P	PLL0 lock time	—	—	—	100	µs
$\|\Delta_{PLL0PHI0SPJ}\|$(3)	CC	T	PLL0_PHI0 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI0}$ = 400 MHz, 6-sigma pk-pk	—	—	200	ps

Table 20. PLL0 electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\|\Delta_{PLL0PHI1SPJ}\|$(3)	CC	D	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma pk-pk	—	—	300(4)	ps
$\Delta_{PLL0LTJ}$(3)	CC	D	PLL0 output long term jitter(4) f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	±250	ps
				16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	±300	ps
				long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	CC	D	PLL0 consumption	FINE LOCK state	—	—	6	mA

1. PLL0IN clock retrieved directly from either internal RCOSC or external FXOSC clock. Input characteristics are granted when using internal RCOSC or external oscillator is used in functional mode.
2. If the PLL0_PHI1 is used as an input for PLL1, then the PLL0_PHI1 frequency shall obey the maximum input frequency limit set for PLL1 (87.5 MHz, according to *Table 21*).
3. Jitter values reported in this table refer to the internal jitter, and do not include the contribution of the divider and the path to the output CLKOUT pin.
4. V_{DD_LV} noise due to application in the range V_{DD_LV} = 1.20 V±5%, with frequency below PLL bandwidth (40 kHz) will be filtered.

4.10.2 PLL1

PLL1 is a frequency modulated PLL with Spread Spectrum Clock Generation (SSCG) support.

Table 21. PLL1 electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{PLL1IN}	SR	—	PLL1 input clock[1]	—	37.5	—	87.5	MHz
Δ_{PLL1IN}	SR	—	PLL1 input clock duty cycle[1]	—	35	—	65	%
f_{INFIN}	SR	—	PLL1 PFD (Phase Frequency Detector) input clock frequency	—	37.5		87.5	MHz
$f_{PLL1VCO}$	CC	P	PLL1 VCO frequency	—	600	—	1400	MHz
$f_{PLL1PHI0}$	CC	D	PLL1 output clock PHI0	—	4.762	—	F_{SYS}[2]	MHz
$t_{PLL1LOCK}$	CC	P	PLL1 lock time	—	—	—	50	μs
$f_{PLL1MOD}$	CC	T	PLL1 modulation frequency	—	—	—	250	kHz
$\|\delta_{PLL1MOD}\|$	CC	T	PLL1 modulation depth (when enabled)	Center spread[3]	0.25	—	2	%
				Down spread	0.5	—	4	%
$\|\Delta_{PLL1PHI0SPJ}\|$[4]	CC	T	PLL1_PHI0 single period peak to peak jitter	$f_{PLL1PHI0}$ = 200 MHz, 6-sigma	—	—	500[5]	ps
I_{PLL1}	CC	D	PLL1 consumption	FINE LOCK state	—	—	5	mA

1. PLL1IN clock retrieved directly from either internal PLL0 or external FXOSC clock. Input characteristics are granted when using internal PPL0 or external oscillator is used in functional mode.
2. Refer to *Section 4.3: Operating conditions* for the maximum operating frequency.
3. The device maximum operating frequency F_{SYS} (max) includes the frequency modulation. If center modulation is selected, the FSYS must be below the maximum by MD (Modulation Depth Percentage), such that FSYS(max)=FSYS(1+MD%). Refer to the Reference Manual for the PLL programming details.
4. Jitter values reported in this table refer to the internal jitter, and do not include the contribution of the divider and the path to the output CLKOUT pin.
5. 1.25 V±5%, application noise below 40 kHz at V_{DD_LV} pin - no frequency modulation.

4.10.3 PLL_ETH

This PLL provides a clock that is not frequency modulated to Ethernet1 IP for managing Delay-on-Source for its Tx clock. The input sources for PLL_ETH are:

1. XOSC
2. ETH1_RX clock div1/div5 based on speed
3. Divided clock from PLL0, derived from CGM_AC2_DC1

Note: PLL_ETH is another instance of PLL0 so the electrical characteristics for PLL_ETH are similar to PLL0, the main difference is PHI0 has to be programmed always to generate 500 MHz.

4.11 Oscillators

4.11.1 Crystal oscillator 40 MHz

Table 22. External 40 MHz oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{XTAL}	CC	D	Crystal Frequency Range(1)	—	4(2)	8	MHz
					>8	20	
					>20	40	
t_{cst}	CC	T	Crystal start-up time (3),(4)	T_J = 150 °C	—	5	ms
t_{rec}	CC	D	Crystal recovery time(5)	—	—	0.5	ms
V_{IHEXT}	CC	D	EXTAL input high voltage(6) (External Reference)	V_{REF} = 0.29 * $V_{DD\_HV\_OSC}$	V_{REF} + 0.75	—	V
V_{ILEXT}	CC	D	EXTAL input low voltage(6) (External Reference)	V_{REF} = 0.29 * $V_{DD\_HV\_OSC}$	—	V_{REF} - 0.75	V
C_{S_EXTAL}	CC	D	Total on-chip stray capacitance on EXTAL pin(7)	—	3	7	pF
C_{S_XTAL}	CC	D	Total on-chip stray capacitance on XTAL pin(7)	—	3	7	pF
g_m	CC	P	Oscillator Transconductance	f_{XTAL} = 4 – 8 MHz freq_sel[2:0] = 000	3.9	13.6	mA/V
		D		f_{XTAL} = 5 - 10 MHz freq_sel[2:0] = 001	5	17.5	
		D		f_{XTAL} = 10 – 15 MHz freq_sel[2:0] = 010	8.6	29.3	
		P		f_{XTAL} = 15 - 20 MHz freq_sel[2:0] = 011	14.4	48	
		D		f_{XTAL} = 20 - 25 MHz freq_sel[2:0] = 100	21.2	69	
		D		f_{XTAL} = 25 – 30 MHz freq_sel[2:0] = 101	27	86	
		D		f_{XTAL} = 30 - 35 MHz freq_sel[2:0] = 110	33.5	115	
		P		f_{XTAL} = 35 - 40 MHz freq_sel[2:0] = 111	33.5	115	
V_{EXTAL}	CC	D	Oscillation Amplitude on the EXTAL pin after startup(8)	T_J = –40 °C to 150 °C	0.5	1.8	V

Table 22. External 40 MHz oscillator electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{HYS}	CC	D	Comparator Hysteresis	T_J = –40 °C to 150 °C	0.1	1.0	V
I_{XTAL}	CC	D	XTAL current(8),(9)	T_J = –40 °C to 150 °C	—	14	mA

1. The range is selectable by UTEST miscellaneous DCF client XOSC_FREQ_SEL.
2. The XTAL frequency, if used to feed the PPL0 (or PLL1), shall obey the minimum input frequency limit set for PLL0 (or PLL1).
3. This value is determined by the crystal manufacturer and board design, and it can potentially be higher than the maximum provided.
4. Proper PC board layout procedures must be followed to achieve specifications.
5. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
6. Applies to an external clock input and not to crystal mode.
7. See crystal manufacturer's specification for recommended load capacitor (C_L) values. The external oscillator requires external load capacitors when operating from 8 MHz to 16 MHz. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating at 20 MHz/40 MHz, the integrated load capacitor value is selected via S/W to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.
8. Amplitude on the EXTAL pin after startup is determined by the ALC block, that is the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid over driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.
9. I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator.

4.11.2 Crystal Oscillator 32 kHz

Table 23. 32 kHz External Slow Oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{sxosc}	SR	T	Slow external crystal oscillator frequency	—	—	32768	—	Hz
g_{msxosc}	CC	P	Slow external crystal oscillator transconductance	—	9.5	—	32	µA/V
V_{sxosc}	CC	T	Oscillation Amplitude	—	0.5	—	1.7	V
I_{sxoosc}	CC	D	Oscillator consumption	—	—	—	9	µA
T_{sxosc}	CC	T	Start up time	—	—	—	2	s

4.11.3 RC oscillator 16 MHz

Table 24. Internal RC oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{Target}	CC	D	IRC target frequency	—	—	16	—	MHz
δf_{var_noT}	CC	P	IRC frequency variation without temperature compensation	T < 150 °C	–5	—	5	%
δf_{var_T}	CC	T	IRC frequency variation with temperature compensation	T < 150 °C	–3	—	3	%
δf_{var_SW}		T	IRC software trimming accuracy	Trimming temperature	–0.5	±0.3	0.5	%
T_{start_noT}	CC	T	Startup time to reach within f_{var_noT}	Factory trimming already applied	—	—	5	µs
T_{start_T}	CC	T	Startup time to reach within f_{var_T}	Factory trimming already applied	—	—	120	µs
I_{FIRC}	CC	T	Current consumption on HV power supply(1)	After T_{start_T}	—	—	1200	µA

1. The actual consumption difference can be higher due to additional consumption of core logic clocked by RCOSC16M.

4.11.4 Low power RC oscillator

Table 25. 1024 kHz internal RC oscillator electrical characteristics

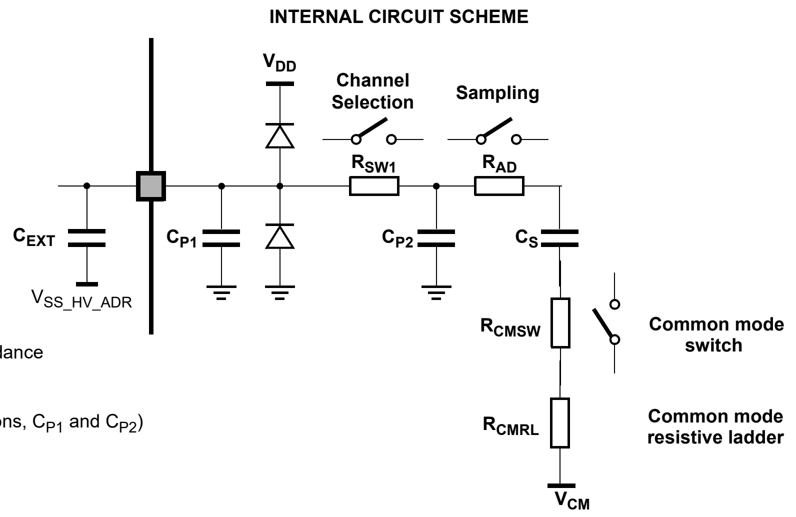
Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{sirc}	CC	T	Slow Internal RC oscillator frequency	—	—	1024	—	kHz
δf_{var_T}	CC	P	Frequency variation across temperature	–40 °C < T < 150 °C	–9	—	+9	%
δf_{var_V}	CC	P	Frequency variation across voltage	–40 °C < T < 150 °C	–5	—	+5	%
I_{sirc}	CC	T	Slow Internal RC oscillator current	T = 55 °C	—	—	6	µA
T_{sirc}	CC	T	Start up time, after switching ON the internal regulator.	—	—	—	12	µS

4.12 ADC system

4.12.1 ADC input description

Figure 8 shows the input equivalent circuit for SARn and SARB channels.

Figure 8. Input equivalent circuit (Fast SARn and SARB channels)



R_{SW1}: Channel Selection Switch Impedance
R_{AD}: Sampling Switch Impedance
C_P: Pin Capacitance (two contributions, C_{P1} and C_{P2})
C_S: Sampling Capacitance
R_{CMSW}: Common mode switch
R_{CMRL}: Common mode resistive ladder
V_{CM}: Common mode voltage (~0.5 V_{DD})
C_{EXT}: External capacitance

The above scheme can be used as approximation circuitry for external filtering definition.

All specifications in the following table valid for the full input voltage range for the analog inputs.

Table 26. ADC pin specification

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
$R_{20K\Omega}$	CC	D	Internal voltage reference source impedance.	—	16	30	KΩ
I_{LKG}	CC	—	Input leakage current, two ADC channels on input-only pin.	See IO chapter *Table 10: I/O input electrical characteristics*, parameter I_{LKG}.			
I_{INJ1}	SR	—	Injection current on analog input preserving functionality at full or degraded performances.	See Operating Conditions chapter *Table 5: Operating conditions*, I_{INJ1} parameter.			
C_{HV_ADC}	SR	D	$V_{DD\_HV\_ADV}$ external capacitance.	See Power Management chapter *Table 31: External components integration*, C_{ADC} parameter.			
C_{P1}	CC	D	Pad capacitance	See IO chapter *Table 10: I/O input electrical characteristics*, parameter C_{P1}.			

Table 26. ADC pin specification (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Max	Unit
C_{P2}	CC	D	Internal routing capacitance	SARB channels	—	2	pF
				SARn 10-bit channels	—	0.5	
				SARn 12-bit channels	—	1	
C_S	CC	D	SAR ADC sampling capacitance	SARn 12bit	—	5	pF
				SARn 10bit	—	2	
R_{SWn}	CC	D	Analog switches resistance	SARB channels	0	1.8	kΩ
				SARn 10-bit channels	0	0.8	
				SARn 12-bit channels	0	1.8	
R_{AD}	CC	D	ADC input analog switches resistance	SARn 12bit	—	0.8	kΩ
				SARn 10bit	—	3.2	
R_{CMSW}	CC	D	Common mode switch resistance	Sum of the two resistances	—	9	kΩ
R_{CMRL}	CC	D	Common mode resistive ladder				kΩ
R_{SAFEPD}(1)	CC	D	Discharge resistance for ADC input-only pins (strong pull-down for safety)	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	—	300	W
				$V_{DD\_HV\_IO}$ = 3.3 V ± 10%	—	500	W
A_{BGAP}	CC	D	ADC digital bandgap accuracy		-1.5	+1.5	%
C_{EXT}	SR	—	External capacitance at the pad input pin	To preserve the accuracy of the ADC, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible. This capacitor contributes to attenuating the noise present on the input pin. The impedance relative to the signal source can limit the ADC's sample rate.			

1. It enables discharge of up to 100 nF from 5 V every 300 ms. Refer to the device pinout Microsoft Excel file attached to the IO_Definition document for the pads supporting it.

4.12.2 SAR ADC 12 bit electrical specification

The SARn ADCs are 12-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Note: The functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maximum may affect device reliability or cause permanent damage to the device.

Table 27. SARn ADC electrical specification

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{ADCK}	SR	P	Clock frequency	Standard frequency mode	7.5	13.33	MHz
		T		High frequency mode	>13.33	16.0	
$t_{ADCINIT}$	SR	—	ADC initialization time	—	1.5	—	μs
$t_{ADCBIASINIT}$	SR	—	ADC BIAS initialization time	—	5	—	μs
$t_{ADCPRECH}$	SR	T	ADC decharge time	Fast SAR	$1/f_{ADCK}$	—	μs
				Slow SAR (SARDAC_B)	$2/f_{ADCK}$	—	
ΔV_{PRECH}	SR	D	Decharge voltage precision	T_J < 150 °C	0	0.25	V
$R_{20K\Omega}$	CC	D	Internal voltage reference source impedance	—	16	30	KΩ
ΔV_{INTREF}	CC	P	Internal reference voltage precision	Applies to all internal reference points ($V_{SS\_HV\_ADR}$, 1/3 * $V_{DD\_HV\_ADR}$, 2/3 * $V_{DD\_HV\_ADR}$, $V_{DD\_HV\_ADR}$)	–0.20	0.20	V

Table 27. SARn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Max	Unit
$t_{ADCSAMPLE}$	SR	P	ADC sample time(1)	Fast SAR – 12-bit configuration	$6/f_{ADCK}$	—	μs
		D		Fast SAR – 10-bit configuration mode 1(2) (Standard frequency mode only)	$6/f_{ADCK}$		
				Fast SAR – 10-bit configuration mode 2(3) (Standard frequency mode only)	$5/f_{ADCK}$		
				Fast SAR – 10-bit configuration mode 3(4) (High frequency mode only)	$6/f_{ADCK}$		
				Slow SAR (SARADC_B)– 12-bit configuration	$12/f_{ADCK}$		
				Slow SAR (SARADC_B)– 10-bit configuration mode 1(2) (Standard frequency mode only)	$12/f_{ADCK}$		
				Slow SAR (SARADC_B) – 10-bit configuration mode 2(3) (Standard frequency mode only)	$10/f_{ADCK}$		
				Slow SAR (SARADC_B) – 10-bit configuration mode 3(4) (High frequency mode only)	$12/f_{ADCK}$		
				Conversion of BIAS test channels through 20 kΩ input.	$40/f_{ADCK}$		
$t_{ADCEVAL}$	SR	P	ADC evaluation time	12-bit configuration	$12/f_{ADCK}$	—	μs
		D		10-bit configuration	$10/f_{ADCK}$	—	
$I_{ADCREFH}$(5),(6)	CC	T	ADC high reference current	Run mode (average across all codes)	—	7	μA
				Power Down mode	—	1	
$I_{ADCREFL}$(6)	CC	D	ADC low reference current	Run mode $V_{DD\_HV\_ADR\_S} \leq 5.5$ V	—	15	μA
				Power Down mode $V_{DD\_HV\_ADR\_S} \leq 5.5$ V	—	1	
I_{ADV_S}(6)	CC	P	$V_{DD\_HV\_ADV}$ power supply current	Run mode	—	4.0	mA
		D		Power Down mode	—	0.04	

Table 27. SARn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Max	Unit
TUE_{12}	CC	T	Total unadjusted error in 12-bit configuration(7)	T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–4	4	LSB (12b)
		P		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–6	6	
		T		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, 3 V > $V_{DD\_HV\_ADR\_S}$ > 2 V	–6	6	
		D		High frequency mode, T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–12	12	
TUE_{10}	CC	D	Total unadjusted error in 10-bit configuration(7)	Mode 1, T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V $V_{DD\_HV\_ADR\_S}$ > 3 V	–1.5	1.5	LSB (10b)
		D		Mode 1, T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, 3 V > $V_{DD\_HV\_ADR\_S}$ > 2 V	–2.0	2.0	
		C		Mode 2, T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V $V_{DD\_HV\_ADR\_S}$ > 3 V	–3.0	3.0	
		C		Mode 3, T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V $V_{DD\_HV\_ADR\_S}$ > 3 V	–4.0	4.0	

Table 27. SARn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Max	Unit
ΔTUE_{12}	CC	D	TUE degradation due to $V_{DD\_HV\_ADR}$ offset with respect to $V_{DD\_HV\_ADV}$	$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [0:25\ mV]$	–1	1	LSB (12b)
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [25:50\ mV]$	–2	2	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [50:75\ mV]$	–4	4	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [75:100\ mV]$	–6	6	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [0:25\ mV]$	–2.5	2.5	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [25:50\ mV]$	–4	4	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [50:75\ mV]$	–7	7	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [75:100\ mV]$	–12	12	
TUE_{INJ2}	CC	T	TUE degradation addition, due to current injection in I_{INJ2} range.(8)	See Operating Conditions chapter Table 5, I_{INJ2} parameter.	+8		LSB
DNL(9)	CC	P	Differential non-linearity	Standard frequency mode, $V_{DD\_HV\_ADV} > 4\ V$ $V_{DD\_HV\_ADR\_S} > 4\ V$	–1	2	LSB (12b)
		T		High frequency mode, $V_{DD\_HV\_ADV} > 4\ V$ $V_{DD\_HV\_ADR\_S} > 4\ V$	–1	2	

1. Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Refer to Figure 8 for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.
2. Mode1: 6 sampling cycles + 10 conversion cycles at 13.33 MHz.
3. Mode2: 5 sampling cycles + 10 conversion cycles at 13.33 MHz.

4. Mode3: 6 sampling cycles + 10 conversion cycles at 16 MHz.
5. $I_{ADCREFH}$ and $I_{ADCREFL}$ are independent from ADC clock frequency. It depends on conversion rate: consumption is driven by the transfer of charge between internal capacitances during the conversion.
6. Current parameter values are for a single ADC.
7. TUE is granted with injection current within the range defined in Table 26, for parameters classified as T and D.
8. All channels of all SAR-ADC12bit and SAR-ADC10bit are impacted with same degradation, independently from the ADC and the channel subject to current injection.
9. DNL is granted with injection current within the range defined in Table 26, for parameters classified as T and D.

4.12.3 SAR ADC 10 bit electrical specification

The ADC comparators are 10-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Note: The functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maximum may affect device reliability or cause permanent damage to the device.

Table 28. ADC-Comparator electrical specification

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{ADCK}	SR	P	Clock frequency	Standard frequency mode	7.5	13.33	MHz
		T		High frequency mode	>13.33	16.0	
$t_{ADCINIT}$	SR	—	ADC initialization time	—	1.5	—	µs
$t_{ADCBIASINIT}$	SR	—	ADC BIAS initialization time	—	5	—	µs
$t_{ADCINITSBY}$	SR	—	ADC initialization time in standby	Standby Mode	8	—	µs
$t_{ADCPRECH}$	SR	T	ADC precharge time	—	$1/f_{ADCK}$	—	µs
ΔV_{PRECH}	SR	D	Precharge voltage precision	$T_J < 150$ °C	0	0.25	V
$t_{ADCSAMPLE}$	SR	P	ADC sample time(1)	10-bit ADC mode, Fast channel	$5/f_{ADCK}$(2)	—	µs
				10-bit ADC mode, Standard channel	$6/f_{ADCK}$	—	µs
$t_{ADCEVAL}$	SR	P	ADC evaluation time	10-bit ADC mode	$10/f_{ADCK}$	—	µs
		D		ADC comparator mode	$2/f_{ADCK}$	—	
$I_{ADCREFH}$(3),(4)	CC	T	ADC high reference current	Run mode (average across all codes)	—	7	µA
				Power Down mode	—	1	
				ADC comparator mode	—	19.5	

Table 28. ADC-Comparator electrical specification (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Max	Unit
$I_{ADCREFL}$(5)	CC	D	ADC low reference current	Run mode $V_{DD\_HV\_ADR\_S} \leq 5.5$ V	—	15	µA
				Power Down mode $V_{DD\_HV\_ADR\_S} \leq 5.5$ V	—	1	
				ADC comparator mode	—	20.5	
I_{ADV_S}(5)	CC	P	$V_{DD\_HV\_ADV}$ power supply current	Run mode	—	4	mA
		D		Power Down mode	—	0.04	
TUE_{10}	CC	T	Total unadjusted error in 10-bit configuration(6)	$T_J < 150$ °C, $V_{DD\_HV\_ADV} > 3$ V, $V_{DD\_HV\_ADR\_S} > 3$ V	–2	2	LSB (10b)
		P		$T_J < 150$ °C, $V_{DD\_HV\_ADV} > 3$ V, $V_{DD\_HV\_ADR\_S} > 3$ V	–3	3	
		T		$T_J < 150$ °C, $V_{DD\_HV\_ADV} > 3$ V, $3\ V > V_{DD\_HV\_ADR\_S} > 2$ V	–3	3	
		D		High frequency mode, $T_J < 150$ °C, $V_{DD\_HV\_ADV} > 3$ V, $V_{DD\_HV\_ADR\_S} > 3$ V	–3	3	

Table 28. ADC-Comparator electrical specification (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Max	Unit
ΔTUE_{10}	CC	D	TUE degradation due to $V_{DD\_HV\_ADR}$ offset with respect to $V_{DD\_HV\_ADV}$	$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–1.0	1.0	LSB (10b)
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–2.0	2.0	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–3.5	3.5	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–6.0	6.0	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–2.5	2.5	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–4.0	4.0	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–7.0	7.0	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–12.0	12.0	
TUE_{INJ2}	CC	T	TUE degradation addition, due to current injection in I_{INJ2} range.(5)	See Operating Conditions chapter Table 5, I_{INJ2} parameter.	3		LSB
DNL(7)	CC	P	Differential non-linearity std. mode	Standard frequency mode, $V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR\_S} > 4$ V	–1	2	LSB (10b)
		T		High frequency mode, $V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR\_S} > 4$ V	–1	2	

1. Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Refer to Figure 8 for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.
2. In case the ADC is used as Fast Comparator the sampling time is $t_{ADCSAMPLE} = 2/f_{ADCK}$.
3. $I_{ADCREFH}$ and $I_{ADCREFL}$ are independent from ADC clock frequency. It depends on conversion rate: consumption is driven by the transfer of charge between internal capacitances during the conversion.

4. Current parameter values are for a single ADC.
5. All channels of all SAR-ADC12bit and SAR-ADC10bit are impacted with same degradation, independently from the ADC and the channel subject to current injection.
6. TUE is granted with injection current within the range defined in Table 26, for parameters classified as T and D.
7. DNL is granted with injection current within the range defined in Table 26, for parameters classified as T and D.

4.13 Temperature Sensor

The following table describes the temperature sensor electrical characteristics.

Table 29. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	—	Temperature monitoring range	—	–40	—	150	°C
T_{SENS}	CC	T	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	CC	P	Accuracy	T_J < 150 C	–3	—	3	°C

4.14 Power management

The power management module monitors the different power supplies as well as it generates the required internal supplies. The device can operate in the following configurations:

Table 30. Power management regulators

Device	External regulator(1)	Internal SMPS regulator	Internal linear regulator external ballast	Internal linear regulator internal ballast	Auxiliary regulator(2)	Clamp regulator(2)	Internal standby regulator(3)
SPC58EHx SPC58NHx	X	—	X	—	X	X	X

1. The application can select between the internal or external regulator mode, by controlling the EXTREG_SEL pin of the device. If EXTREG_SEL is connected to VDD_HV_IO_MAIN, the external regulator mode is selected.
2. In external regulator mode, the auxiliary and clamp regulators can be optionally enabled, to support the compensation of overshoots and undershoots in the supply. In internal regulator mode, the auxiliary and clamp regulators are always active.
3. Standby regulator is automatically activated when the device enters standby mode.

4.14.1 Power management integration

Use the integration schemes provided below to ensure the proper device function, according to the selected regulator configuration.

The internal regulators are supplied by $V_{DD\_HV\_IO\_MAIN}$ supply and are used to generate V_{DD_LV} supply.

Place capacitances on the board as near as possible to the associated pins and limit the serial inductance of the board to less than 5 nH.

It is recommended to use the internal regulators only to supply the device itself.

Figure 9. External regulator mode

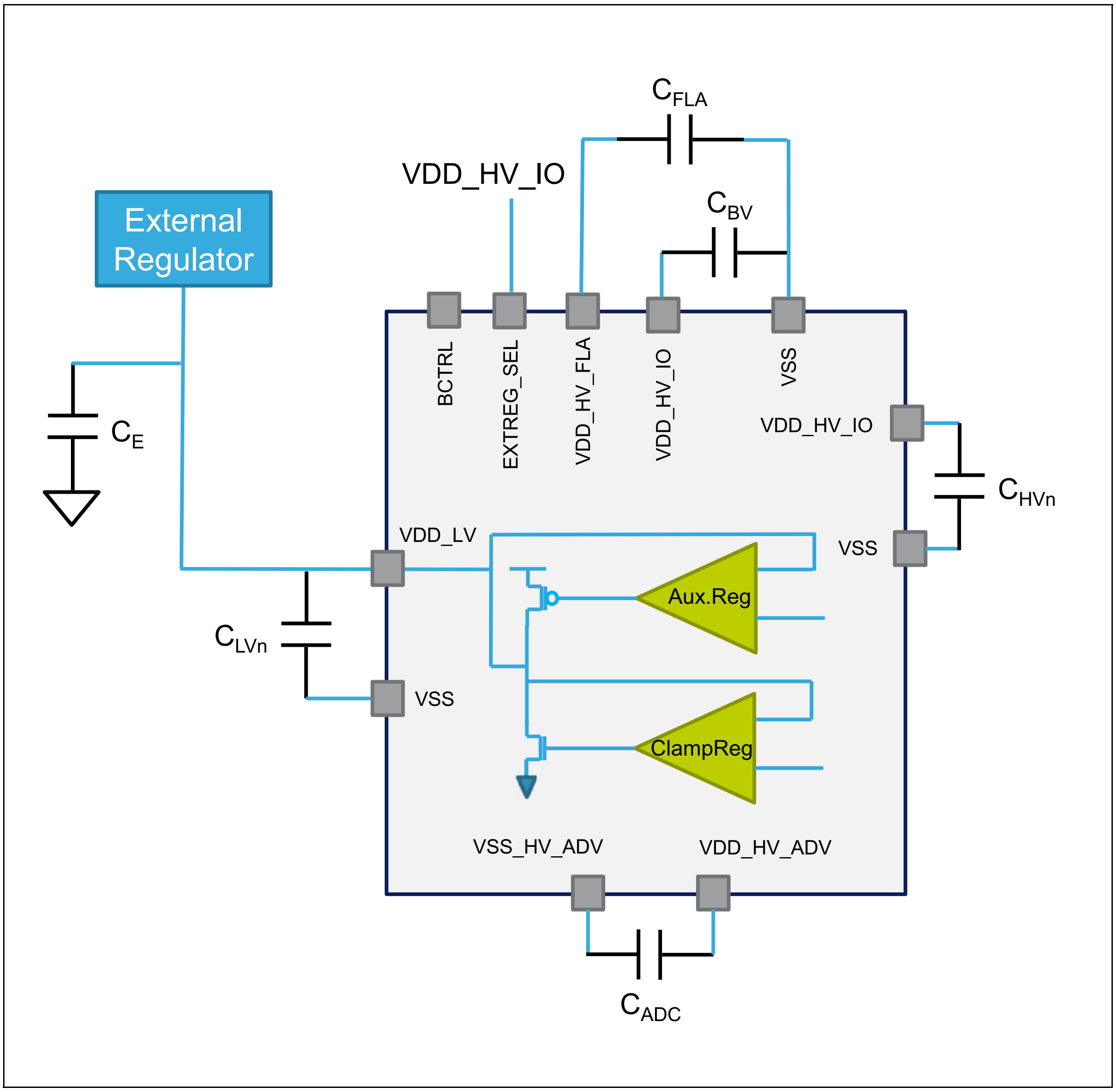


Figure 10. Internal regulator with external ballast mode

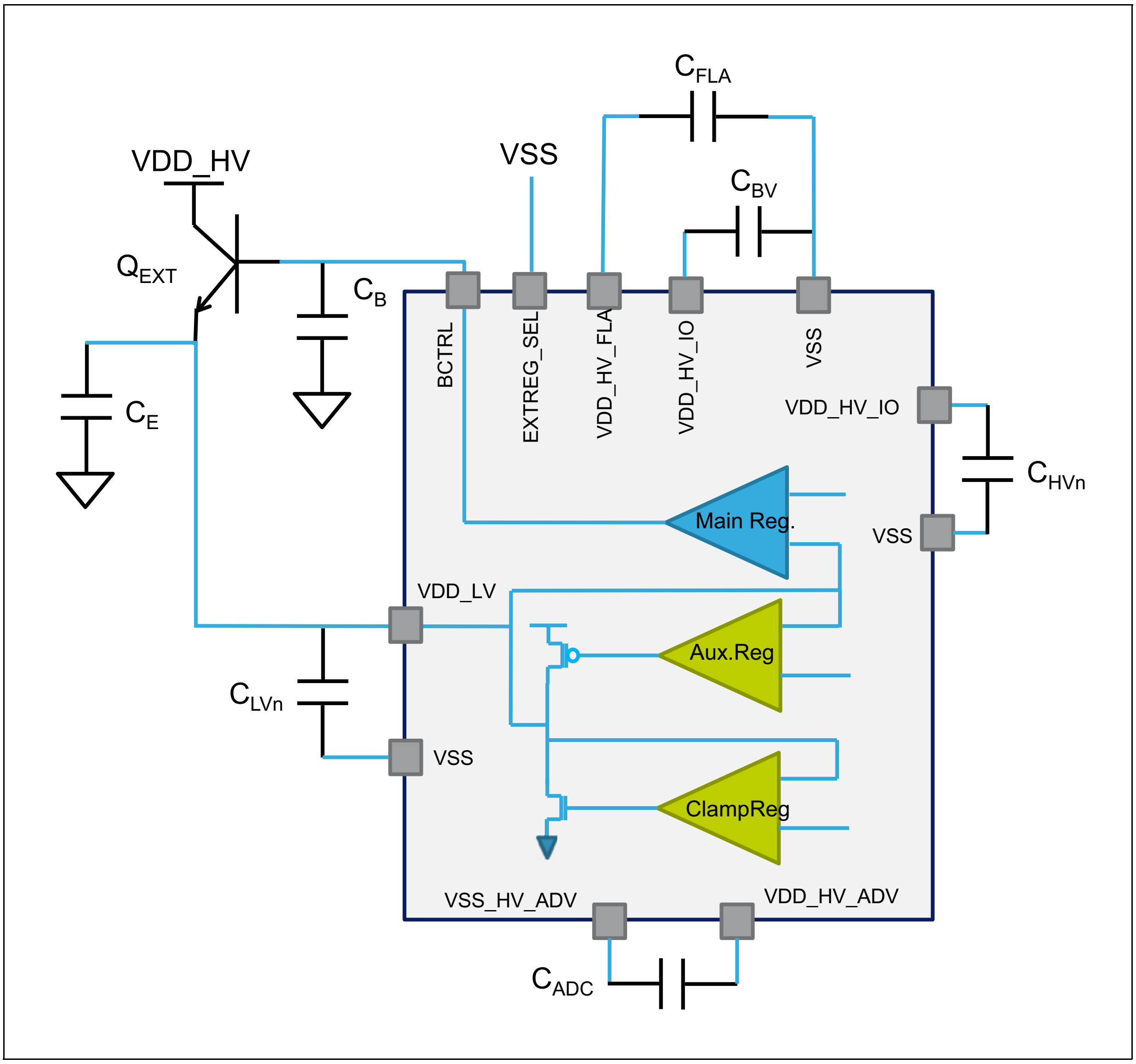


Figure 11. Standby regulator with external ballast mode

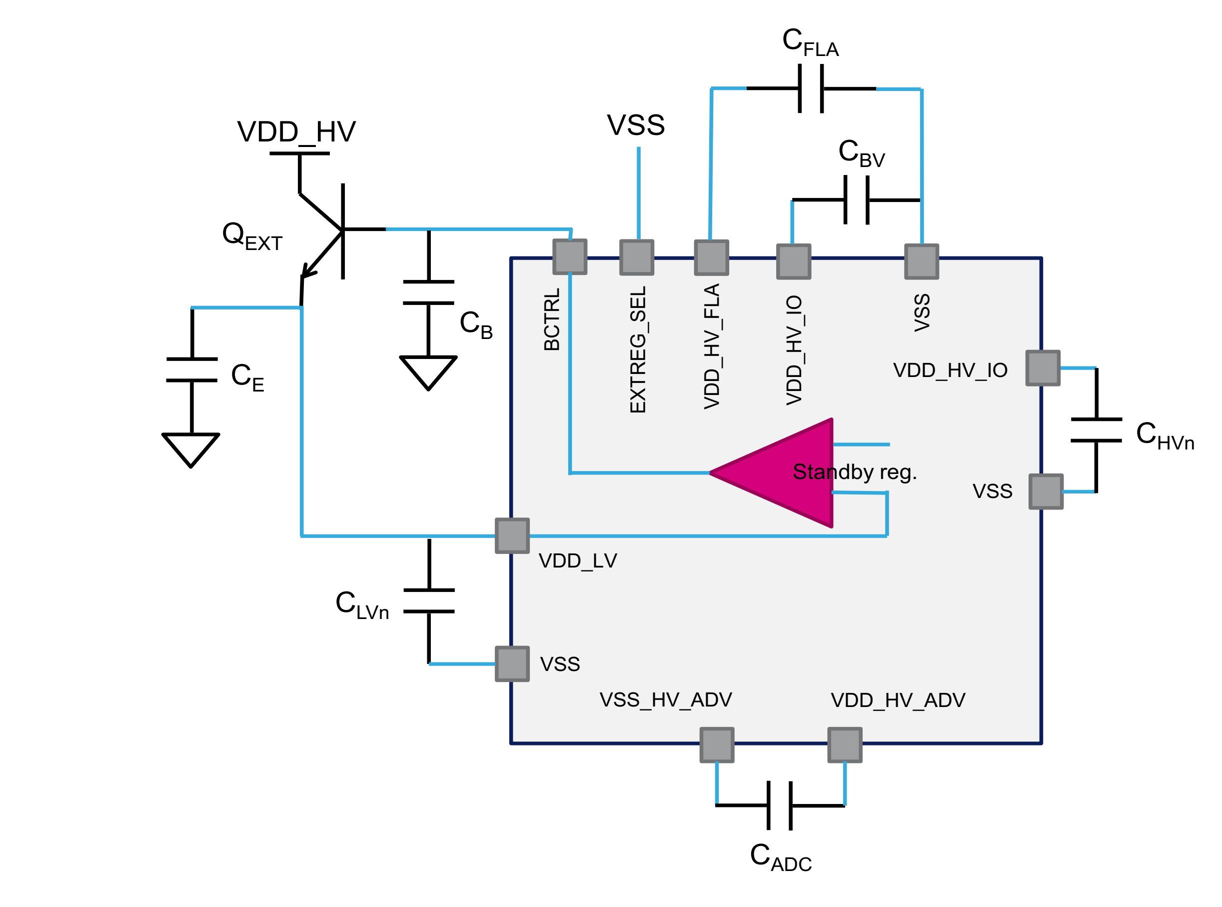


Table 31. External components integration

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
Common Components								
C_E	SR	D	Internal voltage regulator stability external capacitance.[2] [3]		—	2× 2.2	—	µF
R_E	SR	D	Stability capacitor equivalent serial resistance	Total resistance including board track	—	—	50	mΩ
C_{LVn}	SR	D	Internal voltage regulator decoupling external capacitance[2] [4] [5]	Each V_{DD_LV}/V_{SS} pair	—	47	—	nF
R_{LVn}	SR	D	Stability capacitor equivalent serial resistance	—	—	—	50	mΩ
C_{BV}	SR	D	Bulk capacitance for HV supply[2]	on one $V_{DD\_HV\_IO\_MAIN}/V_{SS}$ pair	—	4.7	—	µF
C_{HVn}	SR	D	Decoupling capacitance for ballast and IOs[2]	on all $V_{DD\_HV\_IO}/V_{SS}$ and $V_{DD\_HV\_ADR}/V_{SS}$ pairs	—	100	—	nF

Table 31. External components integration (continued)

Symbol		C	Parameter	Conditions[1]	Value Min	Value Typ	Value Max	Unit
C_{FLA}	SR	D	Decoupling capacitance for Flash supply[6]	—	—	10	—	nF
C_{ADC}	SR	D	ADC supply external capacitance[2]	$V_{DD\_HV\_ADV}$/$V_{SS\_HV\_ADV}$ pair.	—	2.2	—	µF
Internal Linear Regulator with External Ballast Mode								
Q_{EXT}	SR	D	Recommended external NPN transistors	NJD2873T4, BCP68				
V_Q	SR	D	External NPN transistor collector voltage	—	2.0	—	$V_{DD\_HV\_IO\_MAIN}$	V
C_B	SR	D	Internal voltage regulator stability external capacitance on ballast base[4] [7]	—	—	2.2	—	µF
R_B	SR	D	Stability capacitor equivalent serial resistance	Total resistance including board track	—	—	50	mΩ

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_J = –40 / 150 °C, unless otherwise specified.
2. Recommended X7R or X5R ceramic –50% / +35% variation across process, temperature, voltage and after aging.
3. CE capacitance is required both in internal and external regulator mode.
4. For noise filtering, add a high frequency bypass capacitance of 10 nF.
5. For applications it is recommended to implement at least 5 C_{LV} capacitances.
6. Recommended X7R capacitors. For noise filtering, add a high frequency bypass capacitance of 100 nF.
7. CB capacitance is required if only the external ballast is implemented.

4.14.2 Voltage regulators

Table 32. Linear regulator specifications

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
V_{MREG}	CC	P	Main regulator output voltage	Power-up, before trimming, no load	1.12	1.20	1.28	V
	CC	P		After trimming, maximum load	1.08	1.18	1.23	
IDD_{MREG}	CC	T	Main regulator current provided to V_{DD_LV} domain The maximum current required by the device (I_{DD_LV}) may exceed the maximum current which can be provided by the internal linear regulator. In this case, the internal regulator mode cannot be used.	—	—	—	700	mA
IDD_{CLAMP}	CC	D	Main regulator rush current sinked from $V_{DD\_HV\_IO\_MAIN}$ domain during V_{DD_LV} domain loading	Power-up condition	—	—	400	mA
ΔIDD_{MREG}	CC	T	Main regulator output current variation	20 µs observation window	-200	—	200	mA
$I_{MREGINT}$	CC	D	Main regulator current consumption	I_{MREG} = max	—	—	22	mA
		D		I_{MREG} = 0 mA	—	—		

Table 33. Auxiliary regulator specifications

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
V_{AUX}	CC	P	Aux regulator output voltage	After trimming, internal regulator mode	1.08	1.18	1.21	V
	CC	P		After trimming, external regulator mode	1.03	1.12	1.16	
IDD_{AUX}	CC	T	Aux regulator current provided to V_{DD_LV} domain	—	—	—	250	mA
ΔIDD_{AUX}	CC	T	Aux regulator current variation	20 µs observation window	100	—	100	mA
I_{AUXINT}	CC	D	Aux regulator current consumption	I_{MREG} = max	—	—	1.1	mA
		D		I_{MREG} = 0 mA	—	—	1.1	

Table 34. Clamp regulator specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{CLAMP}	CC	P	Clamp regulator output voltage	After trimming, internal regulator mode	1.17	1.21	1.32	V
	CC	P		After trimming, external regulator mode	1.24	1.28	1.39	
ΔIDD_{CLAMP}	CC	T	Clamp regulator current variation	20 µs observation window	100	—	100	mA
$I_{CLAMPINT}$	CC	D	Clamp regulator current consumption	I_{MREG} = 0 mA	—	—	0.7	mA

Table 35. Standby regulator specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{SBY}	CC	P	Standby regulator output voltage	After trimming, maximum load	1.02	1.06	1.26	V
IDD_{SBY}	CC	T	Standby regulator current provided to V_{DD_LV} domain	—	—	—	50	mA

4.14.3 Voltage monitors

The monitors and their associated levels for the device are given in Table 36. Figure 12 illustrates the workings of voltage monitoring threshold.

Figure 12. Voltage monitor threshold definition

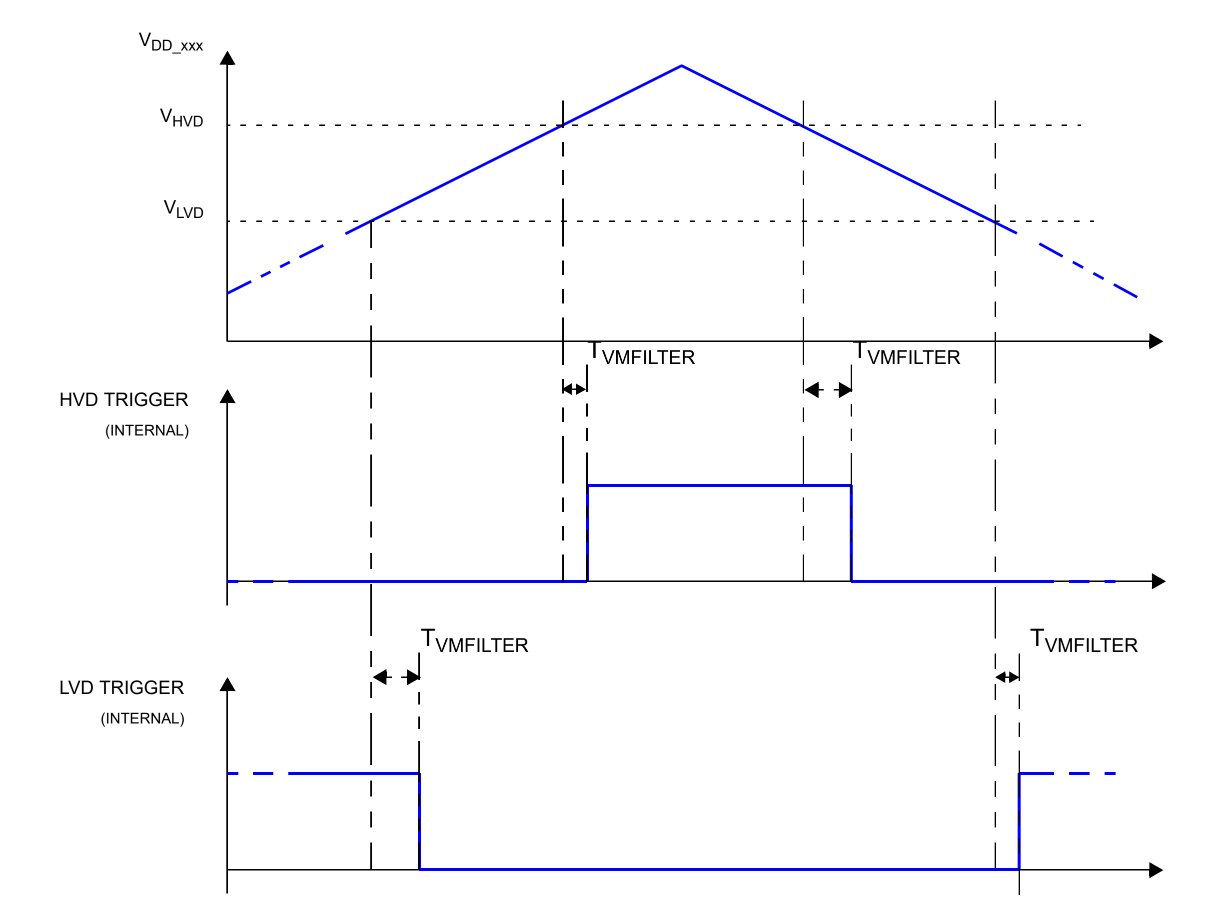


Table 36. Voltage monitor electrical characteristics

Symbol		C	Supply/Parameter[1]	Conditions	Value[2]			Unit
					Min	Typ	Max	
PowerOn Reset HV								
V_{POR200_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	1.80	2.18	2.40	V
Minimum Voltage Detectors HV								
V_{MVD270_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	2.71	2.76	2.80	V
V_{MVD270_F}	CC	P	$V_{DD\_HV\_FLA}$	—	2.71	2.76	2.80	V
V_{MVD270_SBY}	CC	P	$V_{DD\_HV\_IO\_MAIN}$ (in Standby)	—	2.71	2.76	2.80	V
Low Voltage Detectors HV								
V_{LVD290_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	2.89	2.94	2.99	V
V_{LVD290_F}	CC	P	$V_{DD\_HV\_FLA}$	—	2.89	2.94	2.99	V
V_{LVD290_IE}	CC	P	$V_{DD\_HV\_EMMC}$	—	2.89	2.94	2.99	V
V_{LVD290_AS}	CC	P	$V_{DD\_HV\_ADV}$ (ADCSAR pad)	—	2.89	2.94	2.99	V
V_{LVD290_IE1}	CC	P	$V_{DD\_HV\_IO\_ETH1}$	—	2.89	2.94	2.99	V

Table 36. Voltage monitor electrical characteristics (continued)

Symbol		C	Supply/Parameter[1]	Conditions	Value[2] Min	Typ	Max	Unit
V_{LVD290_IE0}	CC	P	$V_{DD\_HV\_IO\_ETH0}$	—	2.89	2.94	2.99	V
V_{LVD400_IE}	CC	P	$V_{DD\_HV\_EMMC}$	—	4.15	4.23	4.31	V
V_{LVD400_AS}	CC	P	$V_{DD\_HV\_ADV}$ (ADCSAR pad)	—	4.15	4.23	4.31	V
V_{LVD400_IM}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	4.15	4.23	4.31	V
V_{LVD400_IE1}	CC	P	$V_{DD\_HV\_IO\_ETH1}$		4.15	4.23	4.31	V
V_{LVD400_IE0}	CC	P	$V_{DD\_HV\_IO\_ETH0}$	—	4.15	4.23	4.31	V
High Voltage Detectors HV								
V_{HVD400_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$		3.68	3.75	3.82	V
V_{HVD400_IE1}	CC	P	$V_{DD\_HV\_IO\_ETH1}$		3.68	3.75	3.82	V
V_{HVD400_IE0}	CC	P	$V_{DD\_HV\_IO\_ETH0}$	—	3.68	3.75	3.82	V
Upper Voltage Detectors HV								
V_{UVD600_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$		5.72	5.82	5.92	V
V_{UVD600_F}	CC	P	$V_{DD\_HV\_FLA}$	—	5.72	5.82	5.92	V
V_{UVD600_IE1}	CC	P	$V_{DD\_HV\_IO\_ETH1}$	—	5.72	5.82	5.92	V
V_{UVD600_IE0}	CC	P	$V_{DD\_HV\_IO\_ETH0}$	—	5.72	5.82	5.92	V
PowerOn Reset LV								
V_{POR031_C}	CC	P	V_{DD_LV}	—	0.29	0.60	0.97	V
Minimum Voltage Detectors LV								
V_{MVD082_C}	CC	P	V_{DD_LV}	—	0.85	0.88	0.91	V
V_{MVD094_C}	CC	P	V_{DD_LV}	—	0.98	1.00	1.02	V
V_{MVD094_FA}	CC	P	V_{DD_LV} (Flash)	—	1.00	1.02	1.04	V
V_{MVD094_FB}	CC	P	V_{DD_LV} (Flash)	—	1.00	1.02	1.04	V
Low Voltage Detectors LV								
V_{LVD100_C}	CC	P	V_{DD_LV}	—	1.06	1.08	1.11	V
V_{LVD100_SB}	CC	P	V_{DD_LV} (In Standby)	—	0.99	1.01	1.03	V
V_{LVD100_F}	CC	P	V_{DD_LV} (Flash)	—	1.08	1.10	1.12	V
High Voltage Detectors LV								
V_{HVD134_C}	CC	P	V_{DD_LV}	—	1.28	1.31	1.33	V
Upper Voltage Detectors LV								
V_{UVD140_C}	CC	P	V_{DD_LV}	—	1.34	1.37	1.39	V
V_{UVD140_F}	CC	P	V_{DD_LV} (Flash)	—	1.34	1.37	1.39	V
Common								
$T_{VMFILTER}$	CC	D	Voltage monitor filter[3]	—	5	—	30	µs

1. Even if LVD/HVD monitor reaction is configurable, the application ensures that the device remains in the operative condition range, and the internal LVDx monitors are disabled by the application. Then an external voltage monitor with minimum threshold of VDD_LV(min) = 1.08 V measured at the device pad, has to be implemented.
For HVDx, if the application disables them, then they need to grant that VDD_LV and VDD_HV voltage levels stay withing the limitations provided in *Section 4.2: Absolute maximum ratings*.
2. The values reported are Trimmed values, where applicable.
3. See Figure 12. Transitions shorter than minimum are filtered. Transitions longer than maximum are not filtered, and will be delayed by $T_{VMFILTER}$ time. Transitions between minimum and maximum can be filtered or not filtered, according to temperature, process and voltage variations.

4.15 Flash memory

The following table shows the Wait State configuration.

Table 37. Wait State configuration

APC	RWSC	Frequency range (MHz)
000(1)	0	f $\leq$ 30
	1	f $\leq$ 60
	2	f $\leq$ 90
	3	f $\leq$ 120
	4	f $\leq$ 150
	5	f $\leq$ 180
	6	f $\leq$ 200
100(2)	0	f $\leq$ 30
	1	f $\leq$ 60
	2	f $\leq$ 90
	3	f $\leq$ 120
	4	f $\leq$ 150
	5	f $\leq$ 180
	6	f $\leq$ 200
001(3)	2	55 <f$\leq$ 80
	3	55 <f$\leq$ 120
	4	55 <f$\leq$ 150
	5	55 <f$\leq$ 180
	6	55 <f$\leq$ 200

1. STD pipelined.
2. No pipeline.
3. Pipeline with 1 Tck address anticipation.

The following table shows the Program/Erase Characteristics.

Table 38. Flash memory program and erase specifications

Symbol	Characteristics[1][2]	Value									Unit
		Typ[3]	C	Initial max			Typical end of life[4]	Lifetime max[5]		C	
				25 °C [6]	All temp [7]	C		< 1 K cycles	≤ 250 K cycles		
$t_{dwprogram}$	Double Word (64 bits) program time (Partition 0, 2 & 3)	55	C	130	—	—	140	650		C	µs
$t_{pprogram}$	Page (256 bits) program time	76	C	240	—	—	255	1000		C	µs
$t_{pprogrameep}$	Page (256 bits) program time (partition 0, 2 & 3)	90	C	300	—	—	315	1300		C	µs
$t_{qprogram}$	Quad Page (1024 bits) program time	220	C	840	1200	P	850	2000		C	µs
$t_{qprogrameep}$	Quad Page (1024 bits) program time (partition 0, 2 & 3)	306	C	1200	1800	P	1270	2600		C	µs
$t_{16kpperase}$	16 KB block pre-program and erase time	190	C	450	500	P	250	1000	—	C	ms
$t_{32kpperase}$	32 KB block pre-program and erase time	250	C	520	600	P	310	1200	—	C	ms
$t_{64kpperase}$	64 KB - Partition 0 32 KB block pre-program and erase time	360	C	700	750	P	420	1600	—	C	ms
$t_{128kpperase}$	128 KB - Partition 0 64 KB - Partition 0 96 KB block pre-program and erase time	600	C	1300	1600	P	800	4000	—	C	ms
$t_{256kpperase}$	256 KB block pre-program and erase time	1050	C	1800	2400	P	1600	4000	—	C	ms
$t_{16kprogram}$	16 KB block program time	25	C	45	50	P	40	1000	—	C	ms
$t_{32kprogram}$	32 KB block program time	50	C	90	100	P	75	1200	—	C	ms
$t_{64kprogram}$	64 KB - Partition 0 32 KB block program time	102	C	175	200	P	150	1600	—	C	ms
$t_{128kprogram}$	128 KB - Partition 0 64 KB - Partition 0 96 KB block program time	205	C	350	430	P	300	2000	—	C	ms
$t_{256kprogram}$	256 KB block program time	410	C	700	850	P	590	4000	—	C	ms
$t_{64kprogrameep}$	Program 64 KB Data Flash - EEPROM (partition 2)	120	C	200	300	P	330	2275		C	ms
$t_{64keraseeep}$	Erase 64 KB Data Flash - EEPROM (partition 2)	530	C	910	1150	P	1040	4700		C	ms
$t_{16kprogrameep}$	Program 16 KB Data Flash - EEPROM (partition 3)	30	C	52	75	P	84	2275		C	ms

Table 38. Flash memory program and erase specifications (continued)

Symbol	Characteristics(1)(2)	Value									Unit
		Typ(3)	C	Initial max			Typical end of life(4)	Lifetime max(5)		C	
				25 °C (6)	All temp (7)	C		< 1 K cycles	≤ 250 K cycles		
$t_{16keraseeep}$	Erase 16 KB Data Flash - EEPROM (partition 3)	225	C	645	715	P	520	4700		C	ms
t_{tr}	Program rate(8)	1.7	C	2.8	3.40	C	2.4	—		C	s/MB
t_{pr}	Erase rate(8)	4.8	C	7.2	9.6	C	6.4	—		C	s/MB
t_{tprfm}	Program rate Factory Mode(8)	1.12	C	1.4	1.6	C	—	—		C	s/MB
t_{erfm}	Erase rate Factory Mode(8)	4.0	C	5.2	5.8	C	—	—		C	s/MB
$t_{ffprogram}$	Full flash programming time(9)	19.8	C	29.3	36.3	P	25.4	—	—	C	s
$t_{fferase}$	Full flash erasing time(9)	41.2	C	66.0	82.4	P	66.0	—	—	C	s
t_{ESRT}	Erase suspend request rate(10)	200	T	—	—	—	—	—		—	µs
t_{PSRT}	Program suspend request rate(10)	30	T	—	—	—	—	—		—	µs
t_{AMRT}	Array Integrity Check - Margin Read suspend request rate	15	T	—	—	—	—	—		—	µs
t_{PSUS}	Program suspend latency(11)	—	—	—	—	—	—	12		T	µs
t_{ESUS}	Erase suspend latency(11)	—	—	—	—	—	—	22		T	µs
t_{AIC0S}	Array Integrity Check (10.0 MB, sequential)(12)	70	T	—	—	—	—	—	—	—	ms
$t_{AIC256KS}$	Array Integrity Check (256 KB, sequential)(12)	1.5	T	—	—	—	—	—	—	—	ms
t_{AIC0P}	Array Integrity Check (10.0 MB, proprietary)(12)	4.0	T	—	—	—	—	—	—	—	s
t_{MR0S}	Margin Read (10.0 MB, sequential)(12)	200	T	—	—	—	—	—	—	—	ms
$t_{MR256KS}$	Margin Read (256 KB, sequential)(12)	4.0	T	—	—	—	—	—	—	—	ms

1. Characteristics are valid both for Data Flash and Code Flash, unless specified in the characteristics column.
2. Actual hardware operation times; this does not include software overhead.
3. Typical program and erase times assume nominal supply values and operation at 25 °C.
4. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations. These values are characteristic, but not tested.

5. Lifetime maximum program & erase times apply across the voltages and temperatures and occur after the specified number of program/erase cycles. These maximum values are characterized but not tested or guaranteed.
6. Initial factory condition: < 100 program/erase cycles, 25 °C typical junction temperature and nominal (± 5%) supply voltages.
7. Initial maximum “All temp” program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, –40 °C < TJ < 150 °C junction temperature and nominal (± 5%) supply voltages.
8. Rate computed based on 256 KB sectors.
9. Only code sectors, not including EEPROM.
10. Time between suspend resume and next suspend. Value stated actually represents Min value specification.
11. Timings guaranteed by design.
12. AIC is done using system clock, thus all timing is dependent on system frequency and number of wait states. Timing in the table is calculated at max frequency.

All the Flash operations require the presence of the system clock for internal synchronization. About 50 synchronization cycles are needed: this means that the timings of the previous table can be longer if a low frequency system clock is used.

Table 39. Flash memory Life Specification

Symbol	Characteristics[(1) (2)]	Value				Unit
		Min	C	Typ	C	
N_{CER16K}	16 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER32K}	32 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER64K}	64 KB CODE Flash endurance	10	—	100	—	Kcycles
$N_{CER128K}$	96 KB and 128 KB CODE Flash endurance	1	—	100	—	Kcycles
$N_{CER256K}$	256 KB CODE Flash endurance	1	—	100	—	Kcycles
	256 KB CODE Flash endurance[(3)]	10	—	100	—	Kcycles
N_{DER64K}	64 KB DATA EEPROM Flash endurance	250	—	—	—	Kcycles
N_{DER16K}	16 KB HSM DATA EEPROM Flash endurance	100	—	—	—	Kcycles
t_{DR1k}	Minimum data retention Blocks with 0 - 1,000 P/E cycles	25	—	—	—	Years
t_{DR10k}	Minimum data retention Blocks with 1,001 - 10,000 P/E cycles	20	—	—	—	Years
t_{DR100k}	Minimum data retention Blocks with 10,001 - 100,000 P/E cycles	15	—	—	—	Years
t_{DR250k}	Minimum data retention Blocks with 100,001 - 250,000 P/E cycles	10	—	—	—	Years

1. Program and erase cycles supported across specified temperature specifications.
2. It is recommended that the application enables the core cache memory.
3. 10K cycles on 4-256 KB blocks is not intended for production. Reduced reliability and degraded erase time are possible.

4.16 AC Specifications

All AC timing specifications are valid up to 150 °C, except where explicitly noted.

4.16.1 Debug and calibration interface timing

4.16.1.1 JTAG interface timing

Table 40. JTAG pin AC electrical characteristics

#	Symbol		C	Characteristic	Value(1),(2)		Unit
					Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	100	—	ns
2	t_{JDC}	CC	T	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	15(3)	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	CC	D	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	CC	D	TCK falling edge to output valid	—	600(4)	ns
12	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only. See Table 41 for functional specifications.
2. JTAG timing specified at $V_{DD\_HV\_IO\_MAIN}$ = 4.0 to 5.5 V and max. loading per pad type as specified in the I/O section of the datasheet.
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

Figure 13. JTAG test clock input timing

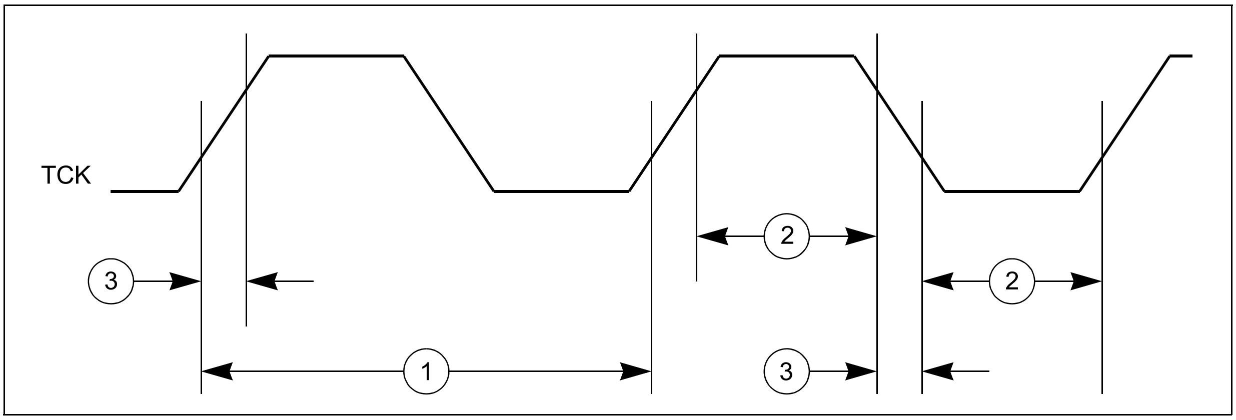


Figure 14. JTAG test access port timing

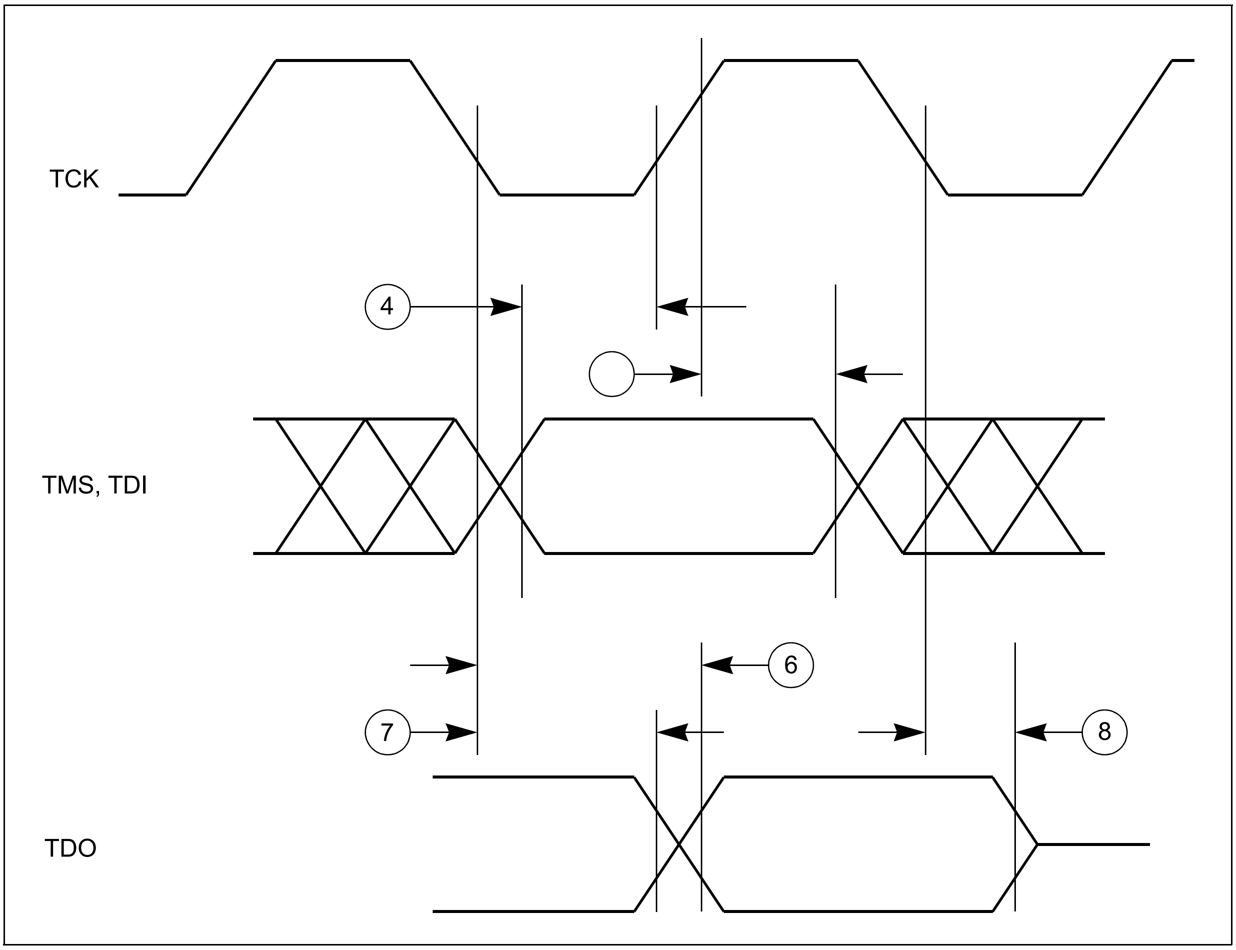


Figure 15. JTAG JCOMP timing

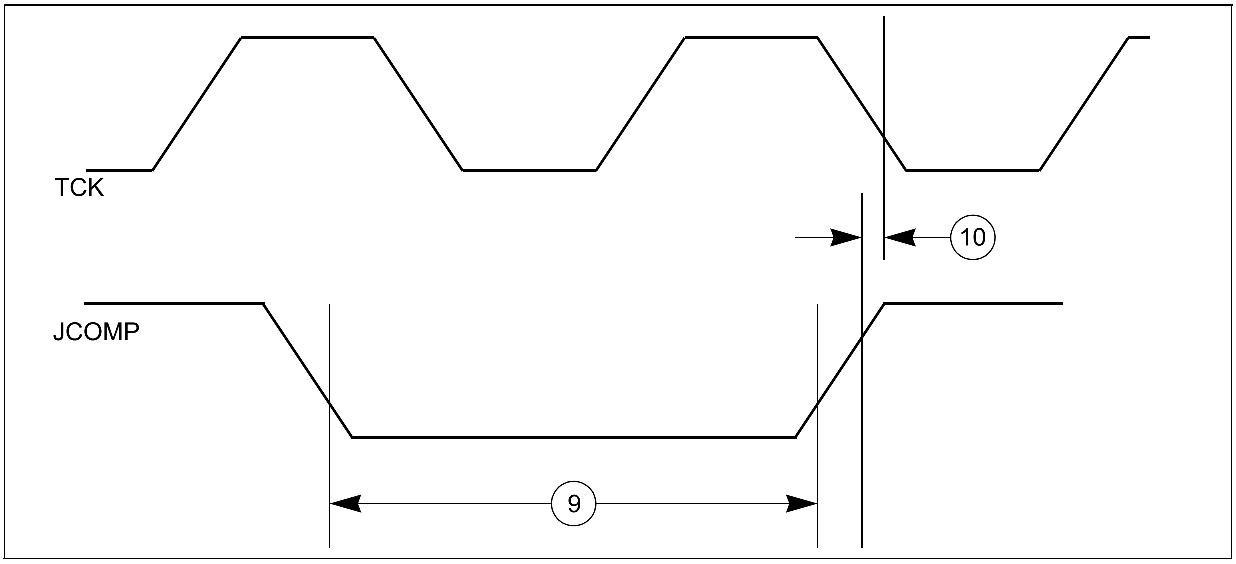
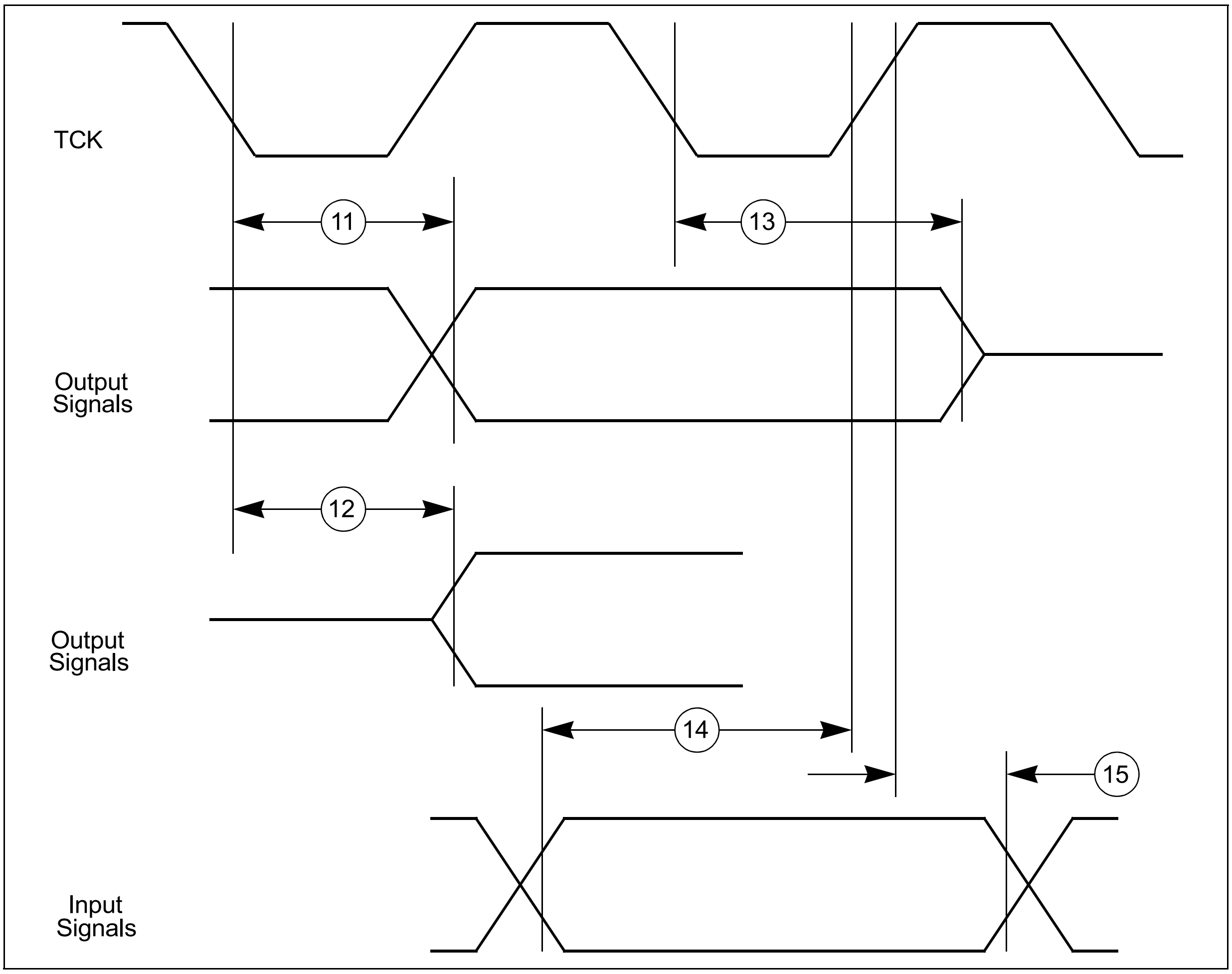


Figure 16. JTAG boundary scan timing



4.16.1.2 Nexus interface timing

Table 41. Nexus debug port timing

#	Symbol		C	Characteristic	Value(1)		Unit
					Min	Max	
7	t_{EVTIPW}	CC	D	$\overline{\text{EVTI}}$ pulse width	4	—	t_{CYC}(2)
8	t_{EVTOPW}	CC	D	$\overline{\text{EVTO}}$ pulse width	40	—	ns
9	t_{TCYC}	CC	D	TCK cycle time	2(3),(4)	—	t_{CYC}(2)
				Absolute minimum TCK cycle time(5) (TDO sampled on posedge of TCK)	60(6)	—	ns
				Absolute minimum TCK cycle time(7) (TDO sampled on negedge of TCK)	30(6)	—	
11	t_{NTDIS}	CC	D	TDI data setup time	5	—	ns
12	t_{NTDIH}	CC	D	TDI data hold time	5	—	ns
13	t_{NTMSS}	CC	D	TMS data setup time	5	—	ns
14	t_{NTMSH}	CC	D	TMS data hold time	5	—	ns
15	—	CC	D	TDO propagation delay from falling edge of TCK(8)	—	25	ns
16	—	CC	D	TDO hold time with respect to TCK falling edge (minimum TDO propagation delay)	2.25	—	ns

1. Nexus timing specified at $V_{DD\_HV\_IO\_MAIN}$ = 3.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.
2. t_{CYC} is system clock period.
3. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual peripheral frequency being used. To ensure proper operation TCK frequency should be set to the peripheral frequency divided by a number greater than or equal to that specified here.
4. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
5. This value is TDO propagation time 36 ns + 4 ns setup time to sampling edge.
6. This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.
7. This value is TDO propagation time 16 ns + 4 ns setup time to sampling edge.
8. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.

Figure 17. Nexus output timing

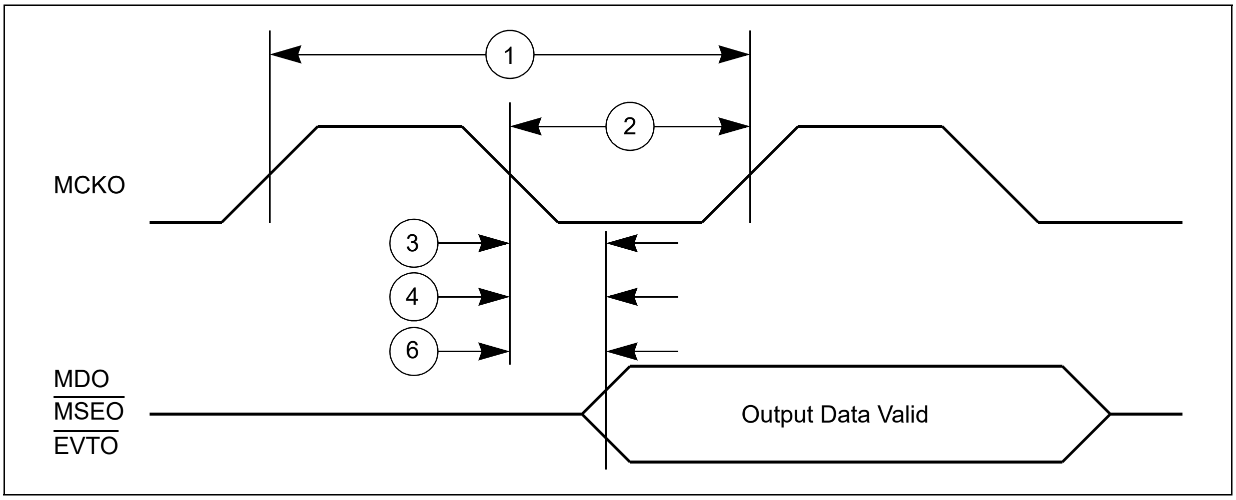


Figure 18. Nexus event trigger and test clock timings

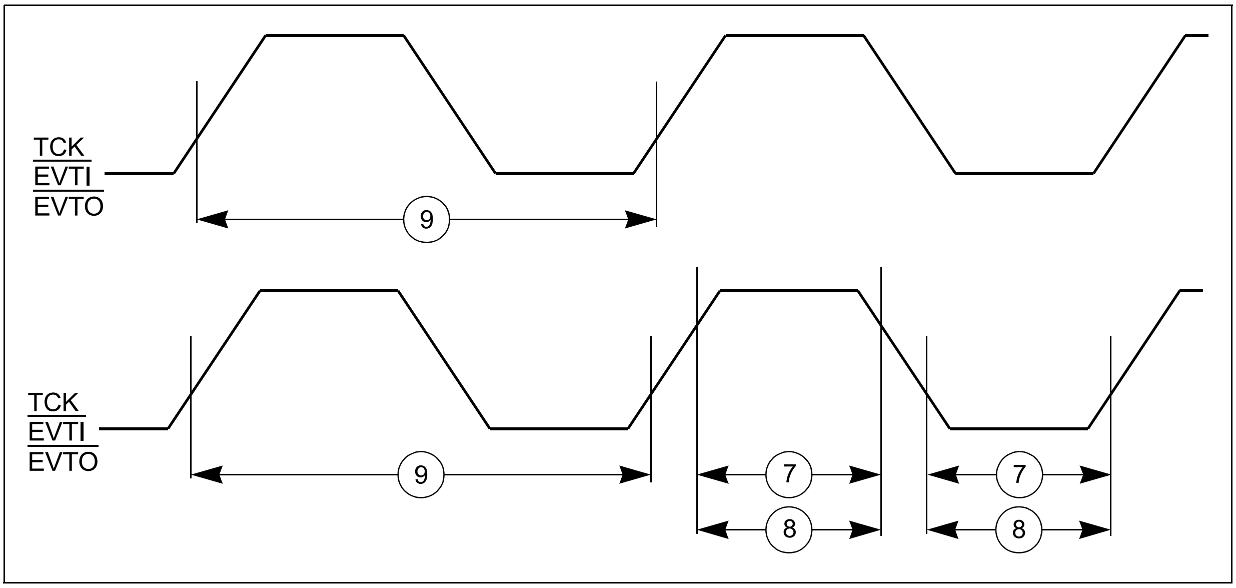
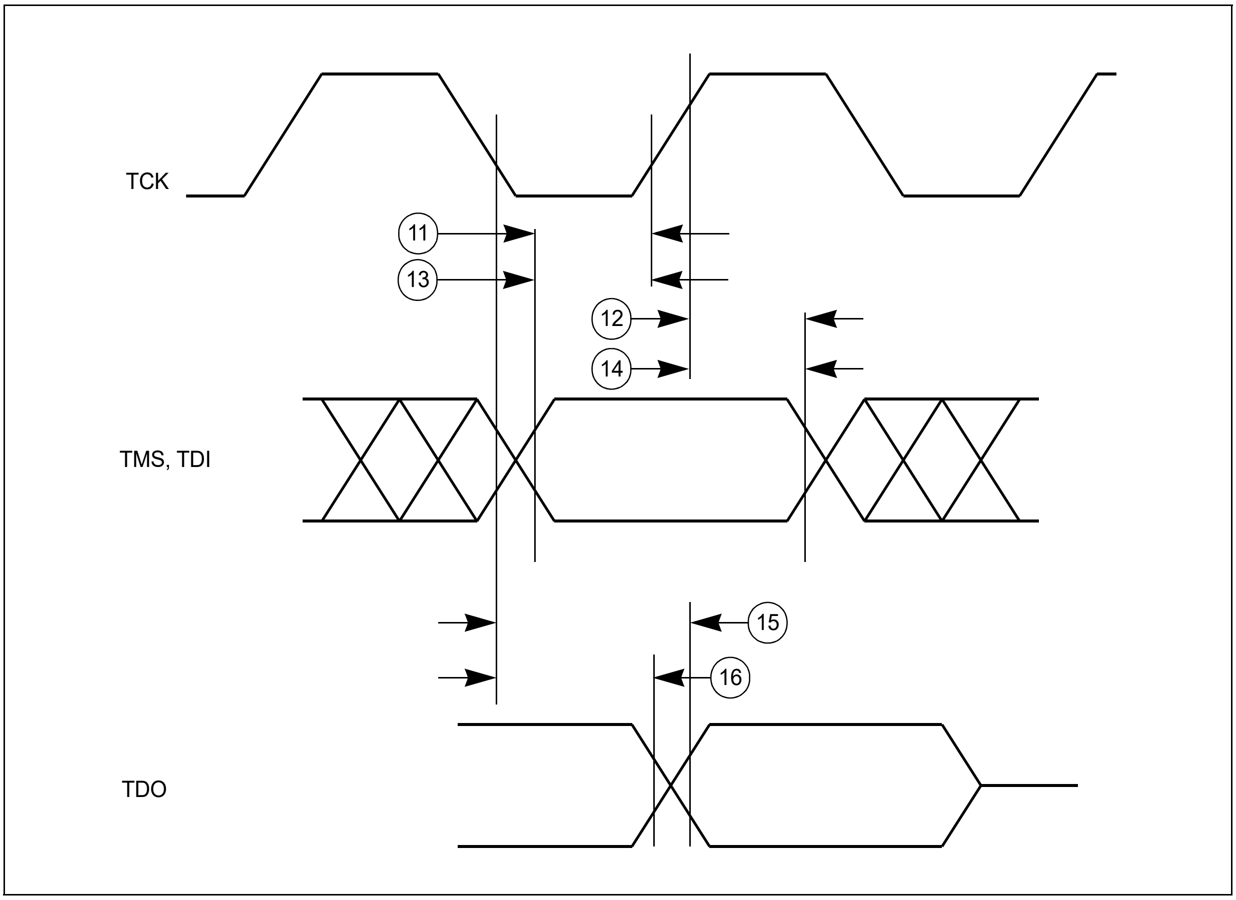


Figure 19. Nexus TDI, TMS, TDO timing



4.16.1.3 External interrupt timing (IRQ pin)

Table 42. External interrupt timing

Characteristic	Symbol	Min	Max	Unit
IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}
IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}
IRQ Edge to Edge Time(1)	t_{ICYC}	6	—	t_{cyc}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

Figure 20. External interrupt timing

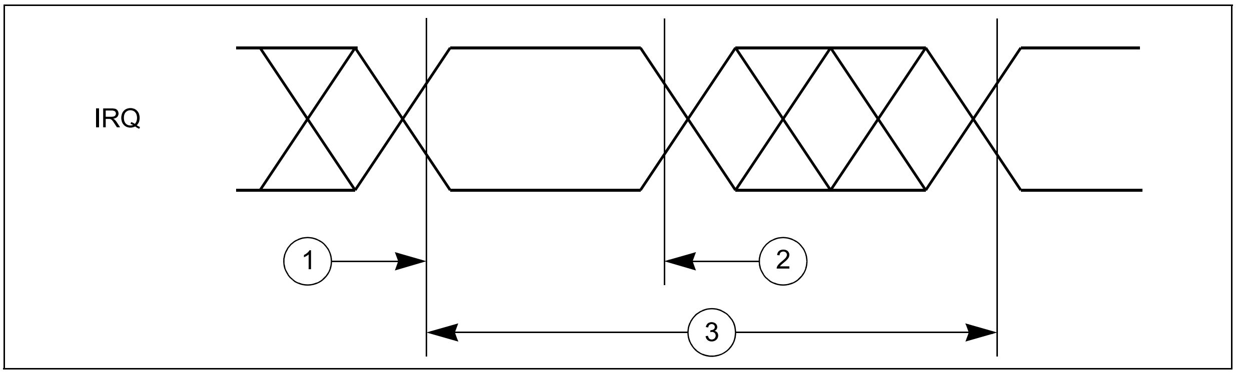
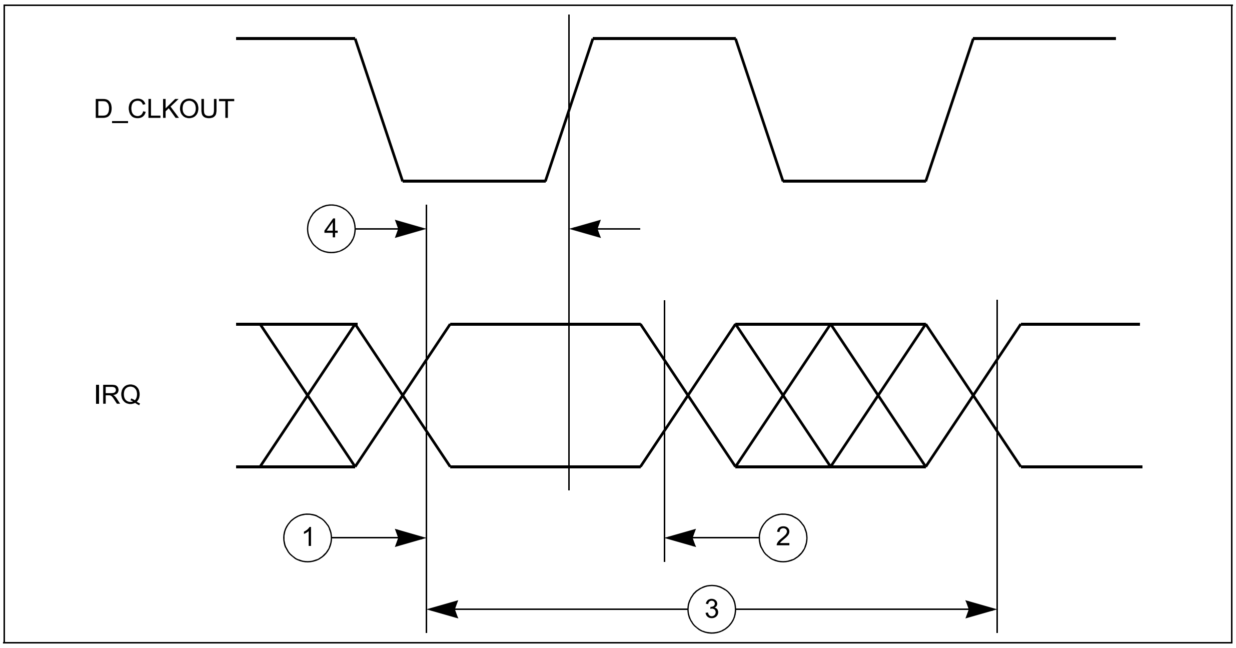


Figure 21. External interrupt timing



4.16.2 DSPI timing with CMOS pads

DSPI channel frequency support is shown in *Table 43*.

Timing specifications are shown in the tables below.

Table 43. DSPI channel frequency support

DSPI use mode(1)			Max usable frequency (MHz)(2),(3)
CMOS (Master mode)	Full duplex – Classic timing (Table 44)	DSPI_0, DSPI_1, DSPI_2, DSPI_3, DSPI_6, DSPI_7, DSPI_8, DSPI_9	10
		DSPI_4, DSPI_5	17
	Full duplex – Modified timing (Table 45)	DSPI_0, DSPI_1, DSPI_2, DSPI_3, DSPI_6, DSPI_7, DSPI_8, DSPI_9	10
		DSPI_4, DSPI_5	30
	Output only mode (SCK/SOUT/PCS) (Table 44 and Table 45)	DSPI_0, DSPI_1, DSPI_2, DSPI_3, DSPI_6, DSPI_7, DSPI_8, DSPI_9	10
		DSPI_4, DSPI_5	30
	Output only mode TSB mode (SCK/SOUT/PCS)	DSPI_0, DSPI_1, DSPI_2, DSPI_3, DSPI_6, DSPI_7, DSPI_8, DSPI_9	10
		DSPI_4, DSPI_5	30
CMOS (Slave mode Full duplex) (Table 46)		—	16

1. Each DSPI module can be configured to use different pins for the interface. Refer to the device pinout Microsoft Excel file attached to the IO_Definition document for the available combinations. It is not possible to reach the maximum performance with every possible combination of pins.
2. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
3. Maximum usable frequency does not take into account external device propagation delay.

4.16.2.1 DSPI master mode full duplex timing with CMOS pads

4.16.2.1.1 DSPI CMOS master mode – classic timing

Note: In the following table, all output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Table 44. DSPI CMOS master classic timing (full duplex and output only) MTFE = 0, CPHA = 0 or 1

#	Symbol		C	Characteristic	Condition		Value[1]		Unit
					Pad drive[2]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	59.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	(N[3] × t_{SYS}[4]) – 16	—	ns
					Strong	50 pF	(N[3] × t_{SYS}[4]) – 16	—	
					Medium	50 pF	(N[3] × t_{SYS}[4]) – 16	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	(N[3] × t_{SYS}[4]) – 29	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	(M[5] × t_{SYS}[4]) – 35	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	(M[5] × t_{SYS}[4]) – 35	—	
					Medium	PCS = 0 pF SCK = 50 pF	(M[5] × t_{SYS}[4]) – 35	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	(M[5] × t_{SYS}[4]) – 35	—	
4	t_{SDC}	CC	D	SCK duty cycle[6]	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time[7]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time[7]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns

Table 44. DSPI CMOS master classic timing (full duplex and output only) MTFE = 0, CPHA = 0 or 1 (continued)

#	Symbol		C	Characteristic	Condition		Value(1)		Unit
					Pad drive(2)	Load (C_L)	Min	Max	
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK(8)	SCK drive strength				
					Very strong	25 pF	25.0	—	ns
					Strong	50 pF	31.0	—	
					Medium	50 pF	52.0	—	
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK(8)	SCK drive strength				
					Very strong	0 pF	–1.0	—	ns
					Strong	0 pF	–1.0	—	
					Medium	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK(9)	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	
					Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK(9)	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	
					Medium	50 pF	–15.0	—	

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
3. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
4. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
5. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. PCSx and PCSS using same pad configuration.
8. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL voltage thresholds.
9. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 22. DSPI CMOS master mode — classic timing, CPHA = 0

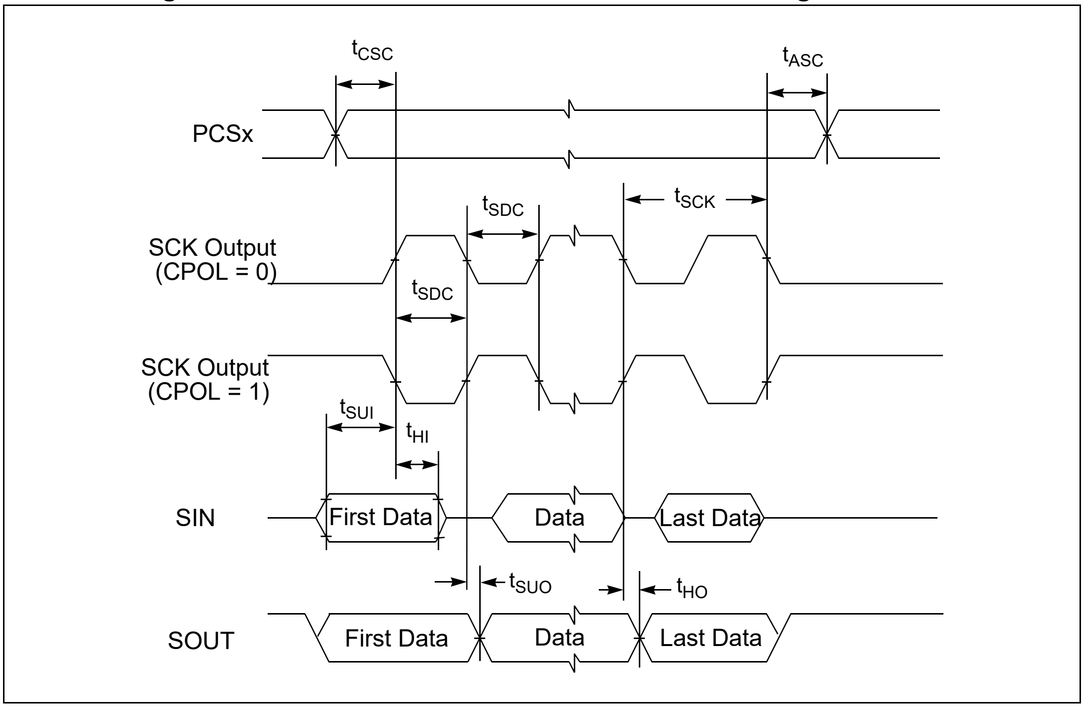


Figure 23. DSPI CMOS master mode — classic timing, CPHA = 1

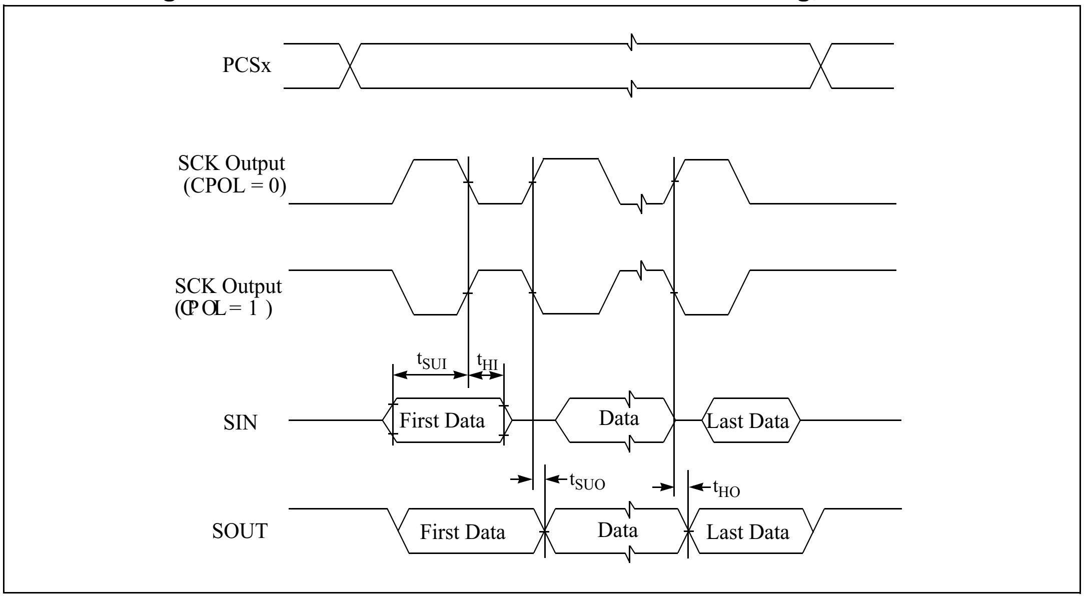
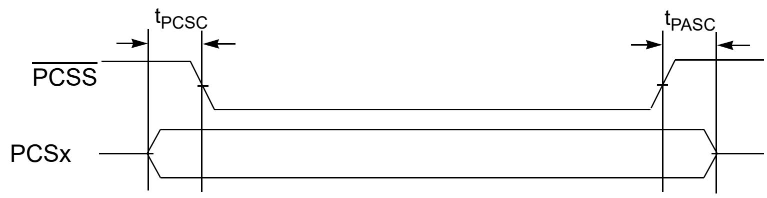


Figure 24. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)



4.16.2.1.2 DSPI CMOS master mode — modified timing

Note: In the following table, all output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Table 45. DSPI CMOS master modified timing (full duplex and output only) MTFE = 1, CPHA = 0 or 1

#	Symbol		C	Characteristic	Condition		Value[1]		Unit
					Pad drive[2]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(3)} \times t_{SYS}{}^{(4)}) - 16$	—	ns
					Strong	50 pF	$(N^{(3)} \times t_{SYS}{}^{(4)}) - 16$	—	
					Medium	50 pF	$(N^{(3)} \times t_{SYS}{}^{(4)}) - 16$	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(3)} \times t_{SYS}{}^{(4)}) - 29$	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}{}^{(4)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}{}^{(4)}) - 35$	—	
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}{}^{(4)}) - 35$	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}{}^{(4)}) - 35$	—	

Table 45. DSPI CMOS master modified timing (full duplex and output only) MTFE = 1, CPHA = 0 or 1 (continued)

#	Symbol		C	Characteristic	Condition		Value[1]		Unit
					Pad drive[2]	Load (C_L)	Min	Max	
4	t_{SDC}	CC	D	SCK duty cycle[6]	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time[7]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time[7]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK CPHA = 0[8]	SCK drive strength				
					Very strong	25 pF	25 – (P[9] × t_{SYS}[4])	—	ns
					Strong	50 pF	31 – (P[9] × t_{SYS}[4])	—	
					Medium	50 pF	52 – (P[9] × t_{SYS}[4])	—	
				SIN setup time to SCK CPHA = 1[8]	SCK drive strength				
					Very strong	25 pF	25.0	—	ns
					Strong	50 pF	31.0	—	
					Medium	50 pF	52.0	—	
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK CPHA = 0[8]	SCK drive strength				
					Very strong	0 pF	–1 + (P[9] × t_{SYS}[3])	—	ns
					Strong	0 pF	–1 + (P[9] × t_{SYS}[3])	—	
					Medium	0 pF	–1 + (P[9] × t_{SYS}[3])	—	
				SIN hold time from SCK CPHA = 1[8]	SCK drive strength				
					Very strong	0 pF	–1.0	—	ns
					Strong	0 pF	–1.0	—	
					Medium	0 pF	–1.0	—	

Table 45. DSPI CMOS master modified timing (full duplex and output only) MTFE = 1, CPHA = 0 or 1 (continued)

#	Symbol		C	Characteristic	Condition		Value[1]		Unit
					Pad drive[2]	Load (C_L)	Min	Max	
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK CPHA = 0, [10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	$7.0 + t_{SYS}$[4]	ns
					Strong	50 pF	—	$8.0 + t_{SYS}$[4]	
					Medium	50 pF	—	$16.0 + t_{SYS}$[4]	
				SOUT data valid time from SCK CPHA = 1[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	
					Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK CPHA = 0[10]	SOUT and SCK drive strength				
					Very strong	25 pF	$-7.7 + t_{SYS}$[4]	—	ns
					Strong	50 pF	$-11.0 + t_{SYS}$[4]	—	
					Medium	50 pF	$-15.0 + t_{SYS}$[4]	—	
				SOUT data hold time after SCK CPHA = 1[10]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	
					Medium	50 pF	–15.0	—	

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
3. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
4. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
5. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. PCSx and PCSS using same pad configuration.
8. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL voltage thresholds.
9. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.

10. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 25. DSPI CMOS master mode — modified timing, CPHA = 0

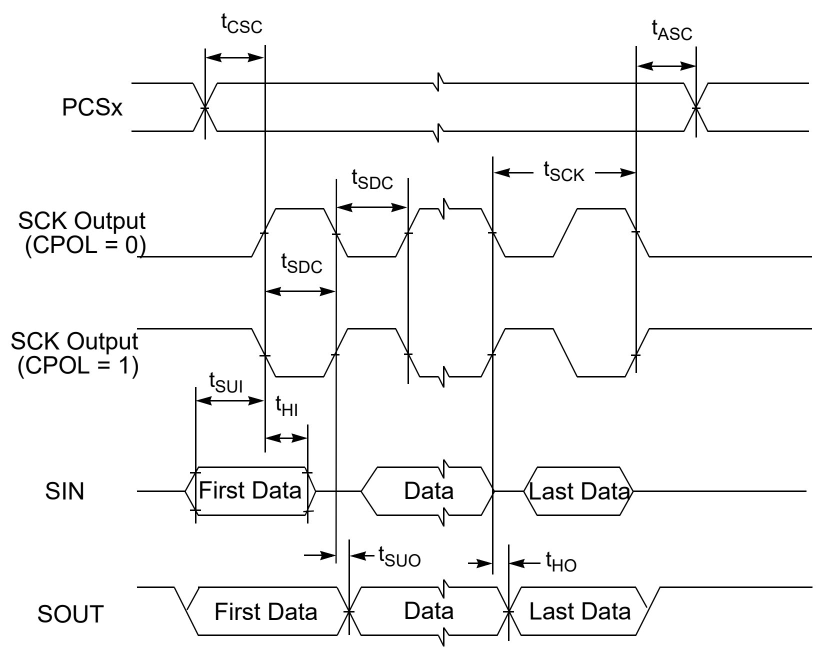


Figure 26. DSPI CMOS master mode — modified timing, CPHA = 1

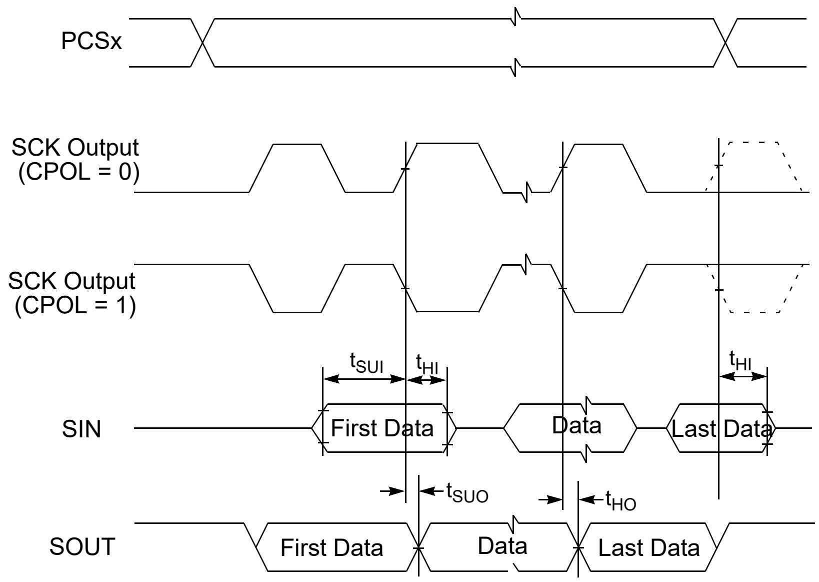
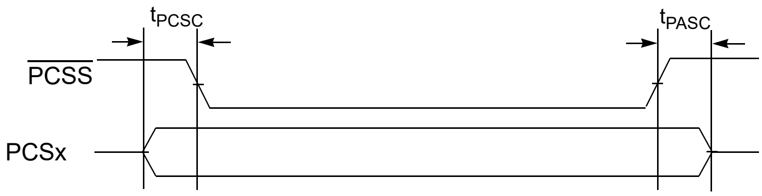


Figure 27. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)



4.16.2.2 Slave mode timing

Table 46. DSPI CMOS slave timing — full duplex — normal and modified transfer formats (MTFE = 0/1)

#	Symbol		C	Characteristic	Condition		Min	Max	Unit
					Pad Drive	Load			
1	t_{SCK}	CC	D	SCK Cycle Time(1)	—	—	62	—	ns
2	t_{CSC}	SR	D	$\overline{SS}$ to SCK Delay(1)	—	—	16	—	ns
3	t_{ASC}	SR	D	SCK to $\overline{SS}$ Delay(1)	—	—	16	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle(1)	—	—	30	—	ns
5	t_A	CC	D	Slave Access Time(1) (2) (3) ($\overline{SS}$ active to SOUT driven)	Very strong	25 pF	—	50	ns
					Strong	50 pF	—	50	ns
					Medium	50 pF	—	60	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time(1) (2) (3) ($\overline{SS}$ inactive to SOUT High-Z or invalid)	Very strong	25 pF	—	5	ns
					Strong	50 pF	—	5	ns
					Medium	50 pF	—	10	ns
9	t_{SUI}	CC	D	Data Setup Time for Inputs(1)	—	—	10	—	ns
10	t_{HI}	CC	D	Data Hold Time for Inputs(1)	—	—	10	—	ns
11	t_{SUO}	CC	D	SOUT Valid Time(1) (2) (3) (after SCK edge)	Very strong	25 pF	—	30	ns
					Strong	50 pF	—	30	ns
					Medium	50 pF	—	50	ns
12	t_{HO}	CC	D	SOUT Hold Time(1) (2) (3) (after SCK edge)	Very strong	25 pF	2.5	—	ns
					Strong	50 pF	2.5	—	ns
					Medium	50 pF	2.5	—	ns

1. Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL voltage thresholds.
2. All timing values for output signals in this table, are measured to 50% of the output voltage.
3. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Figure 28. DSPI slave mode — modified transfer format timing (MFTE = 0/1) CPHA = 0

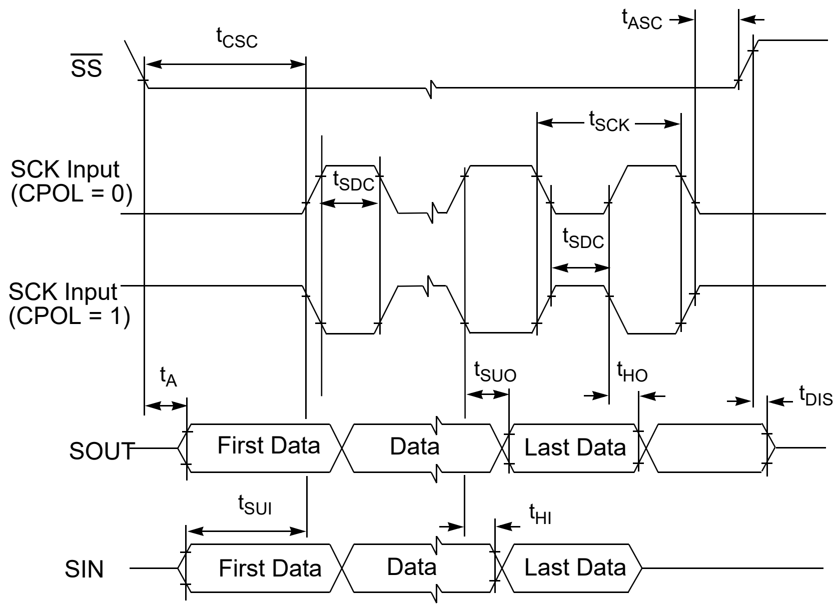
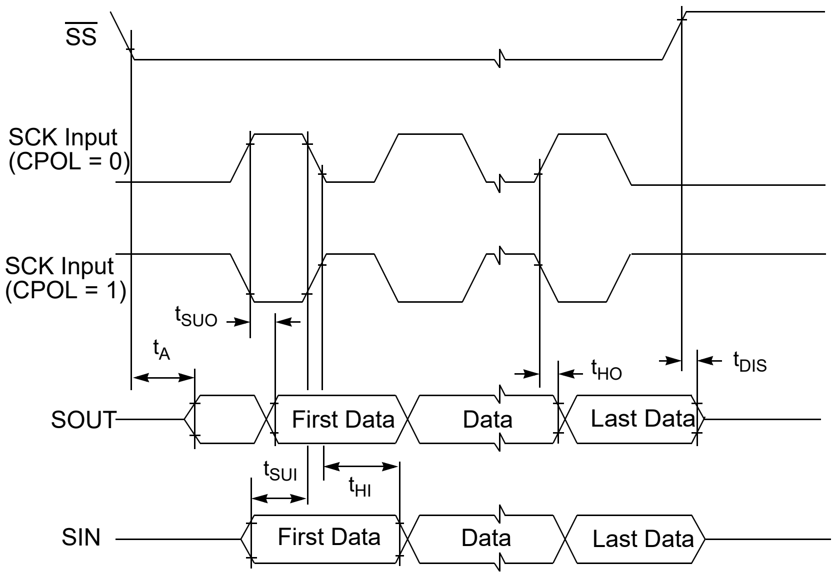


Figure 29. DSPI slave mode — modified transfer format timing (MFTE = 0/1) CPHA = 1



4.16.3 Ethernet port timing

Both Ethernet ports provide MII and RMII interfaces. Moreover Ethernet0 supports TMII (overclocked MII) whereas Ethernet1 supports RGMII. The Ethernet ports signals can be configured for either CMOS or TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V. Check the device pinout details to review package options versus exposed Ethernet ports' interfaces (MII, RMII,TMII, RGMII).

4.16.3.1 MII receive signal timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

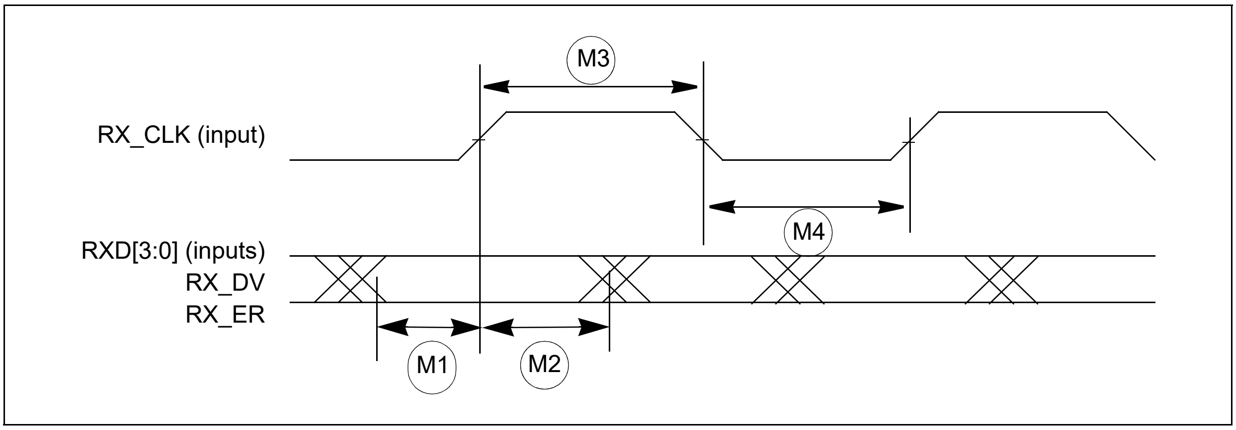
The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

Note: In the following table, all timing specifications are referenced from RX_CLK = 1.4 V to the valid input levels, 0.8 V and 2.0 V.

Table 47. MII receive signal timing

Symbol		C	Characteristic	Value		Unit
				Min	Max	
M1	CC	D	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	CC	D	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	CC	D	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	CC	D	RX_CLK pulse width low	35%	65%	RX_CLK period

Figure 30. MII receive signal timing diagram



4.16.3.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This option allows the use of non-compliant MII PHYs.

Refer to the SPC58EHx, SPC58NHx 32-bit Power Architecture microcontroller *reference manual's* Ethernet chapter for details of this option and how to enable it.

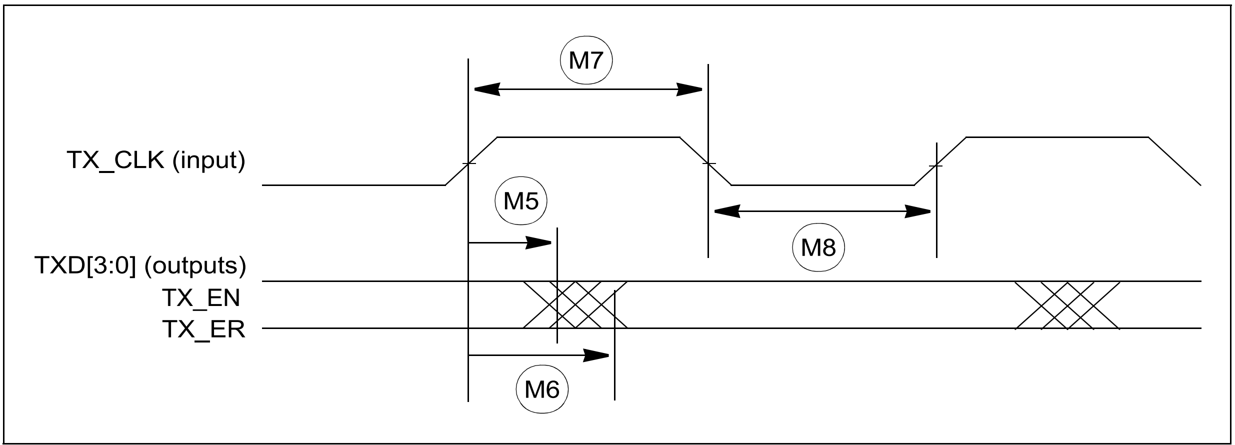
Note: In the following table, all timing specifications are referenced from TX_CLK = 1.4 V to the valid output levels, 0.8 V and 2.0 V.

Table 48. MII transmit signal timing

Symbol		C	Characteristic	Value(1)		Unit
				Min	Max	
M5	CC	D	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	CC	D	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	CC	D	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	CC	D	TX_CLK pulse width low	35%	65%	TX_CLK period

1. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value

Figure 31. MII transmit signal timing diagram



4.16.3.3 MII async inputs signal timing (CRS and COL)

Table 49. MII async inputs signal timing

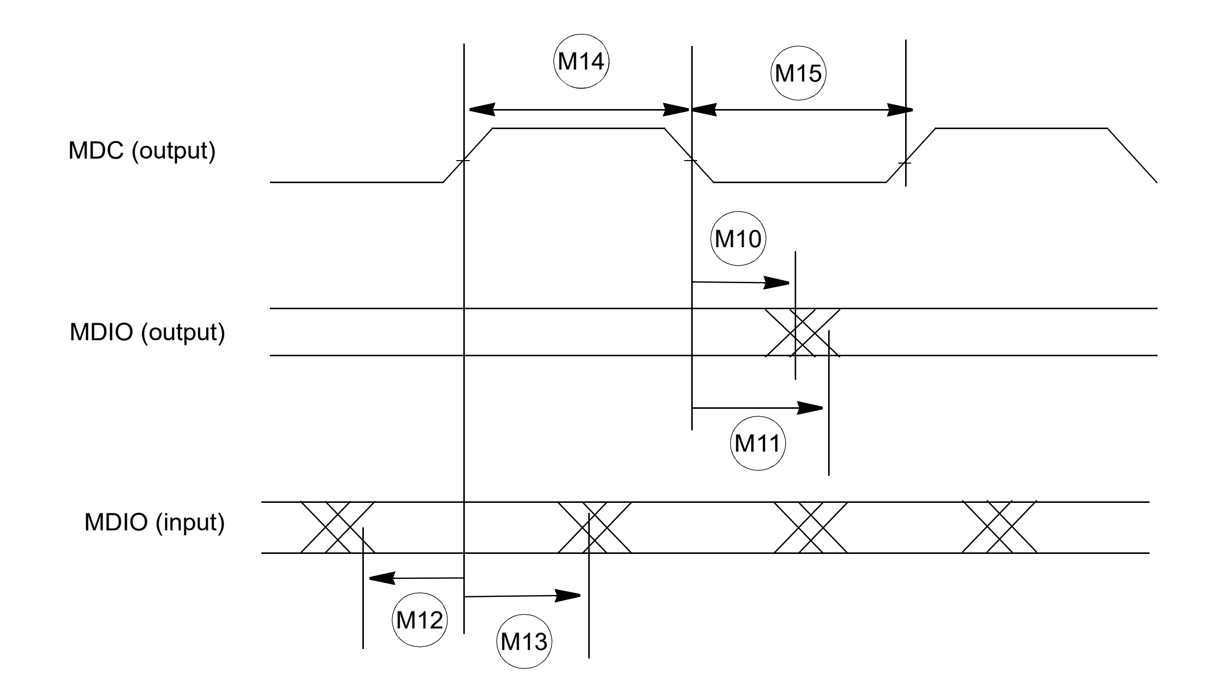
Symbol		C	Characteristic	Value		Unit
				Min	Max	
M9	CC	D	CRS, COL minimum pulse width	1.5	—	TX_CLK period

Figure 32. MII async inputs timing diagram

4.16.3.4 MII and RMII serial management channel timing (MDIO and MDC)

The Ethernet functions correctly with a maximum MDC frequency of 2.5 MHz.

Figure 33. MII serial management channel timing diagram



4.16.3.5 MII and RMII serial management channel timing (MDIO and MDC)

The Ethernet functions correctly with a maximum MDC frequency of 2.5 MHz.

Note: In the following table, all timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.

Table 50. MII serial management channel timing

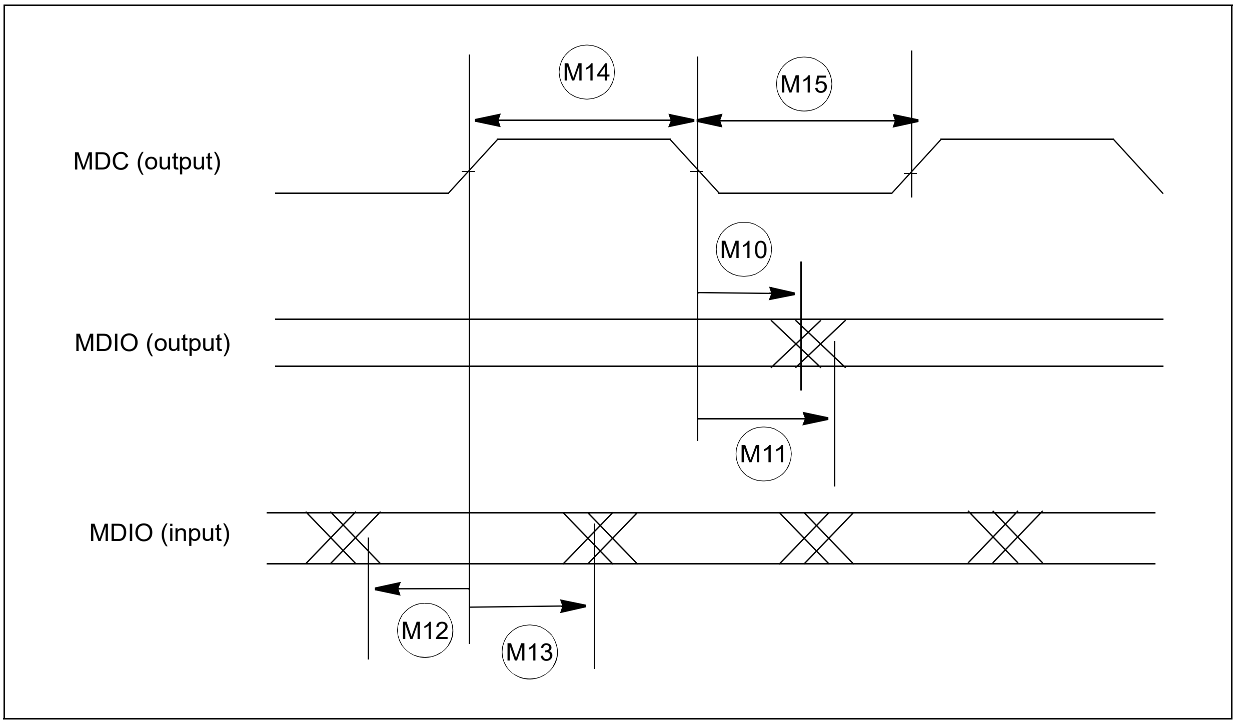
Symbol		C	Characteristic	Value		Unit
				Min	Max	
M10	CC	D	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	CC	D	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	CC	D	MDIO (input) to MDC rising edge setup	10	—	ns
M13	CC	D	MDIO (input) to MDC rising edge hold	0	—	ns
M14	CC	D	MDC pulse width high	40%	60%	MDC period
M15	CC	D	MDC pulse width low	40%	60%	MDC period

Note: In the following table, all timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.

Table 51. RMII serial management channel timing

Symbol		C	Characteristic	Value		Unit
				Min	Max	
M10	CC	D	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	CC	D	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	CC	D	MDIO (input) to MDC rising edge setup	10	—	ns
M13	CC	D	MDIO (input) to MDC rising edge hold	0	—	ns
M14	CC	D	MDC pulse width high	40%	60%	MDC period
M15	CC	D	MDC pulse width low	40%	60%	MDC period

Figure 34. MII serial management channel timing diagram



4.16.3.6 RMII receive signal timing (RXD[1:0], CRS_DV)

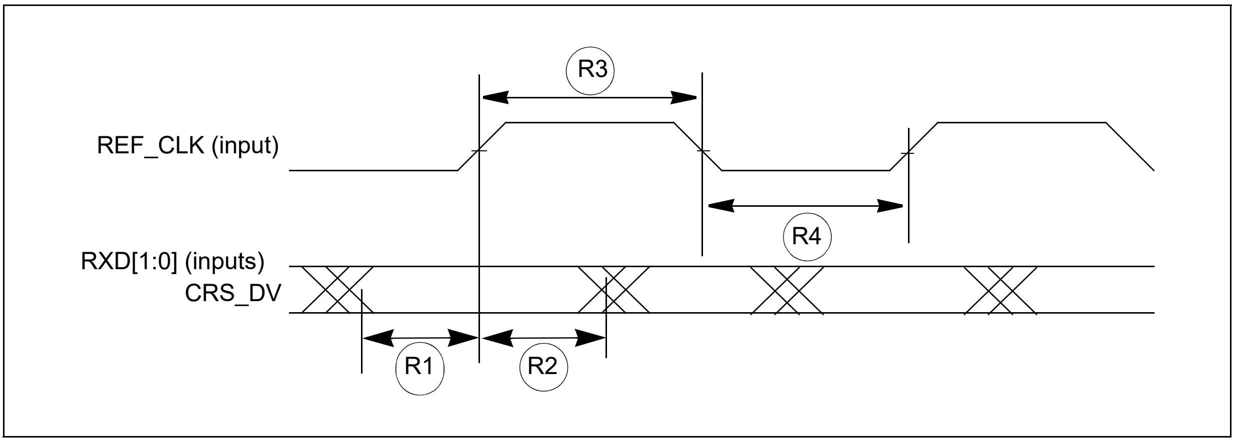
The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

Note: In the following table, all timing specifications are referenced from REF_CLK = 1.4 V to the valid input levels, 0.8 V and 2.0 V.

Table 52. RMII receive signal timing

Symbol		C	Characteristic	Value		Unit
				Min	Max	
R1	CC	D	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	CC	D	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	CC	D	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	CC	D	REF_CLK pulse width low	35%	65%	REF_CLK period

Figure 35. RMII receive signal timing diagram



4.16.3.7 RMII transmit signal timing (TXD[1:0], TX_EN)

The transmitter functions correctly up to a REF_CLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency, which is half that of the REF_CLK frequency.

The transmit outputs (TXD[1:0], TX_EN) can be programmed to transition from either the rising or falling edge of REF_CLK, and the timing is the same in either case. This option allows the use of non-compliant RMII PHYs.

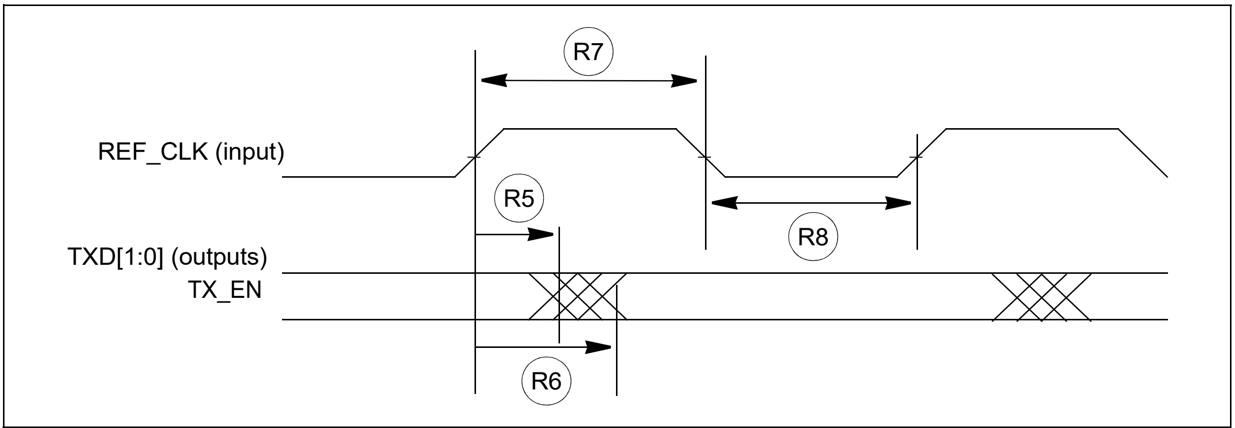
Note: In the following table, all timing specifications are referenced from REF_CLK = 1.4 V to the valid output levels, 0.8 V and 2.0 V.

RMII transmit signal valid timing specified is considering the rise/fall time of the ref_clk on the pad as 1 ns.

Table 53. RMII transmit signal timing

Symbol		C	Characteristic	Value		Unit
				Min	Max	
R5	CC	D	REF_CLK to TXD[1:0], TX_EN invalid	2	—	ns
R6	CC	D	REF_CLK to TXD[1:0], TX_EN valid	—	15	ns
R7	CC	D	REF_CLK pulse width high	35%	65%	REF_CLK period
R8	CC	D	REF_CLK pulse width low	35%	65%	REF_CLK period

Figure 36. RMII transmit signal timing diagram



4.16.3.8 RGMII signal timing

The RGMII interface uses Double Data Rate (DDR) data transfer scheme; it requires that the clock signal is delayed against the data and control signals.

This RGMII interface is compliant with the delay mode Delay on Source (DoS), where the transmitter device already provides a delayed clock signal.

For detailed AC specifications, refer to chapter 7.3 “Signal timing parameters in DoS mode” of specification “OPEN Alliance RGMII EPL (Electrical-Physical Layer) Recommendations” standard v2.3.

4.16.4 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals.

These are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

4.16.4.1 TxEN

Figure 37. TxEN signal

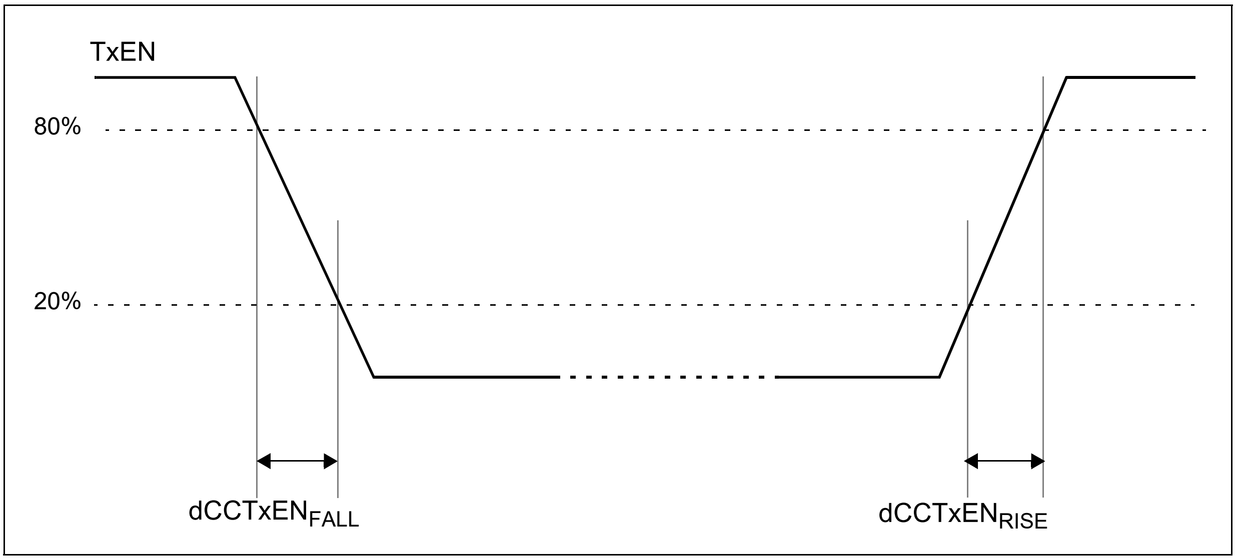
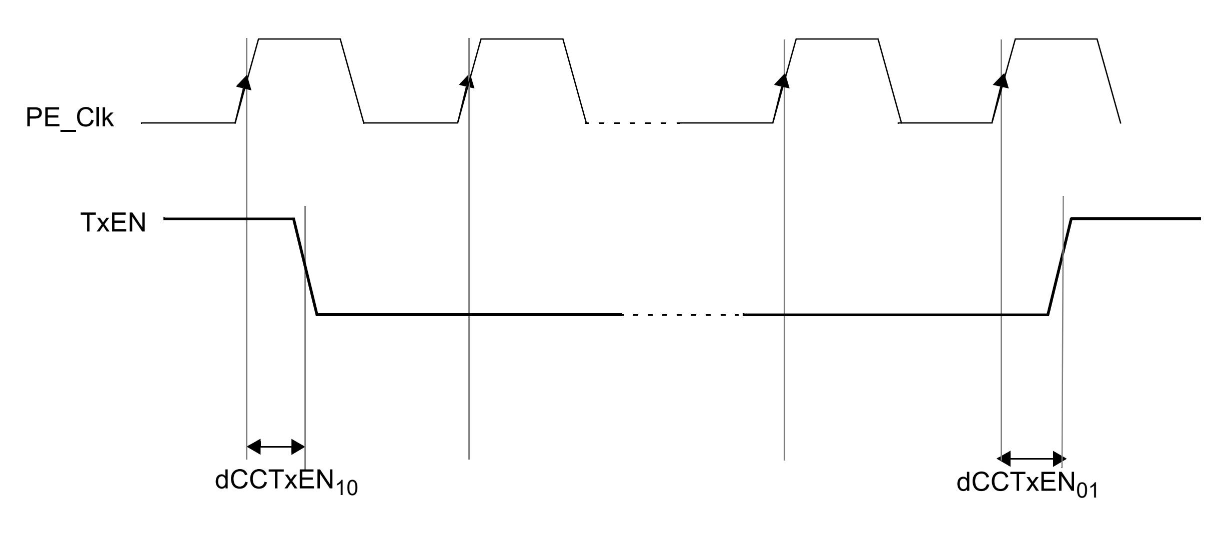


Table 54. TxEN output characteristics

Symbol		C	Characteristic[1] [2]	Value		Unit
				Min	Max	
$dCCTxEN_{RISE25}$	CC	D	Rise time of TxEN signal at CC	—	9	ns
$dCCTxEN_{FALL25}$	CC	D	Fall time of TxEN signal at CC	—	9	ns
$dCCTxEN_{01}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxEN_{10}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

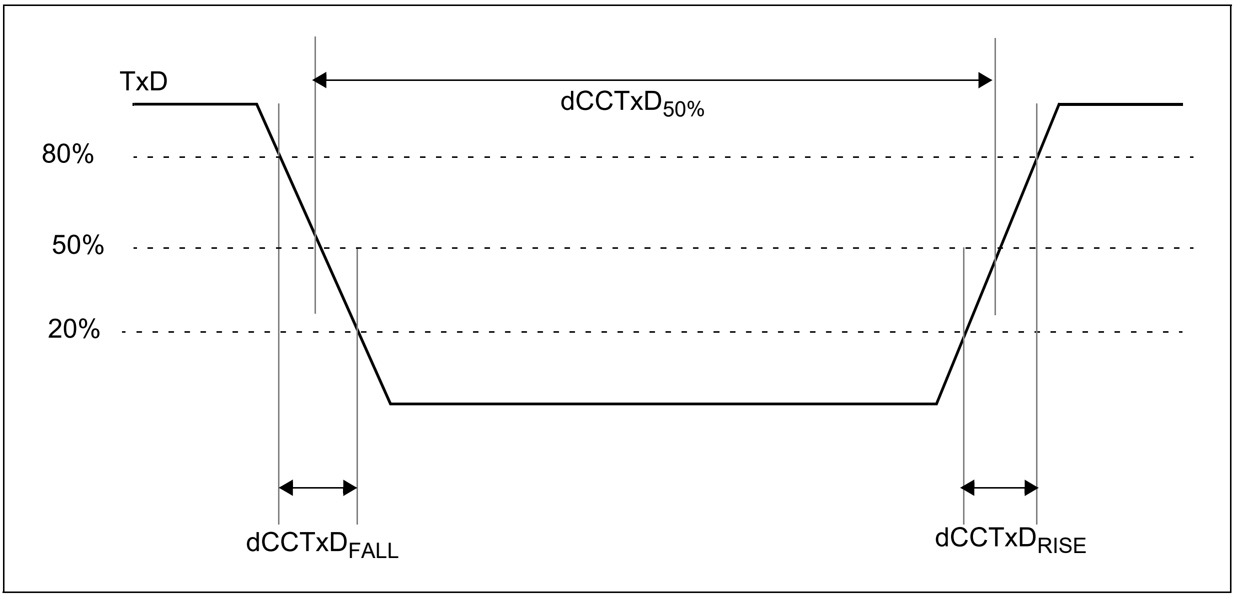
1. TxEN pin load maximum 25 pF.
2. Pad configured as VERY STRONG.

Figure 38. TxEN signal propagation delays



4.16.4.2 TxD

Figure 39. TxD signal



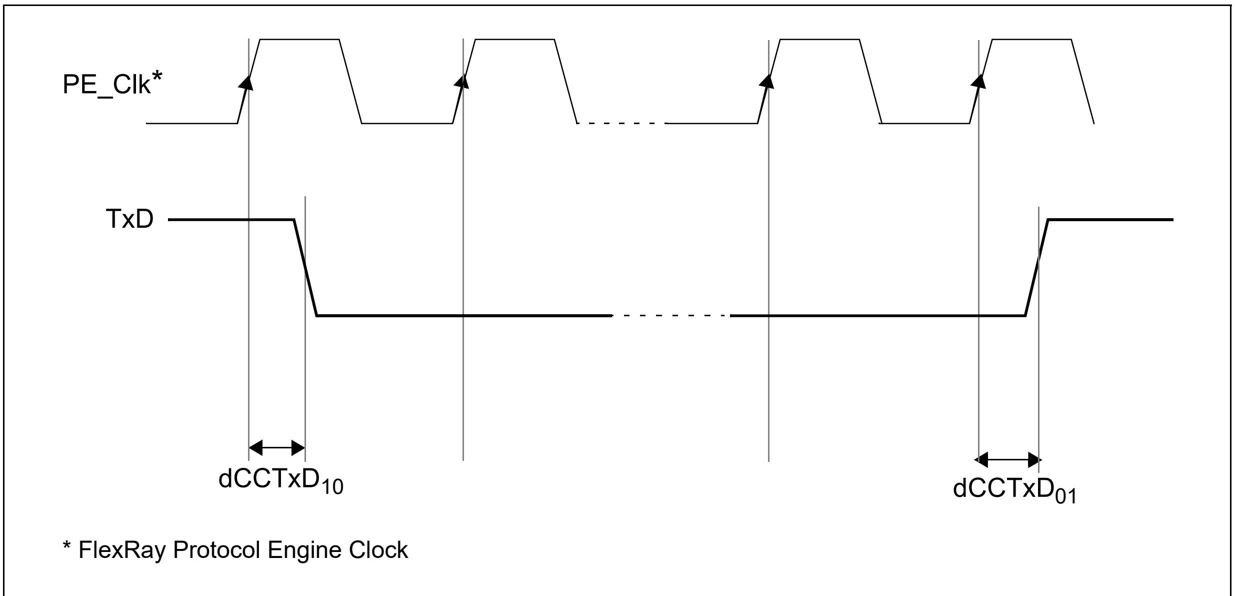
Note: In the following table, specifications valid according to FlexRay EPL 3.0.1 standard with 20%–80% levels and a 10 pF load at the end of a 50 Ohm, 1 ns stripline. Please refer to the Very Strong I/O pad specifications.

Table 55. TxD output characteristics

Symbol		C	Characteristic[(1),(2)]	Value Min	Value Max	Unit
dCCTxAsym	CC	D	Asymmetry of sending CC at 25 pF load (= $dCCTxD_{50\%}$ – 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	CC	D	Sum of Rise and Fall time of TxD signal at the output pin[(3)]	—	9[(4)]	ns
		D		—	9[(5)]	
$dCCTxD_{01}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. TxD pin load maximum 25 pF.
2. Pad configured as VERY STRONG.
3. Sum of transition time simulation is performed according to Electrical Physical Layer Specification 3.0.1 and the entire temperature range of the device has been taken into account.
4. $V_{DD\_HV\_IO}$ = 5.0 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 1 ns, C_L = 10 pF.
5. $V_{DD\_HV\_IO}$ = 3.3 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 0.6 ns, C_L = 10 pF.

Figure 40. TxD Signal propagation delays



4.16.4.3 RxD

Table 56. RxD input characteristics

Symbol		C	Characteristic	Value Min	Value Max	Unit
C_CCRxD	CC	D	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	CC	D	Threshold for detecting logic high	35	70	%

Table 56. RxD input characteristics (continued)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
uCCLogic_0	CC	D	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	CC	D	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	CC	D	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns
dCCRxAsymAccept15	CC	D	Acceptance of asymmetry at receiving CC with 15 pF load	–31.5	44	ns
dCCRxAsymAccept25	CC	D	Acceptance of asymmetry at receiving CC with 25 pF load	–30.5	43	ns

4.16.5 CAN timing

The following table describes the CAN timing.

Table 57. CAN timing

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
$t_{P(RX:TX)}$	CC	D	CAN controller propagation delay time standard pads	Medium type pads 25pF load	—	—	70	ns
	CC	D		Medium type pads 50pF load	—	—	80	
	CC	D		STRONG, VERY STRONG type pads 25pF load	—	—	60	
	CC	D		STRONG, VERY STRONG type pads 50pF load	—	—	65	
$t_{PLP(RX:TX)}$	CC	D	CAN controller propagation delay time low power pads	Medium type pads 25pF load	—	—	90	ns
	CC	D		Medium type pads 50pF load	—	—	100	
	CC	D		STRONG, VERY STRONG type pads 25pF load	—	—	80	
	CC	D		STRONG, VERY STRONG type pads 50pF load	—	—	85	

4.16.6 UART timing

UART channel frequency support is shown in the following table.

Table 58. UART frequency support

LINFlexD clock frequency LIN_CLK (MHz)	Oversampling rate	Voting scheme	Max usable frequency (Mbaud)
80	16	3:1 majority voting	5
	8		10
	6	Limited voting on one sample with configurable sampling point	13.33
	5		16
	4		20
100	16	3:1 majority voting	6.25
	8		12.5
	6	Limited voting on one sample with configurable sampling point	16.67
	5		20
	4		25

4.16.7 I2C timing

The I^2C AC timing specifications are provided in the following tables.

Note: In the following table, I2C input timing is valid for Automotive and TTL inputs levels, hysteresis enabled, and an input edge rate no slower than 1 ns (10% – 90%).

Table 59. I2C input timing specifications – SCL and SDA

No.	Symbol		C	Parameter	Value Min	Value Max	Unit
1	—	CC	D	Start condition hold time	2	—	PER_CLK Cycle(1)
2	—	CC	D	Clock low time	8	—	PER_CLK Cycle
3	—	CC	D	Bus free time between Start and Stop condition	4.7	—	μs
4	—	CC	D	Data hold time	0.0	—	ns
5	—	CC	D	Clock high time	4	—	PER_CLK Cycle
6	—	CC	D	Data setup time	0.0	—	ns
7	—	CC	D	Start condition setup time (for repeated start condition only)	2	—	PER_CLK Cycle
8	—	CC	D	Stop condition setup time	2	—	PER_CLK Cycle

1. PER_CLK is the SoC peripheral clock, which drives the I^2C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

Note: In the following table:

- *All output timing is worst case and includes the mismatching of rise and fall times of the output pads.*

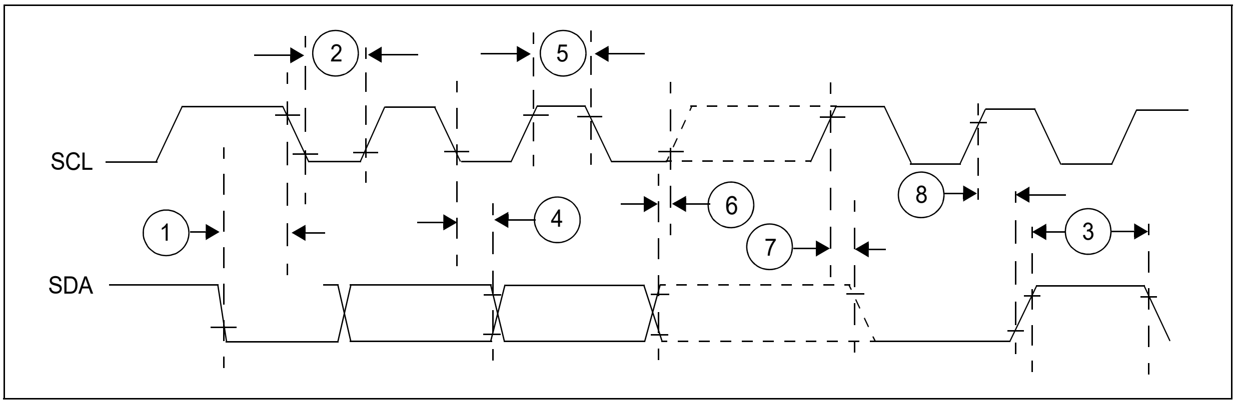
- *Output parameters are valid for CL = 25 pF, where CL is the external load to the device (lumped). The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.*
- *Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.*
- *Programming the IBFD register (I2C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the pre-scale and division values programmed in the IBC field of the IBFD register.*

Table 60. I2C output timing specifications — SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	6	—	PER_CLK Cycle(1)
2	—	CC	D	Clock low time	10	—	PER_CLK Cycle
3	—	CC	D	Bus free time between Start and Stop condition	4.7	—	μs
4	—	CC	D	Data hold time	7	—	PER_CLK Cycle
5	—	CC	D	Clock high time	10	—	PER_CLK Cycle
6	—	CC	D	Data setup time	2	—	PER_CLK Cycle
7	—	CC	D	Start condition setup time (for repeated start condition only)	20	—	PER_CLK Cycle
8	—	CC	D	Stop condition setup time	10	—	PER_CLK Cycle

1. PER_CLK is the SoC peripheral clock, which drives the I^2C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

Figure 41. I^2C input/output timing



4.16.8 PSI5 timing

Table 61. PSI5 timing

Symbol		C	Parameter	Value		Unit
				Min.	Max.	
t_{MSG_DLY}	CC	D	Delay from last bit of frame (CRC0) to assertion of new message received interrupt	—	3	µs
t_{SYNC_DLY}	CC	D	Delay from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin		2	
t_{MSG_JIT}	CC	D	Delay jitter from last bit of frame (CRC0) to assertion of new message received interrupt		1	cycle(1)
t_{SYNC_JIT}	CC	D	Delay jitter from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin		±(1 PSI5_1µs_CLK + 1 PBRIDGEn_CLK)	cycle

1. Measured in PSI5 clock cycles (PBRIDGEn_CLK on the device). Minimum PSI5 clock period is 20 ns.

4.16.9 OctoSPI timing

4.16.9.1 OctoSPI mode

For SDR mode, below table is applied considering:

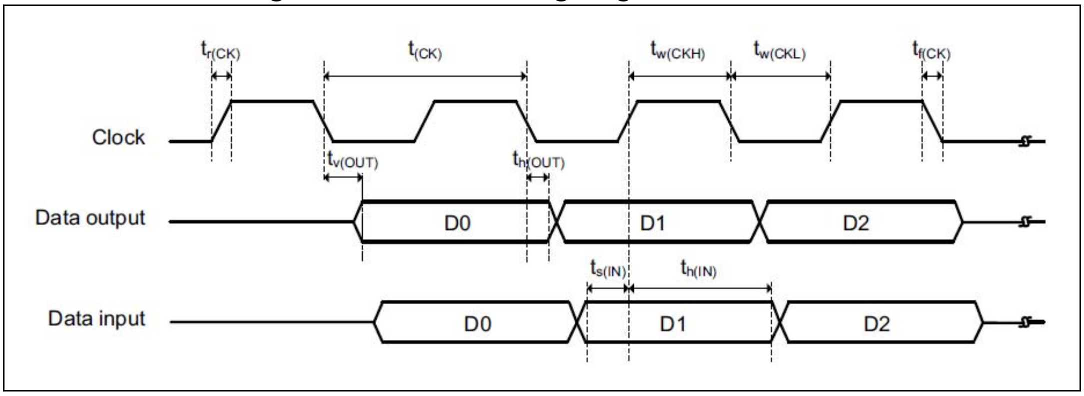
1. OERC for o/p pads are set as “11”
2. No delay module used for input clock
3. DQS being used as input clock. In case Clock Out being used as CLk In, frequency and input timings would depend on memory characteristics and delay module might be needed.
4. These timings are with OCTOSPI_DCR2.PRESCALAR = 1;

Table 62. OctoSPI characteristics in SDR mode

Symbol	Parameter	Conditions	Value(1)			Unit
			Min	Typ	Max	
F(CLK)	OctoSPI clock frequency	2.7 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 8 pF	—	—	100	MHz
$t_{w(CKH)}$	OctoSPI clock high and low time	—	45	—	55	ns
$t_{w(CKL)}$			45	—	55	
$t_{s(IN)}$	Data input setup time	—	0.5	—	—	
$t_{h(IN)}$	Data input hold time	—	2.5	—	—	
$t_{v(OUT)}$	Data output valid time	—	—	—	2	
$t_{h(OUT)}$	Data output hold time	—	-1(2)	—	—	

1. Values in the table applies to Octal and Quad SPI mode.
2. This hold time is with respect to negative edge of CLK_{out}.

Figure 42. OctoSPI timing diagram - SDR mode



4.16.9.2 Hyperbus mode

The SPC58EHx, SPC58NHx microcontroller's OCTOSPI interface supports Hyperbus memory devices with AC specifications compliant with Hyperbus_Specification_Cypress_revF.pdf document (001-99253 Rev. *F, June 2017, chapter 9.3 AC Characteristics). Note that:

- Table 9.2 Clock Timing (on page 33 of this document) is valid if Freq <= 100 Mhz
- Single Ended clock (no CK# signal)
- Only 3.3 +/-10% voltage configuration
- CS/RWDS/DQ/CK should be balanced on board
- tDSS/tDSH specs not met by default. Internal delay module in SPC58EHx, SPC58NHx microcontroller should be used by tuning OCTOSPI_DELAY_CFG and OCTOSPI_DELAY_CTRL registers to achieve 1/12th cycle delay on DQS, to aid correct data latching in OCTOSPI controller.

4.16.10 SDMMC timing

For SD SDIO modes, refer to AC specifications as in “SD Specifications Part 1 Physical Layer Specification” document version 3.01, Feb. 2010, chapter “6.6 Bus Operating Conditions for 3.3V Signaling”).

For eMMC mode, refer to AC specifications as in JEDEC standard “EMBEDDED MULTI-MEDIA CARD (eMMC), ELECTRICAL STANDARD (4.5 Device)”, JESD84-B45, June 2011, chapters “10.5 Bus timing” and “10.6 Bus timing for DAT signals during 2x data rate operation”.

Note: t_{IHddr} and t_{IH} input hold timing parameters minimum value is 1 ns.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

The following table lists the case numbers for SPC58EHx, SPC58NHx.

Table 63. Package case numbers

Package type	Device type
eTQFP144	Production
eLQFP176	Production
FPBGA302	Production
FPBGA386	Production

5.1 eTQFP144 package information

Refer to *Section 5.1.1: Package mechanical drawings and data information* for full description of below figures and table notes.

Figure 43. eTQFP144 package outline

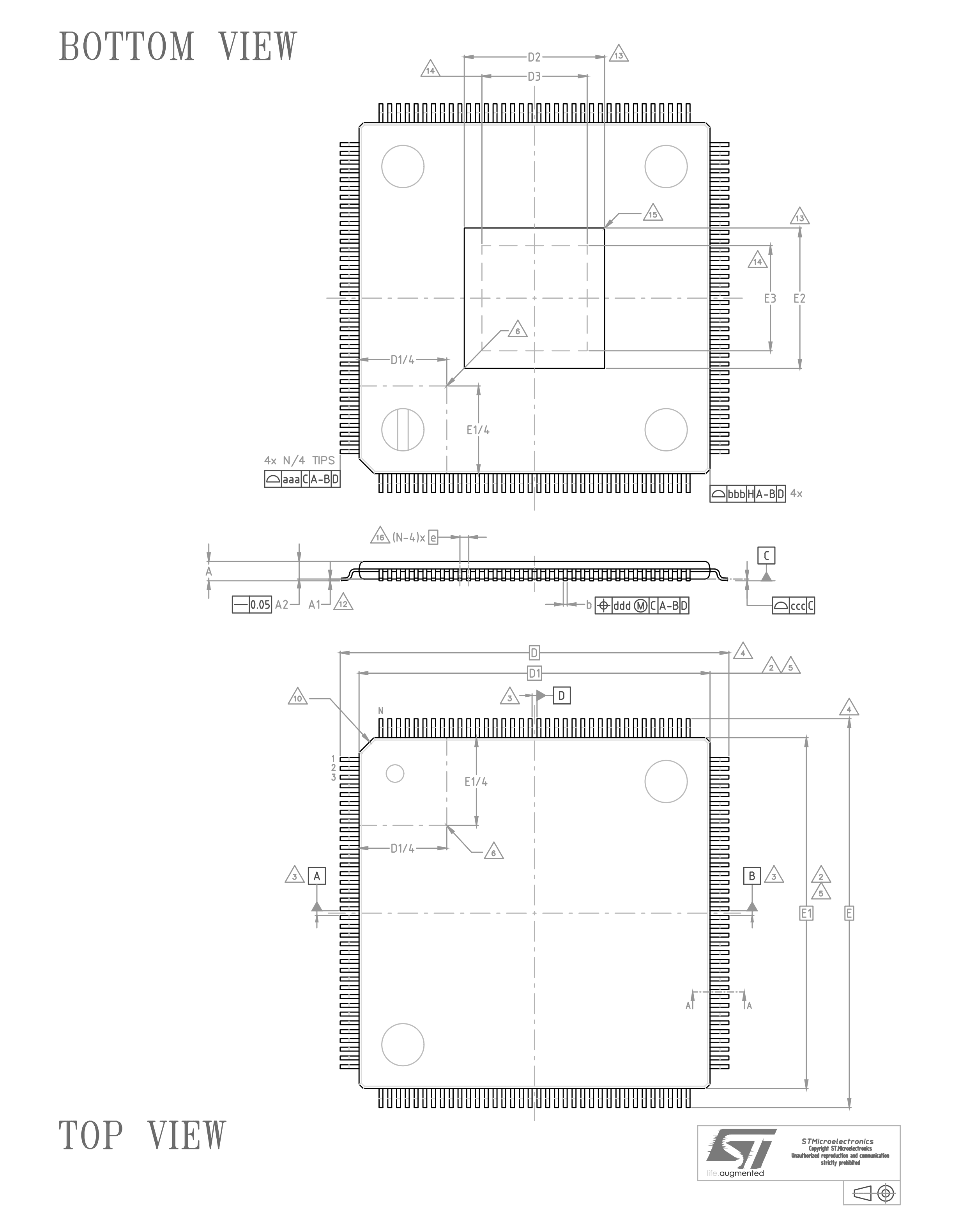


Figure 44. eTQFP144 section A-A

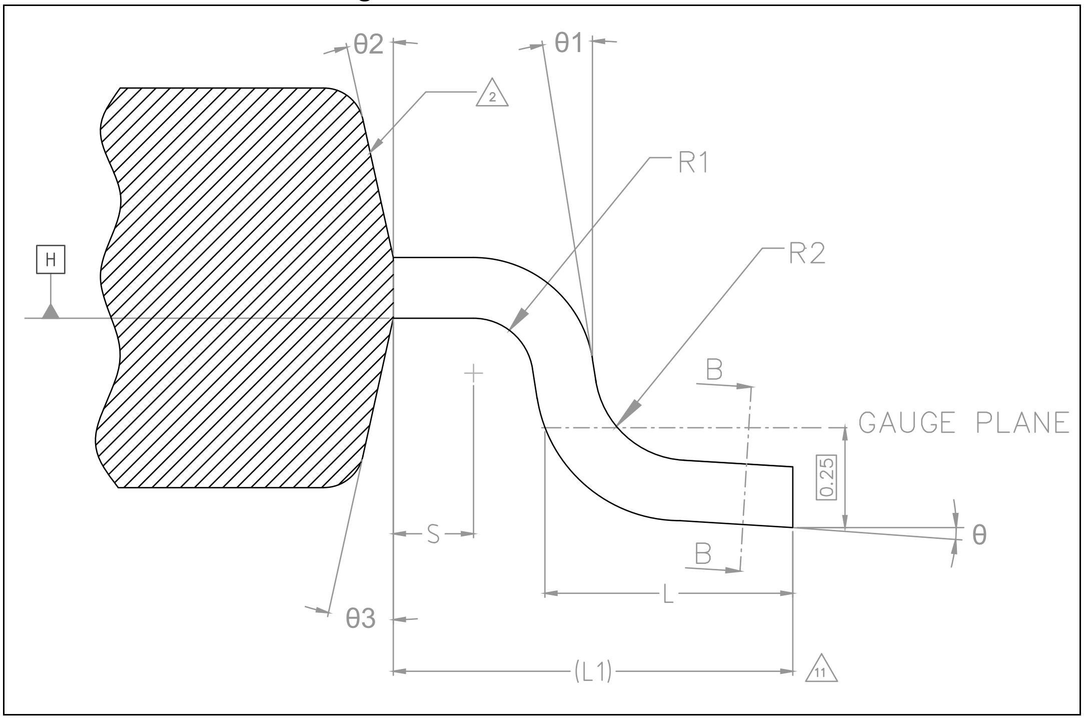


Figure 45. eTQFP144 section B-B

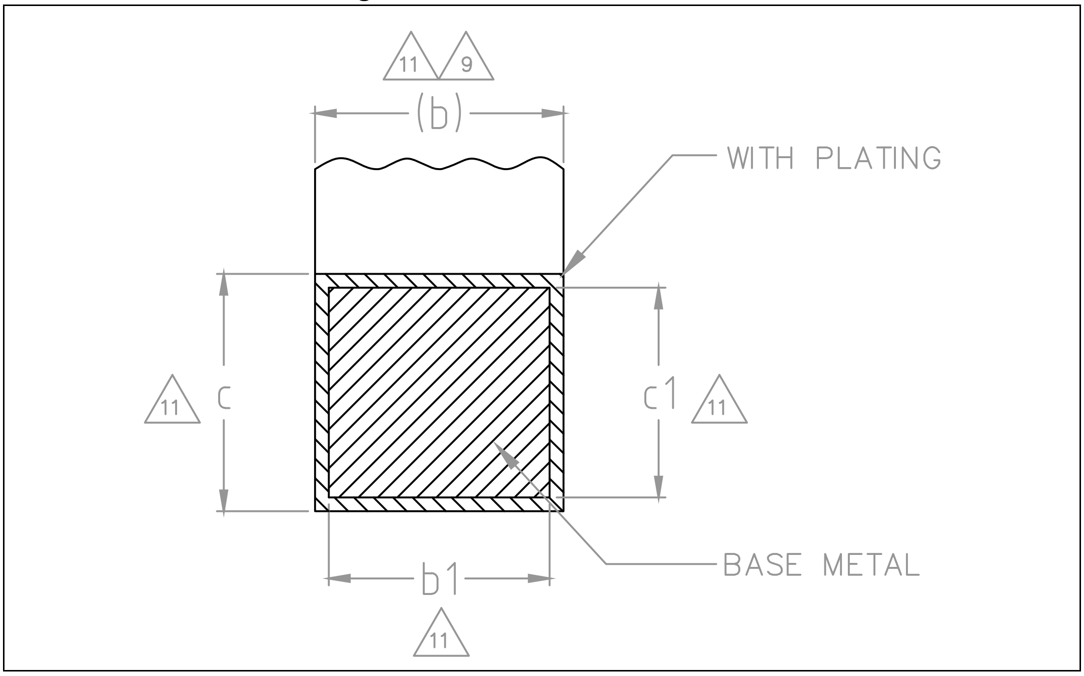


Table 64. eTQFP144 package mechanical data

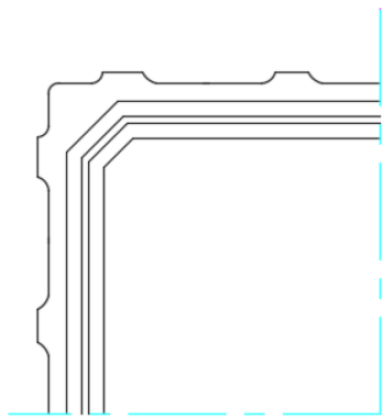
Symbol	Dimensions(7),(17)		
	Min.	Typ.	Max.
θ	0.0°	3.5°	7.0°
θ1	0.0°	—	—
θ2	10.0°	12.0°	14.0°
θ3	10.0°	12.0°	14.0°
A(15)	—	—	1.20
A1(12)	0.05	—	0.15
A2(15)	0.95	1.00	1.05
b(8),(9),(11)	0.17	0.22	0.27
b1(11)	0.17	0.20	0.23
c(11)	0.09	—	0.20
c1(11)	0.09	—	0.16
D(4)	—	22.00 BSC	—
D1(2),(5)	—	20.00 BSC	—
D2(13)	—	—	8.96
D3(14)	7.30	—	—
E(4)	—	22.00 BSC	—
E1(2),(5)	—	20.00 BSC	—
E2(13)	—	—	8.96
E3(14)	7.30	—	—
e	0.50 BSC		
L	0.45	0.60	0.75
L1	—	1.00 REF	—
N(16)	144		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
aaa(1),(18)	0.20		
bbb(1),(18)	0.20		
ccc(1),(18)	0.08		
ddd(1),(18)	0.08		

5.1.1 Package mechanical drawings and data information

The following notes are related to *Figure 43*, *Figure 44*, *Figure 45* and *Table 64*:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeter except where explicitly noted.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad on SPC58EHx, SPC58NHx is as *Figure 46*. End user should verify D2 and E2 dimensions according to the specific device application.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the max number of terminal positions for the specified body size.
17. Critical dimensions:
    a) Stand-Off
    b) Overall Width
    c) Lead Coplanarity
18. For symbols, recommended values and tolerances, see *Table 65*.

Figure 46. eTQFP144 leadframe pad design



Note: number, dimensions and positions of grooves are for reference only.

Table 65. eTQFP144 symbol definitions

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	—
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly know as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by “b”.

5.2 eLQFP176 package information

Refer to *Section 5.2.1: Package mechanical drawings and data information* for full description of below figures and table notes.

Figure 47. eLQFP176 package outline

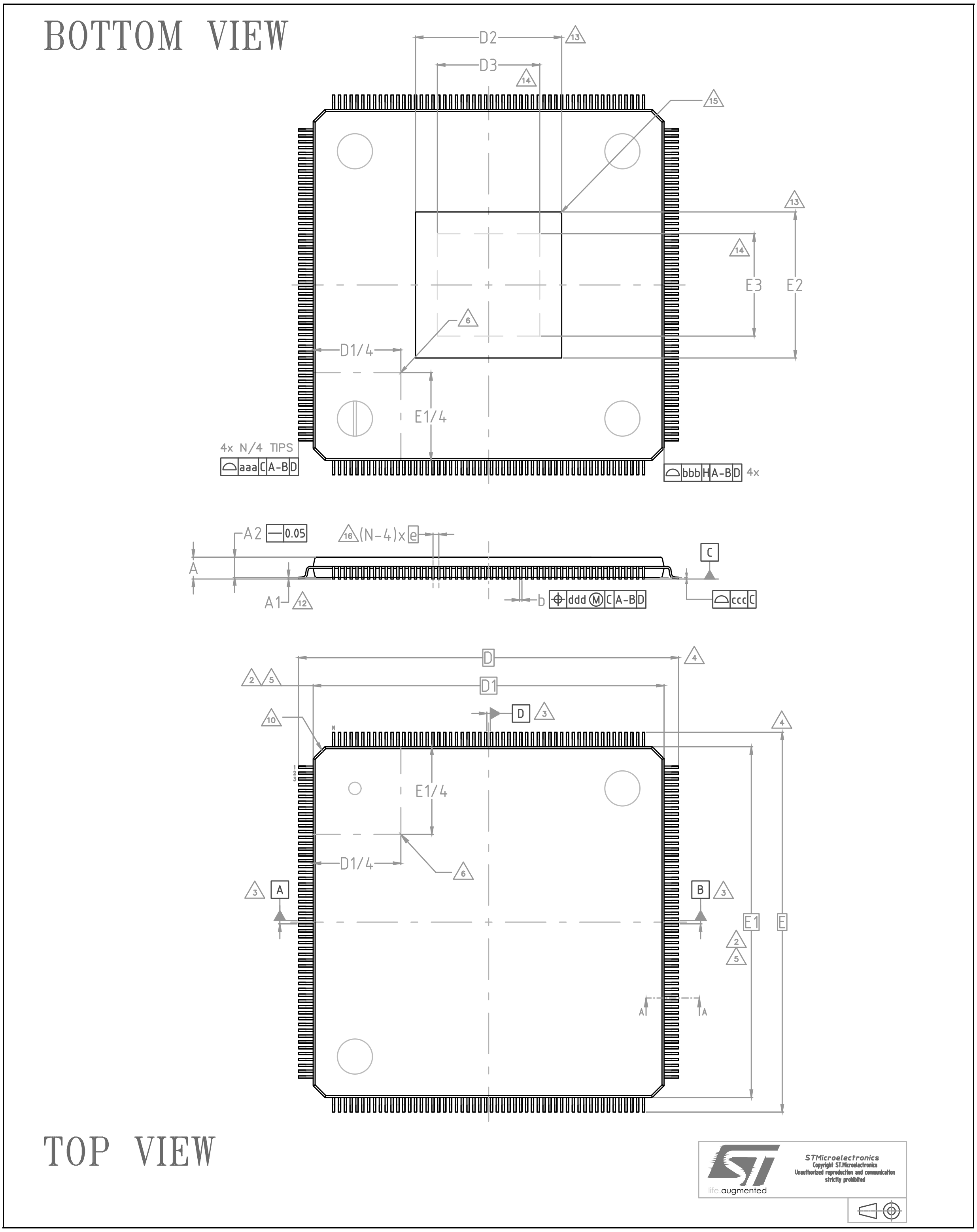


Figure 48. eLQFP176 section A-A

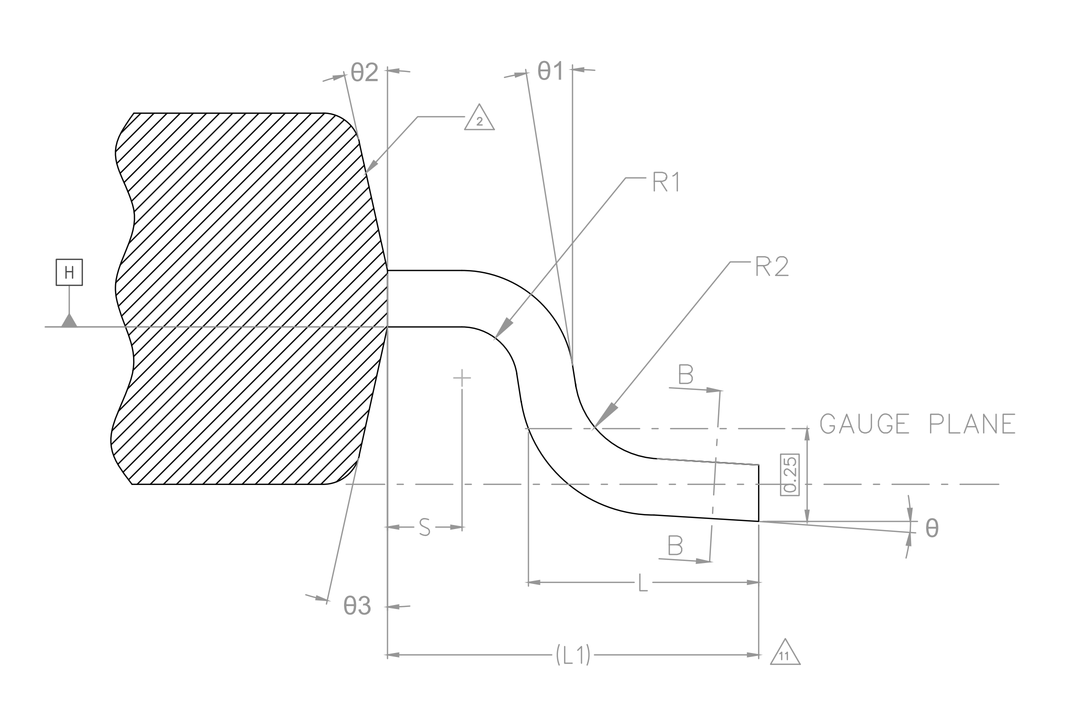


Figure 49. eLQFP176 section B-B

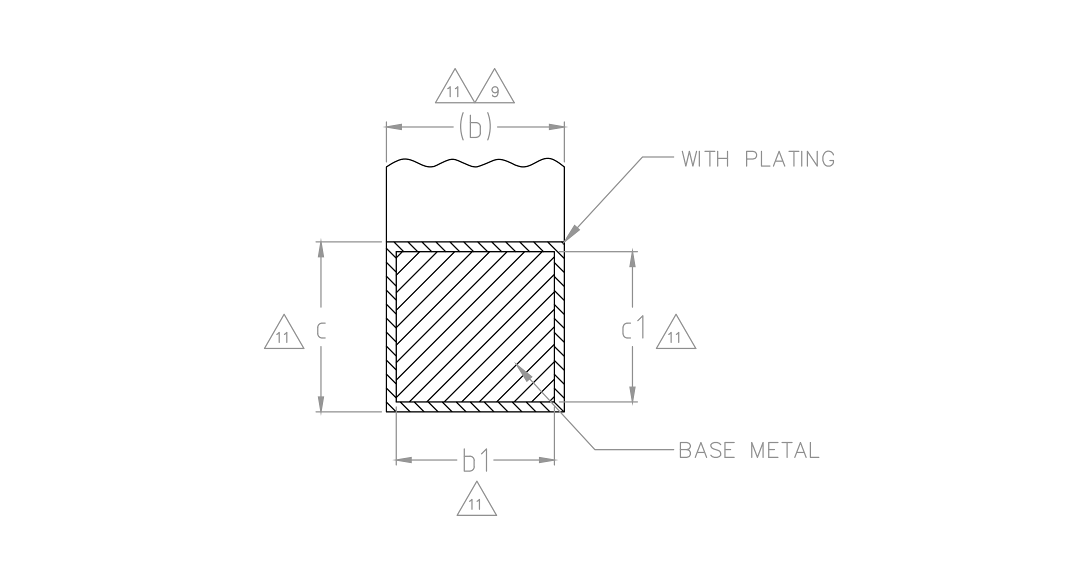


Table 66. eLQFP176 package mechanical data

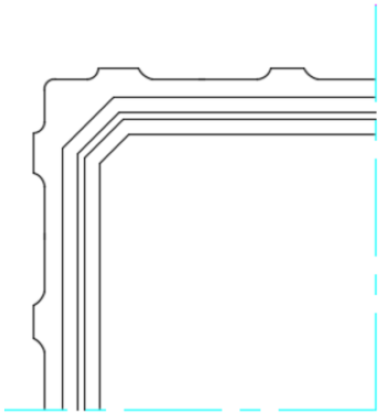
Symbol	Dimensions(7),(17)		
	Min.	Nom.	Max.
Θ	0°	3.5°	7°
Θ1	0°	—	—
Θ2	10°	12°	14°
Θ3	10°	12°	14°
A(15)	—	—	1.60
A1(12)	0.05	—	0.15
A2(15)	1.35	1.40	1.45
b(8),(9),(11)	0.17	0.22	0.27
b1(11)	0.17	0.20	0.23
c(11)	0.09	—	0.20
c1(11)	0.09	—	0.16
D(4)	26.00 BSC		
D1(2),(5)	24.00 BSC		
D2(13)	—	—	8.97
D3(14)	7.30	—	—
e	0.50 BSC		
E(4)	26.00 BSC		
E1(2),(5)	24.00 BSC		
E2(13)	—	—	8.97
E3(14)	7.30	—	—
L	0.45	0.60	0.75
L1	1.00 REF		
N(16)	176		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	
aaa(1),(18)	0.20		
bbb(1),(18)	0.20		
ccc(1),(18)	0.08		
ddd(1),(18)	0.08		

5.2.1 Package mechanical drawings and data information

The following notes are related to *Figure 47*, *Figure 48*, *Figure 49* and *Table 66*:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeter except where explicitly noted.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad on SPC58EHx, SPC58NHx is as *Figure 50*. End user should verify D2 and E2 dimensions according to the specific device application.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the max number of terminal positions for the specified body size.
17. Critical dimensions:
    a) Stand-Off
    b) Overall Width
    c) Lead Coplanarity
18. For symbols, recommended values and tolerances, see *Table 67*.

Figure 50. eLQFP176 leadframe pad design



Note: number, dimensions and positions of grooves are for reference only.

Table 67. eLQFP176 symbol definitions

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	—
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly know as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by “b”.

5.3 FPBGA302 package information

Refer to *Section 5.3.1: Package mechanical drawings and data information* for full description of below figures and table notes.

Figure 51. FPBGA302 package outline

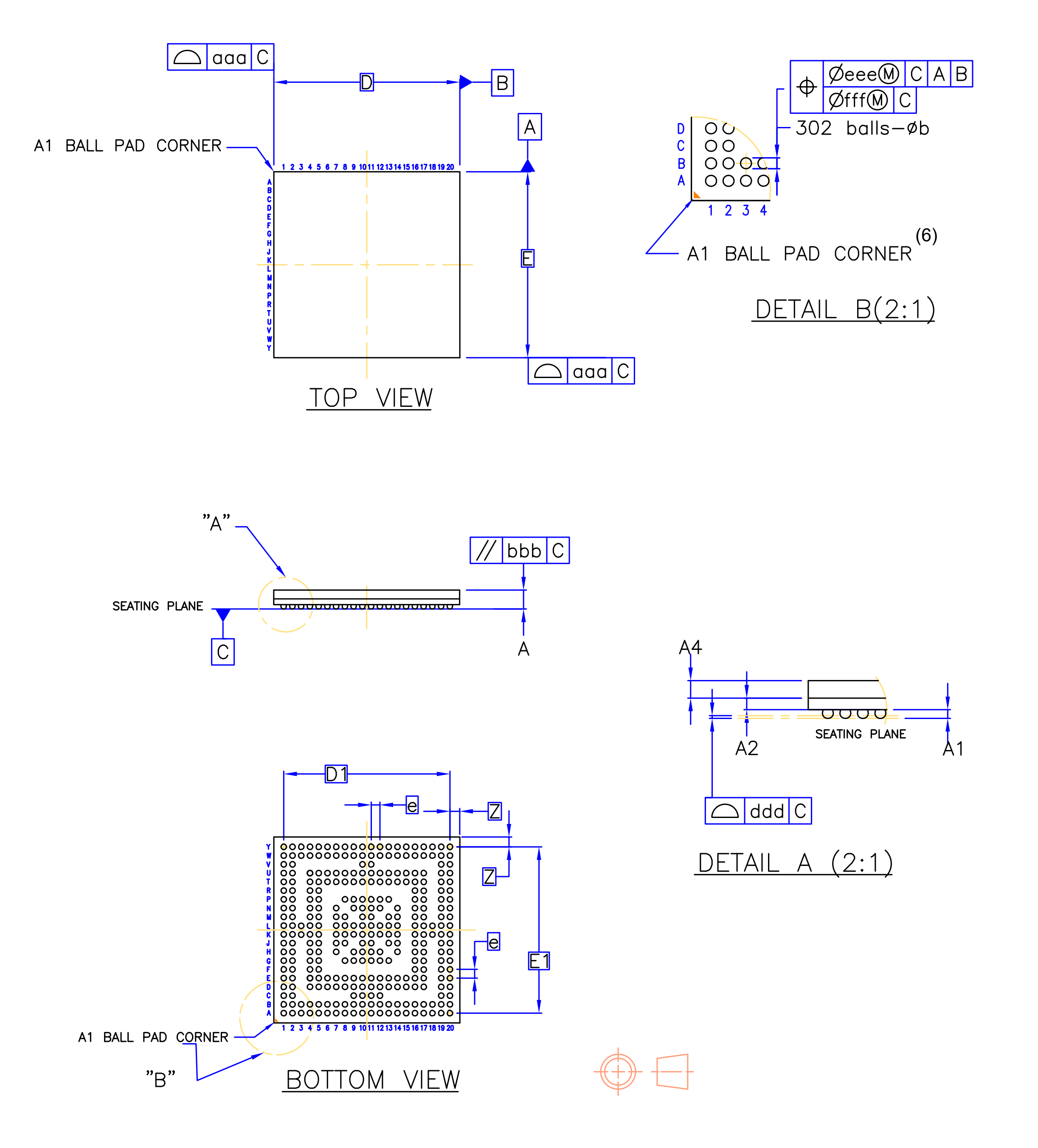


Table 68. FPBGA302 package mechanical data

Symbol	Dimensions (in millimeter)		
	Min.	Typ.	Max.
A(1)	—	—	1.80
A1	0.35	—	—
A2	—	0.50	—
A4	—	—	0.80
D	16.85	17.00	17.15
D1	—	15.20	—
E	16.85	17.00	17.15
E1	—	15.20	—
e	—	0.80	—
b(2)	0.50	0.55	0.60
Z	—	0.90	—
aaa	—	—	0.15
bbb	—	—	0.10
ddd(3)	—	—	0.12
eee(4)	—	—	0.15
fff(5)	—	—	0.08

5.3.1 Package mechanical drawings and data information

The following notes are related to *Figure 51* and *Table 68*:

1. FPBGA stands for Fine Pitch Plastic Ball Grid Array:
   Fine Pitch: e<1 mm pitch
   Low Profile: the total profile height (Dim A) is measured from the seating plane to the top of the component
   The maximum total package height is calculated by the following methodology (tolerance values):

$$\text{Amax} = A_1(\text{TYP}) + A_2(\text{TYP}) + A_4(\text{TYP}) + \sqrt{(A_1)^2 + (A_2)^2 + (A_4)^2}$$

2. The typical ball diameter before mounting is 0.55mm.
3. Ref. JEDEC MO_219G_BGA Low Profile, Fine Pitch Ball Grid Array Family, 0.80MM Pitch (SQ. & RECT.)
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B.
   For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other.
   For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and

located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

6. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heats lug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

5.4 FPBGA386 package information

Refer to *Section 5.4.1: Package mechanical drawings and data information* for full description of below figures and table notes.

Figure 52. FPBGA386 package outline

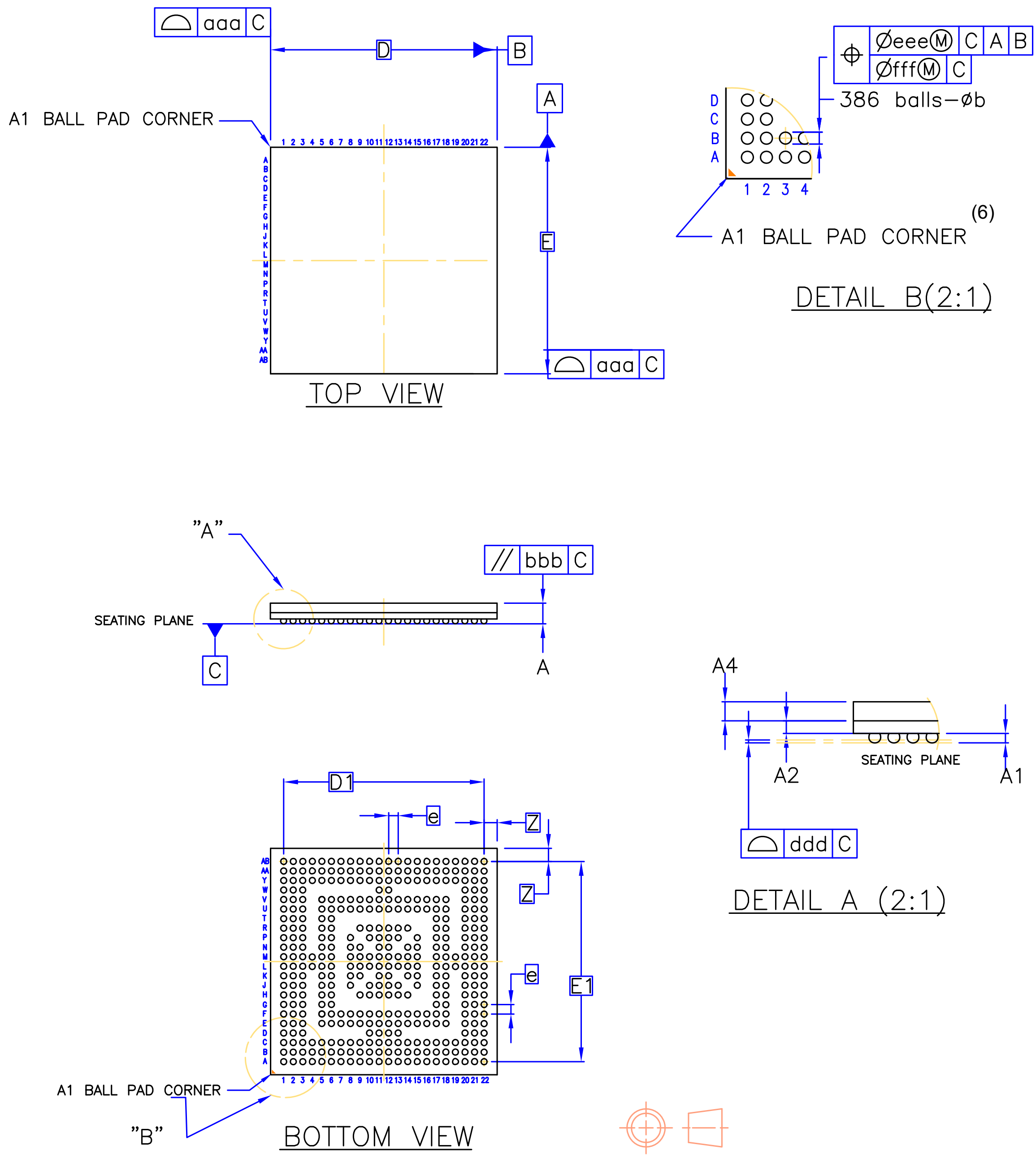


Table 69. FPBGA386 package mechanical data

Symbol	Dimensions (in millimeter)		
	Min.	Typ.	Max.
A(1)	—	—	1.8
A1	0.35	—	—
A2	—	0.50	—
A4	—	—	0.80
D	18.85	19.00	19.15
D1	—	16.80	—
E	18.85	19.00	19.15
E1	—	16.80	—
e	—	0.80	—
b(2)	0.50	0.55	0.60
Z	—	1.10	—
aaa	—	—	0.15
bbb	—	—	0.10
ddd(3)	—	—	0.12
eee(4)	—	—	0.15
fff(5)	—	—	0.08

5.4.1 Package mechanical drawings and data information

The following notes are related to *Figure 52* and *Table 69*:

1. FPBGA stands for Fine Pitch Plastic Ball Grid Array:
   Fine Pitch: e<1 mm pitch
   Low Profile: the total profile height (Dim A) is measured from the seating plane to the top of the component
   The maximum total package height is calculated by the following methodology (tolerance values):

$$Amax = A_1(TYP) + A_2(TYP) + A_4(TYP) + \sqrt{(A_1)^2 + (A_2)^2 + (A_4)^2}$$

2. The typical ball diameter before mounting is 0.55mm.
3. Ref. JEDEC MO_219G_BGA Low Profile, Fine Pitch Ball Grid Array Family, 0.80MM Pitch (SQ. & RECT.).
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B.
   For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other.
   For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and

located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

6. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heats-lug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

5.5 Package thermal characteristics

The following tables describe the thermal characteristics of the device. The parameters in this chapter have been evaluated by considering the device consumption configuration reported in the *Section 4.7: Device consumption*.

5.5.1 eTQFP144

Table 70. Thermal characteristics for 144 exposed pad eTQFP package

Symbol		C	Parameter(1)	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2)	Four layer board (2s2p)	21.3	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board(3)	—	8.1	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top(4)	—	5.4	°C/W
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom(5)	—	1	°C/W
Ψ_{JT}	CC	D	Junction-to-package top(6)	Natural convection	1	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the exposed pad ground on the bottom of the package based on simulation without any interface resistance.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.5.2 LQFP176

Table 71. Thermal characteristics for 176 exposed pad LQFP package

Symbol		C	Parameter(1)	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2)	Four layer board (2s2p)	20.6	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board(3)	—	8.6	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top(4)	—	7.2	°C/W
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom(5)	—	1	°C/W
Ψ_{JT}	CC	D	Junction-to-package top(6)	Natural convection	1	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the exposed pad ground on the bottom of the package based on simulation without any interface resistance.

6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.5.3 FPBGA302

Table 72. Thermal characteristics for 302-pin FPBGA

Symbol		C	Parameter(1)	Conditions	Value(2)	Unit
$Theta_{J-A}$	CC	D	Junction-to-Ambient, Natural Convection(3)	2s2p board	21.2	°C/W
$Theta_{J-B}$	CC	D	Junction-to-board(4)	Ring cold plate 2s2p board	9.6	°C/W
$Theta_{J-C}$	CC	D	Junction-to-case top(5)	Top cold plate 1s board	6.1	°C/W
Ψ_{J-B}	CC	D	Junction-to-board(6)	Operating conditions	9.4	°C/W
Ψ_{J-C}	CC	D	Junction-to-case top	Operating conditions	1	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. These values are preliminary, therefore they are subject to change.
3. Per JEDEC JESD51-6 with the board (JESD51-9) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter

5.5.4 FPBGA386

Table 73. Thermal characteristics for 386-pin FPBGA

Symbol		C	Parameter(1)	Conditions	Value	Unit
$Theta_{J-A}$	CC	D	Junction-to-Ambient, Natural Convection(2)	2s2p board	19.9	°C/W
$Theta_{J-B}$	CC	D	Junction-to-board(3)	Ring cold plate 2s2p board	9.2	°C/W
$Theta_{J-C}$	CC	D	Junction-to-case top(4)	Top cold plate 1s board	5.7	°C/W
Ψ_{J-B}	CC	D	Junction-to-board(5)	Operating conditions	9	°C/W
Ψ_{J-C}	CC	D	Junction-to-case top	Operating conditions	1	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal characterization parameter

5.5.5 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

Equation 1

$$T_J = T_A + (R_{\theta JA} * P_D)$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The differences between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leaves the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

Equation 2

$$T_J = T_B + (R_{\theta JB} * P_D)$$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

Equation 3

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

Equation 4

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

Equation 5

$$T_J = T_B + (\Psi_{JPB} \times P_D)$$

where:

T_T = thermocouple temperature on bottom of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

6 Ordering information

Figure 53. Ordering information scheme

Example code:

SPC58	N	H	92	C3	R	E	H	X	X
Product identifier	*Core*	*Product*	*Memory*	*Package*	*Freq.&T.*	*Custom version*	*Security*	*Silicon revision*	*Packing*

Packing
Y = Tray
X = Tape and Reel (pin 1 top right)

Silicon revision
0 = 1st version
1 = 2nd version

Security
C = HSM medium
E = HSM full
H = HSM medium, ASIL-D
I = HSM full, ASIL-D

Custom version
0 = 16x ISO CAN FD, Flexray, 1x100 Mb Eth
T = 2x100 Mb Eth
G(a) = 1x1 Gb Eth, 1x100 Mb Eth
E = 1x100 Mb Eth, eMMC(b), HyperBus
P = 2x100 Mb Eth, eMMC(b), HyperBus
M(a) = 1x1 Gb Eth, 1x100 Mb Eth, eMMC(b), HyperBus

Freq.&T.
F = 160 MHz at 105 °C
H = 200 MHz at 105 °C
P = 160 MHz at 125 °C
R = 200 MHz at 125 °C

Package
E5 = eTQFP144
E7 = eLQFP176
C3 = FPBGA302
C5 = FPBGA386

Memory
84 = 6 MB
90 = 8 MB
92 = 10 MB

Product
H = SPC58xHx family

Core
N = Triple computing e200z4 core (CPU_2 + CPU_1 + CPU_0)
E = Dual computing e200z4 core (CPU_2 + CPU_0)

Product identifier
SPC58 = Power Architecture in 40 nm

a. Gigabit option is not supported on eTQFP144, up to 2x100Mb is available.

b. eMMC at 4 bit max. is supported on eLQFP176. eMMC is not supported in eTQFP144.

Note: Please contact your ST sales office to ask for the availability of a particular commercial product.

Features (for instance, flash, RAM or peripherals) not included in the commercial product cannot be used.
ST cannot be called to take any liability for features used outside the commercial product.

Table 74. Code Flash Options FOTA (KByte)

SPC58xH92 (10M)	SPC58xH90 (8M)	SPC58xH84 (6M)	Partition		Start address	End address
			RWR	RWW		
16	16	16	0	1	0x00FC0000	0x00FC3FFF
16	16	16	0	1	0x00FC4000	0x00FC7FFF
16	16	16	0	1	0x00FC8000	0x00FCBFFF
16	16	16	0	1	0x00FCC000	0x00FCFFFF
32	32	32	0	1	0x00FD0000	0x00FD7FFF
32	32	32	0	1	0x00FD8000	0x00FDFFFF
64	64	64	0	1	0x00FE0000	0x00FEFFFF
64	64	64	0	1	0x00FF0000	0x00FFFFFF
128	128	128	0	1	0x01000000	0x0101FFFF
128	128	128	0	1	0x01020000	0x0103FFFF
256	256	256	0	1	0x01040000	0x0107FFFF
256	256	256	0	1	0x01080000	0x010BFFFF
256	256	256	0	1	0x010C0000	0x010FFFFF
256	256	256	0	1	0x01100000	0x0113FFFF
256	256	256	0	1	0x01140000	0x0117FFFF
256	256	256	0	1	0x01180000	0x011BFFFF
256	256	256	0	4	0x011C0000	0x011FFFFF
256	256	256	0	4	0x01200000	0x0123FFFF
256	256	256	0	4	0x01240000	0x0127FFFF
256	256	256	0	4	0x01280000	0x012BFFFF
256	256	—	0	4	0x012C0000	0x012FFFFF
256	256	—	0	4	0x01300000	0x0133FFFF
256	—	—	0	4	0x01340000	0x0137FFFF
256	—	—	0	4	0x01380000	0x013BFFFF
256	256	256	1	5	0x013C0000	0x013FFFFF
256	256	256	1	5	0x01400000	0x0143FFFF
256	256	256	1	5	0x01440000	0x0147FFFF
256	256	256	1	5	0x01480000	0x014BFFFF

Table 74. Code Flash Options FOTA (KByte) (continued)

SPC58xH92 (10M)	SPC58xH90 (8M)	SPC58xH84 (6M)	Partition RWR	Partition RWW	Start address	End address
256	256	—	1	5	0x014C0000	0x014FFFFF
256	256	—	1	5	0x01500000	0x0153FFFF
256	—	—	1	5	0x01540000	0x0157FFFF
256	—	—	1	5	0x01580000	0x015BFFFF
256	256	256	0	6	0x015C0000	0x015FFFFF
256	256	256	0	6	0x01600000	0x0163FFFF
256	256	256	0	6	0x01640000	0x0167FFFF
256	256	256	0	6	0x01680000	0x016BFFFF
256	256	—	0	6	0x016C0000	0x016FFFFF
256	256	—	0	6	0x01700000	0x0173FFFF
256	—	—	0	6	0x01740000	0x0177FFFF
256	—	—	0	6	0x01780000	0x017BFFFF
256	256	256	1	7	0x017C0000	0x017FFFFF
256	256	256	1	7	0x01800000	0x0183FFFF
256	256	256	1	7	0x01840000	0x0187FFFF
256	256	256	1	7	0x01880000	0x018BFFFF
256	256	—	1	7	0x018C0000	0x018FFFFF
256	256	—	1	7	0x01900000	0x0193FFFF
256	—	—	1	7	0x01940000	0x0197FFFF
256	—	—	1	7	0x01980000	0x019BFFFF

Table 75. Code Flash Options contiguous (KByte)

SPC58xH92 (10M)	SPC58xH90 (8M)	SPC58xH84 (6M)	Partition RWR	Partition RWW	Start address	End address
16	16	16	0	1	0x00FC0000	0x00FC3FFF
16	16	16	0	1	0x00FC4000	0x00FC7FFF
16	16	16	0	1	0x00FC8000	0x00FCBFFF
16	16	16	0	1	0x00FCC000	0x00FCFFFF
32	32	32	0	1	0x00FD0000	0x00FD7FFF
32	32	32	0	1	0x00FD8000	0x00FDFFFF
64	64	64	0	1	0x00FE0000	0x00FEFFFF

Table 75. Code Flash Options contiguous (KByte) (continued)

SPC58xH92 (10M)	SPC58xH90 (8M)	SPC58xH84 (6M)	Partition		Start address	End address
			RWR	RWW		
64	64	64	0	1	0x00FF0000	0x00FFFFFF
128	128	128	0	1	0x01000000	0x0101FFFF
128	128	128	0	1	0x01020000	0x0103FFFF
256	256	256	0	1	0x01040000	0x0107FFFF
256	256	256	0	1	0x01080000	0x010BFFFF
256	256	256	0	1	0x010C0000	0x010FFFFF
256	256	256	0	1	0x01100000	0x0113FFFF
256	256	256	0	1	0x01140000	0x0117FFFF
256	256	256	0	1	0x01180000	0x011BFFFF
256	256	256	0	4	0x011C0000	0x011FFFFF
256	256	256	0	4	0x01200000	0x0123FFFF
256	256	256	0	4	0x01240000	0x0127FFFF
256	256	256	0	4	0x01280000	0x012BFFFF
256	256	256	0	4	0x012C0000	0x012FFFFF
256	256	256	0	4	0x01300000	0x0133FFFF
256	256	256	0	4	0x01340000	0x0137FFFF
256	256	256	0	4	0x01380000	0x013BFFFF
256	256	256	1	5	0x013C0000	0x013FFFFF
256	256	256	1	5	0x01400000	0x0143FFFF
256	256	256	1	5	0x01440000	0x0147FFFF
256	256	256	1	5	0x01480000	0x014BFFFF
256	256	256	1	5	0x014C0000	0x014FFFFF
256	256	256	1	5	0x01500000	0x0153FFFF
256	256	256	1	5	0x01540000	0x0157FFFF
256	256	256	1	5	0x01580000	0x015BFFFF
256	256	—	0	6	0x015C0000	0x015FFFFF
256	256	—	0	6	0x01600000	0x0163FFFF
256	256	—	0	6	0x01640000	0x0167FFFF
256	256	—	0	6	0x01680000	0x016BFFFF
256	256	—	0	6	0x016C0000	0x016FFFFF
256	256	—	0	6	0x01700000	0x0173FFFF
256	256	—	0	6	0x01740000	0x0177FFFF
256	256	—	0	6	0x01780000	0x017BFFFF

Table 75. Code Flash Options contiguous (KByte) (continued)

SPC58xH92 (10M)	SPC58xH90 (8M)	SPC58xH84 (6M)	Partition		Start address	End address
			RWR	RWW		
256	—	—	1	7	0x017C0000	0x017FFFFF
256	—	—	1	7	0x01800000	0x0183FFFF
256	—	—	1	7	0x01840000	0x0187FFFF
256	—	—	1	7	0x01880000	0x018BFFFF
256	—	—	1	7	0x018C0000	0x018FFFFF
256	—	—	1	7	0x01900000	0x0193FFFF
256	—	—	1	7	0x01940000	0x0197FFFF
256	—	—	1	7	0x01980000	0x019BFFFF

Table 76. RAM Options triple core (KByte)

SPC58NH92 (10M)	SPC58NH90 (8M)	SPC58NH84 (6M)	Type	Start address	End address	Size (Kb)
1280(1)	1024(1)	960(1)				
256	256	256	PRAMC_0	0x40028000	0x40067FFF	256
256	256	256	PRAMC_1	0x40068000	0x400A7FFF	256
8	8	8	PRAMC_2 (STBY)	0x400A8000	0x400A9FFF	8
120	120	120	PRAMC_2 (STBY)	0x400AA000	0x400C7FFF	120
128	128	128	PRAMC_2 (STBY)	0x400C8000	0x400E7FFF	128
64	64	—	PRAMC_3	0x400E8000	0x400F7FFF	64
256	—	—	PRAMC_3	0x400F8000	0x40137FFF	256
0.04	0.04	0.04	HSM emulated registers(2)	0x40137FC0	0x40137FE3	0.04
64	64	64	D-MEM CPU_0	0x50800000	0x5080FFFF	64
64	64	64	D-MEM CPU_1	0x51800000	0x5180FFFF	64
64	64	64	D-MEM CPU_2	0x52800000	0x5280FFFF	64
32	32	32	I-MEM CPU_0	0x50000000	0x50007FFF	32
32	32	32	I-MEM CPU_1	0x51000000	0x51007FFF	32
32	32	32	I-MEM CPU_2	0x52000000	0x52007FFF	32

1. Total RAM size is the sum of TCM and SRAM.
2. Overlayed at the end of PRAMC_3 (if HSM not used, all 256Kbyte of PRAMC_3 can be used in 10M configuration).

Table 77. RAM Options dual core (KByte)

SPC58EH92 (10M)	SPC58EH90 (8M)	SPC58EH84 (6M)	Type	Start address	End address	Size (Kb)
1216(1)	960(1)	896(1)				
256	256	256	PRAMC_0	0x40028000	0x40067FFF	256
256	256	256	PRAMC_1	0x40068000	0x400A7FFF	256
8	8	8	PRAMC_2 (STBY)	0x400A8000	0x400A9FFF	8
120	120	120	PRAMC_2 (STBY)	0x400AA000	0x400C7FFF	120
128	128	128	PRAMC_2 (STBY)	0x400C8000	0x400E7FFF	128
64	64	—	PRAMC_3	0x400E8000	0x400F7FFF	64
256	—	—	PRAMC_3	0x400F8000	0x40137FFF	256
0.04	0.04	0.04	HSM emulated registers(2)	0x40137FC0	0x40137FE3	0.04
64	64	64	D-MEM CPU_0	0x50800000	0x5080FFFF	64
—	—	—	D-MEM CPU_1	0x51800000	0x5180FFFF	64
64	64	64	D-MEM CPU_2	0x52800000	0x5280FFFF	64
32	32	32	I-MEM CPU_0	0x50000000	0x50007FFF	32
—	—	—	I-MEM CPU_1	0x51000000	0x51007FFF	32
32	32	32	I-MEM CPU_2	0x52000000	0x52007FFF	32

1. Total RAM size is the sum of TCM and SRAM.
2. Overlayed at the end of PRAMC_3 (if HSM not used, all 256Kbyte of PRAMC_3 can be used in 10M configuration).

7 Revision history

Table 78. Document revision history

Date	Revision	Changes
14-Nov-2017	1	Initial version.
30-Nov-2017	2	*Section 4.14.1: Power management integration*: added sentence "It is recommended...device itself" for all devices *Table 32: Linear regulator specifications*: updated values for symbol "ΔIDD_{MREG}" – Min: added -200 – Max: added 200 Table 39: SMPS Regulator specifications: symbol "IDD_{SMPS}". changed "C" value from "P" to "T" Figure 16: SMPS Regulator Mode: figure updated and footnote added *Table 37: Wait State configuration* – changed "200" to "180" MHz – added "6 = 200 Mhz" *Table 54: TxEN output characteristics*: added table footnote "Pad configured as VERY STRONG." *Table 55: TxD output characteristics*: changed note 3 to apply to the whole table *Table 57: CAN timing*: added columns for "CC" and "D"
26-Mar-2019	3	Throughout document: Replaced SPC58xEx by SPC58xHx Formatting and editorial changes. The following changes have been made: Removed section "LFAST pad electrical characteristics" *Features*: – Removed bullet "Power supply options selectable via GPIO for BGA packages:". – Replaced "12 MCAN" by "16 MCAN" – Replaced "eMMC rev 4.5.1 module" by "SD/SDIO/eMMC". – Added "with double Chip Select" to OctalSPI module. – Removed USB ULPI. – Replaced "10/100 Mbps/ Gbps" by ",one 10/100Mbps and the other one 10/100Mbps or 1Gbps, – Replaced "10/100 Mbps/ Gbps" by ",one 10/100Mbps and the other one 10/100Mbps or 1Gbps," – Replaced "One I2C module" by "Four I2C module". – Added "Two PSI5 modules" to Communication interfaces bullet. – Changed bullet "Flexible power supply options:" to "Low power supply options:", and removed "Single internal SMPS regulator (FPBGA302 and FPBGA386)" and added "external low voltage supply (1.2V)" to this bullet. – Removed bullet "One I2S module" from Communication interfaces bullet – Replaced bullet "182 KB HSM...(144 KB code + 32 KB data)" by "224 KB HSM...(192 KB code + 32 KB data)" – Removed bullet "One I2S module" from Communication interfaces bullet – Added "1 deserial...low power mode" in Communication interfaces bullet

Table 78. Document revision history (continued)

Date	Revision	Changes
26-Mar-2019	3 (cont'd)	*Chapter 1: Introduction*: *Section 1.3: Device feature summary*: *Table 2: Features list*: – “HyperBus” removed – Changed “Octal SPI” by “Octal SPI w/ HyperBus support” – Other - SMPS deleted. – Other - eMMC changed by SDMMC. – Removed all table notes. – Changed MCAN, I2C, OctalSPI description. – Removed SIPI/LFAST, USB, HyperBus and SMPS features. – Updated row headed User Flash. – Updated row headed Security Flash. – Updated row headed DSPI. – Removed I2S feature. *Section 1.4: Block Diagram*: *Figure 1: Block Diagram*: Updated this figure. *Figure 2: Periphery allocation*: – Added I2C_2 and PLL_DIG_ETH, and removed CCCU and LFAST, on PBRIDGE_2 – Added I2C_1 and I2C_3, and removed SIPI_1 and LFAST_1, on PBRIDGE_1 – Added DSPI_LP, PCM_1, CAN_SUB_3_MESSAGE_RAM, CAN_SUB_3_M_CAN_1, 2, 3, 4 and removed SIPI_0, on PBRIDGE_0 – Added CMU_18_ETH_50M_125M *Section 2.3: Features*: – Flexible Power Supply options: sentence “Single internal SMPS regulator (FPBGA302 and FPBGA386)” removed. – Changed “eMMC 4.51 interface” by “SD3.01/SDIO3.0/MMC4.51” – Eleven DSPI modules, one working even in low power mode. – Sixteen MCAN. – Removed RevMII. – Added Turbo MII ("TMII" , overclocked MII @200Mbps) – Removed Half-duplex operation details. – Removed Standard IEEE 802.3az-2010 and 64-bit data transfer interface. – Removed (64-bit timestamps...). – Removed bullets about VLAN tags. – Changed “Flexible...” to “Fixed address filtering modes:”. – Removed some details of MAC Rx features bullet. – Removed Transaction layer Tx/Rx features bullets. – Removed some details of DMA block features bullet. – Removed some details of Audio and video features bullet. – Removed some Generic queuing features bullet. – Removed USB 2.0 interface.

Table 78. Document revision history (continued)

Date	Revision	Changes
26-Mar-2019	3 (cont'd)	– Added SDMMC feature details. – Added OctalSPI feature details. – Reworked Low power supply options – Updated bullet “182 KB HSM...32 KB data)” to “224 KB HSM...32 KB data)” – Updated “RGMII PHY...on TX clock” in bullet One ethernet controller 10/100/1000 Mbps *Chapter 3: Package pinouts and signal descriptions*: *2.: Pin descriptions*: removed LVDS pins. *Chapter 3: Electrical characteristics* *Section 4.2: Absolute maximum ratings*: *Table 4: Absolute maximum ratings*: Added cross reference to footnote(2) to all V_{DD_HV*} and V_{IN} *Section 4.3: Operating conditions*: *Table 5: Operating conditions*: – changed table footnote on symbol F_{SYS}. – added symbol VRAMP_LV and its descriptions. Removed PRAM wait states configuration table. *Table 6: Device supply relation during power-up/power-down sequence*: added supply VDD_LV to supply1 and supply2 and set their respective descriptions. *Section 4.6: Temperature profile*: Added the second paragraph. *Section 4.7: Device consumption*: *Table 8: Device consumption*: – Updated footnote *4.* – Updated table footnote *5.* “GW use case:...” on $I_{DD\_LV\_GW}$ and $I_{DD\_HV\_GW}$ parameters. – Added table footnote *6.* “IDD_HV_BCM and IDD_HV_GW consumption...vs the validation board used” on $I_{DD\_HV\_GW}$, and $I_{DD\_HV\_BCM}$ parameters. – Updated table footnote *7.* “BCM use case...” on $I_{DD\_LV\_BCM}$ and $I_{DD\_HV\_BCM}$ parameters. – Updated table footnote *10.* “Flash in Low Power. Sysclk at 160 MHz, PLL0_PHI at 160 MHz, XTAL at 40 MHz,...” *Section 4.8: I/O pad specification* Added note “The SPC58EHx, SPC58NHx microcontroller has many GPIOs...to strictly avoid the above situation depicted of electrical contention. *Table 9: I/O pad specification descriptions*: – Changed “the CMOS threshold” by “(VDD_HV_IO_MAIN / 2) +/-20%” at Standby pads type. – Added “SDMMC” and “OctalSPI“ interfaces to Very strong configuration description.

Table 78. Document revision history (continued)

Date	Revision	Changes
26-Mar-2019	3 (cont'd)	– Added sentence “Used for fast interface including Ethernet, SDMMC, OctalSPI and FlexRay interfaces” to Ultra strong configuration description – Removed “Differential configuration” row. – Updated Standby pads description. *Table 14: STRONG/FAST I/O output characteristics*: Updated values for t_{TR_S} for condition CL = 25 pF and CL = 50 pF *Section 3.10: PLLs*: *Table 20: PLL0 electrical characteristics*: – $\lvert\Delta_{PLL0PHI0SPJ}\rvert$: changed “T” by “D” and added pk-pk to Conditions value – $\lvert\Delta_{PLL0PHI1SPJ}\rvert$: added pk-pk to Conditions value – The maximum value of $f_{PLL0PHI0}$ is changed from “400” to “FSYS” with a footnote *Section 4.11: Oscillators*: *Table 22: External 40 MHz oscillator electrical specifications*: – Updated table footnote *1.*: “DCF clients XOSC_LF_EN and XOSC_EN_40MHZ” changed by “XOSC_FREQ_SEL” – Updated table footnote *3.*: This value is determined by the crystal manufacturer and board design, and it can potentially be higher than the maximum provided. *Section 3.12: ADC system*: *Figure 8: Input equivalent circuit (Fast SARn and SARB channels)*: Added parameter “C_{EXT}: external capacitance” and component to scheme. *Table 26: ADC pin specification*: – Added electrical specification for $R_{20K\Omega}$ symbol. – Changed Max value = 1 by 2 for Cp2 SARB channels – Added row for symbol “C_{EXT} / SR”. *Table 27: SARn ADC electrical specification*: – Column “C” splitted and added “D” for I_{ADV_S} – Added row for symbol “TUE_{INJ2} / CC”. *Table 28: ADC-Comparator electrical specification*: – Column “C” splitted and added “D” for I_{ADV_S} – Set min = $5/f_{ADCK}$ µs with footnote “In case the ADC is used as Fast Comparator the sampling time is $t_{ADCSAMPLE} = 2/f_{ADCK}$” – Set min = $6/f_{ADCK}$ for ADC comparator mode, at symbol $t_{ADCSAMPLE}$. – Added row for symbol “TUE_{INJ2} / CC”. – Added “ADC comparator mode” condition to the following two parameters: $I_{ADCREFH}$ Min: - and Max: 19.5 µA and $I_{ADCREFL}$ Min: - and Max: 20.5 µA – Added row for symbol “TUE_{INJ2} / CC”. *Section 4.14: Power management*: – Removed SMPS Regulator Mode figure. – Removed SMPS Regulator specifications table. *Table 30: Power management regulators*: Updated footnote *2.*

Table 78. Document revision history (continued)

Date	Revision	Changes
26-Mar-2019	3 (cont'd)	*Table 31: External components integration*: – Added option "External regulator" – Removed option "Internal SMPS regulator" and relative table footnote. – Added same table footnote to both options "Auxiliary regulator" and "Clamp regulator". *Table 32: Linear regulator specifications*: Removed subsection "SMPS regulator mode" and relative table footnotes. *Table 36: Voltage monitor electrical characteristics*: Changed symbol "$T_{VMFILTER}$" Max. value to 30 µs. *Section 4.15: Flash memory*: *Table 37: Wait State configuration*: – For APC=001 changed the minimum frequency from 40 to 55 MHz and changed the frequency range for RWSC = "4" – For APC=000 and APC=100 changed the frequency range for RWSC = "0", "1", "2", "3" and "4" *Table 38: Flash memory program and erase specifications*: updated this table. *Section 4.16: AC Specifications*: *Section 4.16.1.2: Nexus interface timing*: *Table 41: Nexus debug port timing*: Updated Min Value for # = "9" with Characteristic = "Absolute minimum ... posedge of TCK)" and "Absolute minimum ... negedge of TCK)" *Section 4.16.2: DSPI timing with CMOS pads*: *Table 43: DSPI channel frequency support*: Added DSPI_8 and DSPI_9. *Section 4.16.3: Ethernet port timing*: Updated this section. *Table 53: RMII transmit signal timing*: Changed Symbol R6 Max. value to 15. *Section 4.16.8: PSI5 timing*: added this section. *Section 4.16.9: OctoSPI timing*: added this section. – *Table 62: OctoSPI characteristics in SDR mode*: Updated column headed Conditions for Symbol = "F(QCK)", "t_s(IN)", "t_h(IN)", "t_v(OUT)" and "t_h(OUT)" – Updated *Table 63: OctoSPI characteristics in DTR mode (with DQS)/Octal and Hyperbus* *Section 4.16.10: SDMMC timing*: added this section. *Chapter 4: Package information*: *Figure 44: eTQFP144 package outline*: updated this figure. *Figure 45: eTQFP144 section A-A* and *Figure 46: eTQFP144 section B-B*: added this figures. *Table 64: Package case numbers*: removed Package references column. *Table 65: eTQFP144 package mechanical data*: updated this table. *Section 4.1: eTQFP144 package information*: added notes relative to above figures and table.

Table 78. Document revision history (continued)

Date	Revision	Changes
26-Mar-2019	3 (cont'd)	*Figure 47: eTQFP144 leadframe pad design*: added this figure. *Table 66: eTQFP144 Symbol definitions*: added this table. *Figure 48: eLQFP176 package outline*: updated this figure. *Figure 49: eLQFP176 section A-A* and *Figure 50: eLQFP176 section B-B*: added this figures. *Table 67: eLQFP176 package mechanical data*: updated this table. *Section 4.2: eLQFP176 package information*: added notes relative to above figures and table. *Figure 51: eLQFP176 leadframe pad design*: added this figure. *Table 68: eLQFP176 Symbol definitions*: added this table. *Section 4.3: FPBGA302 package information*: added notes relative to *Figure 52: FPBGA302 package outline* and *Table 69: FPBGA302 package mechanical data*. *Figure 52: FPBGA302 package outline*: updated this figure. *Table 69: FPBGA302 package mechanical data*: updated this table. *Section 4.4: FPBGA386 package information*: added notes relative to *Figure 53: FPBGA386 package outline* and *Table 70: FPBGA386 package mechanical data*. *Figure 53: FPBGA386 package outline*: updated this figure. *Table 70: FPBGA386 package mechanical data*: updated this table. *Section 5.5: Package thermal characteristics*: *Table 70: Thermal characteristics for 144 exposed pad eTQFP package*: – changed $R_{\theta JA}$ and $R_{\theta JB}$ values. – removed Symbol $R_{\theta JMA}$. *Table 71: Thermal characteristics for 176 exposed pad LQFP package*: – changed $R_{\theta JA}$, $R_{\theta JB}$ and $R_{\theta JCto}$ values. – removed Symbol $R_{\theta JMA}$. *Table 72: Thermal characteristics for 302-pin FPBGA*: changed $Theta_{J-A}$, $Theta_{J-B}$, $Theta_{J-C}$ and Ψ_{J-B} values. *Table 73: Thermal characteristics for 386-pin FPBGA*: updated $Theta_{J-A}$, $Theta_{J-B}$, $Theta_{J-C}$, Ψ_{J-B} and Ψ_{J-C} values. *Chapter 6: Ordering information*: *Figure 53: Ordering information scheme*: – Updated Security codification. – Updated to “16x ISO CAN FD” and removed “USB ulpi” from Custom version codification. – Updated value X for Packing R. Removed Code Flash Options and RAM Options tables for the following table: *Table 74: Code Flash Options FOTA (KByte)*: added this table. *Table 75: Code Flash Options contiguous (KByte)*: added this table. *Table 77: RAM Options triple core (KByte)*: added this table. *Table 78: RAM Options dual core (KByte)*: added this table.

Table 78. Document revision history (continued)

Date	Revision	Changes
12-May-2020	4	Throughout document: Formatting and editorial changes. The following changes have been made: Updated the sub-title for Cover page Updated *Chapter 1: Introduction*: removed “Document overview” section title. Updated section 1.2 Description to *Chapter 2: Description* *Chapter 4: Electrical characteristics*: *Section 4.3: Operating conditions*: – *Section Table 5.: Operating conditions*: $V_{DD\_HV\_ADR\_S}$: removed line for C condition. Updated *Section 4.6: Temperature profile* *Section 4.7: Device consumption*: *Table 8: Device consumption*: added Footnote in row-headed $I_{DDSTBY8}$, $I_{DDSTBY128}$ and $I_{DDSTBY256}$. *Section 4.8: I/O pad specification*: *Table 16: ULTRA STRONG/ULTRA FAST I/O output characteristics*: updated Min and Max values for row-headed t_{TR_U} and I_{DCMAX_U} *Section 4.9: Reset pad (PORST) electrical characteristics*: *Figure 5: Startup Reset requirements*: deleted V_{DDMIN} Updated content for *Section 4.10: PLLs*: *Section 4.10.1: PLL0*: *Table 20: PLL0 electrical characteristics*: – Changed condition from T to D for $\|\Delta_{PLL0PHI1SPJ}\|$, $\Delta_{PLL0LTJ}$ and I_{PLL0}. – Updated Max value for $f_{PLL0PHI0}$ symbol and removed the footnote. *Section 4.10.2: PLL1*: *Table 21: PLL1 electrical characteristics*: changed condition from T to D for I_{PLL1} Added *Section 4.10.3: PLL_ETH* *Section 4.11: Oscillators*: *Section 4.11.1: Crystal oscillator 40 MHz*: *Table 22: External 40 MHz oscillator electrical specifications*: updated conditions in row-headed V_{IHEXT} and V_{ILEXT} *Section 4.11.3: RC oscillator 16 MHz*: *Table 24: Internal RC oscillator electrical specifications*: – Updated *1*. – Updated Max value for I_{FIRC}.

Table 78. Document revision history (continued)

Date	Revision	Changes
12-May-2020	4 (cont'd)	*Section 4.14: Power management*: *Section 4.14.1: Power management integration* Added *Figure 9: External regulator mode* *Table 31: External components integration* – Updated Conditions for C_{BV}. – Updated table, notes content and numbering *Section 4.14.3: Voltage monitors* – *Table 36: Voltage monitor electrical characteristics*: added footnote “Even if LVD/HVD...” *Section 4.15: Flash memory*: *Table 38: Flash memory program and erase specifications*: updated this table. *Table 39: Flash memory Life Specification*: updated this table. *Section 4.16: AC Specifications*: *Section 4.16.1.1: JTAG interface timing* Updated footnote *2.* for *Table 40: JTAG pin AC electrical characteristics* *Section 4.16.1.2: Nexus interface timing* *Table 41: Nexus debug port timing*: – Updated Max value on line 15. – Updated footnote *1.* *Section 4.16.3.7: RMII transmit signal timing (TXD[1:0], TX_EN)*: added Note “RMII transmit... as 1ns”. Updated *Section 4.16.9.1: OctoSPI mode* Updated *Table 62: OctoSPI characteristics in SDR mode*: – Updated row-headed F(QCK) symbol to F(CLK) – Updated conditions for row-headed $t_{w(CKH)}$ – Updated Min value for row-headed $t_{h(IN)}$ – Updated Typ and Max value for row-headed $t_{v(OUT)}$ – Updated Min value for row-headed $t_{h(OUT)}$ Removed Table 72: OctoSPI characteristics in DTR mode (with DQS)/Octal and Hyperbus Removed Figure 52: OctoSPI timing diagram - DDR mode Removed Figure 53: OctoSPI Hyperbus clock Updated bullet 4 and 5 in *Section 4.16.9.2: Hyperbus mode* *Chapter 5: Package information*: Added introduction sentence in each Package section. Added sub-section “Package mechanical drawings and data information” and introduction sentence to the notes list. *Table 64: eTQFP144 package mechanical data*: updated table, notes content and numbering. Moved notes to new section *Section 5.1.1: Package mechanical drawings and data information*.

Table 78. Document revision history (continued)

Date	Revision	Changes
12-May-2020	4 (cont'd)	*Table 66: eLQFP176 package mechanical data*: updated table, notes and numbering. Moved notes to new section *Section 5.2.1: Package mechanical drawings and data information*. *Table 68: FPBGA302 package mechanical data*: updated table, notes and numbering. Moved notes to new section *Section 5.3.1: Package mechanical drawings and data information*. *Table 69: FPBGA386 package mechanical data*: updated table, notes and numbering. Moved notes to new section *Section 5.4.1: Package mechanical drawings and data information* *Section 5.5: Package thermal characteristics*: *Section 5.5.3: FPBGA302*: updated package name. *Section 5.5.4: FPBGA386*: updated package name. *Chapter 6: Ordering information*: *Figure 53: Ordering information scheme* – Removed Packing option R. – Set X as example. – Packing option X: Replaced “90°” by “(pin 1 top right)”. – Added footnotes *a.* and *b.* for custom version – Removed Freq.&T. option E = 120 MHz at 105 and N = 120 MHz at 125 Updated *Figure 76: RAM Options triple core (KByte)* Updated *Figure 77: RAM Options dual core (KByte)*
07-Jun-2021	5	Changed document classification from ST Restricted to Public.