

HF/VHF/UHF RF power N-channel MOSFET

Datasheet - production data

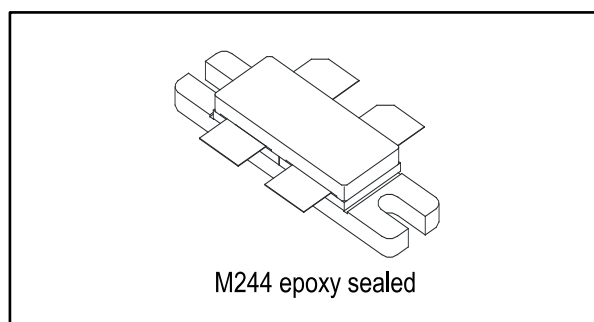
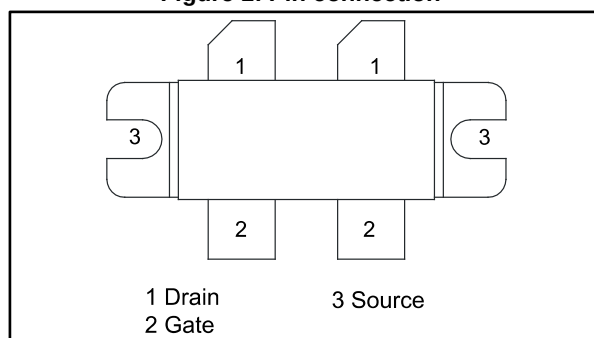


Figure 1: Pin connection



Features

- Gold metallization
- Excellent thermal stability
- Common source push-pull configuration
- $P_{OUT} = 350\text{ W min. with } 15\text{ dB gain @ } 175\text{ MHz}$
- Low $R_{DS(on)}$

Description

The SD2942 is a gold metallized N-channel MOS field-effect RF power transistor. The SD2942 offers 25% lower $R_{DS(ON)}$ than industry standard and 20% higher power saturation than ST SD2932. These characteristics make the SD2942 ideal for 50 V DC very high power applications up to 250 MHz.

Table 1: Device summary

Order code	Marking	Package	Packing
SD2942W	SD2942 ⁽¹⁾	M244	Tube

Notes:

⁽¹⁾For more details please refer to [Section 6: "Marking, packing and shipping specifications"](#).

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1 Electrical data

1.1 Maximum ratings

$T_{\text{CASE}} = 25\text{ °C}$

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{(\text{BR})\text{DSS}}^{(1)}$	Drain source voltage	130	V
V_{DGR}	Drain-gate voltage ($R_{\text{GS}} = 1\text{ M}\Omega$)	130	V
V_{GS}	Gate-source voltage	± 40	V
I_{D}	Drain current	40	A
P_{DISS}	Power dissipation	500	W
T_{J}	Max. operating junction temperature	+200	°C
T_{STG}	Storage temperature	-65 to +150	°C

Notes:

⁽¹⁾ $T_{\text{J}} = 150\text{ °C}$

1.2 Thermal data

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction-to-case thermal resistance	0.35	°C/W

2 Electrical characteristics

$T_{CASE} = 25\text{ }^{\circ}\text{C}$

Table 4: Static

Symbol	Test conditions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}^{(1)}$	$V_{GS} = 0\text{ V}$	$I_{DS} = 100\text{ mA}$	130			V
I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 50\text{ V}$			100	μA
I_{GSS}	$V_{GS} = 20\text{ V}$	$V_{DS} = 0\text{ V}$			250	nA
$V_{GS(Q)}$	$V_{DS} = 10\text{ V}$	$I_D = 250\text{ mA}$	1.5		4	V
$V_{DS(ON)}$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}$			3.0	V
G_{FS}	$V_{DS} = 10\text{ V}$	$I_D = 5\text{ A}$	5			mho
C_{ISS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 50\text{ V}$		415		pF
C_{OSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 50\text{ V}$		236		pF
C_{RSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 50\text{ V}$		17		pF

Notes:

⁽¹⁾ $T_J = 150\text{ }^{\circ}\text{C}$

Table 5: Dynamic

Symbol	Test conditions		Min.	Typ.	Max.	Unit
P_{OUT}	$V_{DD} = 50\text{ V}$	$I_{DQ} = 500\text{ mA}$ $f = 175\text{ MHz}$	350			W
G_{PS}	$V_{DD} = 50\text{ V}$	$I_{DQ} = 500\text{ mA}$ $P_{OUT} = 350\text{ W}$ $f = 175\text{ MHz}$	15	17		dB
η_D	$V_{DD} = 50\text{ V}$	$I_{DQ} = 500\text{ mA}$ $P_{OUT} = 350\text{ W}$ $f = 175\text{ MHz}$	55	61		%
Load mismatch	$V_{DD} = 50\text{ V}$	$I_{DQ} = 500\text{ mA}$ $P_{OUT} = 350\text{ W}$ $f = 175\text{ MHz}$ All phase angles	5:1			VSWR

3 Impedance data

Figure 2: Impedance data

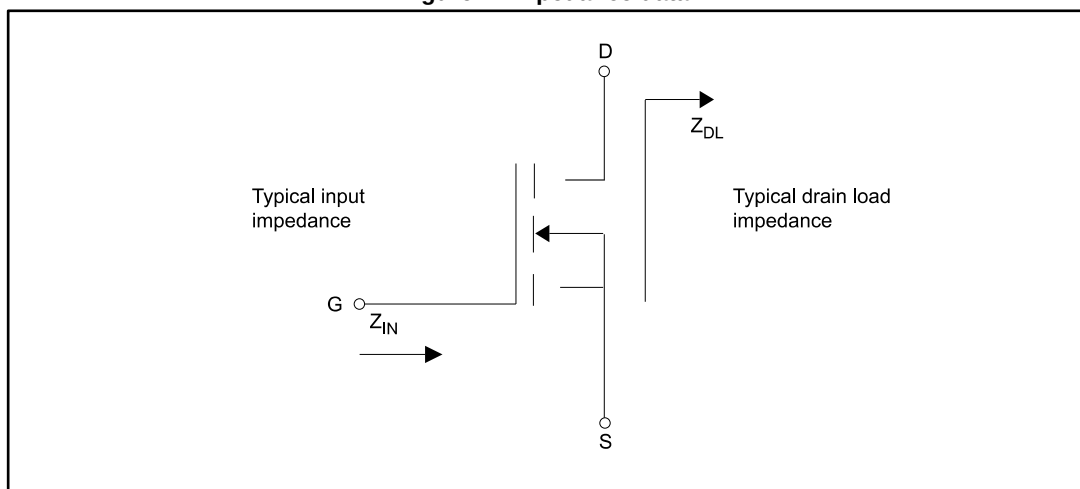


Table 6: Impedance data

f	$Z_{IN}(\Omega)$	$Z_{DL}(\Omega)$
250 MHz	1.3 - j 1.9	1.9 + j 3.2
230 MHz	1.2 - j 1.8	2.1 + j 3.7
200 MHz	1.1 - j 1.6	2.7 + j 4.2
175 MHz	1.0 - j 1.4	3.3 + j 4.8
100 MHz	1.8 - j 2.5	7.5 + j 9
50 MHz	3.2 - j 4.4	10 + j 12

4 Typical performance

Figure 3: Capacitance vs. drain voltage

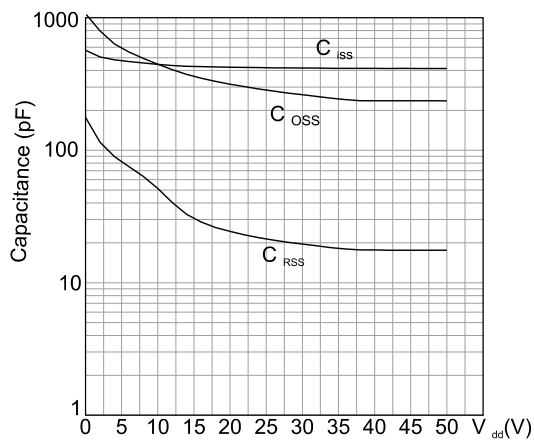


Figure 4: Drain current vs. gate voltage

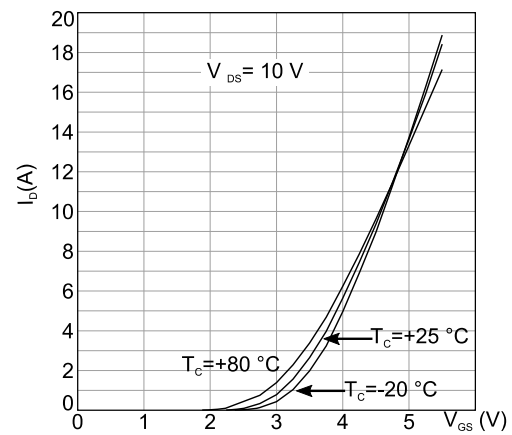


Figure 5: Gate-source voltage vs. case temperature

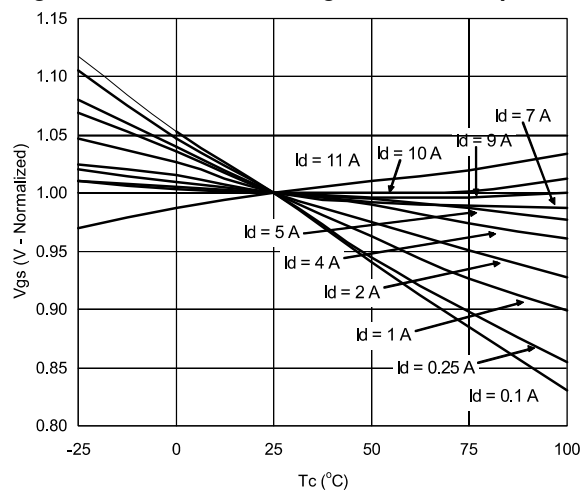


Figure 6: Power gain vs. POUT and case temperature

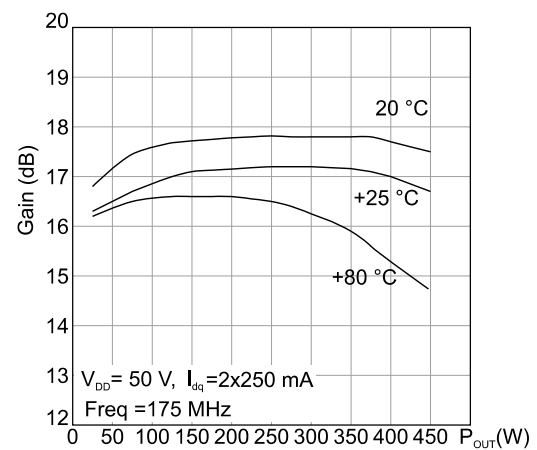


Figure 7: Efficiency vs. case temperature

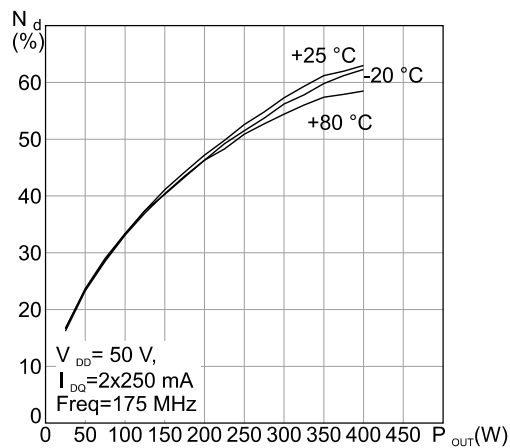
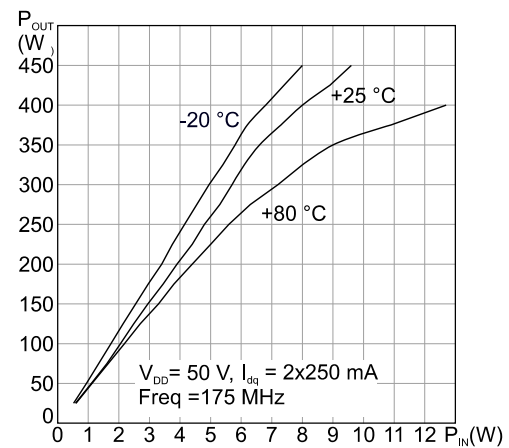
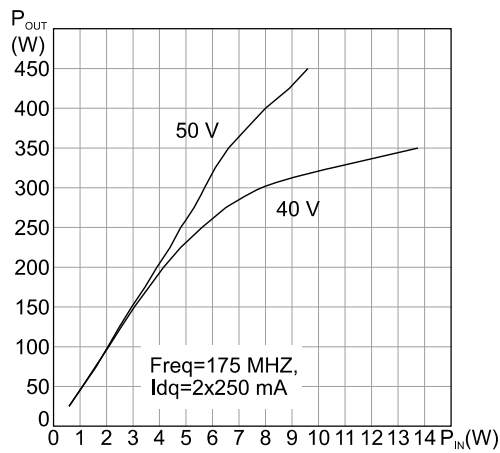
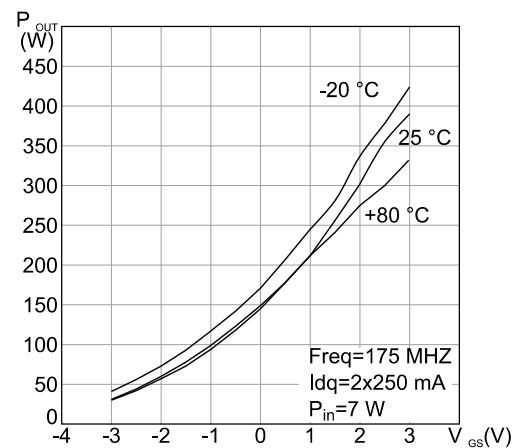
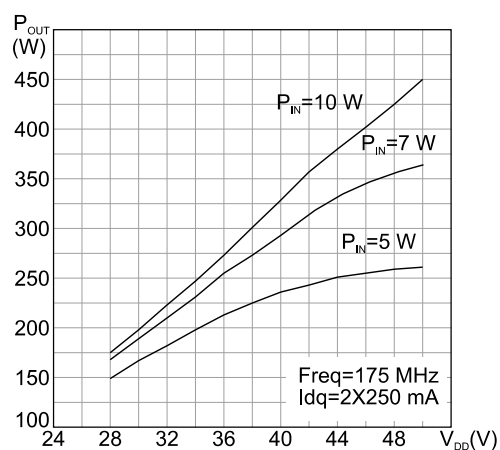
Figure 8: P_{OUT} vs. input power and case temperatureFigure 9: P_{OUT} vs. input power and drain voltageFigure 10: P_{OUT} vs. gate voltage and case temperatureFigure 11: P_{OUT} vs. drain voltage and input power

Figure 12: Maximum thermal resist vs. case temperature

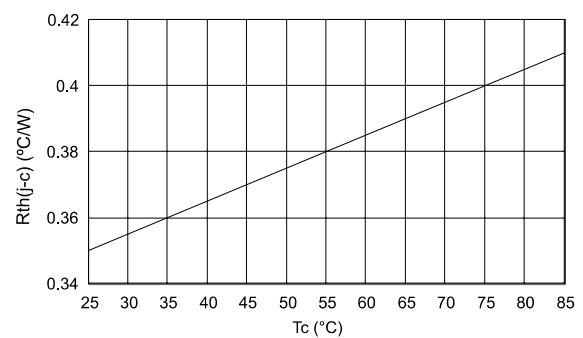


Figure 13: Maximum safe operating area

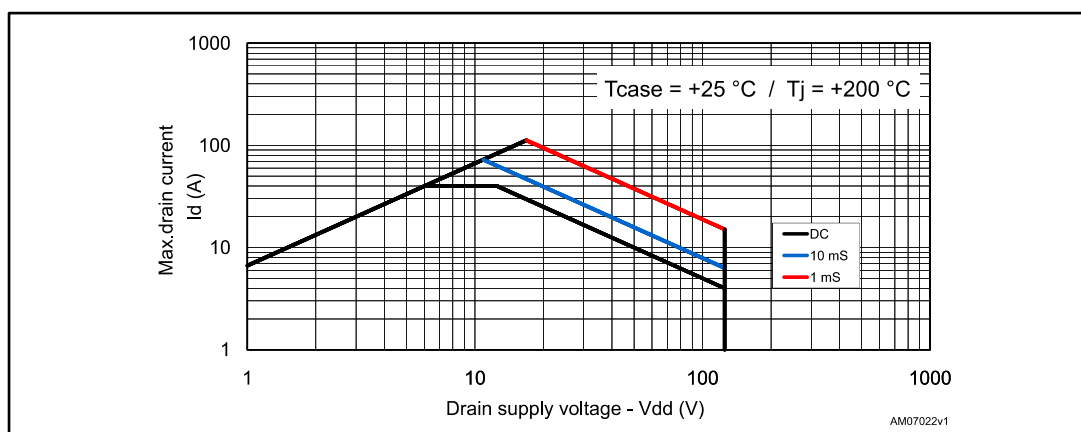


Figure 14: Transient thermal impedance

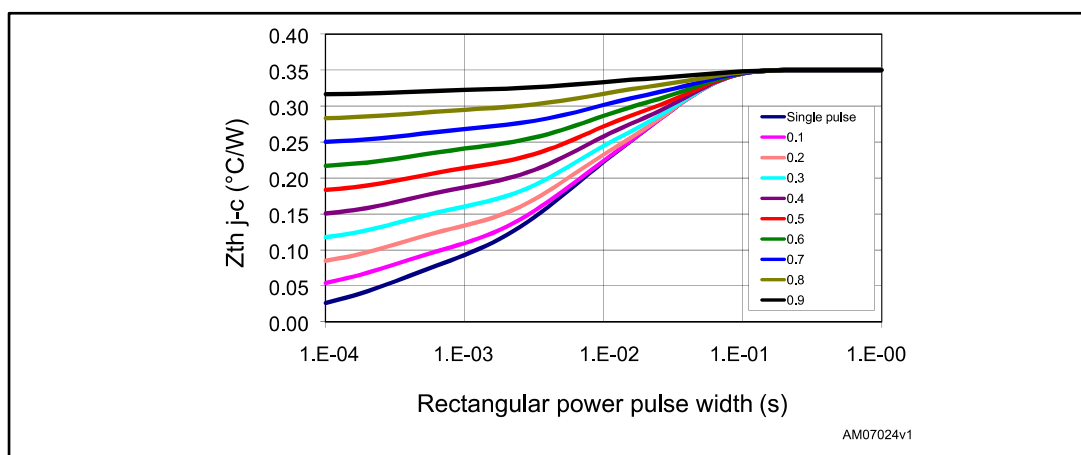
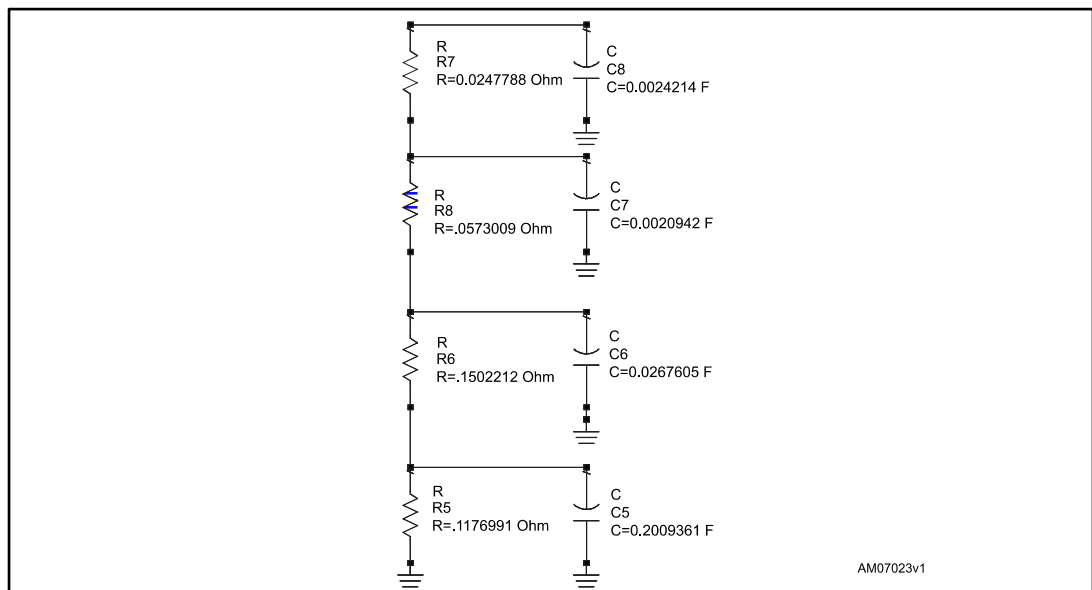
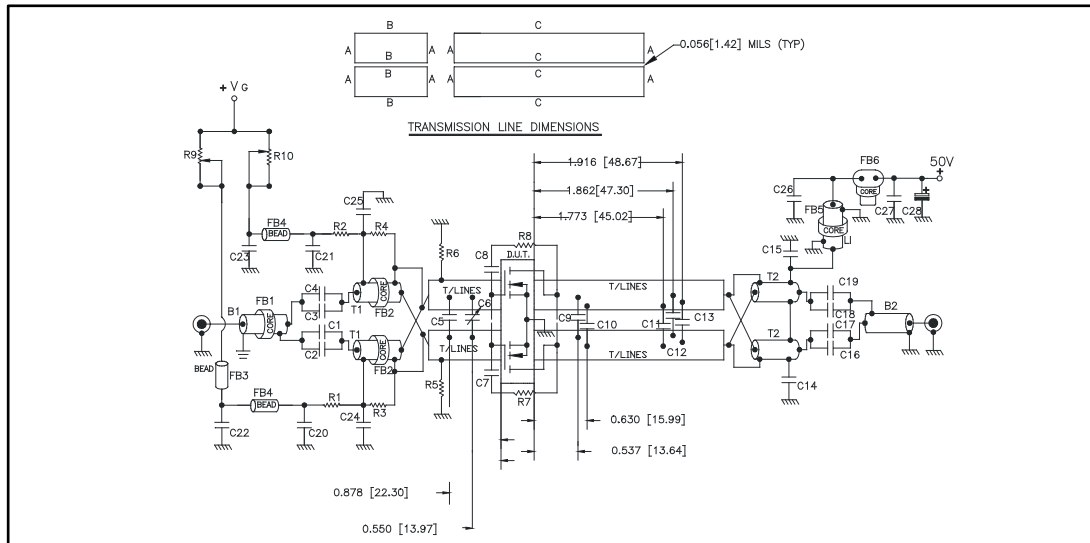


Figure 15: Transient thermal model



5 Test circuit (175 MHz)

Figure 16: 175 MHz production test circuit schematic



Dimensions at component symbols are references for component placement. Gap between ground and transmission lines is + 0.002{0.05} - 0.000{0.00} typ.

Table 7: 175 MHz test circuit part list

Component	Description
R1, R2, R5, R6	470 Ohm 1 W, surface mount chip resistor
R3, R4	360 Ohm 0.5 W, carbon comp. axial lead resistor or equivalent
R7, R8	560 Ohm 2 W, resistor 2 turn wire air-wound axial lead resistor
R9, R10	20 kOhm 3.09 W, 10 turn wirewound precision potentiometer
C1, C4	680 pF ATC 130B surface mount ceramic chip capacitor
C2, C3, C7, C8, C17, C19, C20, C21	10000 pF ATC 200B surface mount ceramic chip capacitor
C5	75 pF ATC 100B surface mount ceramic chip capacitor
C6	ST40 25 pF - 115 pF miniature variable trimmer
C9, C10	47 pF ATC 100B surface mount ceramic chip capacitor
C11, C12, C13	43 pF ATC 100B surface mount ceramic chip capacitor
C14, C15, C24, C25	1200 pF ATC 700B surface mount ceramic chip capacitor
C16, C18	470 pF ATC 700B surface mount ceramic chip capacitor
C22, C23	0.1 μ F / 500 V surface mount ceramic chip capacitor
C26, C27	0.01 μ F / 500 V surface mount ceramic chip capacitor
C28	10 μ F / 63 aluminum electrolytic axial lead capacitor

Component	Description
B1	50 Ohm RG316 O.D 0.076[1.93] L = 11.80[299.72] flexible coaxial cable 4 turns through ferrite bead
B2	50 Ohm RG-142B O.D 0.165[4.19] L = 11.80[299.72] flexible coaxial cable
T1	R.F. transformer 4:1, 25 Ohm O.D RG316-25 O.D 0.080[2.03] L = 5.90[149.86] flexible coaxial cable 2 turns through ferrite multi-aperture core
T2	R.F. transformer 1:4, 25 Ohm semi-rigid coaxial cable O.D. 0.141[3.58] L = 5.90[149.86]
L1	Inductor λ 1/4 wave 50 Ohm O.D 0.165[4.19] L = 11.80 [299.72] flexible coaxial cable 2 turns through ferrite bead
FB1, FB5	Shield bead
FB2, FB6	Multi-aperture core
FB3	Multilayer ferrite chip bead (surface mount)
FB4	Surface mount EMI shield bead
PCB	Woven glass reinforced PTFE microwave laminate 0.06", 1 oz EDCu, both sides, $\epsilon_r = 2.55$

Figure 17: 175 MHz test circuit photomaster

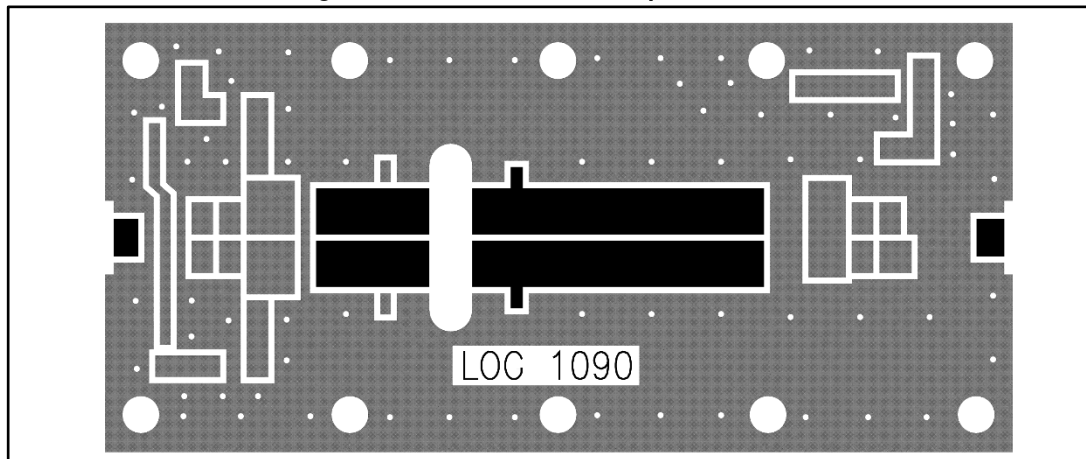
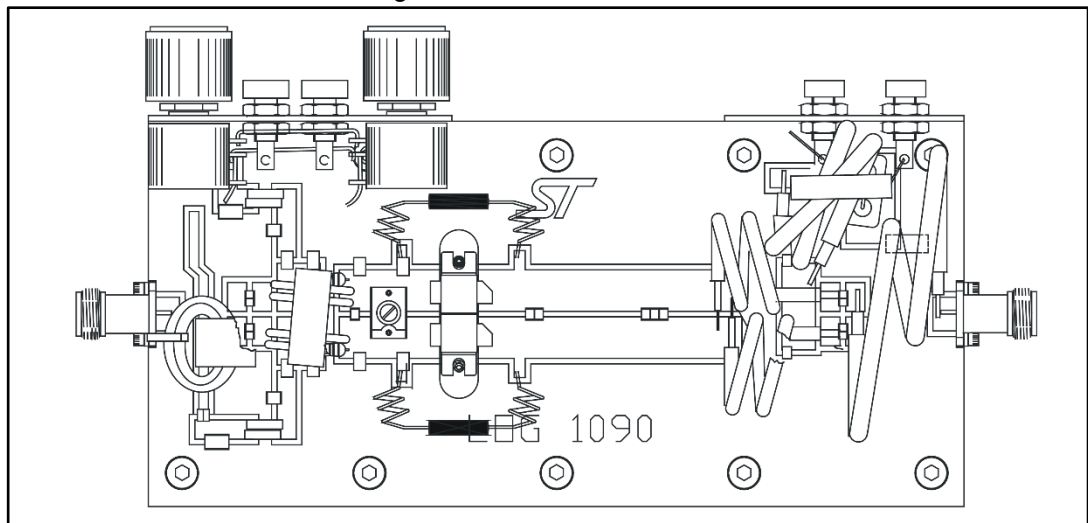


Figure 18: 175 MHz test circuit



6 Marking, packing and shipping specifications

Table 8: Packing and shipping specifications

Order code	Packing	Pieces per tray	Dry pack humidity	Lot code
SD2942W	Tube	15	< 10%	Not mixed

Figure 19: SD2942 marking layout

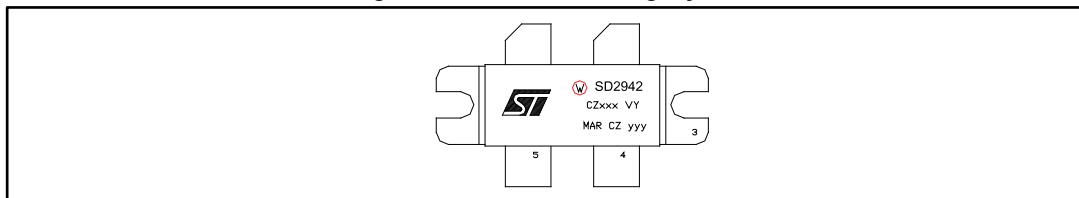


Table 9: Marking specifications

Symbol	Description
W	Wafer process code
CZ	Assembly plant
xxx	Last 3 digits of diffusion lot
VY	Diffusion plant
MAR	Country of origin
CZ	Test and finishing plant
y	Assembly year
yy	Assembly week

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 M244 package information

Figure 20: M244 (0.400 x .860 4L BAL N/HERM W/FLG) package outline

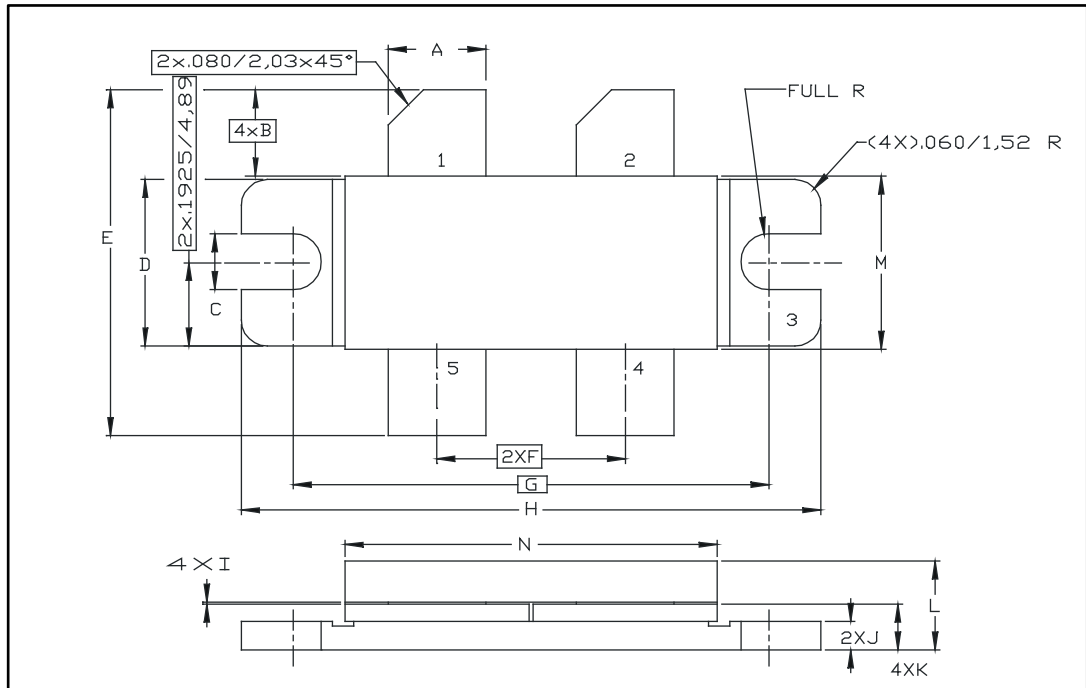


Table 10: M244 (0.400 x .860 4L BAL N/HERM W/FLG) package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.59		5.84
B		5.08	
C	3.02		3.28
D	9.65		9.91
E	19.81		20.82
F	10.92		11.18
G		27.94	
H	33.91		34.16
I	0.10		0.15
J	1.52		1.78
K	2.59		2.84
L	4.83		5.84
M	10.03		10.34
N	21.59		22.10

8 Revision history

Table 11: Document revision history

Date	Revision	Changes
18-Oct-2005	1	First issue.
04-Jan-2006	2	Complete version.
14-Apr-2010	3	Added <i>Figure 13</i> , <i>Figure 14</i> and <i>Figure 15</i> .
25-Oct-2011	4	Inserted <i>Chapter 7: Marking, packing and shipping specifications</i> .
24-Nov-2016	5	Updated Table 2: "Absolute maximum ratings" .

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