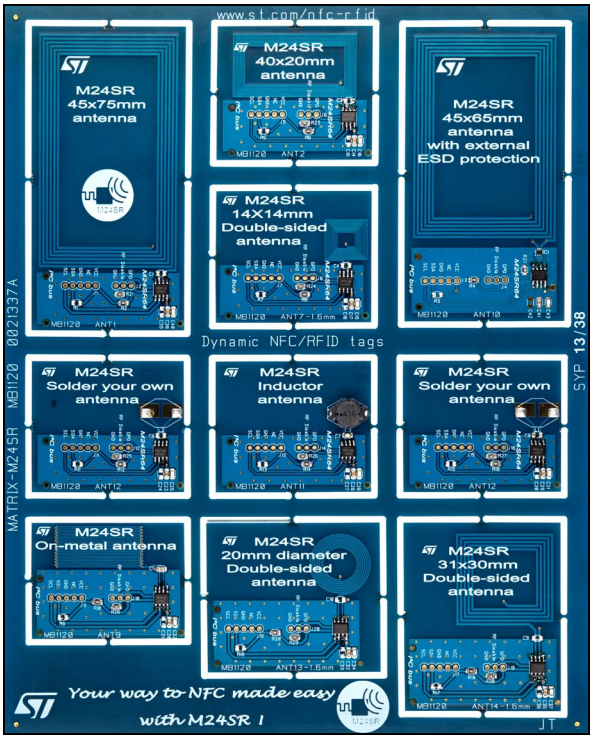
MATRIX-M24SR

Antenna matrix for the M24SRXX-Y Dynamic NFC/RFID tag IC family

Data brief



Features

Ready-to-use printed circuit board including 10 divisible antenna boards. Each of those antenna board can be connected to an MCU thanks to the I^2C interface.

The MATRIX-M24SR antenna boards are based on the M24SR64-Y device which is compatible with NFC phones. As such, any NFC phone can communicate with those antenna boards.

- Various antenna designs
  - 45 mm x 75 mm 13.56 MHz inductive antenna etched on the PCB (ANT1)
  - 20 mm x 40 mm 13.56 MHz inductive antenna etched on the PCB (ANT2)
  - 14 mm x 13.5 mm 13.56 MHz double layer inductive antenna etched on the PCB (ANT7)
  - 45 mm x 65 mm 13.56 MHz inductive antenna etched on the PCB with a DSILC6-4P6 external ESD protection (ANT10)
  - 4.7 µH SMD-inductor based antenna (ANT11)
  - 2 spare circuits for customer antenna development (ANT12)
  - Metal Tag 13 .56 MHz inductive antenna etched on the PCB (ANT9)
  - 20 mm round 13.56 MHz double layer inductive antenna etched on the PCB (ANT13)
  - 31 mm x 30 mm 13.56 MHz double layer inductive antenna etched on the PCB (ANT14)
- M24SR64-Y Dynamic NFC/RFID tag IC
- I^2C bus connection
- RF disable input connection with 30 kΩ pull-down resistor
- GPO (General Purpose Output) output connection with 20 kΩ pull up resistor
- 100 pF and 10 nF capacitors for VCC decoupling

1 Description

The MATRIX-M24SR board features various antenna designs for M24SRXX-Y Dynamic NFC/RFID tag IC family combined on a single ready-to-use divisible PCB.

Each individual antenna features an M24SR64-Y Dynamic NFC/RFID tag IC connected to an RF antenna on one side, and to an I^2C bus on the other side.

All antennas are populated with M24SR64-Y Dynamic NFC/RFID tag IC but are applicable to other densities.

The MATRIX-M24SR antenna matrix allows system designers to evaluate the M24SRXX-Y family performance and capabilities and to get started with their design.

The MATRIX-M24SR gerber files can be downloaded from http://www.st.com.

Figure 1. ANT1, ANT2, ANT7, ANT13 and ANT14 block diagram

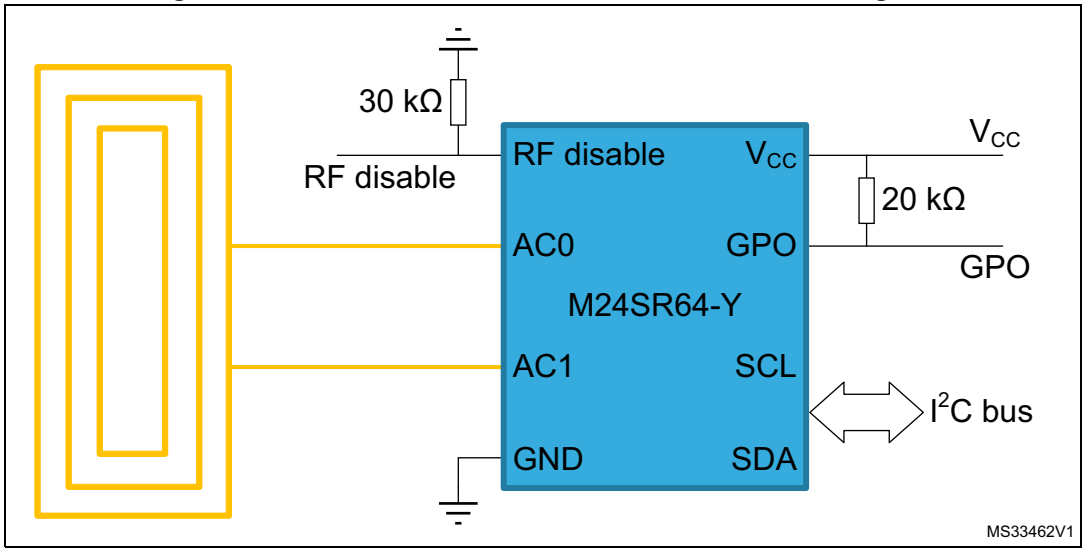
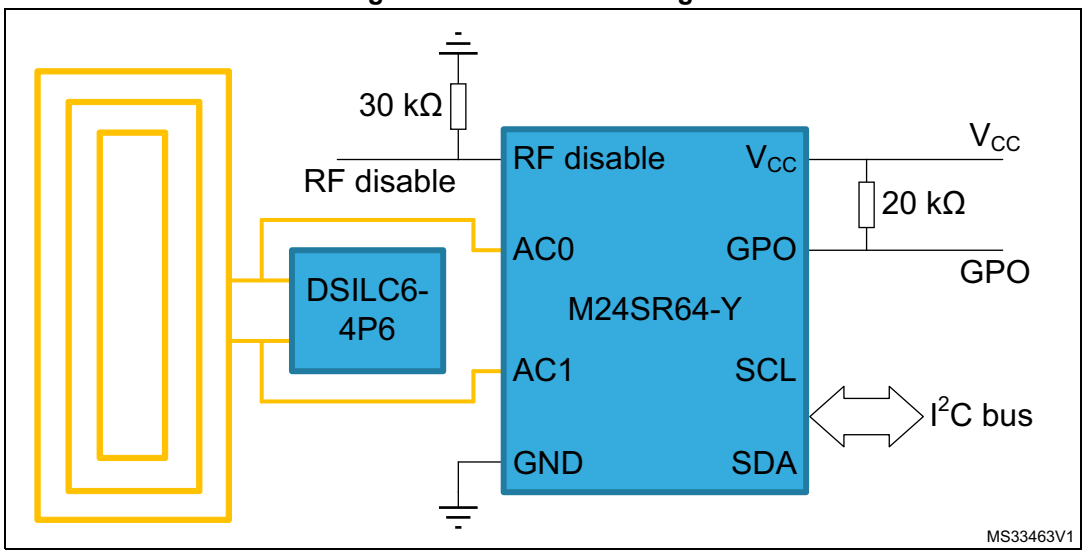


Figure 2. ANT10 block diagram



When associated with the DSILC6-4P6 (V_{BR} = 8.1 V), the M24SR64-Y is compliant with the IEC61000-4-2, level 3 (10 kV).

Figure 3. ANT9 block diagram

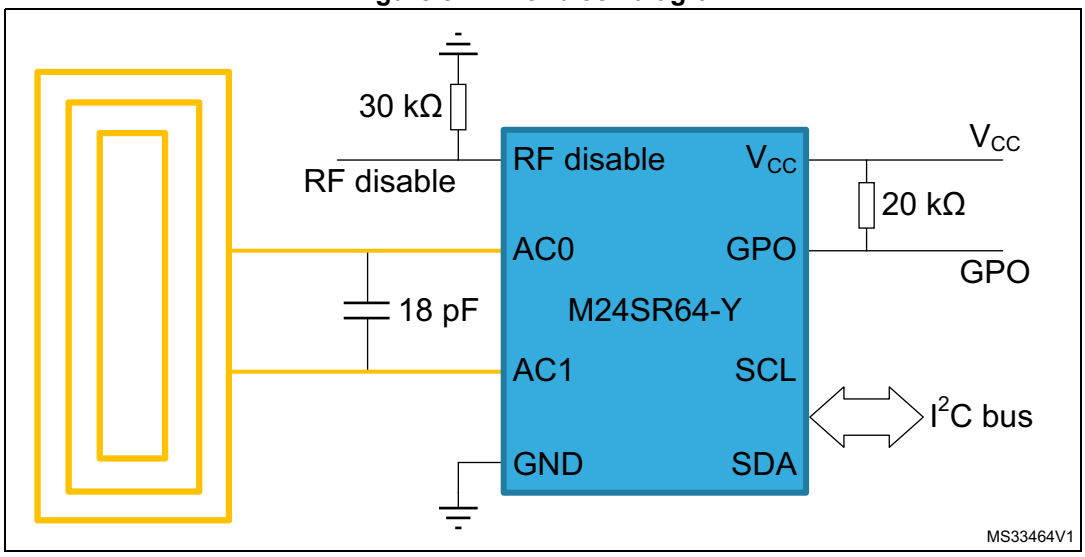


Figure 4. ANT11 block diagram

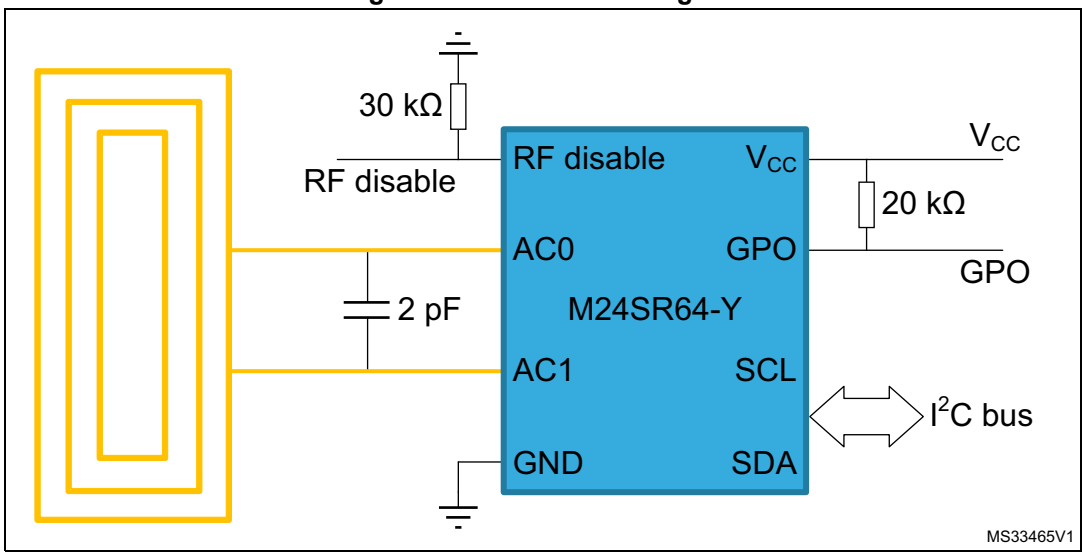
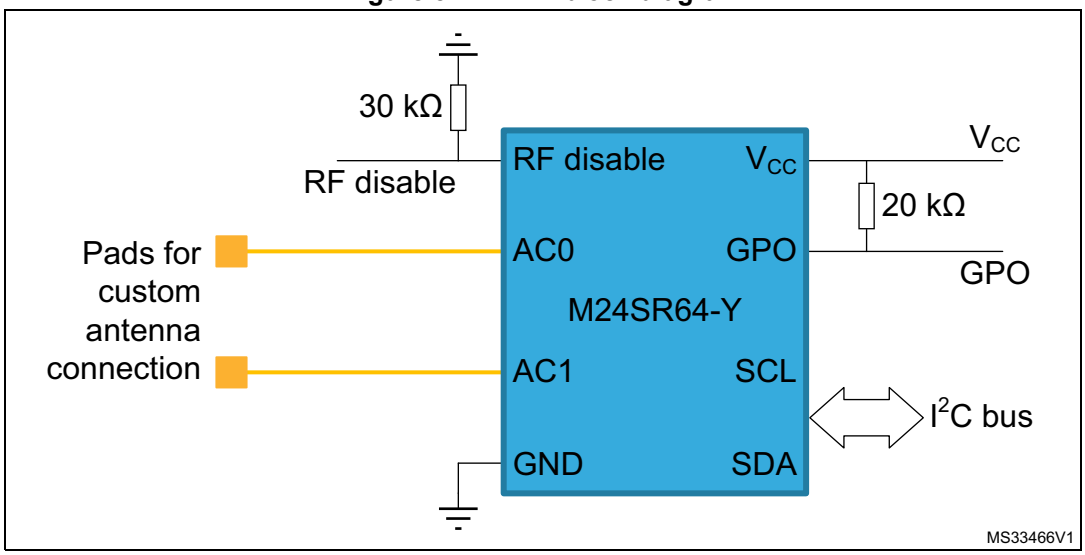


Figure 5. ANT12 block diagram



2 Revision history

Table 1. Document revision history

Date	Revision	Changes
04-Dec-2013	1	Initial release.
20-Dec-2013	2	Revised document classification

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