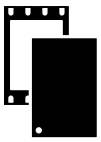
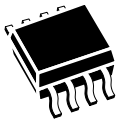
Datasheet

Ultra low-power 32-Mbit serial SPI page EEPROM with dual and quad outputs



UFDFPN8

(4 x 4 mm)



SO8N

(4.9 x 6 mm)

WLCSP8

(2.608 x 1.531 mm)

Product status link
M95P32-I
M95P32-E

Features

SPI interface

- Supports serial peripheral interface (SPI) and dual/quad outputs
- Wide voltage range:
  - V_{CC} from 1.6 to 3.6 V
- Temperature range:
  - Industrial range: -40 °C to +85 °C
  - Extended range: -40 °C to +105 °C
- Fast read:
  - 50 MHz read single output
  - 80 MHz fast read single/dual/quad output with one dummy byte

Memory

- 32 Mbits of page EEPROM
  - 64-Kbyte blocks, 4-Kbyte sectors
  - Page size: 512 bytes
  - Two identification pages
- Write endurance:
  - 500 kcycles on full temperature range
- Data retention:
  - 100 years
  - 10 years after 500 kcycles

Ultra-low power consumption

- 0.6 µA (typ) in deep power-down mode
- 16 µA (typ) in Standby mode
- 800 µA (typ) for read single at 10 MHz
- 1.5 mA (typ) for page write
- Current peak control < 3 mA

High write erase performance

- Fast Write/Prog/Erase times:
  - 2 ms (typ) for byte and page write (includes auto erase and program) for 512 bytes
  - 1.2 ms (typ) for page program (512 bytes)
  - 1.1 ms (typ) for page erase
  - 1.3 ms (typ) for sector erase
  - 4 ms (typ) for block erase
  - 15 ms (typ) for chip erase
- Page program with buffer load

Advanced features

- ECC for high memory reliability (DEC,TED)
- Schmitt trigger inputs for noise filtering
- Output buffer programmable strength
- Operating status flags for ISO26262
- Software reset
- Write protection by block, with top/bottom option
- Unique ID upon request
- Electronic identification
- Support of serial flash memory discoverable parameters (SFDP) mode
- JEDEC standard manufacturer identification

Package

- ECOPACK2 (RoHS compliant) and halogen-free packages:
  - DFN8
  - SO8N
  - WLCSP8

ESD protection:

- HBM (human body model): 2000 V
- CDM: 500 V

1 Description

The M95P32-I and M95P32-E are manufactured with ST's advanced proprietary NVM technology. They offer byte flexibility, page alterability, high page cycling performance, and ultra-low power consumption, equivalent to that of EEPROM technology.

The M95P32-I and M95P32-E are a 32-Mbit SPI page EEPROM device organized as 8192 programmable pages of 512 bytes each, accessed through an SPI bus with high-performance dual- and quad-SPI outputs.

The device offers two additional (identification) pages of 512 bytes:

- The first contains identification data and, upon request, the UID.
- The second can be used to store sensitive application parameters, which can (later) be permanently locked in read-only mode.

Additional status, configuration, and volatile registers set the desired device configuration, while the safety register gives device status information.

The M95P32-I operates with a supply voltage from 1.6 to 3.6 V over an ambient temperature range of -40 °C to +85 °C (+105 °C for the extended range). The M95P32-E offers an extended range of temperature of -40°C to +105 °C. The device supports a clock frequency of up to 80 MHz.

The M95P32-I and M95P32-E offer byte and page write instructions of up to 512 bytes. Write instructions consist of self-timed auto erase and program operations, resulting in flexible data byte management.

The devices also accept page/block/sector/chip erase commands in order to set the memory to an erased state.

The memory can then be fast-programmed by pages of 512 bytes, and further optimized using the "page program with buffer load" to hide the SPI communication latency.

Table 1. Signal names

Pad number	Signal name	Function	Direction
1	$\overline{S}$	Chip select	Input
2	Q-DQ1	Serial data output / Serial data output 1 for dual / quad	Output
3	$\overline{W}$-DQ2	Write protect / Serial data output 2 for quad	Input / Output
4	VSS	Ground	-
5	D-DQ0	Serial data input / Serial data output 0 for dual / quad	Input / Output
6	C	Serial clock	Input
7	$\overline{HOLD}$-DQ3	Hold / Serial data output 3 for quad	Input / Output
8	VCC	Supply voltage	-

Figure 1. 8-pin package connections (top view)

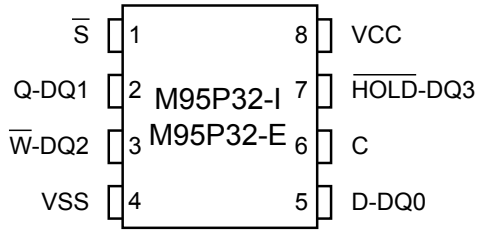
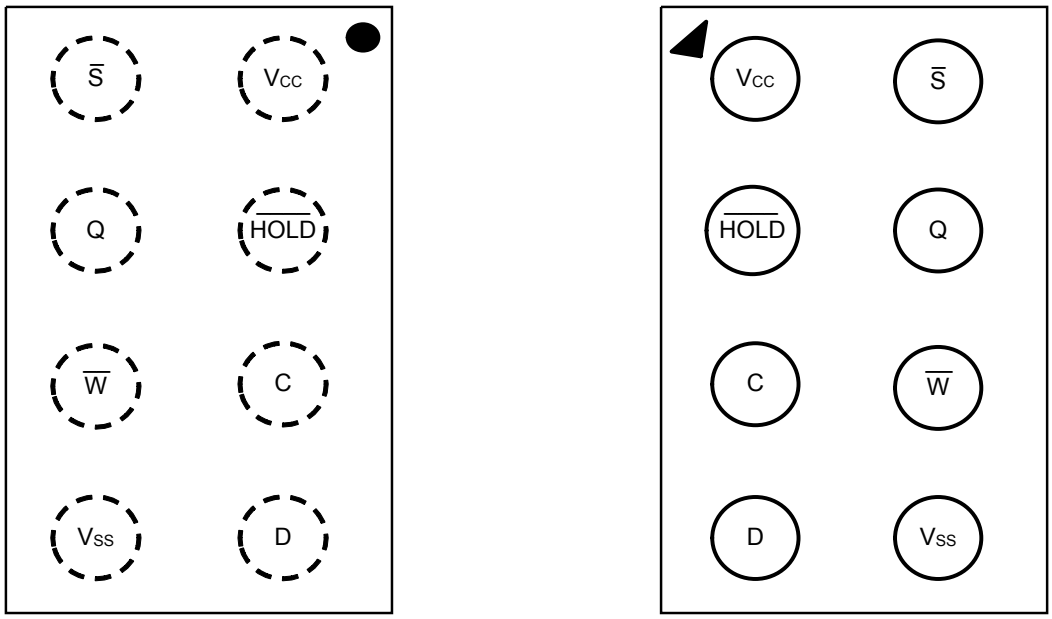


Figure 2. **8-bump ultra thin WLCSP8 connection**



Marking side
(top view)

Bump side
(bottom view)

2 Memory

2.1 Block diagram

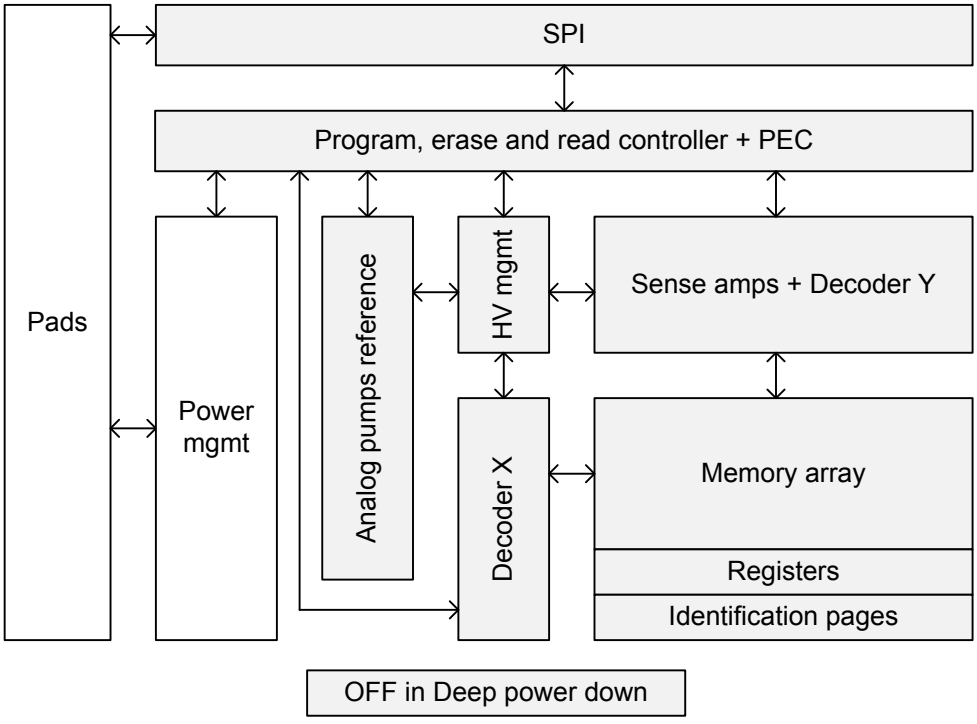
The device contains: the memory array, the registers, the identification pages, the high voltage, and the decoding blocks. (see Figure 3. Block diagram)

The memory array is divided into 8192 erasable pages of 512 bytes.

The PEC (program erase controller) executes all the algorithms managing the correct execution of erase and program operations. It mainly improves the cycling and data retention performance and keeps erase and program times at the typical value during the product operating life.

Deep power down mode is available to place the device (switching OFF the circuitry of several internal blocks) into a minimum power consumption mode. In this configuration, the current consumption is reduced to Icc2 (see Table 23. DC characteristics (M95P32-I; industrial temperature range) and Table 24. DC characteristics (M95P32-E; extended temperature range)).

Figure 3. Block diagram



2.2 Memory map

The memory array is divided into 8192 erasable pages of 512 bytes, and is organized either as 1024 erasable sectors of 4 Kbytes, 64 erasable blocks of 64 Kbytes, or as an entirely erasable array.

The device offers two additional (Identification) pages of 512 bytes. The first contains identification data and, upon request, the UID. The second page can be used to store sensitive application parameters that can (later) be permanently locked in Read-only mode.

In addition, the device embeds a memory protection scheme with block granularity coded in four non-volatile bits of the status register.

The memory array configuration is organized as:

- 4 194 304 bytes
- 64 blocks of 64 Kbytes, or 1024 sectors of 4 Kbytes, or 8192 pages of 512 bytes, hence:
  - each block contains 16 sectors
  - each sector contains 8 pages
  - each page contains 512 bytes

  See the address range in Table 2.

Table 2. **Address range by sector**

64-Kbyte block number	4-Kbyte sector number	Address range	
		Start	End
63	1023	3FF000	3FFFFF
	1022	3FE000	3FEFFF
	1021	3FD000	3FDFFF
	1020	3FC000	3FCFFF
	1019	3FB000	3FBFFF
	1018	3FA000	3FAFFF
	1017	3F9000	3F9FFF
	1016	3F8000	3F8FFF
	1015	3F7000	3F7FFF
	1014	3F6000	3F6FFF
	1013	3F5000	3F5FFF
	1012	3F4000	3F4FFF
	1011	3F3000	3F3FFF
	1010	3F2000	3F2FFF
	1009	3F1000	3F1FFF
	1008	3F0000	3F0FFF
....	....	....	....
0	15	F000	FFFF
	14	E000	EFFF
	13	D000	DFFF
	12	C000	CFFF
	11	B000	BFFF
	10	A000	AFFF
	9	9000	9FFF
	8	8000	8FFF
	7	7000	7FFF
	6	6000	6FFF
	5	5000	5FFF
	4	4000	4FFF
	3	3000	3FFF
	2	2000	2FFF
	1	1000	1FFF
	0	0	FFF

Table 3. **Example of pages inside sector 0**

Sector 0	Page number	Start address	End address
Last page:	page 7	E00	FFF
	page 6	C00	DFF
….	…..	…..	…..
	page 2	400	5FF
	page 1	200	3FF
First page:	page 0	000	1FF

3 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range $V_{CC(min)}$ to $V_{CC(max)}$.

All the input and output signals described in the following sections must be held high or low, or transit between levels, according to the V_{IH}, V_{OH}, V_{IL} or V_{OL} voltages specified in Table 25. DC characteristics - other parameters.

3.1 Serial data output (Q-DQ1)

This output is a push-pull buffer. The signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock (C).

With the dual-output and quad-output read commands, this pin remains an output (DQ1) in conjunction with other pins, to allow four bits of data on DQn pins to be clocked out on every falling edge of SCK.

To maintain consistency with the SPI nomenclature, the data output Q (DQ1) pin is referred to as the MISO pin, unless specifically addressing the dual output and quad output modes (in which case it is referred to as DQ1).

The serial output pin is in a high impedance state (high-Z) whenever the device is deselected ($\overline{S}$ is de-asserted).

3.2 Serial data input (D-DQ0)

D is a CMOS input with no internal pull-up/down and an output push-pull buffer. The signal transfers data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of the serial clock (C).

With the dual-output and quad-output read commands, this pin becomes a push/pull output buffer (DQ0) in conjunction with other pins to allow four bits of data on DQn pins to be clocked out on every falling edge of SCK.

To maintain consistency with the SPI nomenclature, the data input D (DQ0) pin is referred to as MOSI.

The D pin is in high-Z whenever the device is deselected ($\overline{S}$ is de-asserted).

3.3 Serial clock (C)

This is a CMOS input with no internal pull up/down. This signal synchronizes the timing of the serial interface. The instructions, the addresses, or the data present on the serial data input (D) are latched on the rising edge of the serial clock (C), while the output data on the DQn pins is changed after the falling edge of the serial clock (C).

3.4 Chip select ($\overline{S}$)

This is a CMOS input with no internal pull up/down. When this signal is high, the device is deselected and serial data outputs are in high impedance. The device is in Standby power mode (not deep power-down mode) unless an internal write cycle is in progress.

Driving chip select ($\overline{S}$) low selects the device, placing it in active power mode.

After power-up, a falling edge on chip select ($\overline{S}$) is required prior to the start of any instruction. A low to high transition is required to end an operation.

An external pull-up on $\overline{S}$ is required so that at power-up the voltage on $\overline{S}$ follows the power supply voltage on V_{CC}.

3.5 Hold ($\overline{HOLD}$-DQ3)

The hold pin is a CMOS input with no internal pull-up/down, and a push-pull output buffer. This signal is used to pause all serial communications with the device without deselecting it.

During the hold condition, the serial data output (Q) is high-Z, and the serial data input (D) and serial clock (C) are don't care.

To start the hold condition, the device must be selected by driving chip select ($\overline{S}$) low.

When the device is selected with $\overline{HOLD}$ low and C high, it switches into the hold condition when C transits low. The hold pin supports dual and quad output reads- (see Section 6.11 Fast read dual output with one dummy byte (3Bh) and Section 6.12 Fast read quad output with one dummy byte (6Bh).

With the fast read quad output command, the $\overline{HOLD}$ function is no longer available after the last bit of the third address bytes of the command, and the $\overline{HOLD}$ pin becomes an output pin (DQ3). In conjunction with other pins, this allows four-bit data to be clocked into DQ3 on every falling edge of SCK.

To maintain consistency with the SPI nomenclature, this pin is referred to as the $\overline{HOLD}$ pin, unless specifically addressing the quad output mode, in which case it is referred to as DQ3.

3.6 Write protect ($\overline{W}$-DQ2)

The write protect pin is a CMOS input with no internal pull-up/down, and an output push-pull buffer. The main purpose of this signal is to freeze the size of the area of memory protected against Write instructions (as specified by the values in the BPn and TB bits of the Status register).

This pin must be driven either high or low, and must be stable during all Write instructions. This pin supports fast read dual and fast read quad output commands. See Section 4.3 Dual output read and Section 4.4 Quad output read.

With the fast read quad output command, the Write protect pin ($\overline{W}$-DQ2) becomes an output pin, after the last bit of the third address bytes of the command. In conjunction with other pins, this allows four bits of data on DQ2 to be clocked-in on every falling edge of SCK.

To maintain consistency with the SPI nomenclature, the Write protect pin is referred to as the $\overline{W}$ pin unless specifically addressing the Quad output mode, in which case it is referred to as DQ2.

3.7 VCC (V_{CC}, supply voltage)

V_{CC} is the device core power supply.

3.8 VSS (V_{SS}, ground)

V_{SS} is the reference for all signals, including the V_{CC} supply voltage.

4 Device operation

4.1 Connecting to the SPI bus

All instructions, addresses, and input data bytes are shifted in to the device, the most significant bit first. The serial data input (D) is sampled on the first rising edge of the serial clock (C) after chip select ($\overline{S}$) goes low.

All output data bytes are shifted out of the device, the most significant bit first. The serial data output (on DQn pins) is output on the first falling edge of the serial clock (C) after eight instruction bits (such as the read from memory array and read status register instructions) have been clocked into the device.

The write protect ($\overline{W}$) and hold ($\overline{HOLD}$) signals must be driven high or low as appropriate.

Figure 4. Bus master and memory devices on the SPI bus

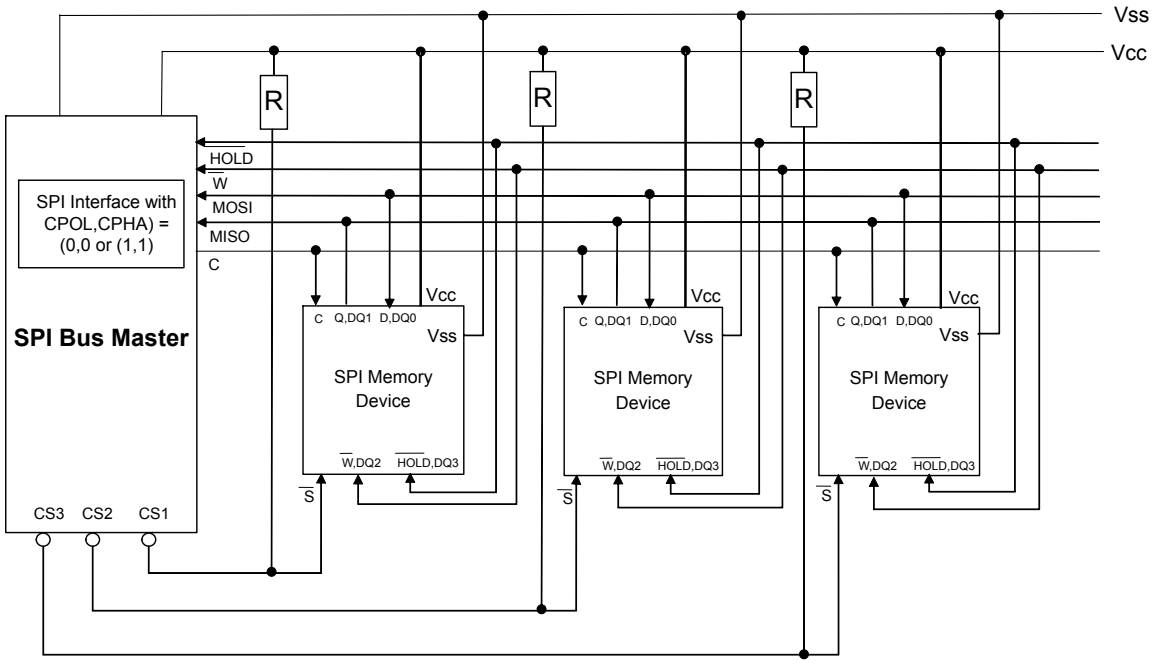


Figure 4 shows an example of three memory devices connected to an SPI bus master. Only one memory device is selected at a time, so only one memory drives the serial data output (Q) line at a time. The other memory devices are high impedance.

The pull-up resistor R (whose typical value is 100 kΩ) ensures that a device is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state.

4.2 SPI modes

This device can be driven by a microcontroller through its SPI peripheral running in either of the following two modes:

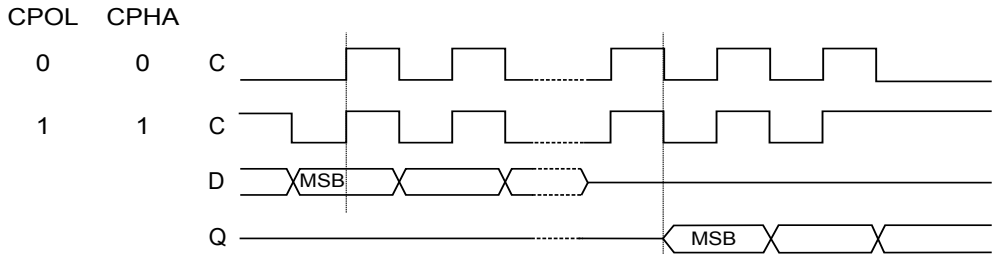
- CPOL = 0, CPHA = 0
- CPOL = 1, CPHA = 1

In these modes, input data is latched on the rising edge of the serial clock (C), and data is output on the falling edge of the serial clock (C).

The difference between these two modes, as shown in Figure 5, is the polarity of the clock state when the bus master is in standby mode and not transferring data:

- C remains at 0 for (CPOL = 0, CPHA = 0)
- C remains at 1 for (CPOL = 1, CPHA = 1)

Figure 5. SPI modes supported



Because at a given instant only one device is selected, only one device drives the serial data output (Q-DQn) at a time. The other devices are in a high impedance state (high-Z). An example of three devices connected to an MCU through an SPI bus is shown in Figure 4. Bus master and memory devices on the SPI bus.

4.3 Dual output read

The M95P32-I and M95P32-E feature a dual output read mode that allows two bits of data to be clocked out of the device on every clock cycle to improve throughput. With the fast read dual output command, the D pin becomes an output (D-DQ0) along with the Q-DQ1 pin.

4.4 Quad output read

The M95P32-I and M95P32-E feature a quad output read mode that allows four bits of data to be clocked out of the device on every clock cycle to improve throughput. With the fast read quad output command, the D, $\overline{W}$, and $\overline{HOLD}$ pins become outputs (D-DQ0, $\overline{W}$-DQ2, $\overline{HOLD}$-DQ3), along with the Q-DQ1 pin.

4.5 Supply voltage

Prior to selecting the memory and issuing instructions to it, a valid and stable supply voltage within the specified $V_{CC(min)}$ to $V_{CC(max)}$ range must be applied (see Table 18. Operating conditions). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a modify instruction, until the completion of the internal write cycle (See Table 26. Programming times).

To ensure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually in the range of between 10 and 100 nF), close to the V_{CC} / V_{SS} device pins.

4.6 Power-up conditions

When the power supply is turned on, V_{CC} rises continuously from V_{SS} to V_{CC}. During this time, the Chip select ($\overline{S}$) line is not allowed to float but follows the V_{CC} voltage. It is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see Figure 4. Bus master and memory devices on the SPI bus).

In addition, the Chip select ($\overline{S}$) input offers a built-in safety feature - its input is edge-sensitive as well as level-sensitive. Thus, after power-up, the device is not selected until a falling edge has first been detected on $\overline{S}$. This ensures that Chip select ($\overline{S}$) was high, prior to going low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in Table 18. Operating conditions.

4.7 Power-down conditions

During power-down (continuous decrease of the supply voltage below the minimum V_{CC} operating voltage defined in Table 18. Operating conditions), the device must be:

- deselected ($\overline{S}$ must follow the voltage applied on V_{CC})
- in standby power mode (there must not be any internal write cycle in progress).

4.8 Active power, standby power, and deep power-down modes

When chip select ($\overline{S}$) is low, the device is selected, and in active power mode.

When chip select ($\overline{S}$) is high, the device is deselected, but remains in active power mode until all internal cycles have completed (program, erase, write status register). The device then goes into standby power mode. The device consumption drops to I_{CC1} as specified in Table 23. DC characteristics (M95P32-I; industrial temperature range) and Table 24. DC characteristics (M95P32-E; extended temperature range).

Deep power-down mode is entered when the deep power-down command is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until the release from power-down command is executed. While in deep power-down mode the device ignores all write, program and erase commands. This provides an extra software protection mechanism when the device is not in active use, by protecting it from inadvertent operations. For further information, see Section 6.21 Deep power-down enter (B9h).

4.9 Device reset

A power-on-reset (POR) circuit prevents erroneous instruction decoding, inadvertent programming, and write or erase operations during power-up. At power-up, the device does not respond to instructions until V_{CC} reaches the POR threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Table 18. Operating conditions).

At power-up, when V_{CC} exceeds the POR threshold, the device is reset, and is in the following state:

- in standby power mode
- deselected
- Status register:
  - write enable latch (WEL) bit reset to 0
  - write in progress (WIP) bit reset to 0
  - all nonvolatile bits unchanged
- Configurable and safety registers:
  - all volatile bits reset to 0
  - all nonvolatile bits (DRV1, DRV0) unchanged
- Volatile register:
  - all bits reset to 0 except BUFLD set to 1

Important: The device must not be accessed until V_{CC} reaches a valid and stable level within the specified $V_{CC(min)}$ to $V_{CC(max)}$ range, as defined in Table 18. Operating conditions.

4.10 Hold condition

The hold ($\overline{HOLD}$) signal is used to pause serial communications with the device, without resetting the clocking sequence. However, setting this signal low does not terminate the write status register, program, write, or erase cycles that are in progress.

To enter the hold condition, the device must be selected with chip select ($\overline{S}$) low.

During the hold condition, the serial data output (Q) is high-Z, and the serial data input (D) and serial clock (C) are don't care.

Normally, the device is kept selected for the duration of the hold condition. This ensures that the internal logic state remains unchanged from the moment of entry into the hold condition. Deselecting the device during the hold condition resets the state of the device. This mechanism can be used to reset the ongoing processes.

Note: This resets the internal logic, except the WEL and WIP bits of the status register.

The hold condition starts when the $\overline{\text{HOLD}}$ signal is driven low when the serial clock (C) is already low (as shown in Figure 6). If the falling edge does not coincide with C being low, the hold condition starts when C next goes low.

The hold condition ends on the rising edge of the $\overline{\text{HOLD}}$ signal, if this coincides with C being low. If the rising edge does not coincide with C being low, the hold condition ends when C next goes low.

Figure 6. Hold condition activation

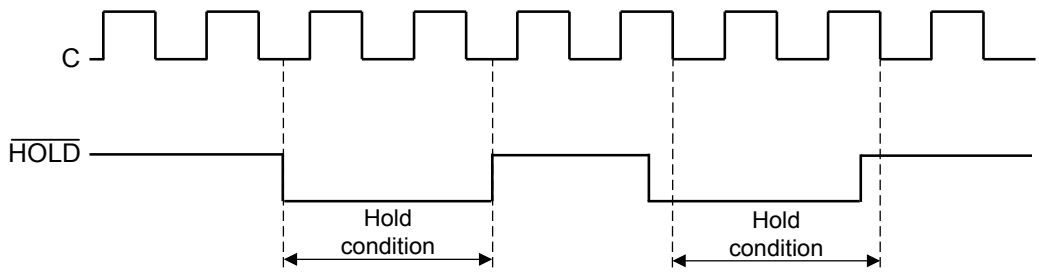


Figure 6 also shows what happens if the rising and falling edges are not timed to coincide with the serial clock (C) being low.

To restart communication with the device, it is necessary to drive $\overline{\text{HOLD}}$ high, and then to drive chip select ($\overline{\text{S}}$) low. This prevents the device from returning to the hold condition.

4.11 ECC

The error correction code (ECC) is an internal logic function that significantly improves the data integrity of the M95P32-I and M95P32-E. It is always active, and is transparent for SPI communication.

The ECC offers double-bit correction over 16 bytes (128 bits), and triple-bit error detection. When a 3-error detection occurs, no correction is applied to the data. The single, double, and triple error detection bits are readable in the safety register.

The ECC flag information is cumulative, meaning that on the same read instruction the flags are raised as soon as a correction or a detection occurs, and all flags may be raised. The status bit is detailed in Section 5.2.2 Safety register.

4.12 Data protection and protocol control

The device features the following data protection mechanisms:

- Power on reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Before accepting the execution of the program, write and erase, and write status register instructions, the device checks whether the number of clock pulses comprising the instructions is a multiple of eight.
- For any instruction to be accepted, and executed, chip select ($\overline{S}$) must be driven high after the rising edge of the serial clock (C) for the last bit of the instruction, and before the next rising edge of the serial clock (C).
- All instructions that modify data must be preceded by a write enable (WREN) instruction to set the write enable latch (WEL) bit.
- The block protection (BP2, BP1, and BP0) and TB bits in the status register are used to configure part of the memory as read-only.
- The write protect ($\overline{W}$) signal is used to protect the block protection (BP2, BP1, BP0) and TB bits in the status register in conjunction with the SRWD bit.

In addition to the low power consumption feature, the DEEP POWER-DOWN mode offers extra software protection because all PROGRAM, and ERASE commands are ignored when the device is in this mode.

4.12.1 Memory protection scheme

The memory can be configured as read-only using the block protection (BP2, BP1, BP0) and TB bits, as shown in Table 4. Refer to Section 5.1 Status register for more information on the BPn bits.

Table 4. Protected area sizes

TB	BP2	BP1	BP0	Protected block(s)	Protected addresses	Protected size(1)	Protected portion
X	0	0	0	None	None	None	None
0	0	0	1	63	3F0000h – 3FFFFFh	64 KB	Upper 1/64
0	0	1	0	62 and 63	3E0000h – 3FFFFFh	128 KB	Upper 1/32
0	0	1	1	60 → 63	3C0000h – 3FFFFFh	256 KB	Upper 1/16
0	1	0	0	56 → 63	380000h – 3FFFFFh	512 KB	Upper 1/8
0	1	0	1	48 → 63	300000h – 3FFFFFh	1 MB	Upper 1/4
0	1	1	0	32 → 63	200000h – 3FFFFFh	2 MB	Upper 1/2
1	0	0	1	0	000000h – 00FFFFh	64 KB	Lower 1/64
1	0	1	0	0 and 1	000000h – 01FFFFh	128 KB	Lower 1/32
1	0	1	1	0 → 3	000000h – 03FFFFh	256 KB	Lower 1/16
1	1	0	0	0 → 7	000000h – 07FFFFh	512 KB	Lower 1/8
1	1	0	1	0 → 15	000000h – 0FFFFFh	1 MB	Lower 1/4
1	1	1	0	0 → 31	000000h – 1FFFFFh	2 MB	Lower 1/2
X	1	1	1	0 → 63	000000h – 3FFFFFh	4 MB	All

1. *The device is ready to accept any chip erase command only if all block protection bits (BP2, BP1, BP0) are at 0.*

4.12.2 Hardware data protection

Hardware data protection is implemented using the write protect signal applied on the $\overline{W}$ pin. This freezes the nonvolatile bits of the status register in a read-only mode. In this mode, the block protection bits (BPn), the top/bottom bit (TB), and the status register write disable bit (SRWD) are protected (for further details, refer to Section 5.1 Status register).

Table 5. Protection modes

$\overline{W}$	SRWD bit	Mode	Write protection of the status register	Memory content(1)	
				Protected area	Unprotected area
1	0	Software protected (SPM)	• Status register is writable (if the WREN instruction has set the WEL bit) • BP2, BP1, BP0, and TB bits can be changed	Write protected	Ready to accept write instructions
0	0				
1	1				
0	1	Hardware protected (HPM)	• Status register is hardware write-protected • BP2, BP1, BP0, and TB bits cannot be changed		

1. *As defined by the values in the block protection (BP2, BP1, BP0) and TB bits of the status register.*

4.13 Polling during a program, write, or erase cycle

A reduction in the time taken to complete the following commands is possible by not waiting for the worst-case delay (t_{pW}, t_{wscr}, t_{PP}, t_{SE}, $_{BE}$, or t_{CE}) to elapse. See Table 26. Programming times:

- Write
- Write status register
- Program
- Erase (page, sector, block, and chip erase)

The write in progress (WIP) bit in the status register is provided so that the application program can monitor whether the write, program, or erase cycle is complete (refer to Section 5.1 Status register).

5 Status, configurable, safety, volatile, and SFDP registers

These registers provide the status of the following:

- availability and the setting of the memory array protection
- output buffer strength
- device after power-up and the ECC bit detection

The write status/configuration register instructions can be used to configure the device write protection features.

5.1 Status register

The status register can be read with the RDSR instruction in loop mode. The nonvolatile bits SRWD, TB, BP2, BP1, and BP0 can be changed with the WRSR instruction when sending a data byte. The MSB (b7) is sent first.

Table 6. Status register format

b7	b6	b5	b4	b3	b2	b1	b0
SRWD	TB	x(1)	BP2	BP1	BP0	WEL	WIP

1. *x: Don't care bit.*

Status register write protect (SRWD) bit

The nonvolatile status register write disable (SRWD) bit is used in conjunction with the write protect ($\overline{W}$) signal. The status register write disable (SRWD) bit and write protect ($\overline{W}$) signals enable the device to be put into hardware protected mode (when the status register write disable (SRWD) bit is set to 1, and write protect ($\overline{W}$) is driven low). In this mode, the nonvolatile bits of the status register (SRWD, BP2, BP1, BP0 and TB) become read-only bits, and the write status register (WRSR) instruction is no longer accepted for execution. The protection modes are described in Table 5. Protection modes.

Top / bottom protection (TB) bit

The nonvolatile Top/Bottom bit (TB) controls whether the block protection bits (BP2, BP1, BP0) protect from the top (TB = 0) or from the bottom (TB = 1) of the array, as shown in Table 4. Protected area sizes. The factory default setting is TB = 0. The TB bit can be set with the write status register instruction, depending on the state of the SRWD and WEL bits.

Block protection (BP2, BP1, BP0) bits

These are nonvolatile read/write bits in the status register, which provide write protection control and status. All, none, or a portion of the memory array can be protected from program and erase instructions (see Table 4. Protected area sizes). The factory default setting for the block protection bits is 0 (array unprotected).

The block protection bits can be set using the write status register instruction.

Write enable latch (WEL) bit

This is a read-only bit in the status register, which is set to 1 after executing a write enable instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up, or after correct completion of any of the following instructions: Write disable, write, page program, sector erase, block erase, chip erase, write status register.

Write in progress (WIP) bit

This is a read-only bit in the status register, set to 1 when:

1. the device is executing a modify operation. During this time, the device ignores further instructions except for the read status register. When the program, write, erase, or write status/configuration register instruction has completed, the WIP bit is cleared to 0, indicating that the device is ready for further instructions.
2. the device is in power-up (see Table 14. Power-up/down conditions).

5.2 Configuration and safety register format

5.2.1 Configuration register

This register can be read with the RDCR instruction in loop mode. The two nonvolatile bits DRV[1:0] can be changed with the WRSR instruction when sending a second data byte. The MSB (b7) is sent first.

Table 7. Configuration register format

b7	b6	b5	b4	b3	b2	b1	b0
x(1)	DRV1	DRV0	x(1)	x(1)	x(1)	x(1)	LID

1. *x: Don't care bit.*

The nonvolatile DRV1 and DRV0 bits determine the output driver strength (R_{ON} of the buffer) for the read operations. The values of DRV1 and DRV0 are given in Table 8. Output driver strength.

The nonvolatile LID bit determines if the identification page is locked or not. When LID = 0, the identification page can be modified by the user. When LID = 1, this page is locked in read-only mode and cannot be changed. The LID bit can be modified with a WRSR instruction when two data bytes are sent, see Section 6.8 Write status and configuration registers (01h).

Table 8. Output driver strength

DRV1, DRV0	Buffer strength	R_{ON} typical at 3.3 V / 25 °C	R_{ON} typical at 1.8 V / 25 °C
0, 0	Do not use.	-	-
0, 1	Medium	110 Ω	200 Ω
1, 0	Low	175 Ω	300 Ω
1, 1	Do not use.	-	-

Note: The delivered state is with buffer strength "Medium".

5.2.2 Safety register

This 8-bit register can be read with the RDCR instruction in loop mode.

All bits are volatile and are read-only. They can be reset with the CLRSF instruction.

Table 9. Safety register format

b7	b6	b5	b4	b3	b2	b1	b0
PAMAF	PUF	ERF	PRF	ECC1C	ECC2C	ECC3D	ECC3DS

Protected array modify attempt flag (PAMAF) bit

This bit indicates whether a modify operation to a protected memory area has been attempted:

- 0: clear
- 1: modify attempt detected

This is a sticky volatile bit that can be reset to 0 only by issuing a clear safety flag instruction. This flag is cleared to 0 after a successful power-up or by a software reset instruction.

Power-up flag (PUF) bit

This bit indicates if the power-up operation was completed successfully:

- 0: successful
- 1: error

This volatile bit is refreshed at each power-up, and after a software reset instruction. The flag is cleared to 0 by the clear safety flag instruction.

Note: In case the PUF bit remains at 1 after the power-up, the status register is read as FF.

Erase flag (ERF) bit

This bit indicates if a previously executed erase operation was completed successfully.

- 0: successful
- 1: error

This volatile bit is refreshed at each erase/write operation. This flag is cleared to 0 at power-up, or by a clear safety flag or software reset instruction.

Program flag (PRF) bit

Indicates if the previously executed program operation was completed successfully.

- 0: successful
- 1: error

This volatile bit is refreshed at each program/write operation. In buffer mode, the flag becomes a sticky flag. This flag is cleared to 0 at power-up, or by a clear safety flag or software reset instruction.

ECC1 correction flag (ECC1C) bit

This bit indicates if the ECC corrected a single-bit error during a previously executed read/program/write operation.

- 0: no correction
- 1: correction done

This volatile bit is refreshed at each read/program/write operation. This flag is cleared to 0 at power-up, or after a clear safety flag or software reset instruction.

ECC2 correction flag (ECC2C) bit

This bit indicates if the ECC corrected a double-bit error in a previously executed read/program/write operation.

- 0: no correction
- 1: correction done

This volatile bit refreshed at each read/program/write operation. This flag is cleared to 0 at power-up, or after a clear safety flag or software reset instruction.

ECC 3 detection flag (ECC3D) bit

This bit indicates that the ECC detected a triple-bit error in at least one word of 16 bytes in a previously executed read/program/write operation.

- 0: no detection
- 1: error detection

This volatile bit is refreshed at each read/program/write operation. This flag is cleared to 0 at power-up, or after a clear safety flag or software reset instruction.

ECC 3 detection flag (ECC3DS) bit

This bit indicates that the ECC detected a triple bit error in at least one word of 16 bytes in a previously executed read/program/write operation.

- 0: no detection
- 1: error detection

This is a sticky volatile bit that can only be reset by issuing a clear safety flag instruction. This flag is cleared to 0 at power-up, or after a software reset instruction.

The ECC flag information is cumulative: on the same read instruction, the flags are raised as soon as a correction or a detection occurs, and all flags may be raised.

5.3 Volatile register format

This byte can be read with the RDVR instruction in loop mode.

Table 10. Volatile register format

b7	b6	b5	b4	b3	b2	b1	b0
x(1)	x	x	x	x	x	BUFEN	BUFLD

1. *Don't care.*

Buffer loading activation (BUFEN) bit

This Buffer mode is activated by setting the volatile configuration bit (BUFEN) to 1 with a WREN + WRVR instruction.

When this bit is set to 1, it allows Page program instruction decoding and buffering while a previous Program instruction is executing.

When this bit is at 0, a Page program instruction is not decoded while the program is being executed. At power-up, or after Software reset instruction, this flag is cleared to 0.

Buffer loading status (BUFLD) bit

When this bit is at 0, the buffer is free and accepts the loading of a new Page program instruction.

When this bit is at 1, the buffer is full and a Page program instruction is discarded and lost.

This bit:

- is set to 1 at power-up
- switches to 0 when BUFEN is set to 1
- is automatically set to 1 when BUFEN is 0

5.4 SFDP register format

The M95P32-I and M95P32-E feature a 512-byte Serial Flash discoverable parameter (SFDP) register that contains information about device configuration, available instructions, and other features, in a standard set of internal parameter tables.

These parameter tables can be interrogated by host-system software, enabling any adjustments needed to accommodate divergent features from multiple vendors.

The Read SFDP register instruction is compatible with the SFDP standard and with the JEDEC standard JESD216.

For further information, refer to www.st.com “Serial flash discovery parameters for M95P family” documentation.

6 Instructions

All instructions can run at the maximum frequency of 80 MHz, except read instructions (READ and RDID), which can run at 50 MHz maximum.

Each command is composed of several bytes (the MSB is transmitted first), initiated with the instruction byte as summarized in Table 11. If an invalid instruction (that is, one that is not contained in Table 11) is sent, the device automatically enters a wait state until the device or the state is deselected.

Table 11. M95P32-I and M95P32-E instruction set

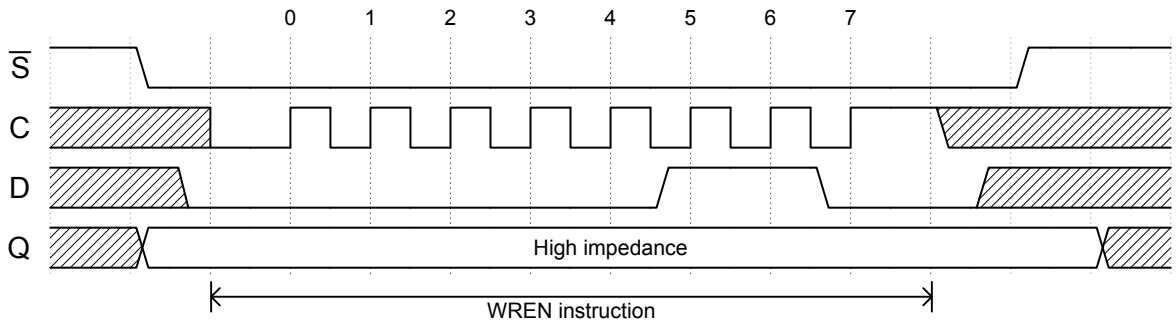
Instruction				Number of bytes			Frequency (MHz)
Name	Description	Binary code	Hex code	Address	Dummy	Data	
WREN	Write enable	0000 0110	06	0	0	0	80
WRDI	Write disable	0000 0100	04	0	0	0	
RDSR	Read status register	0000 0101	05	0	0	1 (rollover)	
WRSR	Write status register	0000 0001	01	0	0	1 or 2	
READ	Read data single output	0000 0011	03	3	0	1 to 4 M (rollover)	50
FREAD	Fast read single output with 1 dummy byte	0000 1011	0B	3	1		80
FDREAD	Fast read dual output with 1 dummy byte	0011 1011	3B	3	1		
FQREAD	Fast read quad output with 1 dummy byte	0110 1011	6B	3	1		
PGWR	Page write (erase and program)	0000 0010	02	3	0	1 to 512	
PGPR	Page program	0000 1010	0A	3	0	1 to 512	
PGER	Page erase (512 bytes)	1101 1011	DB	3	0	0	
SCER	Sector erase (4 Kbytes)	0010 0000	20	3	0	0	
BKER	Block erase (64 Kbytes)	1101 1000	D8	3	0	0	
CHER	Chip erase	1100 0111	C7	0	0	0	
RDID	Read identification (EE)	1000 0011	83	3	0	1 to 1024 (rollover)	50
FRDID	Fast read identification (EE)	1000 1011	8B	3	1		80
WRID	Write identification page (EE)	1000 0010	82	3	0	1 to 512	
DPD	Deep power- down enter	1011 1001	B9	0	0	0	
RDPD	Deep power- down release	1010 1011	AB	0	0	0	
JEDID	JEDEC identification (SF)	1001 1111	9F	0	0	3	
RDCR	Read configuration and safety register	0001 0101	15	0	0	2 (rollover)	
RDVR	Read volatile register	1000 0101	85	0	0	1	
WRVR	Write volatile register	1000 0001	81	0	0	1	
CLRSF	Clear safety sticky flags	0101 0000	50	0	0	0	
RDSFDP	Read SFDP	0101 1010	5A	3	1	1 to 512 (rollover)	
RSTEN	Enable reset	0110 0110	66	0	0	0	
RESET	Software reset	1001 1001	99	0	0	0	

6.1 Write enable (06h)

The write enable (WREN) instruction sets the write enable latch (WEL) bit in the status register to 1. The WEL bit must be set before every page program, page write, page erase, sector erase, block erase, chip erase, write status register, write volatile register, and write identification page instruction.

The write enable instruction is entered by driving $\overline{S}$ low, shifting the instruction code 06h into the data input (D) pin on the rising edge of C, and then driving $\overline{S}$ high. The $\overline{S}$ pin must be driven high after the eighth bit has been latched. If this is not done the write enable instruction is not executed.

Figure 7. Write enable

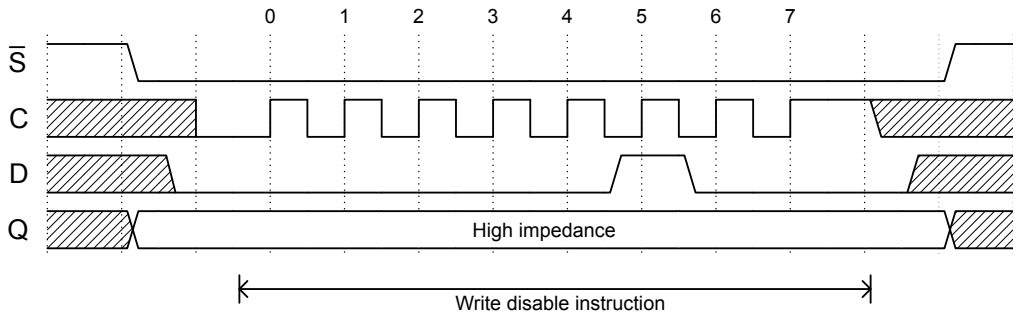


6.2 Write disable (04h)

The write disable (WRDI) instruction resets the write enable latch (WEL) bit in the status register to 0. The write disable instruction is entered by driving $\overline{S}$ low, shifting the instruction code 04h into the D pin, and then driving $\overline{S}$ high.

The $\overline{S}$ pin must be driven high after the eighth bit has been latched. If this is not done the write disable instruction is not executed.

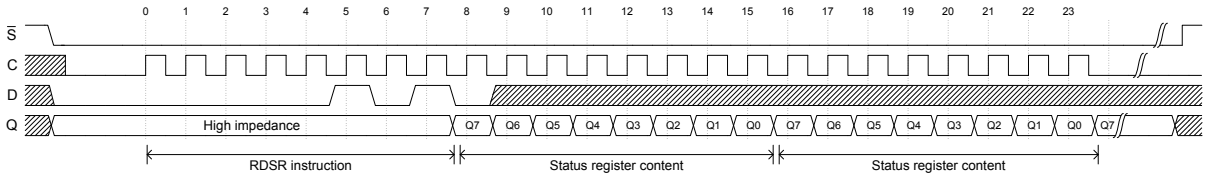
Figure 8. Write disable



6.3 Read status register (05h)

The read status register (RDSR) instruction allows the 8-bit status registers to be read. The instruction is entered by driving $\overline{S}$ low and shifting the instruction code 05h into the D pin on the rising edge of C. The status register bits are then shifted out (MSB first) on the Q pin, on the falling edge of C as shown in Figure 9.

Figure 9. Read status register



The read status register instruction can be used at any time, even while a program, erase or write status register cycle is in progress. This allows the WIP status bit to be checked to determine when the cycle is complete, and if the device is ready to accept another instruction. The status register can be read continuously in loop mode. The instruction is completed by driving $\overline{S}$ high. The content of the status register is described in Section 5.1 Status register.

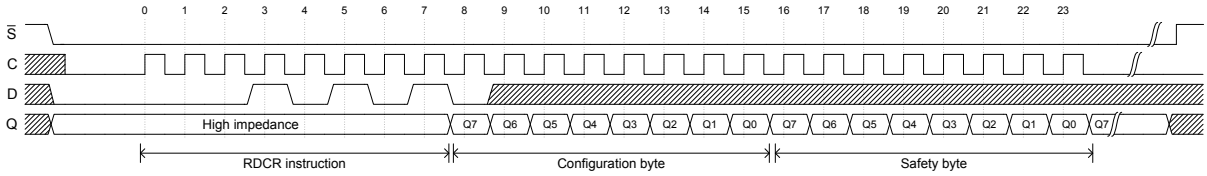
6.4 Read configuration and safety registers (15h)

The read configuration and safety register (RDCR) instruction reads the two configuration and safety register bytes (one for each register). It is sent without an address, and the device first outputs the configuration byte, followed by the safety register byte in loop mode.

The instruction is entered by driving $\overline{S}$ low, and shifting the instruction code 15h into the D pin on the rising edge of C. The configuration and safety register bit values are then shifted out (MSB first) on the Q pin, on the falling edge of C as shown in Figure 10. The configuration and safety registers can be read continuously.

The instruction is completed by driving $\overline{S}$ high.

Figure 10. Read configuration and safety registers



The content of configuration and safety registers is described in Section 5.2 Configuration and safety register format.

6.5 Clear safety register (50h)

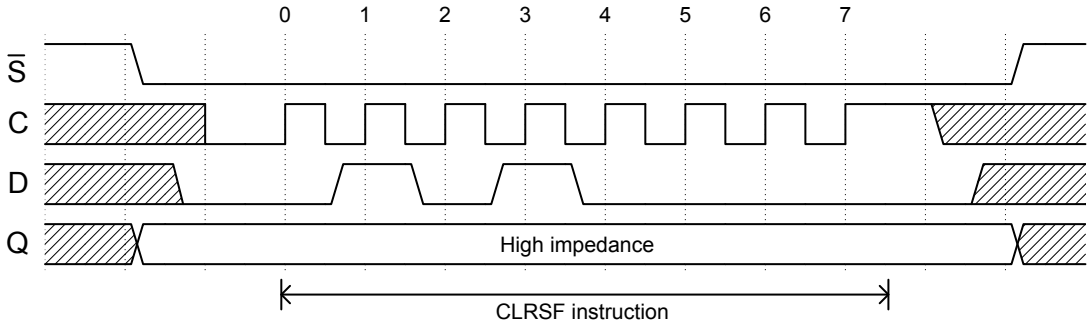
The clear safety register (CLRSF) instruction resets all the bits of the safety register.

This instruction is entered (without an address) by driving $\overline{S}$ low, and shifting the instruction code 50h into the data input (D) pin on the rising edges of C. The instruction is completed by driving $\overline{S}$ high.

As soon as $\overline{S}$ goes high, the device immediately resets all the volatile bits of the safety register.

The $\overline{S}$ pin must be driven high after the eighth bit has been latched. If this is not done the clear safety register instruction is not executed.

Figure 11. Clear safety register



6.6 Read volatile register (85h)

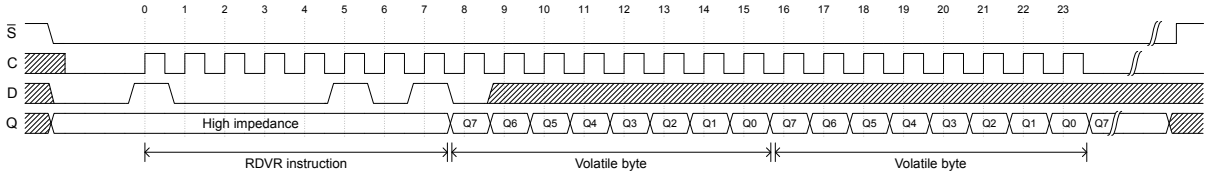
The read volatile register (RDVR) instruction is used to read the 8-bit volatile register.

The instruction is entered by driving $\overline{S}$ low and shifting the instruction code 35h into the D pin on the rising edge of C. The volatile register bits are then shifted out (MSB first) on the Q pin, on the falling edge of C. The volatile register can be read continuously, as shown in Figure 12. The instruction is completed by driving $\overline{S}$ high.

The read volatile register instruction can be used at any time, even while a program, erase or write status register cycle is in progress.

Refer to Section 5 Status, configurable, safety, volatile, and SFDP registers for the register description.

Figure 12. Read volatile register



6.7 Write volatile register (81h)

The write volatile register (WRVR) instruction is used to write the volatile register. The writable volatile register bits include BUFEN and BUFLD.

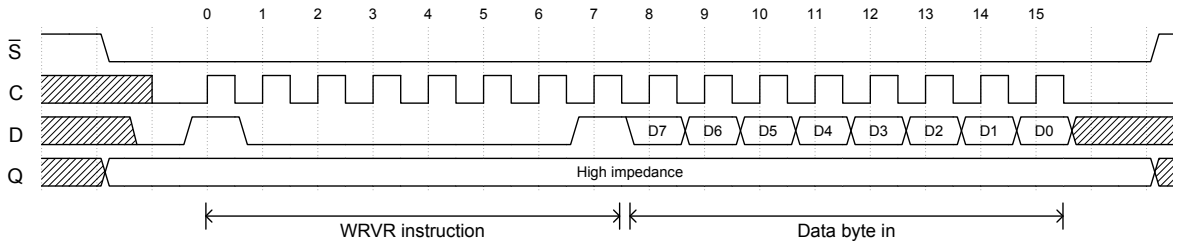
Only the BUFEN bit can be updated. The BUFLD bit is a status bit.

All other bit locations MSB [7:4], LSB[3;2:0] are read-only and are not affected by this instruction.

To write the Volatile register bits, a Write enable (06h) instruction must have been previously executed, or the device does not accept the volatile register instruction (Status register bit WEL must be set to 1). Once write is enabled, the instruction is entered by driving $\overline{S}$ low, sending the instruction code 81h, and then the volatile register data byte. The instruction is completed by driving $\overline{S}$ high.

The $\overline{S}$ pin must be driven high after the eighth bit has been latched. If this is not done, the Write Volatile register instruction is not executed.

Figure 13. Write Volatile register



During the Volatile register write operation (06h combined with 81h), after $\overline{S}$ is driven high, the self-timed Write register cycle starts and the WRVR time is instantaneous (see Table 26. Programming times). The content of volatile register is described in Section 5.3 Volatile register format.

6.8 Write status and configuration registers (01h)

The write status register (WRSR) instruction allows the status and configuration register to be written.

A WRSR instruction, used with one data byte, changes status register bits SRWD, TB, BPx, and WEL.

A WRSR instruction, used with two data bytes, can change status register bits, configuration bits (DVx), and lock ID bit (LID), located in the configuration register.

To write the status and configuration registers, a write enable (06h) instruction must have been previously executed from the device to accept the instruction (Status register bit WEL must be 1). Once write is enabled, the write status register (WRSR) instruction is entered (MSB first) by driving the $\overline{S}$ low, sending the instruction code 01h, followed by one or two data byte(s) on serial data input (D), and driving the $\overline{S}$ high.

The $\overline{S}$ pin must be driven high after the eighth bit has been latched. If this is not done the write status and configurable registers instruction is not executed.

The status register byte and configuration byte are stored in different pages to avoid losing the second byte if, after having changed the first one, a power-down occurs.

A WRSR instruction with more data bytes than defined above is discarded.

The instruction is not accepted, and is not executed, if a write cycle is in progress.

The content of the status and configuration register is described in Section 5.1 Status register and Section 5.2 Configuration and safety register format.

Figure 14. Write status register

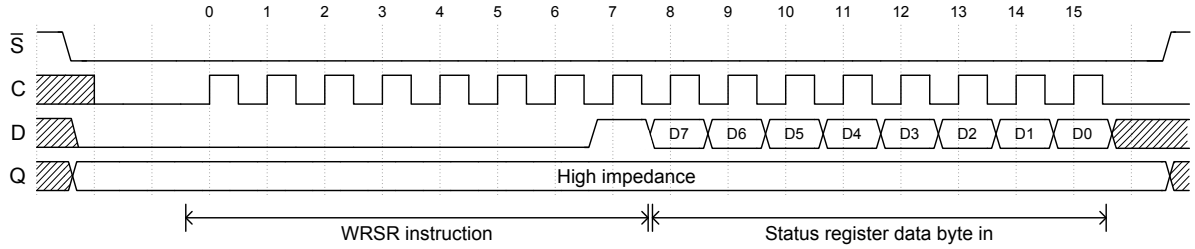
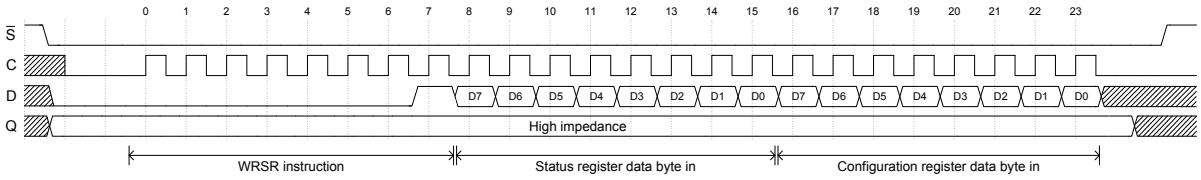


Figure 15. Write status and configuration registers

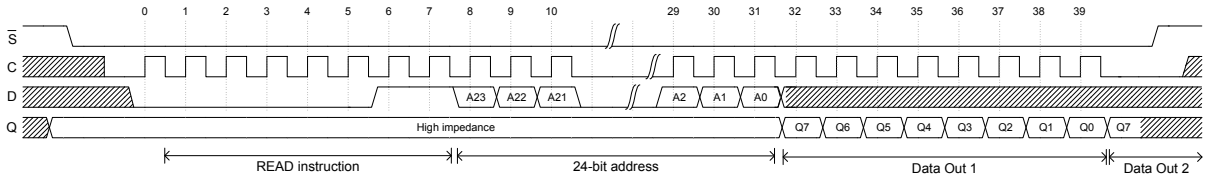


6.9 Read data single output (03h)

The read data single output (READ) instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the $\overline{S}$ pin low and then shifting the instruction code 03h, followed by a 24-bit address (A23-A0) into the D pin. The code and address bits are latched on the rising edge of the C pin. After the address is received, the data byte of the addressed memory location is shifted out (MSB first) on the Q pin, on the falling edge of C. The address is automatically incremented to the next higher address after each data byte is shifted out, allowing a continuous stream of data. This means that the whole memory can be accessed with a single instruction, as long as the clock continues to cycle. The address counter rolls over to 0 after the highest address is reached. The instruction is completed by driving $\overline{S}$ high.

The read data single output instruction sequence is shown in Figure 16.

Figure 16. Read data single output



6.10 Fast read single output with one dummy byte (0Bh)

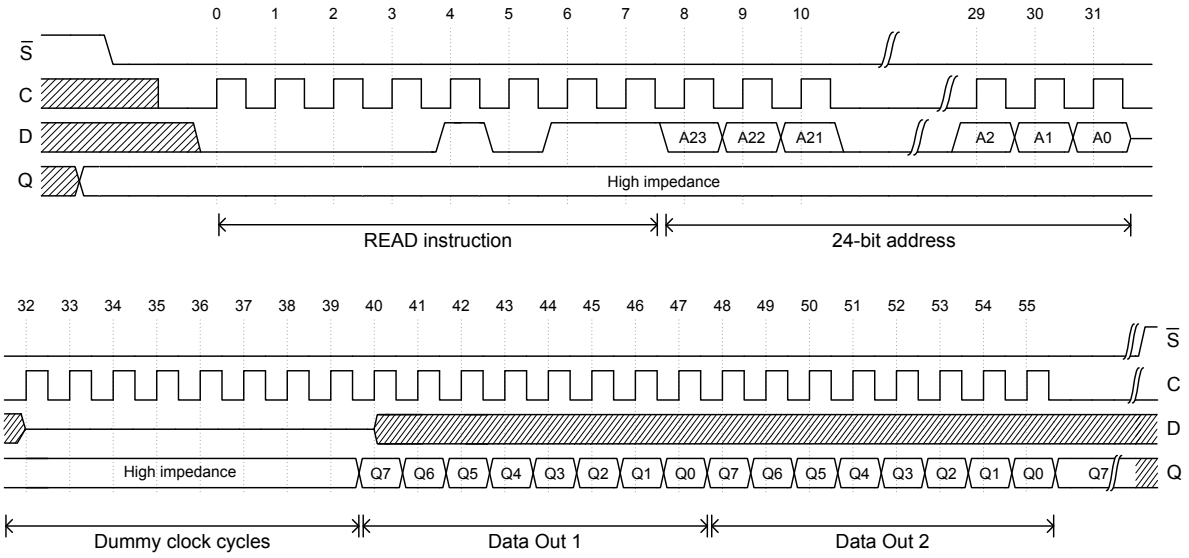
The fast read single output with dummy byte (FREAD) instruction allows one or more data bytes to be sequentially read from the memory. However, through the addition of eight dummy clocks after the 24-bit address, it can operate at the highest possible frequency (see Table 27. AC characteristics).

The instruction is initiated by driving the $\overline{S}$ pin low and then shifting the instruction code 0Bh followed, first by a 24-bit address (A23-A0) into the D pin, then by eight additional dummy clock cycles.

The code and address bits are latched on the rising edge of the C pin. After the eight dummy clock cycles are received, the data byte of the addressed memory location is shifted out (MSB first) on the Q pin, on the falling edge of C. The address is automatically incremented to the next higher address after each byte of data is shifted out, allowing a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues to cycle. The address counter rolls over to 0 after the highest address is reached. The instruction is completed by driving $\overline{S}$ high.

During the dummy clock cycles the data value on the D pin is Don't care, and the Q pin is Hi-Z.

Figure 17. Fast read single output with one dummy byte



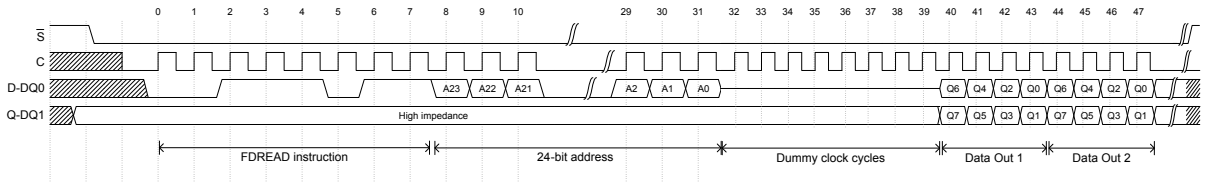
6.11 Fast read dual output with one dummy byte (3Bh)

The fast read dual output with one dummy byte (FDREAD) instruction is similar to the fast read single output with one dummy byte instruction, except that data is output on pins DQ1 and DQ0. This allows the data to be transferred at the highest possible frequency of f_C (see Table 27. AC characteristics).

The instruction is initiated by driving the $\overline{S}$ pin low, then shifting the instruction code 3Bh followed by a 24-bit address (A23-A0) into the D pin, and finally adding eight dummy clock cycles, as shown in Figure 18. The code and address bits are latched on the rising edge of the C pin. After the eight dummy clock cycles are received, the data byte of the addressed memory location is shifted out (MSB first) on the DQ1 and DQ0 pins (every two bits interleave on the two I/O pins), on the falling edge of C.

The address is automatically incremented to the next higher address after each data byte is shifted out, so the whole memory can be read out with a fast read dual instruction. The address counter rolls over to 0 after the highest address is reached. The instruction is completed by driving the $\overline{S}$ pin high. During the dummy clock cycles, the data value on the D pin is don't care, and the Q pin is high-Z.

Figure 18. Fast read dual output with one dummy byte



6.12 Fast read quad output with one dummy byte (6Bh)

The fast read quad output with one dummy (FQREAD) instruction is similar to the fast read dual output with one dummy byte instruction, except that data is output on four pins (DQ3, DQ2, DQ1, and DQ0). This allows data to be transferred at the highest possible frequency f_C (see Table 27. AC characteristics).

The instruction is initiated by driving the $\overline{S}$ pin low, then shifting the instruction code 6Bh, followed by a 24-bit address (A23-A0) into the D pin, and then adding eight dummy clock cycles as shown in Figure 19. The code and address bits are latched on the rising edge of the C pin. After the eight dummy clock cycles are received, the data byte in the addressed memory location is shifted out (MSB first) on the DQ3, DQ2, DQ1, and DQ0 pins (every four bits interleave on the four I/O pins) on the falling edge of C.

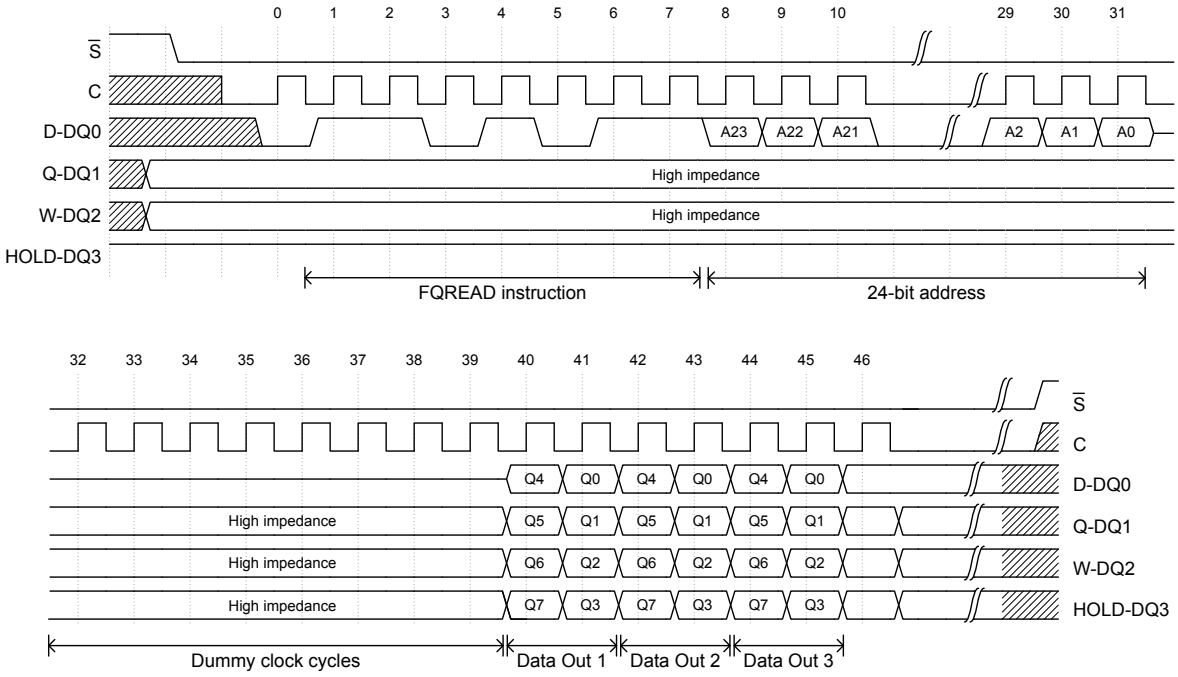
The address is automatically incremented to the next higher address after each data byte is shifted out, so the whole memory can be read out with a fast read quad instruction. The address counter rolls over to 0 after the highest address is reached.

The instruction is completed by driving the $\overline{S}$ pin high.

During the dummy clock cycles, the data value on the D pin is don't care, and the Q pin is high-Z.

Note: The "$\overline{W}$-DQ2" and "$\overline{HOLD}$-DQ3" pins switch in high impedance after the last bit of the third address byte of the instruction.

Figure 19. Fast read quad output with one dummy byte



6.13 Erase operations

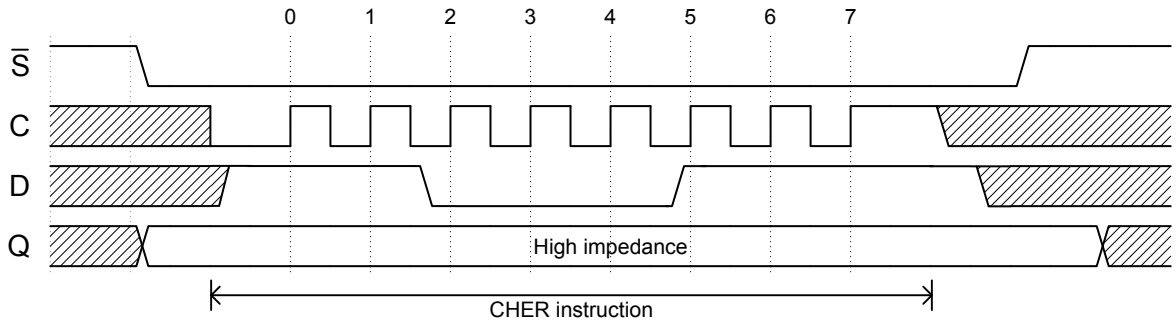
Chip erase, Block erase, Sector erase and Page erase operations set the selected area bits to 1.

6.13.1 Chip erase (C7h)

The chip erase (CHER) instruction sets all memory bits within the device to the erased state of 1 (FFh). A write enable instruction must be executed before the device accepts the chip erase instruction (Status register bit WEL must be 1). The instruction is initiated by driving the $\overline{S}$ pin low and shifting-in the instruction code C7h. The instruction is completed by driving $\overline{S}$ high. The chip erase instruction sequence is shown in Figure 20.

The $\overline{S}$ pin must be driven high after the eighth bit has been latched. If this is not done the chip erase instruction is not executed. After $\overline{S}$ is driven high, the self-timed chip erase instruction starts, with a time duration of t_{CE} (see Table 26). While the chip erase cycle is in progress, the read status register instruction can still be accessed to check the status of the WIP bit. The WIP bit is automatically set to 1 during the chip erase cycle. It is reset to 0 when the device is ready to accept commands. After the chip erase cycle has finished, the write enable latch (WEL) bit in the status register is cleared to 0. The chip erase instruction is not executed if any addressed pages of the chip are protected by the block protection (BP2, BP1, and BP0) and TB bits. The status is reported with PAMAF and ERF flags. See Table 9. Safety register format.

Figure 20. Chip erase

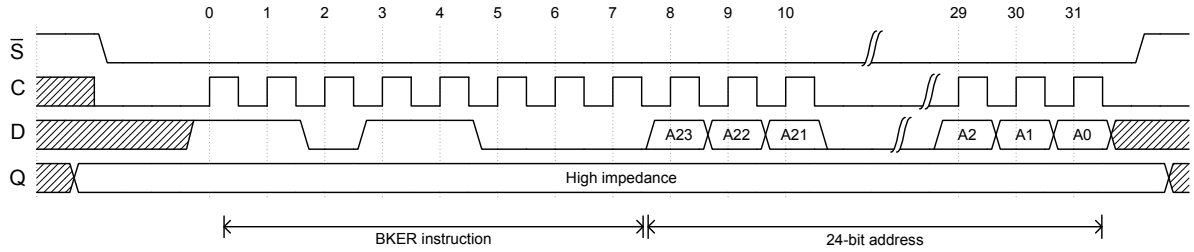


6.13.2 Block erase (D8h)

The block erase (BKER) instruction sets all memory bits within a specified block (64 Kbytes) to the erased state of all 1s (FFh). A write enable instruction must be executed before the device accepts the block erase instruction (the WEL status register bit must be 1). The instruction is initiated by driving the $\overline{S}$ pin low and shifting-in the instruction code “D8h” followed by a 24-bit block address (A23-A0). The instruction is completed by driving $\overline{S}$ high. The block erase instruction sequence is shown in Figure 21.

The $\overline{S}$ pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the block erase instruction is not executed. After $\overline{S}$ is driven high, the self-timed block erase instruction starts, with a time duration of t_{BE1} (see Table 26. Programming times). While the block erase cycle is in progress, the read status register instruction can still be accessed to check the status of the WIP bit. The WIP bit is at 1 during the block erase cycle. It transits to 0 when the cycle has finished and the device is ready to accept further instructions. After the block erase cycle is complete, the write enable latch (WEL) bit in the status register is cleared to 0. The block erase instruction is not executed if any addressed pages of the block are protected by the block protection (BP2, BP1, and BP0) and TB bits. The status is reported with PAMAF and ERF flags. See Table 9. Safety register format.

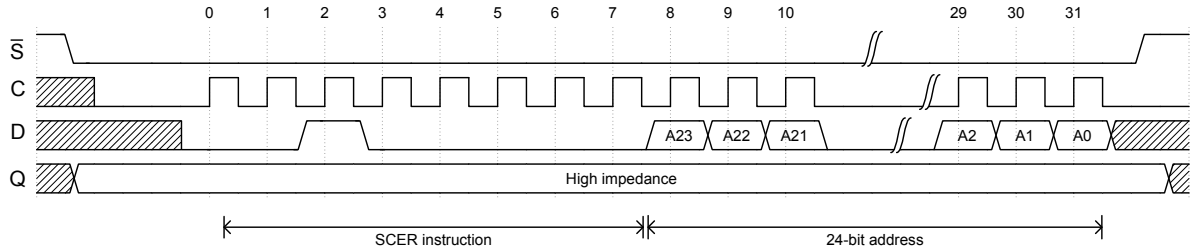
Figure 21. **Block erase**



6.13.3 Sector erase (20h)

The sector erase (SCER) instruction sets all memory bits within a specified sector (4 Kbytes) to the erased state of all 1s (FFh). A writeable instruction must be executed before the device accepts the sector erase instruction (Status register bit WEL must equal 1). The instruction is initiated by driving the $\overline{S}$ pin low and shifting-in the instruction code 20h, followed a 24-bit sector address (A23-A0). The instruction is completed by driving $\overline{S}$ high. The sector erase instruction sequence is shown in Figure 22.

Figure 22. **Sector erase**



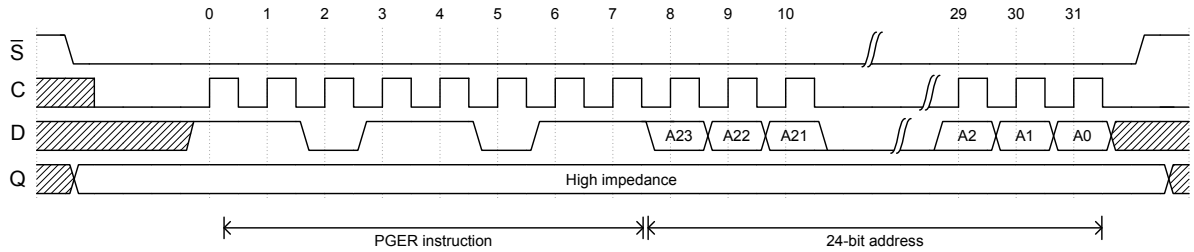
The $\overline{S}$ pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the sector erase instruction is not executed. After $\overline{S}$ is driven high, the self-timed sector erase instruction starts, for a time duration of t_{SE} (see Table 26. Programming times). While the sector erase cycle is in progress, the read status register instruction can still be accessed to check the status of the WIP bit. The WIP bit is set 1 during the sector erase cycle. It transits to 0 when the cycle is finished and the device is ready to accept further instructions. After the sector erase cycle is complete, the write enable latch (WEL) bit in the status register is cleared to 0. The sector erase instruction is not executed if any addressed pages of the sector are protected by the block protection (BP2, BP1, and BP0) and TB bits. The status is reported with PAMAF and ERF flags. See Table 9. Safety register format.

6.13.4 Page erase (DBh)

The page erase instruction (PGER) sets a page of 512 bytes within the device to the erased state of all 1s (FFh). A write enable instruction must first be executed before the device accepts the Page erase instruction (Status register bit WEL must equal 1). The instruction is initiated by driving the $\overline{S}$ pin low and shifting-in the instruction code DBh. The instruction is completed by driving $\overline{S}$ high. The Page erase instruction sequence is shown in Figure 23.

The $\overline{S}$ pin must be driven high after the eighth bit has been latched. If this is not done the page erase instruction is not executed. After $\overline{S}$ is driven high, the self-timed page erase instruction starts, for a time duration of t_{PE} (see Table 26. Programming times). While the page erase cycle is in progress, the Read status register instruction can still be accessed to check the status of the WIP bit. The WIP bit is 1 during the page erase cycle, and becomes 0 when finished and the device is ready to accept further instructions. After the page erase cycle has finished, the write enable latch (WEL) bit in the status register is cleared to 0. The page erase instruction is not executed if the addressed page is protected by the bock protection (BP2, BP1, and BP0) and TB bits. The status is reported with PAMAF and ERF flags. See Table 9. Safety register format.

Figure 23. Page erase



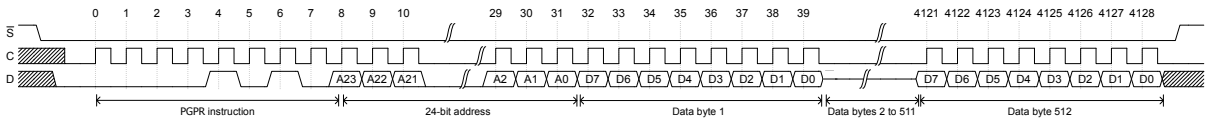
6.14 Page program operations

6.14.1 Page program (0Ah)

The page program instruction (PGPR) allows from one to 512 bytes of data, initially in the erased state (FFh), to be programmed to 0. A write enable instruction must be executed before the device accepts the page program instruction (Status register bit WEL = 1).

The page program instruction is initiated by driving $\overline{S}$ low, then shifting the instruction code 0Ah, followed by a 24-bit address (A23-A0) and at least one data byte into the D-DQ0 pin. The $\overline{S}$ pin must be held low for the whole length of the instruction. The instruction is completed by driving $\overline{S}$ high. The sequence is shown in Figure 24.

Figure 24. Page program



$\overline{S}$ must be driven high after the eighth bit of the last byte has been latched, otherwise the page program instruction is rejected and is not executed. After $\overline{S}$ is driven high, the self-timed page program instruction starts for a time duration of t_{pp} (see Table 26. Programming times). While the page program cycle is in progress, the read status register instruction can still be accessed to check the status of the WIP bit, which is at 1 during the page program cycle. It becomes 0 when the cycle is finished and the device is ready to accept further instructions. When the page program cycle finishes, the write enable latch (WEL) bit in the status register is cleared to 0. The page program instruction is not executed if the addressed page is protected by the block protection bits, and the status is reported with PAMAF, ERF, and PRF flags. See Table 9. Safety register format.

Due to the ECC architecture, the page program operation can be executed only once within a data word of 16 bytes (modulo 16). The page program operation is limited to writing bytes within a single physical page (where address A23 to A9 are the same), regardless of the number of bytes being programmed. After each data byte is received, the address on the nine lowest-order address bits (A8 to A0) is internally incremented by one, and the remaining bits (A23 to A9) remain constant. If more than 512 bytes are transmitted, the address counter rolls over to the beginning of the same page and, the previously stored data is overwritten.

6.14.2 Page program with buffer load (0Ah)

Similarly to the page program instruction, the page program (PGPR) with buffer load instruction allows from one to 512 bytes of data, initially in the erased state (FFh), to be programmed. It also allows the buffer of 512 data bytes for the next page program operation to be loaded during page program execution.

The buffer mode must be activated by setting the buffer loading activation bit (BUFEN) to 1. See Section 5.3 Volatile register format

A write enable instruction must be executed before the device accepts a page program instruction (Status register bit WEL = 1).

The page program with buffer load instruction is initiated by driving pin $\overline{S}$ low, then shifting-in the instruction code 0Ah, followed by a 24-bit address (A23-A0) and at least one data byte into the D-DQ0 pin. The $\overline{S}$ pin must be held low for the whole length of the instruction. The $\overline{S}$ pin must be driven high after the eighth bit of the last byte has been latched. After $\overline{S}$ is driven high, the self-timed page program instruction starts for a time duration of t_{pp} (see Table 26. Programming times). The sequence is shown in Figure 24. Page program.

While the self-timed page program is in progress, and if buffer is available (BUFLD equal to 0), a new page program instruction (no WREN needed) can be sent. This new page program command is executed with the information stored in the buffer as soon as the ongoing page program execution is complete.

- If the buffer is empty, the device waits for a new page program instruction.
- If the buffer is not available (BUFLD equal to 1), the user must wait for the buffer free ((BUFLD equal to 0) before sending a new page program instruction.
- The read volatile register instruction (RDVR) allows buffer status to be checked.

To exit from buffer mode, the volatile configuration bit (BUFEN) in the volatile register must be reset to 0. See Section 6.7 Write volatile register (81h).

Table 12. Buffer load

BUFEN	WIP	BUFLD	Description
0	x	1	Buffer mode inactive. BUFLD is always at 1 when BUFEN is at 0 (buffer mode not active).
1	0	0	Buffer mode activated. All the buffers are empty, page program allowed.
1	1	0	Buffer mode activated. A buffer is empty and the page program is ongoing. New page program authorized to load the available buffer.
1	1	1	Buffer mode activated. All buffers are full and the page program is ongoing. New page program not allowed.

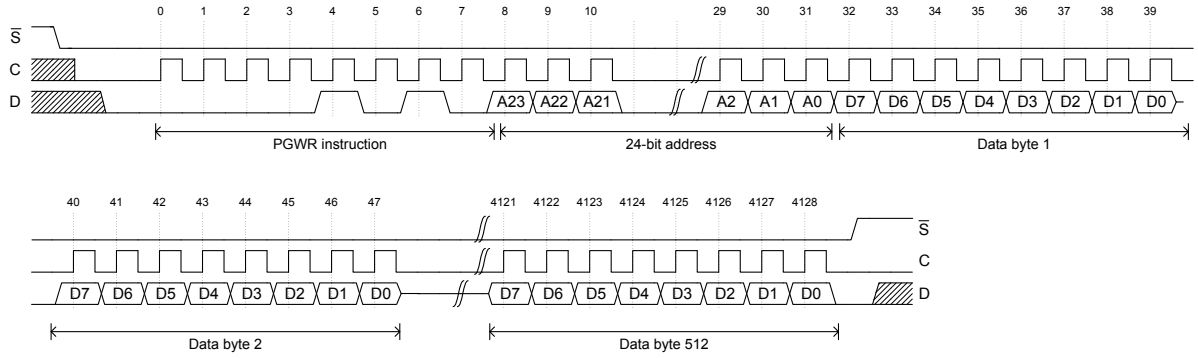
Caution: In buffer mode, only a reduced set of instructions is decoded to allow programming of a selected area. When programming is complete, the BUFEN flag must be reset to enable the device to decode the full set of instructions. In particular, to check programmed content, the user must exit from buffer mode to launch a READ instruction over the programmed area.

6.15 Page write (02h)

The page write (PGWR) instruction allows from one to 512 bytes of data to be written in a single instruction (auto erase + program) leaving the other bytes of the page unchanged. A write enable instruction must be executed before the device accepts this instruction (Status register bit WEL = 1).

The page write instruction is initiated by driving the $\overline{S}$ pin low then shifting the instruction code 02h, followed by a 24-bit address (A23-A0) and at least one data byte, into the D-DQ0 pin. $\overline{S}$ must be held low for the entire length of the instruction while data is being sent to the device. The instruction is completed by driving $\overline{S}$ high. The whole sequence is shown in Figure 25.

Figure 25. Page write



$\overline{S}$ must be driven high after the eighth bit of the last byte has been latched, or the page write instruction is not executed. After $\overline{S}$ is driven high, the self-timed page write instruction starts for a time duration of t_{pw} (Table 26. Programming times). While the page write cycle is in progress, the read status register instruction can still be accessed to check the status of the WIP bit, which is at 1 during the page program cycle, and becomes 0 when the cycle is finished and the device is ready to accept further instructions. After the page write cycle has finished, the write enable latch (WEL) bit in the status register is cleared to 0.

The page write operation is limited to writing bytes within a single physical page (where address A23 to A9 are the same). After each data byte received, the address on the nine lowest order address bits (A8 to A0) is internally incremented by one, and the remaining bits (A23 to A9) remain constant. If more than 512 bytes are transmitted, the address counter rolls over to the beginning of the same page and the previously stored data is overwritten.

The write page instruction is not executed if a part of the targeted area is protected by the block protection bits. In this case, the status is reported with the PAMAF, ERF, and PRF flags.

6.16 Read identification (83h)

The read identification (RDID) instruction allows one or more data bytes in the two identification pages (512 bytes each) to be read sequentially:

- The first page contains three device identification bytes.
- In the case of a UID, one byte for length and a unique ID value on N bytes (N specified in UID length), as defined in Table 13.
- The second page is located at the address 200h. It is delivered erased and available for customer data.

Table 13. Identification page content

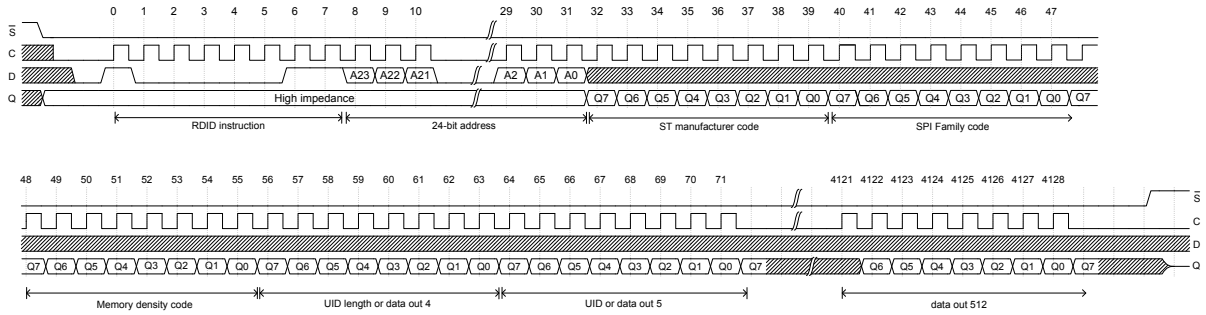
Address (in the first identification page)	Content	Value
00h	ST manufacturer code	20h
01h	SPI family code	00h
02h	Memory density code	15h (16-Mbit) (32-Mbit)
03h	UID length	00h
04h	UID	FFh

Note: The first three bytes (address 00h, 01h, and 02h) of the identification page can also by read with the read JEDEC identification (JDID) instruction.

The read identification (RDID) instruction is initiated by driving the $\overline{S}$ pin low and shifting the instruction code 83h, followed by a 24-bit address (A23-A0) into the D-DQ0 pin.

The data byte pointed to by the lower address bits [A9:A0] is shifted out (MSB first) on the serial data output (Q), as shown in Figure 26. Read identification. The address is automatically incremented to the next higher address of the identification pages after each data byte is shifted out, thus enabling a continuous stream of data. This means that the entire area of identification pages (1024 bytes) can be accessed with a single instruction as long as the clock continues to cycle. The instruction is completed by driving $\overline{S}$ high.

Figure 26. Read identification



6.17 Fast read identification (8Bh)

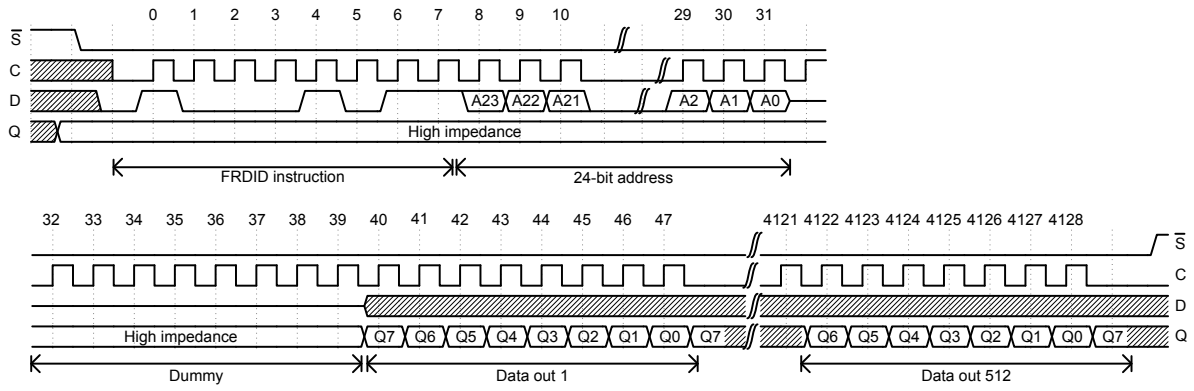
The fast read identification instruction (FRDID) allows one or more data bytes in the two identification pages to be sequentially read. However, through the addition of eight dummy clocks after the 24-bit address, it can operate at the highest possible frequency f_C (see Table 27. AC characteristics).

This instruction is initiated by driving the $\overline{S}$ pin low and shifting the instruction code 8Bh, followed first by a 24-bit address (A23-A0) into the D-DQ0 pin, then by eight additional dummy clocks. The code and address bits are latched on the rising edge of the C pin. After the eight dummy clocks are received, the data byte of the addressed memory location is shifted out (MSB first) on the Q pin, on the falling edge of C. The address is automatically incremented to the next higher address after each data byte is shifted out, thus enabling a continuous stream of data. This means that the entire identification page (1024 bytes) can be accessed with a single instruction as long as the clock continues to cycle.

The address counter rolls over to 0 after the highest address of the second identification page is reached. The instruction is completed by driving the $\overline{S}$ pin high. During the dummy clock cycles the data value on the D pin is don't care, and the Q pin is Hi-Z.

The fast read instruction sequence is shown in Figure 27.

Figure 27. Fast read identification

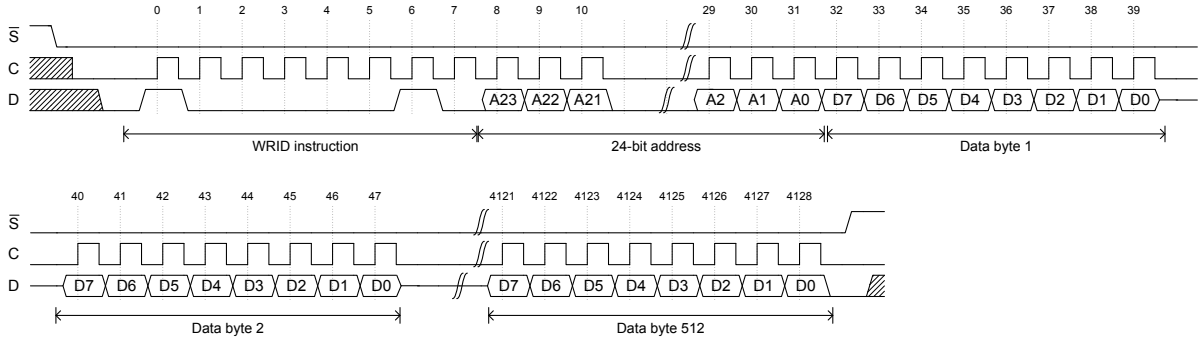


6.18 Write identification page (82h)

The Write identification page instruction (WRID) is used to write the identification page.

To write the Identification page, a Write enable (06h) instruction must have been executed previously for the device to accept the instruction (Status register bit WEL must equal 1). Once write is enabled, the write identification page instruction is initiated by driving the $\overline{S}$ pin low, then shifting the instruction code 82h followed by a 24-bit address (A23-A0) and at least one data byte, into the D pin. The $\overline{S}$ pin must be held low for the whole length of the instruction while data is being sent to the device. The instruction is completed by driving $\overline{S}$ high. (see Figure 28).

Figure 28. Write identification page



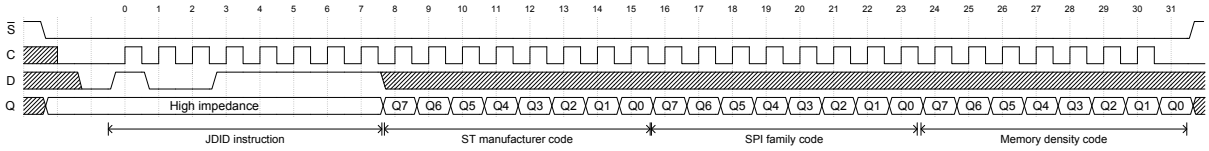
Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the address counter exceeds the page boundary (the page size is 512 bytes), the internal address pointer rolls over to the beginning of the page where next data bytes are written. If more than 512 bytes are received, only the last 512 bytes are written.

6.19 JEDEC identification (9Fh)

The JEDEC identification instruction (JDID) allows the three device identification bytes to be read in loop mode. See Table 13. Identification page content.

This instruction is initiated by driving the $\overline{S}$ pin low and then shifting the instruction code 9Fh into the D pin. The code bits are latched on the rising edge of the C pin. After the last bit of instruction code is received, the three identification bytes are shifted out (MSB first) on the Q pin, on the next falling clock edge. The same three bytes are continuously shifted out as long as the clock continues to cycle. The instruction is stopped by driving the $\overline{S}$ pin high, as shown in Figure 29.

Figure 29. JEDEC identification



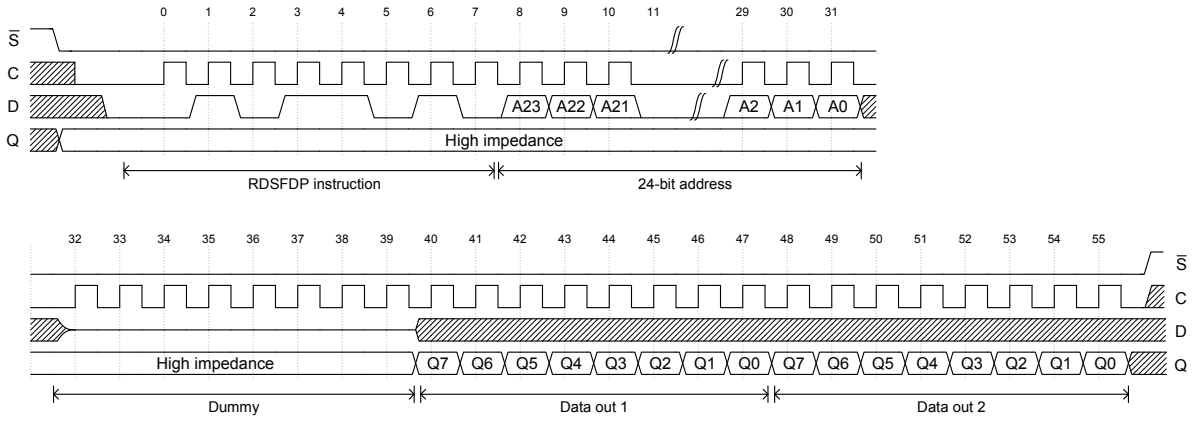
6.20 Read SFDP (5Ah)

The read SFDP instruction (RDSFDP) is used to read the SFDP register format.

This instruction is initiated by driving the $\overline{S}$ pin low and shifting the instruction code 5Ah, followed first by a 24-bit address (A23-A0) into the D pin, then by eight additional dummy clock cycles. The code and address bits are latched on the rising edge of the C pin. After the eight dummy clocks are received, the data byte of the SFDP register is shifted out (MSB first) on the Q pin, on the falling edge of C. The address is automatically incremented to the next higher address after each data byte is shifted out, thus enabling a continuous stream of data. This means that the whole SFDP register (512 bytes) can be accessed with a single instruction, as long as the clock continues to cycle. The instruction is completed by driving $\overline{S}$ high. During the dummy clock cycles the data value on the D pin is don't care, and the Q pin is high-Z.

The read SFDP sequence is shown in Figure 30. Read SFDP.

Figure 30. Read SFDP

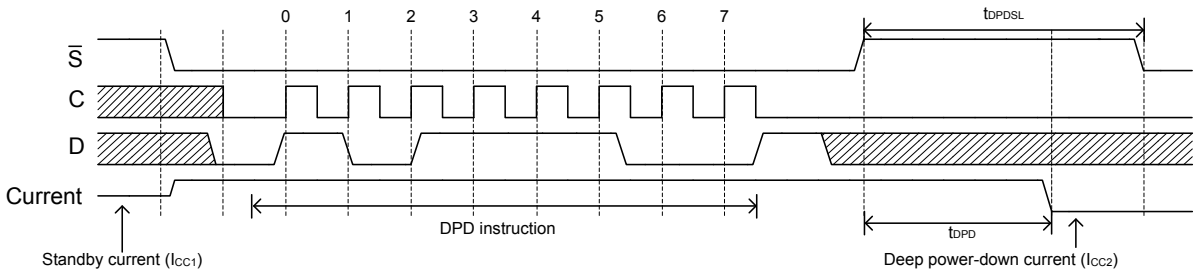


6.21 Deep power-down enter (B9h)

The deep power-down enter (DPD) instruction puts the device in a very low consumption state, in which a limited number of commands are available. This instruction is initiated by driving $\overline{S}$ low and shifting the instruction code B9h into the D pin. The $\overline{S}$ pin must be held low for the entire length of the instruction. Pin $\overline{S}$ must be driven high after the eighth bit has been latched, otherwise the instruction is not executed. After $\overline{S}$ is driven high, the device enters in deep power-down state after a delay of t_{DPD} (see Table 15. Deep power-down conditions).

The deep power-down enter instruction sequence is shown in Figure 31.

Figure 31. Deep power-down enter



While in deep power-down state, only the deep power-down release and reset instructions, which restore the device to normal operation, are recognized. The device is always in normal operation on power-up, with a standby current of I_{CC1}.

Refer to Table 15. Deep power-down conditions for t_{DPD} and t_{RDPDSL}.

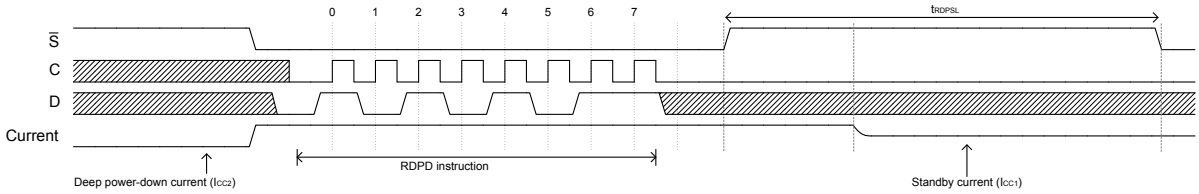
6.22 Deep power-down release (ABh)

The power-down release instruction (RDPD) releases the device from deep power-down state to Standby mode state.

This instruction is initiated by driving $\overline{S}$ low and shifting the instruction code ABh into the D pin. The $\overline{S}$ pin must be held low for the full length of the instruction. Pin $\overline{S}$ must be driven high after the eighth bit has been latched, otherwise the instruction is not executed. After $\overline{S}$ is driven high, it must remain high for at least t_{RDPSL} as specified in Table 15. Deep power-down conditions). Once in standby power mode, the device waits to be selected so that it can receive, decode, and execute instructions.

The deep power-down release instruction sequence is shown in Figure 32.

Figure 32. Deep power-down release



Refer to Table 15. Deep power-down conditions for t_{DPD} and t_{RDPSL}.

6.23 Enable reset (66h) and Software reset (99h)

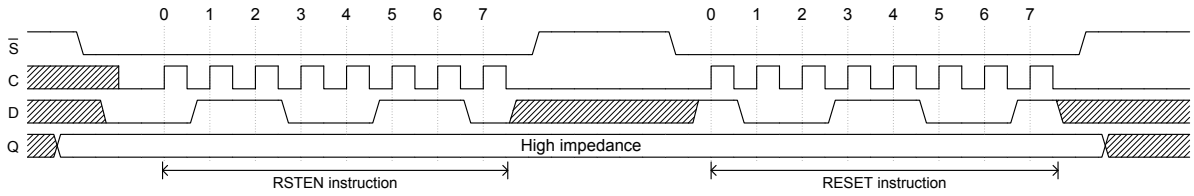
The enable reset (RSTEN) and Software reset (RESET) instructions reset the device.

The RSTEN instruction enables the RESET instruction.

The RSTEN instruction is initiated by driving $\overline{S}$ low and shifting the instruction code 66h into the D pin. The $\overline{S}$ pin must be held low for the entire length of the instruction . Pin $\overline{S}$ must be driven high after the eighth bit has been latched. Once the $\overline{S}$ pin is driven high, the RESET instruction is initiated by driving $\overline{S}$ low and shifting the instruction code 99h into the D pin. The $\overline{S}$ pin must be held low for the entire length of the instruction . Pin $\overline{S}$ must be driven high after the eighth bit has been latched, otherwise the instruction is not executed.

To avoid accidental resets, these two instructions must be issued in sequence. Any command other than a Software reset (99h) after an Enable reset (66h) command disables the Reset enable state. A new sequence of Enable reset (66h) and Software reset (99h) is needed to reset the device. Once the Reset command is accepted by the device, the reset is effective after a delay given in Table 16. Reset recovery time. During this period, no command is accepted.

Figure 33. Software reset



RSTEN and RESET instructions are understood in Deep power-down mode.

When the device is in Deep Power mode or Standby mode, a Software reset command can be decoded and executed. In this case, the device is reset and after t_{RST1} or t_{RST2} and enters Standby mode, ready to accept all instructions.

When the device is executing a modify operation (including Write Status register command) a Software reset command can be decoded and executed. In this case either: the ongoing operation is properly completed: the device is reset it goes in Standby mode, ready to accept all instructions or the ongoing operating does not finish correctly, the data being processed can be damaged or lost, the device resets and it goes in Standby mode, ready to accept all instructions.

7 Power-up/down

7.1 Power-up/down

Figure 34. **Power-up timing**

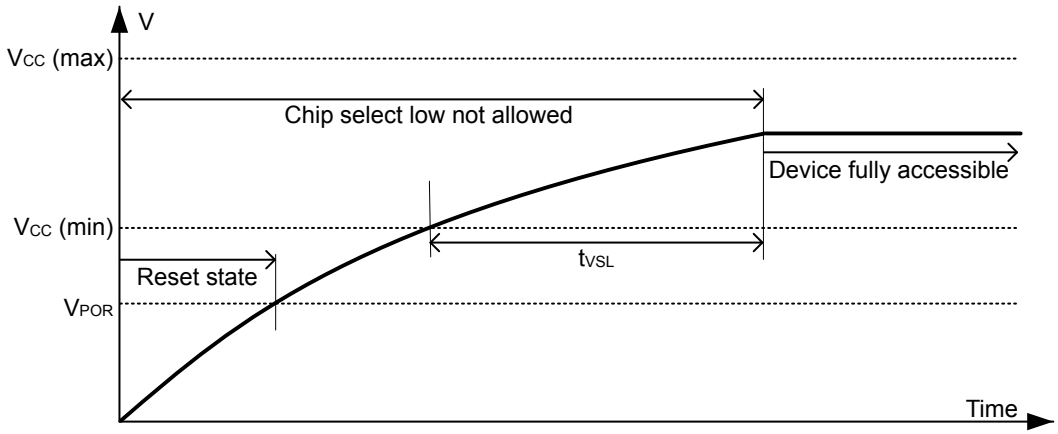


Figure 35. **Power-down timing**

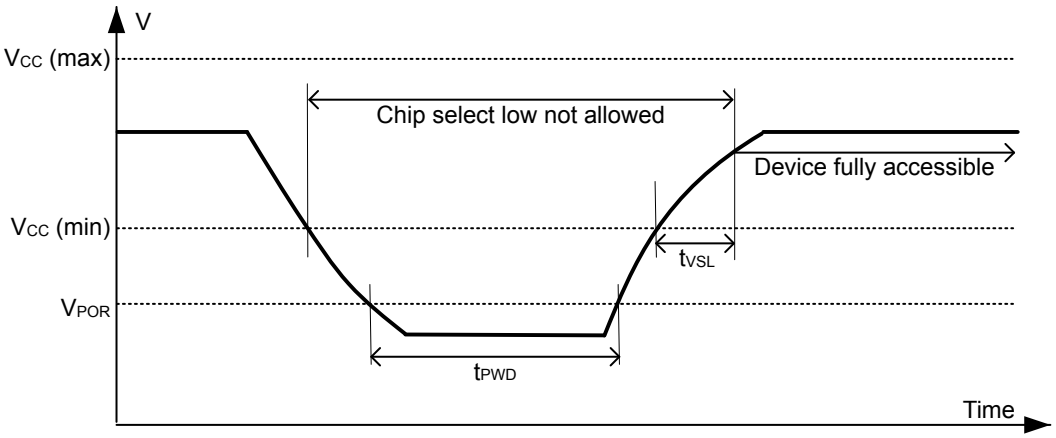


Table 14. **Power-up/down conditions**

Parameter		Symbol	Min	Max	Unit
Power-up	$V_{CC(min)}$ to $\overline{S}$ low(2)	t_{VSL}	30(1)	-	µs
	Power-on reset voltage(2)	V_{POR}	1.1	1.45	V
Power-down	Power-down time for reset(2)	t_{PWD}	10	-	µs
	Power-on reset voltage(2)	V_{POR}	1.1	1.45	V

1. *The WIP bit can be monitored after T_{VSL} has elapsed (WIP = 1 at power-up and before t_{VSL} = 30 µs).*
2. *Evaluated by characterization - not tested in production.*

7.2 Deep power-down

Table 15. Deep power-down conditions

Symbol	Parameter	Min	Max	Unit
t_{DPDSL} (1)(2)	Delay for $\overline{S}$ low (new instruction after $\overline{S}$ high from deep power-down enter instruction)	10	-	µs
t_{DPD} (3)	Time delay for deep power-down mode after $\overline{S}$ high	-	10	µs
t_{RDPDSL} (1)(2)	Release deep power-down delay to $\overline{S}$ low (new instruction)	30	-	µs

1. *Evaluated by characterization - not tested in production.*
2. *Refer to Figure 31. Deep power-down enter and Figure 32. Deep power-down release.*
3. *Specified by design - not tested in production.*

7.3 Reset

Table 16. Reset recovery time

Symbol	Parameter	Min	Max	Unit
t_{RST1} (1)	Reset time when reset occurs with WIP = 0	-	30	µs
t_{RST2} (1)	Reset time when reset occurs in modify operation except chip erase	-	12	ms
t_{RST3} (1)	Reset time when reset occurs in chip erase execution	-	25	ms

1. *Specified by design - not tested in production.*

8 Delivery state

The device is delivered with the following configuration:

- Memory array erased: all bits set to 1 (each byte = FFh)
- Status register: 00h (all bits are initialized to 0)
- Safety register: 00h (all bits are initialized to 0)
- Configuration register: 20h (0010 0000d)
- Volatile register: 01h (0000 0001d)
- Jedec ID delivered with 3 bytes set as specified in Table 13. Identification page content
- Identification pages not protected and content as described in Section 6.16 Read identification (83h)

9 Maximum ratings

Stressing the device outside the ratings listed in Table 17 may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 17. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{AMB}	Ambient operating temperature	–40	125	°C
T_{STG}	Storage temperature	–65	150	
T_{LEAD}	Lead temperature during soldering	See note (1)		
V_O	Output voltage	–0.50	V_{CC} + 0.6	V
V_I	Input voltage	–0.50	4.2	
V_{CC}	Supply voltage	–0.50	4.2	
I_{OL}	DC output current (Q = 0)	-	5	mA
I_{OH}	DC output current (Q = 1)	-	5	
V_{ESD}	Electrostatic discharge voltage (human body model) (2)	-	2000	V

1. *Compliant with JEDEC standard J-STD-020 (for small-body, Sn-Pb or Pb free assembly), the ST ECOPACK 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS directive 2011/65/EU of July 2011).*
2. *Positive and negative pulses applied on different combinations of pin connections, according to ANSI/ESDA/JEDEC JS-001, C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω.*

10 DC and AC parameters

This section summarizes the operating conditions and the DC/AC characteristics.

Table 18. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.6	3.6	V
T_A	Ambient operating temperature, industrial range	-40	85	°C
	Ambient operating temperature, extended range	-40	105	°C

Table 19. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
-	Input rise/fall time	-	5	ns
-	Input waveforms levels	0.1 V_{CC}	0.9 V_{CC}	V
-	Input timing reference levels	0.3 V_{CC}	0.7 V_{CC}	
-	Output timing reference level	0.5 V_{CC}		
Cbus	Capacitive load on output pins (CL)	-	30 or 100	pF

Figure 36. AC measurement levels

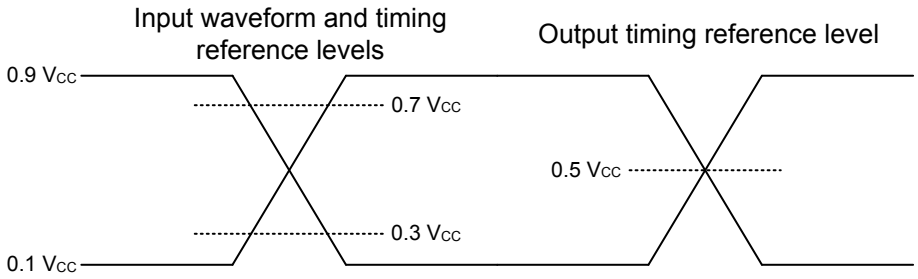


Table 20. Cycling performance by pages

Symbol	Parameter	Test conditions	Min.	Max.	Unit
Ncycle	Write cycle endurance	–40 °C ≤ T_A ≤ 85 °C, (1) $V_{CC}(min) < V_{CC} < V_{CC}(max)$	-	500000	Write cycle (2)
-	Chip erase endurance	–40 °C ≤ T_A ≤ 85 °C, (1) $V_{CC}(min) < V_{CC} < V_{CC}(max)$	-	100	Cycle

1. *–40 °C ≤ T_A ≤ 105 °C for extended range.*
2. *A write cycle is executed when either a page write, a page program, a page erase, a WRSR, a WRID, or an LID is decoded. When using the page write or the WRID instruction refer also to Section 4.11 ECC.*

Table 21. Memory cell data retention

Parameter	Test conditions	Min.	Unit
Data retention (1)	T_A = 40 °C	100	Year
Data retention after cycling (after 500K cycles)(1)		10	

1. *The data retention behavior is checked in production, while the 100-year limit is defined from characterization and qualification results.*

Table 22. Capacitance

Symbol	Parameter	Test conditions (1)	Min.	Max.	Unit
C_{OUT}	Output pins capacitance	V_{OUT} = 0 V	-	8	pF
C_{IN}	Input capacitance (D)	V_{IN} = 0 V	-	6	

1. *Specified by design - not tested in production.*

Table 23. DC characteristics (M95P32-I; industrial temperature range)

Symbol	Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{CC1}	Standby supply current		$\overline{S}$ = V_{CC}; T_A = 25 °C V_{IN} = V_{SS} or V_{CC}; 1.6 V ≤ V_{CC} ≤ 3.6 V	-	16	35	µA
			$\overline{S}$ = V_{CC}; T_A = 85 °C V_{IN} = V_{SS} or V_{CC}; 1.6V ≤ V_{CC} ≤ 3.6 V	-	35(1)	40(1)	
I_{CC2}	Deep power-down current		$\overline{S}$ = V_{CC}; T_A = 25 °C V_{IN} = V_{SS} or V_{CC}; V_{CC} = 1.8 V	-	0.6	1.0	µA
			$\overline{S}$ = V_{CC}; T_A = 25 °C V_{IN} = V_{SS} or V_{CC}; V_{CC} = 3.6 V	-	1.5	2.0	
			$\overline{S}$ = V_{CC}; T_A = 85 °C V_{IN} = V_{SS} or V_{CC}; V_{CC} = 1.8 V	-	0.6(1)	2.0(1)	µA
			$\overline{S}$ = V_{CC}; T_A = 85 °C V_{IN} = V_{SS} or V_{CC}; V_{CC} = 3.6 V	-	1.5(1)	3.0(1)	
I_{CC3}	Read current single	10 MHz	Q open	-	0.8(1)	1.5(1)	mA
	Read current dual			-	0.8(1)	2.0(1)	
	Read current quad			-	0.9(1)	2.0(1)	
	Read current single	20 MHz	Q open	-	1.0	2.0	mA
	Read current dual			-	1.2	2.0	
	Read current quad			-	1.5	3.0	
	Read current single	50 MHz	Q open	-	1.5(1)	3.0(1)	mA
	Read current dual			-	1.8(1)	3.0(1)	
	Read current quad			-	2.0(1)	3.0(1)	
	Read current single	80 MHz	Q open	-	2.0	3.0	mA
	Read current dual			-	2.5	4.0	
	Read current quad			-	3.0	5.0	
I_{CC4}(1)	Page program current		$\overline{S}$ = V_{CC}, no polling Averaged on execution time	-	2.0	3.0	mA
I_{CC5}(1)	Write status current			-	1.5	3.0	mA
I_{CC6}(1)	Page write current			-	1.5	3.0	mA
I_{CC7}(1)	Page erase current			-	1.0	3.0	mA
I_{CC8}(1)	Sector/block erase current			-	2.0	3.0	mA
I_{CC9}(2)	Chip erase current			-	10	25	mA

1. *Evaluated by characterization - not tested in production.*
2. *Specified by design - not tested in production.*

Table 24. DC characteristics (M95P32-E; extended temperature range)

Symbol	Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{CC1}	Standby supply current		$\overline{S}$ = V_{CC}; T_A = 25 °C V_{IN} = V_{SS} or V_{CC}; 1.6 V ≤ V_{CC} ≤ 3.6 V	-	16	35	µA
			$\overline{S}$ = V_{CC}; T_A = 105 °C V_{IN} = V_{SS} or V_{CC}; 1.6 V ≤ V_{CC} ≤ 3.6 V	-	45	150	
I_{CC2}	Deep power-down current		$\overline{S}$ = V_{CC}; T_A = 25 °C V_{IN} = V_{SS} or V_{CC}; V_{CC} = 1.8 V	-	0.6	1.0	µA
			$\overline{S}$ = V_{CC}; T_A = 25 °C V_{IN} = V_{SS} or V_{CC}; V_{CC} = 3.6 V	-	1.5	2.0	
			$\overline{S}$ = V_{CC}; T_A = 105 °C V_{IN} = V_{SS} or V_{CC}; V_{CC} = 1.8 V	-	1.5	2.0	µA
			$\overline{S}$ = V_{CC}; T_A = 105 °C V_{IN} = V_{SS} or V_{CC}; V_{CC} = 3.6 V	-	2.5	4.0	
I_{CC3}	Read current single	10 MHz	Q open	-	0.8(1)	1.5(1)	mA
	Read current dual			-	0.8(1)	2.0(1)	
	Read current quad			-	0.9(1)	2.0(1)	
	Read current single	20 MHz	Q open	-	1.0	2.0	
	Read current dual			-	1.2	2.0	
	Read current quad			-	1.5	3.0	
	Read current single	50 MHz	Q open	-	1.5(1)	3.0(1)	
	Read current dual			-	1.8(1)	3.0(1)	
	Read current quad			-	2.0(1)	3.0(1)	
	Read current single	80 MHz	Q open	-	2.0	3.0	
	Read current dual			-	2.5	4.0	
	Read current quad			-	3.0	5.0	
I_{CC4}(1)	Page program current		$\overline{S}$ = V_{CC}, no polling. Averaged on execution time.	-	2.0	3.0	
I_{CC5}(1)	Write status current			-	1.5	3.0	
I_{CC6}(1)	Page write current			-	1.5	3.0	
I_{CC7}(1)	Page erase current			-	1.0	3.0	
I_{CC8}(1)	Sector/block erase current			-	2.0	3.0	
I_{CC9}(2)	Chip erase current			-	10	25	

1. *Evaluated by characterization - not tested in production.*
2. *Specified by design - not tested in production.*

Table 25. DC characteristics - other parameters

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}	-	±2	µA
I_{LO}	Output leakage current		-	±2	
V_{IL}	Input low voltage	Q open	-0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage		0.75 V_{CC}	V_{CC} + 0.6	
V_{OL}	Output low voltage	V_{CC} = 1.8 V, I_{OL} = 0.15 mA	-	0.3	
		V_{CC} = 2.5 V, I_{OL} = 1.5 mA	-	0.4	
V_{OH}	Output high voltage	V_{CC} = 1.8 V, I_{OH} = 0.15 mA	0.8 V_{CC}	-	
		V_{CC} = 2.5 V, I_{OH} = 1.5 mA	0.8 V_{CC}	-	
V_{por}(1)	Voltage reset	-	1.1	1.45	

1. *Evaluated by characterization - not tested in production.*

Table 26. Programming times

Symbol	Parameter	Min.	Typ.(1)(2)	Max.(3)	Unit
t_{PP}	Page program cycle time (512 bytes)	-	1.2	1.5	ms
t_{PE}	Page erase cycle time (512 bytes)	-	1.1	4.5(3)	
t_{PW}	Page write cycle time (512 bytes)	-	2	4(3)	
t_{SE}	Sector erase cycle time	-	1.3	5(3)	
t_{BE}	Block erase cycle time	-	4	8(3)	
t_{CE}	Chip erase cycle time	-	15	25(3)	
t_{WSCR}	Write status and configuration registers and lock ID cycle time	-	4	8(3)	

1. *T_A = 25 °C*
2. *No degradation with aging.*
3. *Maximum duration occurrence is estimated at 1/1000.*

Table 27. AC characteristics

Test conditions specified in Table 18 and Table 19							
Symbol	Parameter		1.6 V ≤ V_{CC} ≤ 2.6 V		2.6 V < V_{CC} ≤ 3.6 V		Unit
			Min.	Max.	Min	Max.	
F_C	Clock frequency		-	40	-	80	MHz
t_{SLCH}	$\overline{S}$ active setup time		5	-	5	-	ns
t_{SHCH}	$\overline{S}$ not active setup time		3	-	3	-	
t_{SHSL}	$\overline{S}$ deselect time		50	-	50	-	
t_{CHSH}	$\overline{S}$ active hold time		5	-	5	-	
t_{CHSL}	$\overline{S}$ not active hold time		5	-	5	-	
t_{CH}(1)	Clock high time		10	-	5.5	-	
t_{CL}(1)	Clock low time		10	-	5.5	-	
t_{CLCH}(2)	Clock rise time		0.1	-	0.1	-	V / ns
t_{CHCL}(2)	Clock fall time		0.1	-	0.1	-	
t_{DVCH}	Data in set-up time		2	-	2	-	ns
t_{CHDX}	Data in hold time		2	-	2	-	
t_{CLHL}	Clock low setup time before $\overline{HOLD}$ active		0	-	0	-	
t_{CLHH}	Clock low setup time before HOLD not active		0	-	0	-	
t_{HLCH}	HOLD active setup time before clock high		5	-	5	-	
t_{HHCH}	HOLD not active time before clock high		5	-	5	-	
t_{SHQZ}(2)	Output disable time		-	8	-	8	
t_{CLQV}(2)(3)	Clock low to output valid	Load 30 pf	-	20(4)	-	11(5)	ns
t_{CLQX}(2)	Output hold time		1	-	1	-	
t_{HHQV}	$\overline{HOLD}$ high to output valid	Load 30 pF	-	25	-	15	
t_{HHQX}(2)	$\overline{HOLD}$ high to output low / high-Z	Load 30 pF	1	-	1	-	
t_{HLQZ}(2)	$\overline{HOLD}$ low to output high-Z		-	8	-	8	
t_{WHSL}	WRITE PROTECT setup time		10	-	10	-	
t_{SHWL}	WRITE PROTECT hold time		10	-	10	-	

1. *t_{CH} + t_{CL} must never be less than the shortest possible clock period that is 1 / $f_{C(max)}$.*
2. *Evaluated by characterization - not tested in production.*
3. *With buffer strength medium (DRV1; DRV0 = 0; 1).*
4. *T_{CLQV} = 30 ns with buffer strength low (DRV1; DRV0 = 1; 0). Evaluated by characterization - not tested in production.*
5. *T_{CLQV} = 15 ns with buffer strength low (DRV1; DRV0 = 1; 0). Evaluated by characterization - not tested in production.*

Figure 37. **Serial input timing**

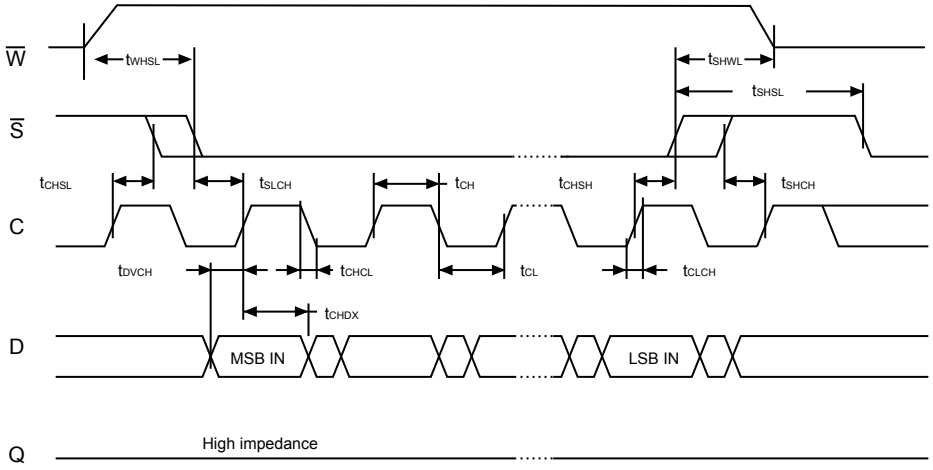


Figure 38. **Hold timing**

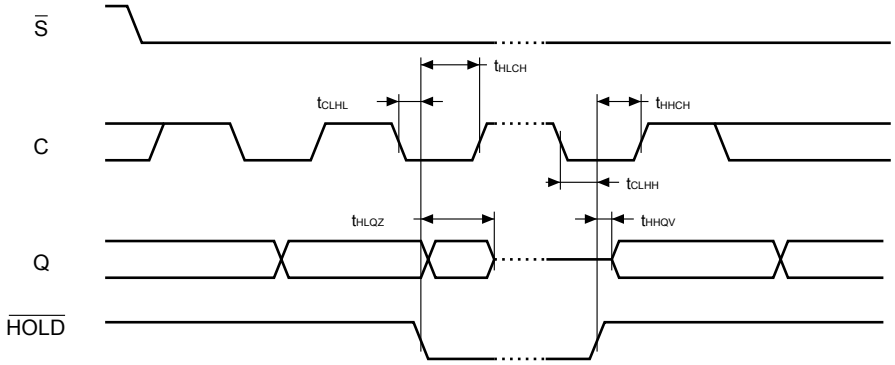
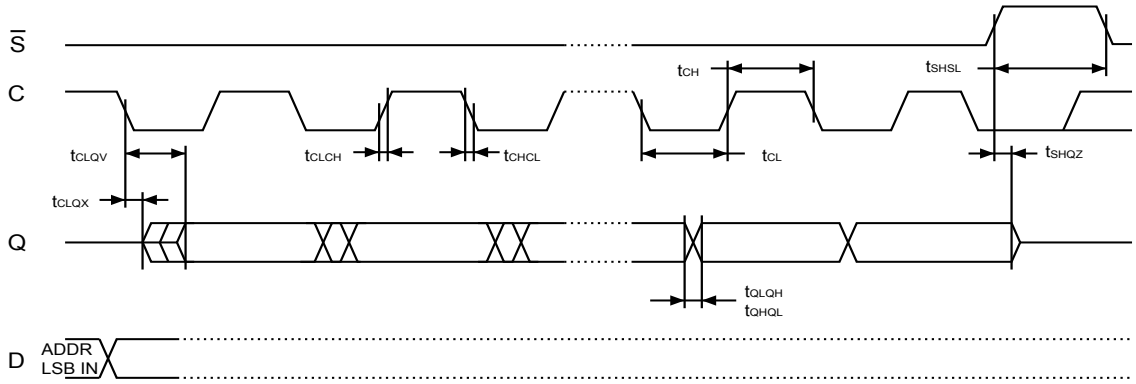


Figure 39. **Serial output timing**



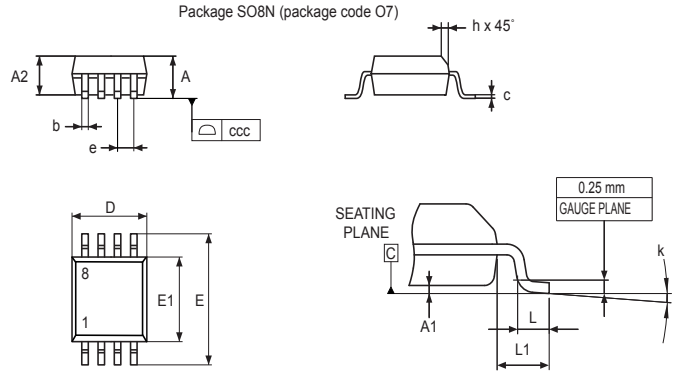
11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 SO8N package information

This SO8N is an 8-lead, 4.9 x 6 mm, plastic small outline, 150 mils body width, package.

Figure 40. SO8N – Outline



1. Drawing is not to scale.

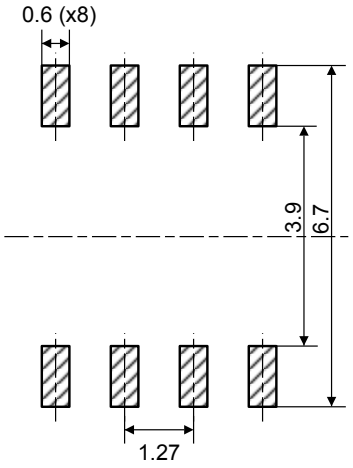
Table 28. SO8N – Mechanical data

Symbol	millimeters			inches (1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.100	-	0.230	0.0039	-	0.0091
D(2)	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1(3)	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side*
3. *Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

Note: The package top may be smaller than the package bottom. Dimensions D and E1 are determinated at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interleads flash, but including any mismatch between the top and bottom of plastic body. Measurement side for mold flash, protusions or gate burrs is bottom side.

Figure 41. SO8N - Recommended footprint

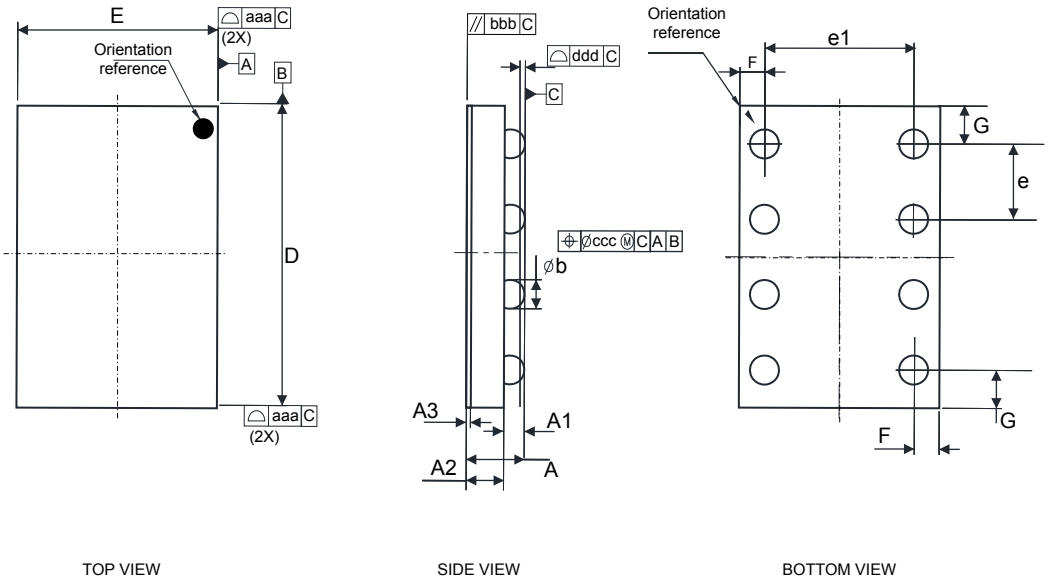


1. Dimensions are expressed in millimeters.

11.2 WLCSP8 package information

This WLCSP is a 8-ball, 2.608 x 1.531 mm, 0.7 x 0.8 mm pitch, wafer level chip scale package.

Figure 42. WLCSP8 - Outline with BSC



1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum C and seating plane are defined by the spherical crowns of the bump.

Table 29. WLCSP8 - Mechanical data

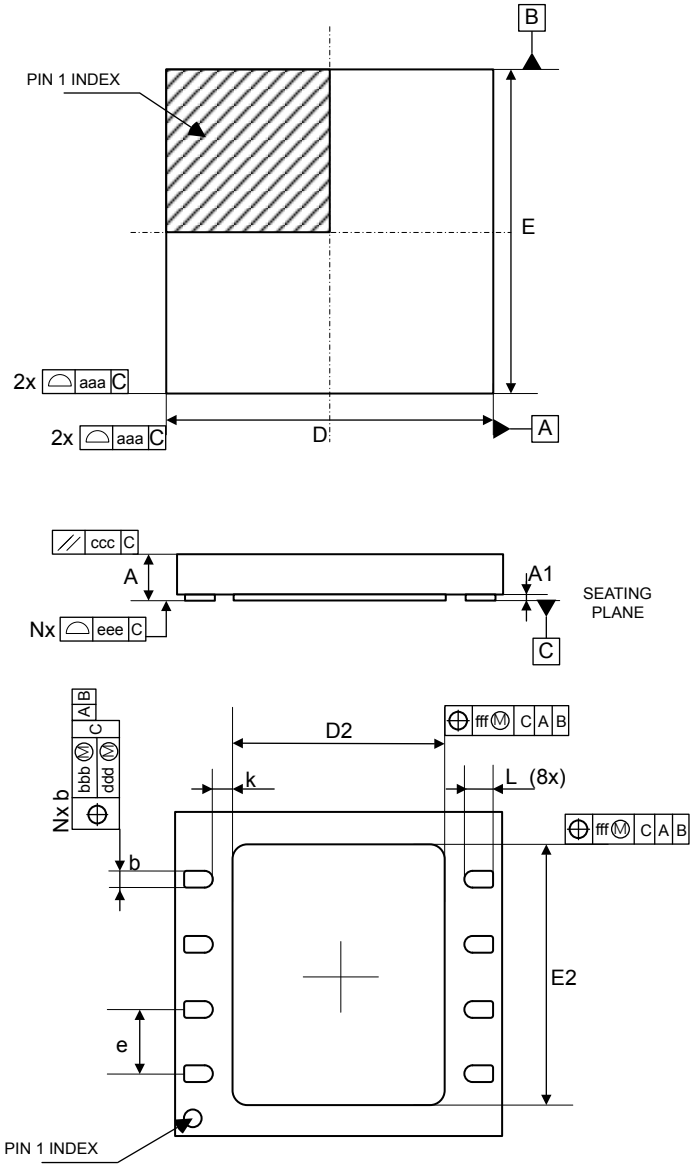
Symbol	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.520	0.550	0.580	0.0205	0.0216	0.0228
A1	-	0.194	-	-	0.0076	-
A2 (including A3)	-	0.355	-	-	0.0140	-
A3	-	0.025	-	-	0.0010	-
b	-	0.268	-	-	0.0105	-
D	-	2.608	2.639	-	0.1027	0.1039
E	-	1.531	1.562	-	0.0603	0.0615
e	-	0.700	-	-	0.0276	-
e1	-	0.800	-	-	0.0315	-
F	-	0.366	-	-	0.0144	-
G	-	0.254	-	-	0.0100	-
aaa	-	-	0.110	-	-	0.0043
bbb	-	-	0.110	-	-	0.0043
ccc	-	-	0.110	-	-	0.0043
ddd	-	-	0.060	-	-	0.0024

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

11.3 UFDFPN8 (DFN8) package information

This UFDFPN is a 8-lead, 4 x 4 mm, 0.8 mm pitch ultra thin profile fine pitch dual flat package.

Figure 43. UFDFPN8 - Outline



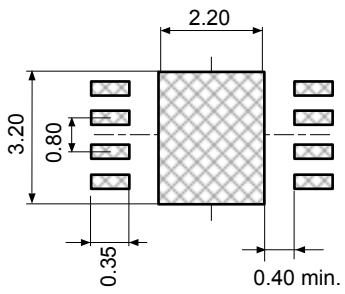
1. Exposed copper is not systematic and can appear partially or totally according to the cross section.
2. Drawing is not to scale.
3. The central pad (the area E2 by D2 in the above illustration) must be either connected to V_{SS} or left floating (not connected) in the end application.
4. Exact shape of the leads at the edge of the package is optional.
5. Dimensions “b” and “L” are measured at terminal plating surface.

Table 30. UFDFPN8 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.45	0.55	0.65	0.0177	0.0217	0.0256
A1[2][3]	0.00	-	0.05	0.000	-	0.0020
b[4][5]	0.20	0.25	0.30	0.0079	0.0098	0.0118
D		4.00 BSC			0.1574	
D2	2.10	2.20	2.30	0.0827	0.0866	0.0905
E		4.00 BSC			0.1574	
E2	3.10	3.2	3.3	0.1220	0.1260	0.1299
e	-	0.80	-	-	0.0315	-
L	0.30	0.35	0.40	0.0118	0.0138	0.0157
k	0.40	-	-	0.0157	-	-
N	8					
aaa[6]	0.15			0.0059		
bbb[6]	0.10			0.0039		
ccc[6]	0.10			0.0039		
ddd[6]	0.05			0.0020		
eee[6]	0.08			0,0031		
fff[6]	0.10			0.0039		

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *A1 is defined as the distance from the seating plane to the lowest point on the package body (standoff).*
3. *Terminal A1 identifier and terminal numbering convention shall conform to JEP95 SPP-002. Terminal A1 identifier must be located within the zone indicated on the outline drawing. Topside terminal A1 indicator may be a molded, or metalized feature. Optional indicator on bottom surface may be a molded, marked or metallized feature.*
4. *Dimension 'b' applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension 'b' should not be measured in that radius area.*
5. *Inner edge of corner terminals may be chamfered or rounded in order to achieve minimum gap "k". This feature should not affect the terminal width "b", which is measured L/2 from the edge of the package body.*
6. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*

Figure 44. UFDFPN8 - Footprint example



1. Dimensions are expressed in millimeters.

12 Ordering information

Table 31. Ordering information scheme

Example	M95	P32-	I	X	MN	T	/E

Device type

M95 = SPI serial access EEPROM

Device function

P32 = 32-Mbit (4 194 304 x 8-bit)

Device Grade

I = Industrial temperature range, -40 °C to 85 °C

E = Extended temperature range, -40 °C to 105 °C

Operating voltage

X = V_{CC} = 1.6 V to 3.6 V

Package(1)

MN = SO8N (150 mil width)

CS = WLCSP8 (13 mil width)

MG = DFN8 (4 x 4 mm)

Option

Blank = tube packing

T = tape and reel packing

Process

/E = Manufacturing technology code

1. *All packages are ECOPACK2 (RoHS-compliant and free of brominated, chlorinated and antimony-oxide flame retardants).*

Note: For a list of available options (speed, package, etc.) or for further information on any aspect of this device, contact your nearest ST sales office.

Note: Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Revision history

Table 32. **Document revision history**

Date	Revision	Changes
15-Jun-2022	1	Initial release.
05-Oct-2022	2	Updated: • Cover image • Section 6.10 Fast read single output with one dummy byte (0Bh) • Section 6.16 Read identification (83h) • Figure 26. Read identification • Figure 27. Fast read identification • Table 17. Absolute maximum ratings • Table 25. DC characteristics - other parameters • Section 11.2 WLCSP8 package information • Section 11.3 UFDFPN8 (DFN8) package information • Table 26. Programming times

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