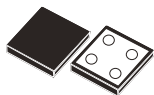


Low input voltage, 200 mA ultra-low noise LDO



Flip-Chip4



SOT23-5L

Maturity status link

[LD56020](#)

Features

- Input voltage from 1.1 V to 5.5 V
- Ultra-low dropout voltage (190 mV max. at 200 mA load)
- Low ground current (18 μ A typ. at no load)
- Output voltage tolerance: $\pm 2\%$ overtemperature, $\pm 1\%$ at 25 °C
- 200 mA guaranteed output current
- Ultra-low output noise: 8.8 μ V_{RMS} (10 Hz to 100 kHz)
- 50 mV output voltage steps (available on request) from 0.6 V to 4.0 V
- Logic-controlled electronic shutdown
- Thermal shutdown
- Output active discharge function
- Packages: Flip-chip4 0.65 x 0.65 mm² and SOT23-5L

Applications

- Smartphones/tablets
- Image sensors
- VCO and RF modules

Description

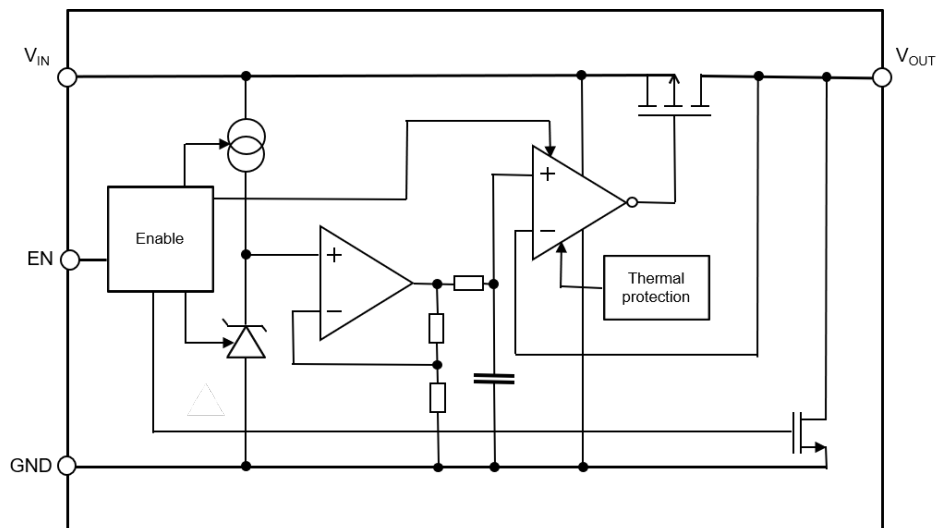
The **LD56020** is a high accuracy voltage regulator which provides 0.2 A of current. It is available in CSP 0.65 x 0.65 mm² package, SOT23-5L, allowing the maximum space saving.

The device is stabilized with a small ceramic capacitor on input and output. The ultra-low drop, low quiescent current and short-circuit current foldback make the **LD56020** suitable for low power battery-operated applications.

An enable logic control function puts the **LD56020** in shutdown mode allowing a total current consumption lower than 0.1 μ A. Thermal protection is also included.

1 Diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin connection

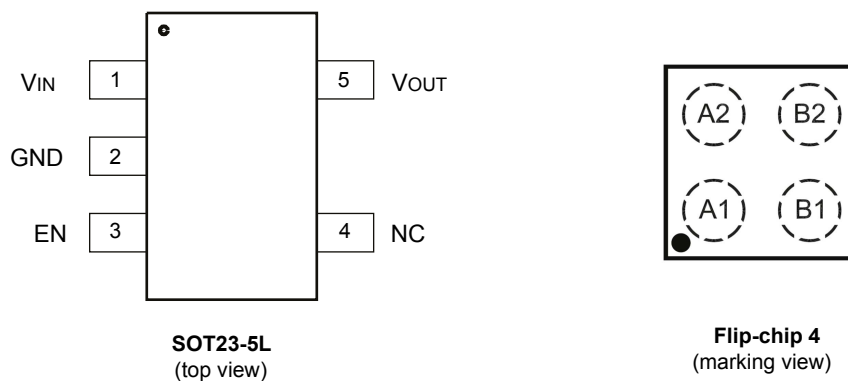
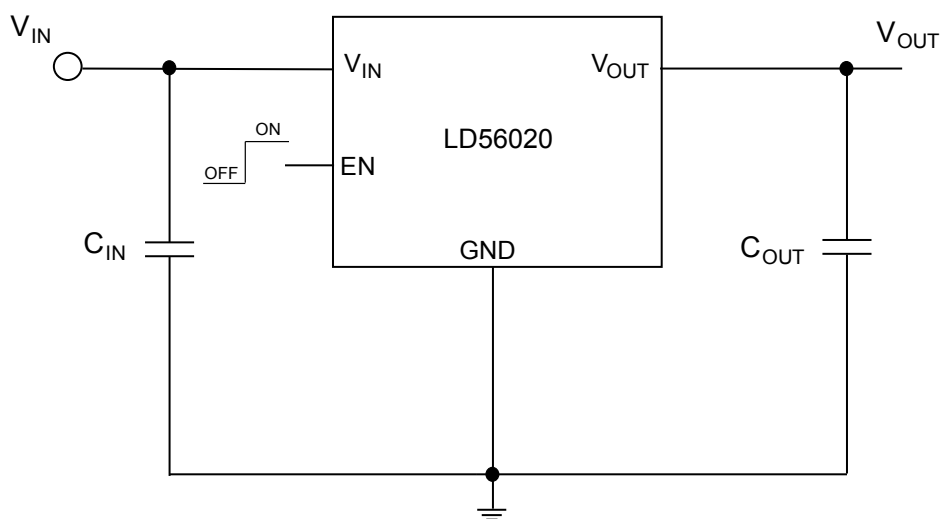


Table 1. Pin description

Symbol	SOT23-5L	Flip-Chip 4	Description
V _{IN}	1	A1	LDO Supply voltage
V _{OUT}	5	A2	LDO Output voltage
GND	2	B2	Ground
EN	3	B1	Enable input: set V _{EN} = high to turn on the device; V _{EN} = low to turn off the device. This pin is internally pulled down via a 1 MΩ resistor
NC	4	-	Not internally connected: can be connected to GND
Exposed pad	-	-	Must be connected to GND.

3 Typical application diagram

Figure 3. Application diagram



4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input supply voltage	- 0.3 to 7	V
V_{OUT}	Output voltage	- 0.3 to 7	V
I_{OUT}	Output current	Internally limited	A
EN	Enable pin voltage	- 0.3 to $V_{IN} + 0.3$	V
PD	Power dissipation	Internally limited	W
ESD	Charge device model	± 1000	V
	Human body model	± 2000	
T_{J-OP}	Operating junction temperature	- 40 to 125	°C
T_{J-MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature	- 55 to 150	°C

Table 3. Thermal data

Symbol	Parameter	Flip-Chip4	SOT23-5L	Unit
R_{thja}	Thermal resistance, junction-to-ambient	210	200	°C/W

5 Electrical characteristics

$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$; $I_{OUT} = 1 \text{ mA}$; $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \mu\text{F}$; $V_{EN} = 1 \text{ V}$; typical values are at $T_J = 25 \text{ }^\circ\text{C}$; min/max values are at $-40 \text{ }^\circ\text{C} \leq T_J \leq 85 \text{ }^\circ\text{C}$, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.1		5.5	V
V_{OUT}	Output voltage accuracy	$V_{OUT(NOM)} + 0.3 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$; $V_{OUT} \geq 1.5 \text{ V}$	-2.0		+2.0	%
		$V_{OUT(NOM)} + 0.3 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$; $V_{OUT} \leq 1.5 \text{ V}$	-30		+30	mV
V_{OUT}	Output voltage range	50 mV steps	0.6		4.0	V
ΔV_{OUT-IN}	V_{IN} Static regulation	$V_{OUT(NOM)} + 0.3 \text{ V} \leq V_{IN} \leq 5.0 \text{ V}$, $I_{OUT} = 1 \text{ mA}$		0.01	0.1	%/V
ΔV_{OUT}	Static load regulation for CSP	$I_{OUT} = 1 \text{ mA}$ to 200 mA		1.5	5	mV
	Static load regulation for SOT 23-5L	$I_{OUT} = 1 \text{ mA}$ to 200 mA		15	20	
V_{DROP}	Dropout voltage	$I_{OUT} = 0.05 \text{ A}$; $V_{OUT} = 1.05 \text{ V}$ $V_{OUT} = 97\%$ of $V_{OUT(NOM)}$		40	90	mV
V_{DROP}	Dropout voltage for CSP	$I_{OUT} = 0.10 \text{ A}$; $V_{OUT} = 1.05 \text{ V}$ $V_{OUT} = 97\%$ of $V_{OUT(NOM)}$		70	130	mV
		$I_{OUT} = 0.11 \text{ A}$; $V_{OUT} = 1.2 \text{ V}$ $V_{OUT} = 97\%$ of $V_{OUT(NOM)}$		60	140	
		$I_{OUT} = 0.2 \text{ A}$; $V_{OUT} = 1.2 \text{ V}$ $V_{OUT} = 97\%$ of $V_{OUT(NOM)}$		110	190	
	Dropout voltage for SOT 23-5L	$I_{OUT} = 0.10 \text{ A}$; $V_{OUT} = 1.05 \text{ V}$ $V_{OUT} = 97\%$ of $V_{OUT(NOM)}$		80	100	mV
		$I_{OUT} = 0.11 \text{ A}$; $V_{OUT} = 1.2 \text{ V}$ $V_{OUT} = 97\%$ of $V_{OUT(NOM)}$		70	150	
		$I_{OUT} = 0.2 \text{ A}$; $V_{OUT} = 1.2 \text{ V}$ $V_{OUT} = 97\%$ of $V_{OUT(NOM)}$		120	200	
eN	Output noise voltage	$V_{OUT(NOM)} = 1.0 \text{ V}$; $V_{IN} = 1.5 \text{ V}$ 10 Hz to 100 kHz, $I_{OUT} = 1 \text{ mA}$		8.8		μV_{RMS}
SVR_{IN}	V_{IN} Supply voltage rejection	$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2 V_{pp}$, Freq = 100 Hz, $I_{OUT} = 20 \text{ mA}$		90		dB
		$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2 V_{pp}$ Freq = 1 kHz, $I_{OUT} = 20 \text{ mA}$		95		
		$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2 V_{pp}$ Freq = 10 kHz, $I_{OUT} = 20 \text{ mA}$		85		
		$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2 V_{pp}$ Freq = 100 kHz, $I_{OUT} = 20 \text{ mA}$		55		
I_Q	Quiescent current	$I_{OUT} = 0 \text{ mA}$		20	25	μA
I_{Q_OFF}	Standby Current	$V_{EN} = \text{GND}$		0.01	1	μA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LIM}	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(NOM)}$	250	300		mA
I_{SC}	Short-circuit current	$V_{OUT} = 0$ (foldback protection)		100	TBD	mA
V_{EN}	Enable input logic low				0.2	V
	Enable input logic high		0.7			
I_{EN}	Enable pin input current	$V_{EN} = 1.1$ V (internal pull-down)		0.2	0.5	μ A
T_{ON}	Turn-on time	$V_{OUT(NOM)} = 1.0$ V		150		μ s
T_{SHDN}	Thermal shutdown			160		$^{\circ}$ C
	Hysteresis			20		

Table 5. Recommended Input and output capacitors

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
C_{IN}	Input capacitance	Stability	0.7	1		μ F
C_{OUT}	Output capacitance		0.7	1	10	
ESR	Output/Input capacitance		5		500	m Ω

6 Typical performance characteristics

The following plots are referred to LD56020 in the typical application circuit and, unless otherwise noted, at $T_A = 25\text{ }^{\circ}\text{C}$

Figure 4. Output voltage vs. temperature ($V_{IN} = 1.4\text{ V}$)

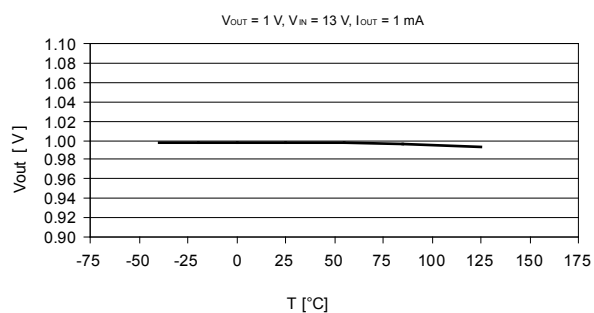


Figure 5. Output voltage vs. V_{IN}

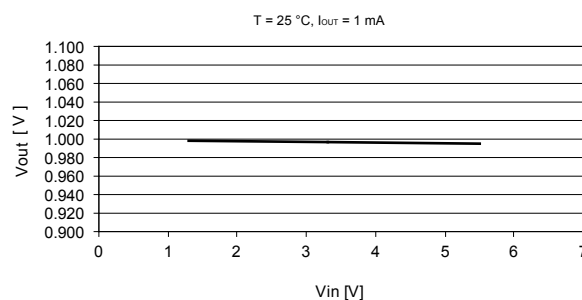


Figure 6. Line regulation vs. temperature

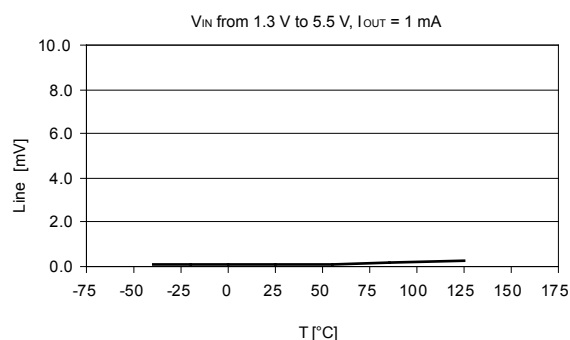


Figure 7. Load regulation vs. temperature

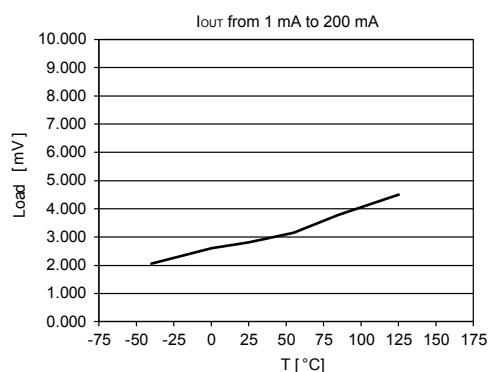


Figure 8. Dropout voltage vs. temperature, ($I_{OUT} = 50\text{ mA}$)

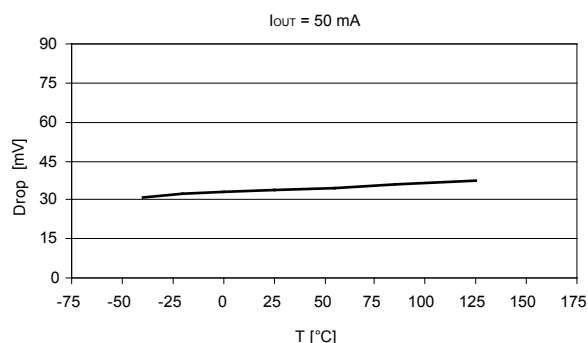


Figure 9. Dropout voltage vs. temperature, ($I_{OUT} = 200\text{ mA}$)

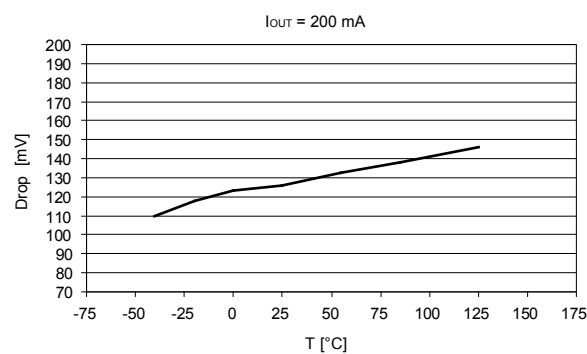


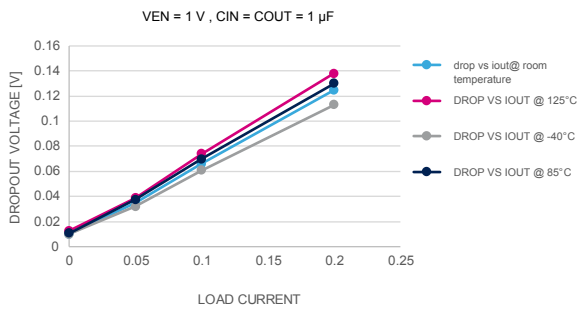
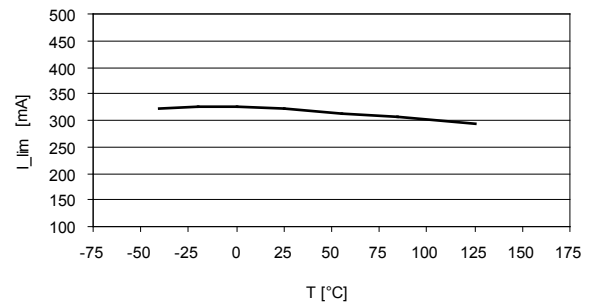
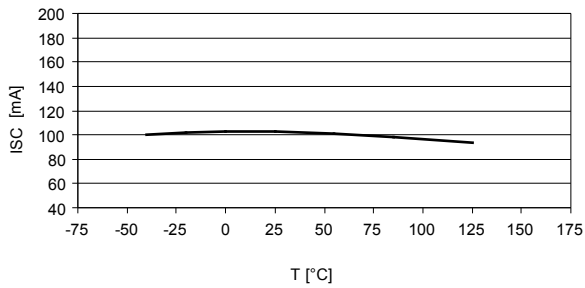
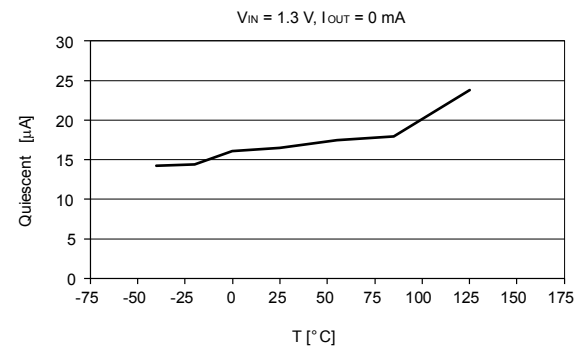
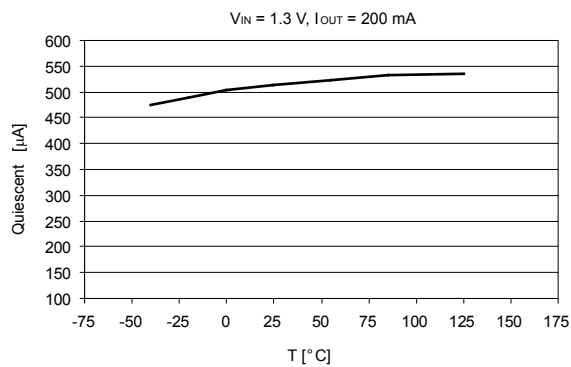
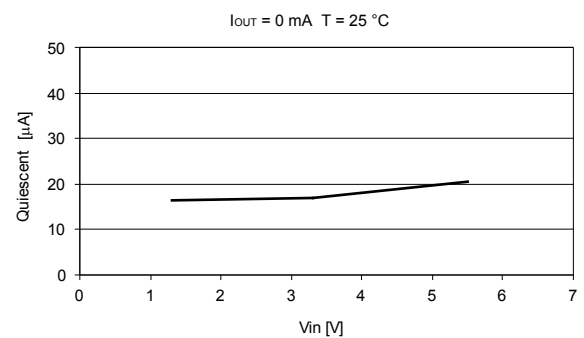
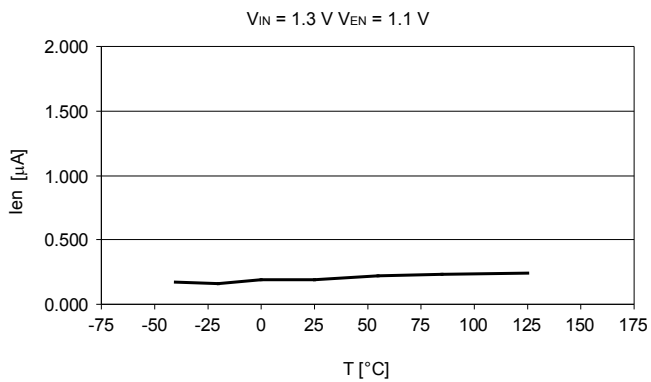
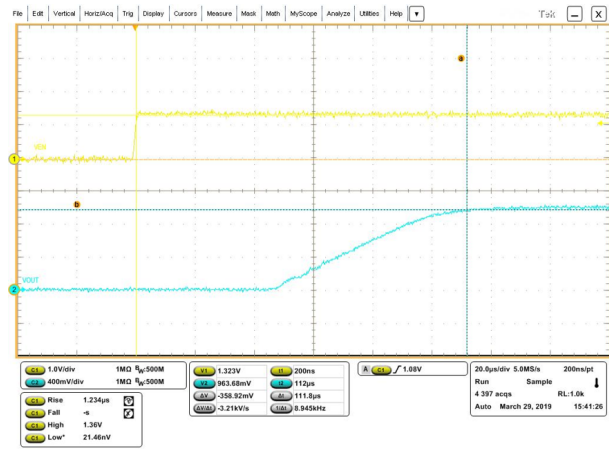
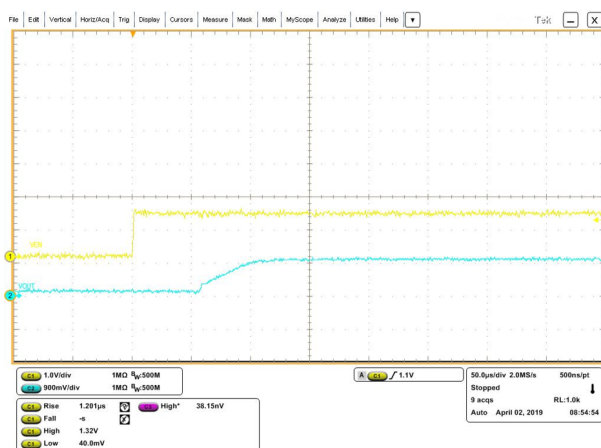
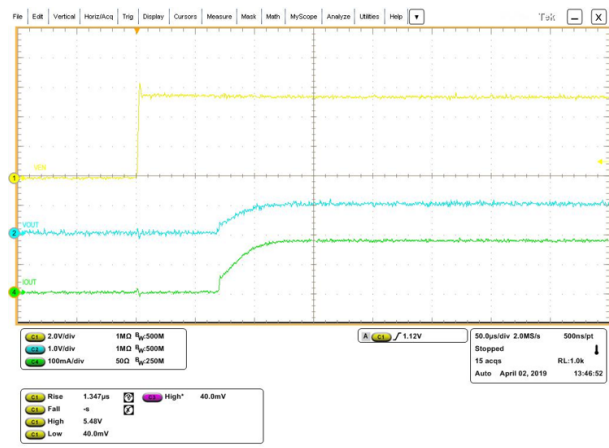
Figure 10. Dropout voltage vs. output current

Figure 11. I_{LIM} vs. temperature

Figure 12. I_{short} vs. temperature

Figure 13. Quiescent current vs. temperature

Figure 14. Quiescent current vs. temperature $I_{OUT} = 200$ mA

Figure 15. Quiescent current vs. input voltage


Figure 16. Enable current vs. temperature

Figure 17. Turn-on time


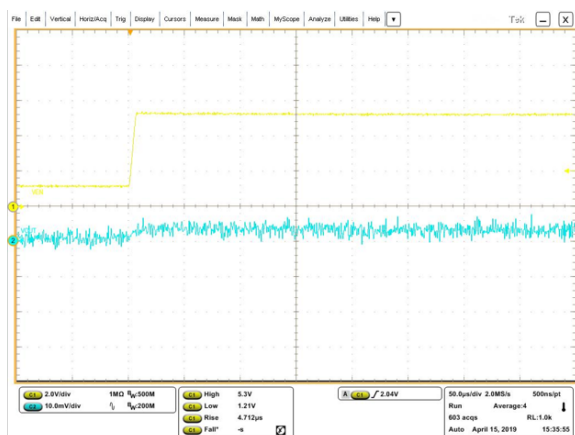
$V_{in} = V_{out(nom)} + 0.3\text{ V}$, V_{en} from 0 to V_{in} , $t_r = t_f = 1\mu s$, $C_{IN} = C_{OUT} = 1\mu F$, $I_{out} = 0\text{ mA}$

Figure 18. Turn-on time $I_{OUT} = 0\text{ mA}$


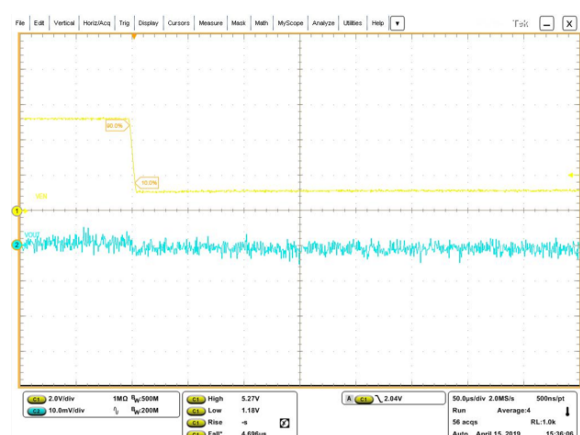
$V_{in} = V_{en}$ from 0 to 1.3 V $t_r = 1\mu s$, $C_{IN} = C_{OUT} = 1\mu F$ $I_{out} = 0\text{ mA}$

Figure 19. Turn-on time $I_{OUT} = 200\text{ mA}$


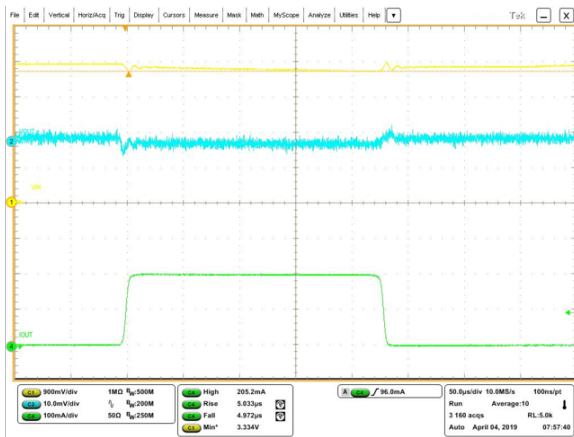
$V_{in} = V_{en}$ from 0 to 5.5 V $t_r = 1\mu s$, $C_{IN} = C_{OUT} = 1\mu F$ $I_{out} = 200\text{ mA}$

Figure 20. Line regulation transient


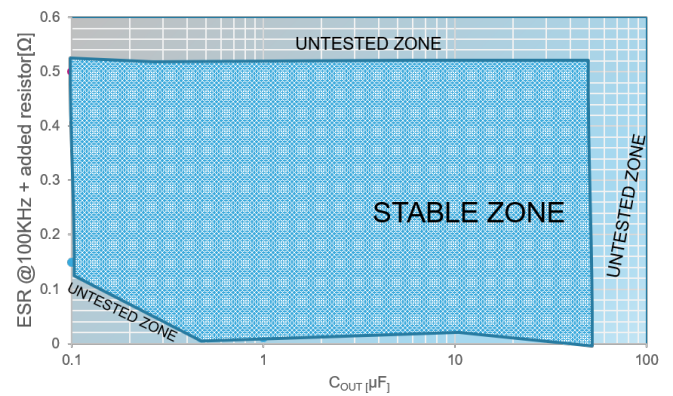
$V_{EN} = 1\text{ V}$ $V_{in} = V_{out(nom)} + 0.3\text{ V}$ to 5.5 V , $t_r = t_f = 5\mu s$ $I_{out} = 1\text{ mA}$ $C_{IN} = C_{OUT} = 1\mu F$

Figure 21. Line regulation transient ($I_{OUT} = 1\mu A$)


$V_{EN} = 1\text{ V}$ $V_{in} = V_{out(nom)} + 0.3\text{ V}$ to 5.5 V , $t_r = t_f = 5\mu s$ $I_{out} = 1\mu A$ $C_{IN} = C_{OUT} = 1\mu F$

Figure 22. Load transient


$V_{EN}=1\text{ V}$, $V_{in}=3.3\text{ V}$, $I_{out}=1\text{ mA}$ to 200 mA , $t_r=t_f=5\text{ }\mu\text{s}$ $C_{IN}=C_{OUT}=1\text{ }\mu\text{F}$

Figure 23. Stability plane


$V_{EN}=1\text{ V}$ V_{in} =from $V_{out}(\text{nom})+0.3\text{ V}$ to 5.5 V I_{out} =from 1 mA to 200 mA , $C_{IN}=1\text{ }\mu\text{F}$

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SOT23-5L package information

Figure 24. SOT23-5L package outline

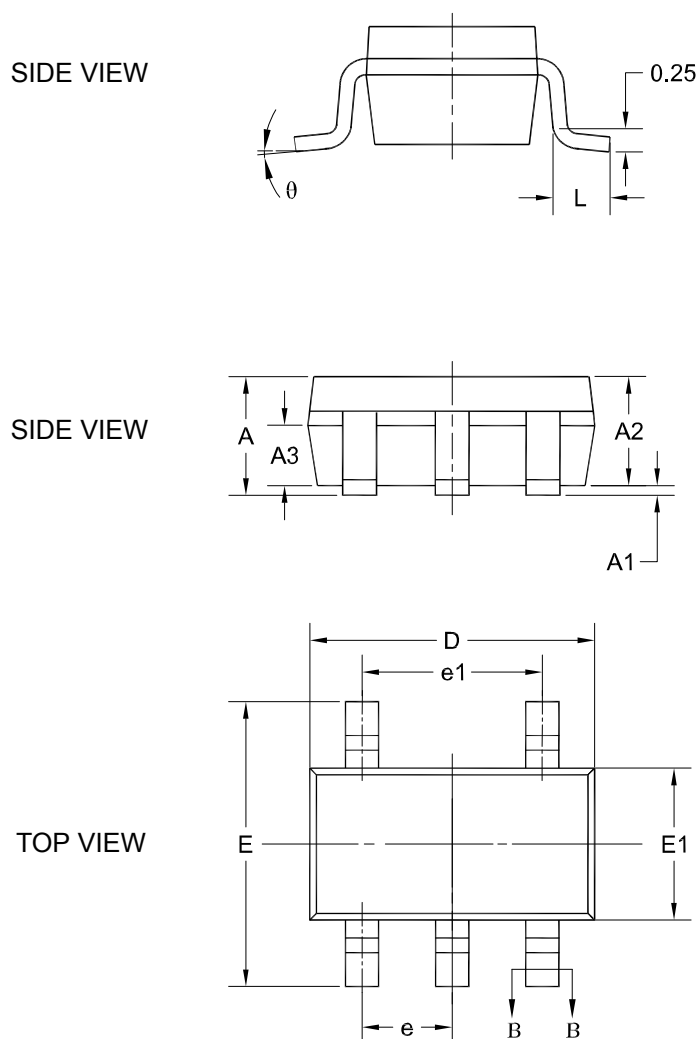
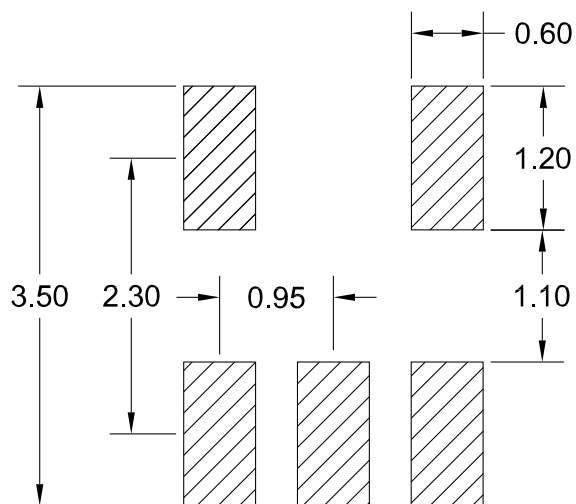


Table 6. SOT23-5L mechanical data

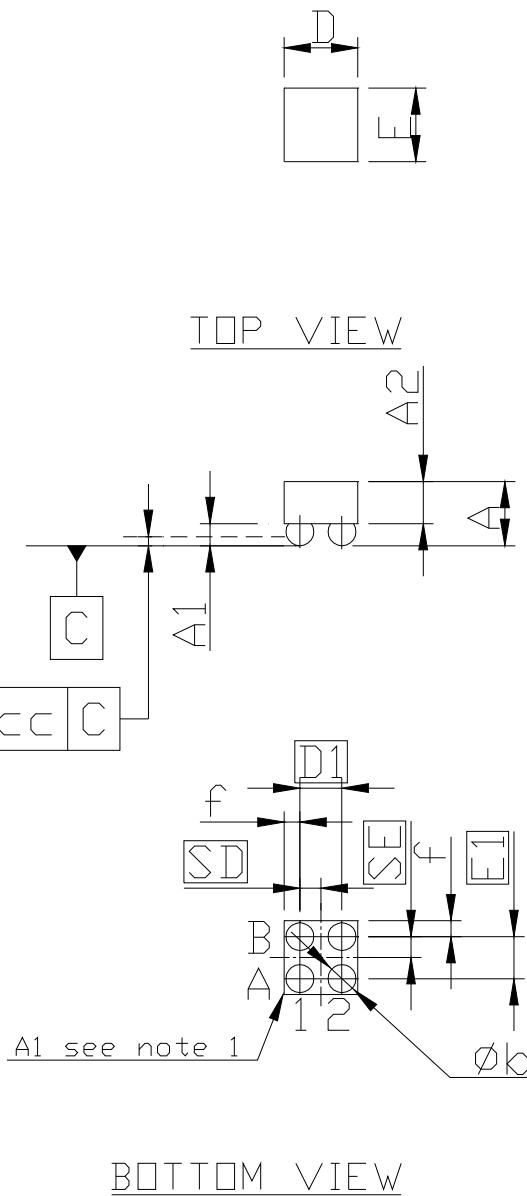
Dim.	mm		
	Min.	Typ.	Max.
A			1.25
A1	0.04		0.10
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33		0.41
b1	0.32	0.35	0.38
c	0.15		0.19
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 CS		
e1	1.90 BSC		
L	0.30		0.60
Θ	0		8°

Figure 25. SOT23-5L recommended footprint



7.2

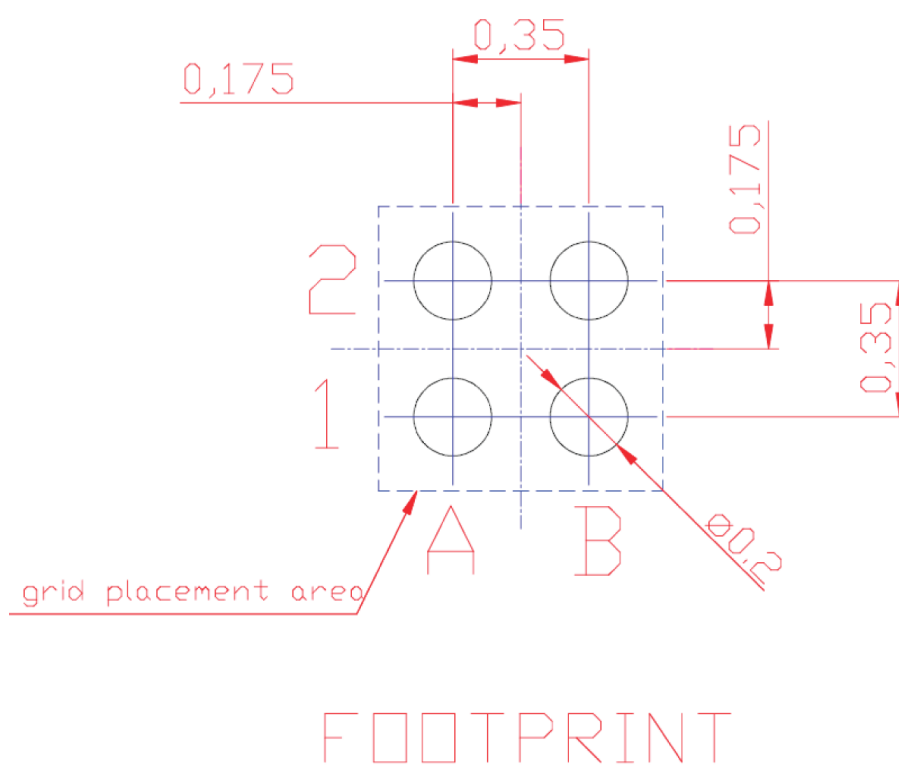
Figure 26. Flip-chip 4 package mechanical outline



8387748 option F

Table 7. Flip-chip 4 mechanical data

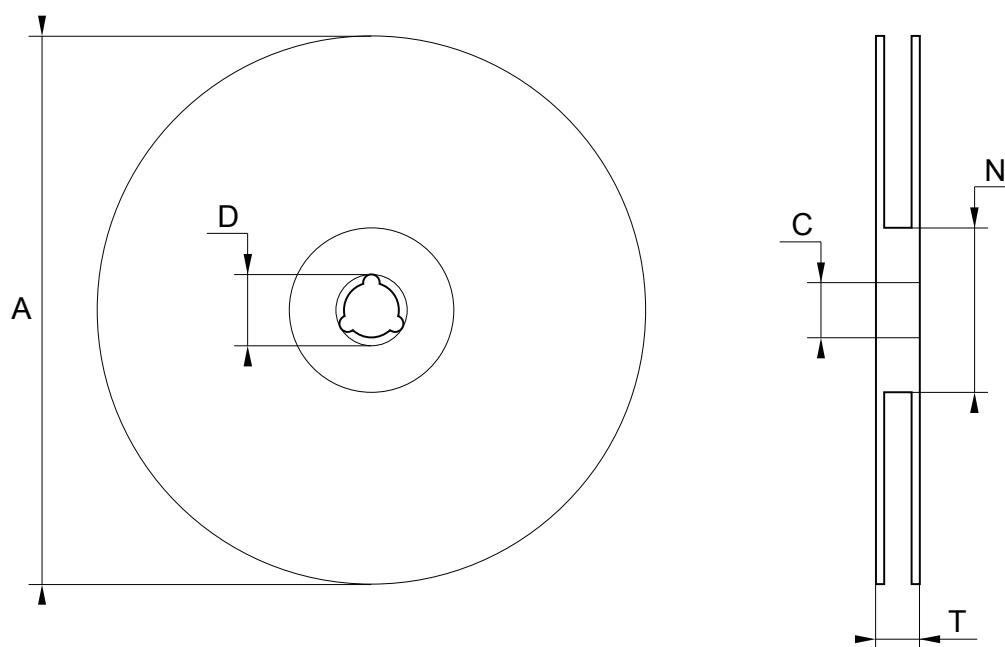
Dim.	mm		
	Min.	Typ.	Max.
A	0.375	0.410	0.445
A1	0.145	0.160	0.175
A2	0.230	0.250	0.270
b	0.189	0.210	0.231
D	0.660	0.690	0.72
D1		0.350	
E	0.660	0.690	0.720
E1		0.350	
SD		0.175	
SE		0.175	
f		0.170	
ccc		0.075	

Figure 27. Flip-chip 4 package footprint


7.3 Flip-chip 4 packing information

Table 8. Reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			180
C	12.8	13	13.2
D	20.2		
N	60		
T			14.4

Figure 28. Reel


Note: Drawing not in scale

Figure 29. Tape drawing

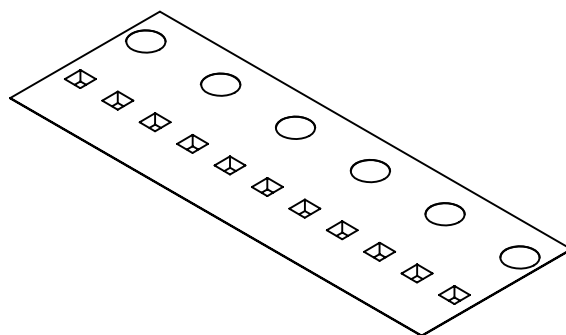
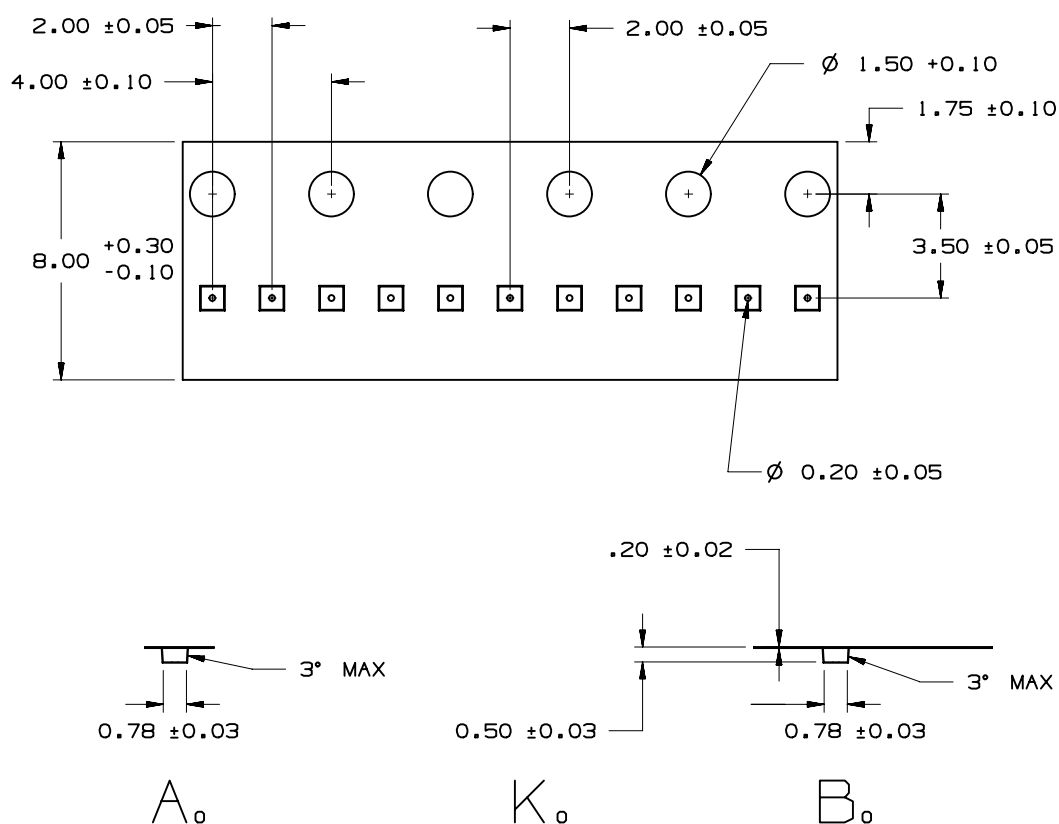
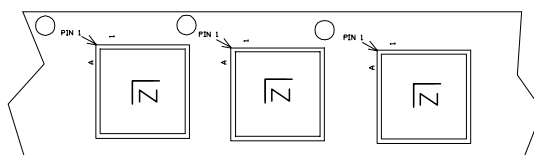


Figure 30. Reel orientation

MARKING VIEW



8 Ordering information

Table 9. Order codes

Order code	Package	Output voltage	Marking	Packing
LD56020M100R	SOT23-5L ⁽¹⁾	1.0 V	TBD	Tape and reel
LD56020M110R		1.1 V	TBD	
LD56020M120R		1.2 V		
LD56020M180R		1.8 V		
LD56020M300R		3.0 V		
LD56020M330R		3.3 V		
LD56020J100R	Flip-Chip4	1.0 V	TBD	Tape and reel
LD56020J110R		1.1 V	TBD	
LD56020J120R		1.2 V		
LD56020J180R		1.8 V		
LD56020J300R ⁽¹⁾		3.0 V		
LD56020J330R ⁽¹⁾		3.3 V		

1. Available on request.

Revision history

Table 10. Document revision history

Date	Revision	Changes
01-Mar-2022	1	Initial release.

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