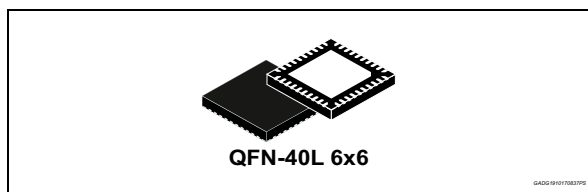


## High power LED driver for automotive applications

Datasheet - production data



### Features

- AEC-Q100 qualified
- General
  - ST SPI communication v4.1
  - 5.5 to 24 V Operating battery voltage range
  - Load dump protected
  - QFN40L 6x6 (wetable flanks) with exposed pad
  - Timeout watchdog and limp home function
  - Low standby current
- Boost Section
  - Fixed frequency architecture, programmable by SPI
  - Peak current mode control
  - Dual phase operation supported
  - Input current limitation
  - Soft start
  - Overvoltage protection (OVP)
  - Short feedback failure protection
  - Constant voltage control
- Buck section
  - Integrated switching mosfets
  - Lossless current sensing without need of external components
  - Very accurate LED current setting programming inductor's peak current and peak-to-peak current ripple
  - Adjustable peak current by SPI
  - Adjustable current ripple by SPI
  - Integrated PWM generation unit with 10-bit resolution and phase shift



- Peak current control
- Constant VLED x TOFF architecture
- Protection and diagnostic
  - Battery under voltage
  - Temperature warning (2 thresholds)
  - Overtemperature shutdown
  - LED voltage digital feedback through SPI
  - Buck outputs short circuit and open load protection

### Applications

- Low Beam
- High beam
- Daytime running light
- Turn indicator
- Position light
- Side marker
- Fog light

### Description

The L99LD21 is a flexible LED driver, which is specifically designed for the control of two independent high brightness LED strings for automotive front lighting applications. It consists of a high efficiency monolithic boost controller and a dual buck converter.

The boost controller integrates a high current gate driver for an external n-channel mosfet. It delivers a constant output voltage, up to 60 V, which supplies the inputs of the two integrated or external buck converters.

The boost controller of two devices can be stacked, in order to operate in dual phase for high power applications, with an interleaving pattern for an improved input current ripple.

The buck converters integrate n-channel mosfet which is driven by a bootstrap circuit.

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# 1 Introduction

The L99LD21 is a monolithic driver IC, which controls the current of two independent high power LED strings, whose forward current and voltage can reach up to 1.5 A (average) and up to 50V respectively.

This device has been designed with dedicated functions, in order to fulfill the stringent requirements of automotive front lighting applications.

The device offers a high level of flexibility, without any change of the external components, thanks to its programmability through the ST SPI interface. This feature support generic platform approaches, which require a software configurability of several parameters. This robust interface, offers a detailed diagnostic of the device itself, as well as of the controlled LED strings.

As the device potentially controls safety critical functions such as low beams and turn indicators, built-in features are integrated in order to support a high level of functional safety. The L99LD21 features a timeout watchdog, a monitoring of the watchdog counter, a limp home function and a direct input. The ST SPI protocol takes into account FMEA case.

The device consists of a boost controller, which controls the PWM of an external n-channel mosfet and provides a stabilized voltage ( $V_{\text{BOOST}}$ ). The input of the boost stage must be connected to the battery voltage through a reverse polarity protection.

The boost controllers of two L99LD21 can be combined to form a dual-phase, interleaved boost controller. Special care has been taken for the current balancing between the different phases and for the switching activity of the boost mosfets with 180° phase shift.

The output of the boost controller supplies the input of the two independent integrated buck converters, or any other external buck converters, whose input voltage is compatible with  $V_{\text{BOOST}}$ . The integrated buck converters are based on constant off-time architecture (for a given LED output voltage) and control the peak current and the peak-to-peak current ripple of their respective inductors.

Operating in continuous conduction mode, the average of each LED string's current, which is connected to the output of each buck converter, is tightly controlled.

This architecture, which consists of cascaded boost and buck stages (see [Figure 2](#)), allows the control of a wide range of LED strings, whose forward voltage is independent from the battery voltage.

With the aim of ensuring a wide operating inductor current range, the Buck mosfets can be set in low or high  $R_{\text{DS\_ON}}$  modes, so that two different inductor peak current ( $I_{\text{LX\_PEAK}}$ ) ranges [0.179 A ÷ 0.849 A] or [0.362 A ÷ 1.695 A] can be selected.

The average LED current is controlled by setting the inductor's peak current and peak-to-peak current ripple. Sensing of the peak current is integrated, not requiring any external shunt resistance, which saves cost and reduces the power dissipation.

Buck n-channel mosfet  $R_{\text{DS\_ON}}$  value depends on the operative conditions as junction temperature, Input voltage and LED string current. For example, at  $V_{\text{Buckin}} = 45 \text{ V}$ ,  $I_{\text{led}} = 700 \text{ mA}$ ,  $T_j = 25 \text{ °C}$  the maximum  $R_{\text{DS\_ON}}$  is 400 mΩ (low  $R_{\text{DS\_ON}}$  mode).



## 1.1 Typical application

Figure 1. Functional block diagram

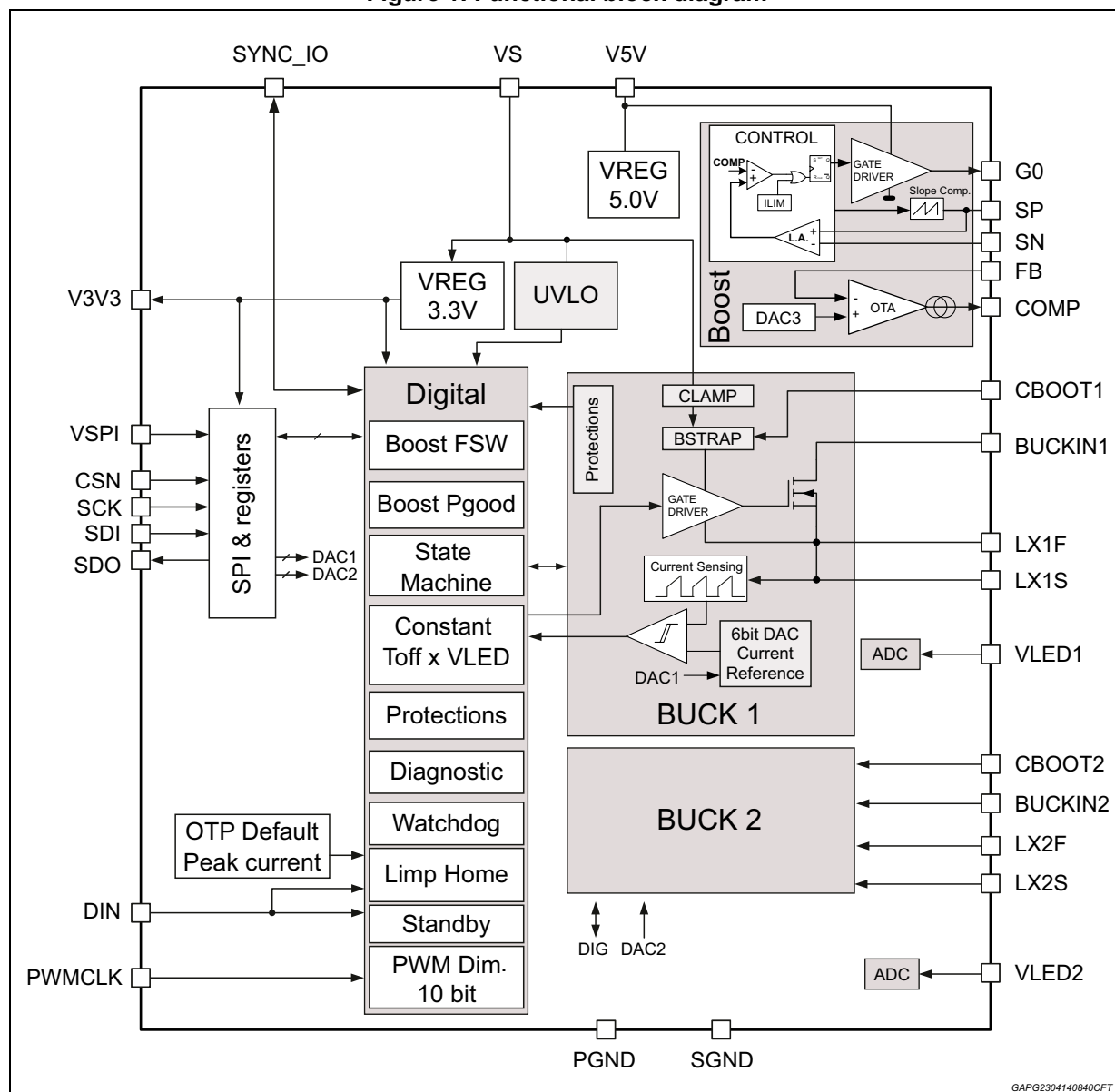


Figure 2. Typical application schematic

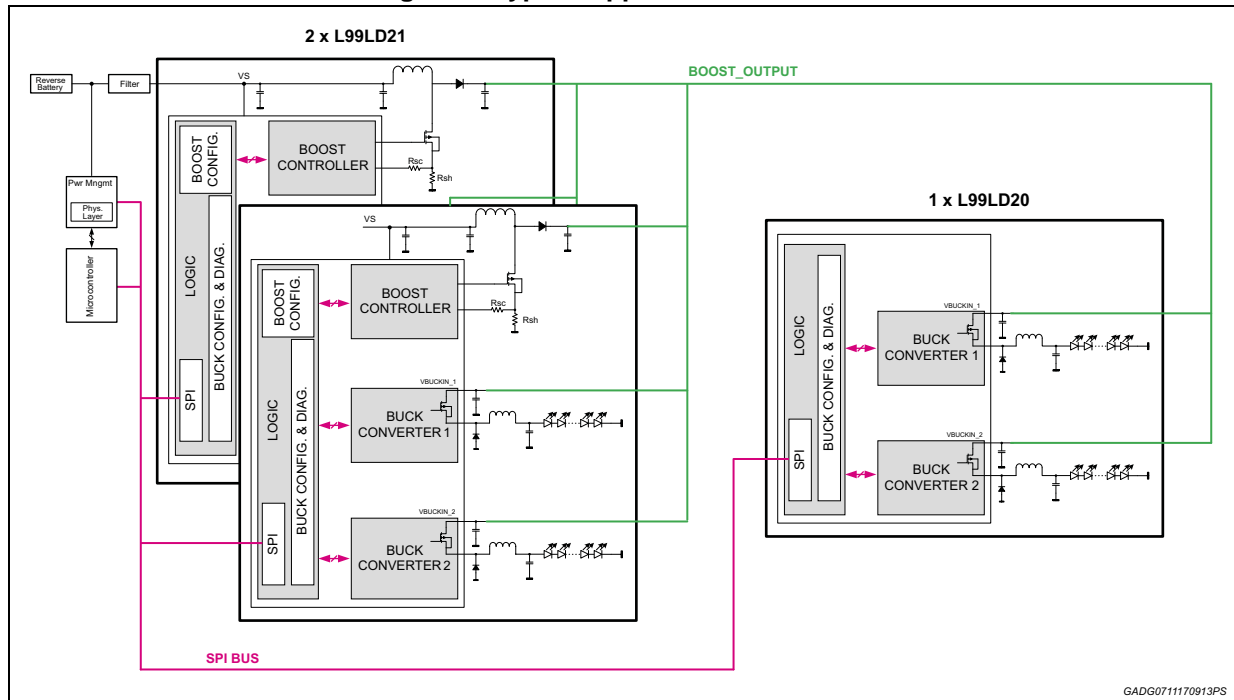


Figure 3. Application diagram

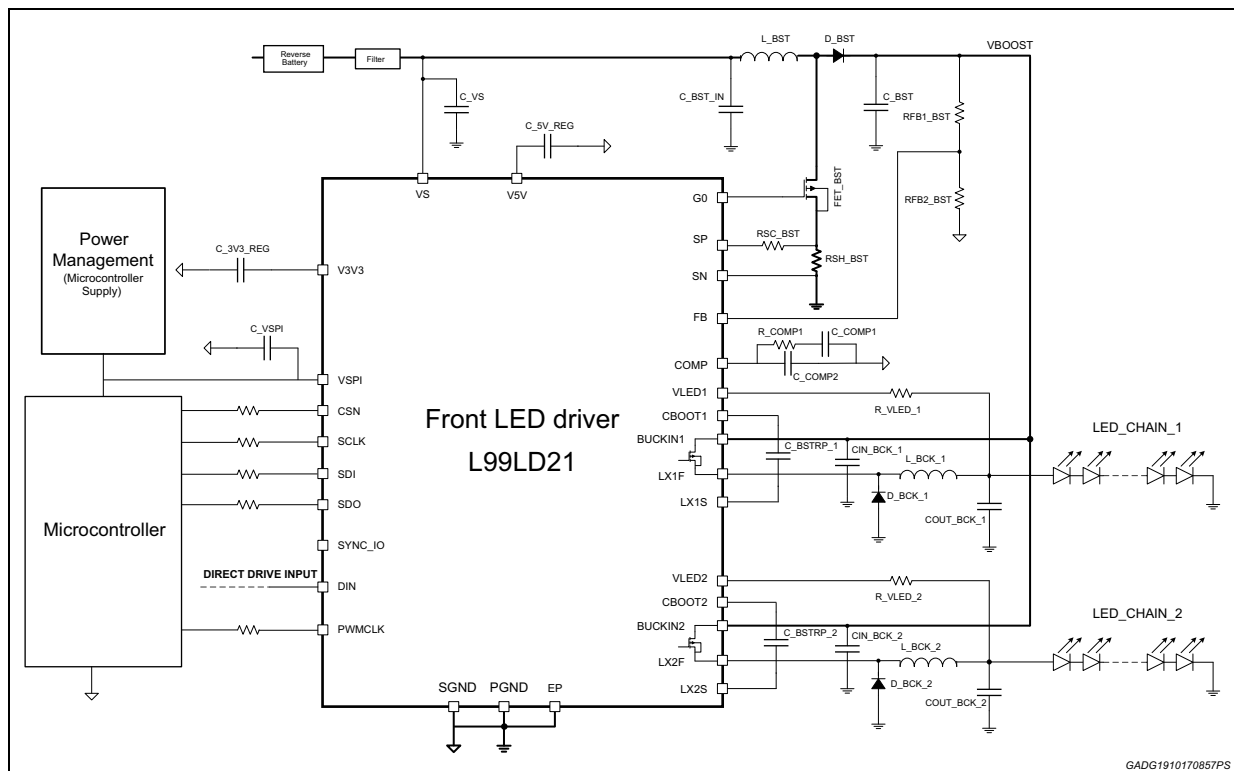


Figure 4. Connection diagram

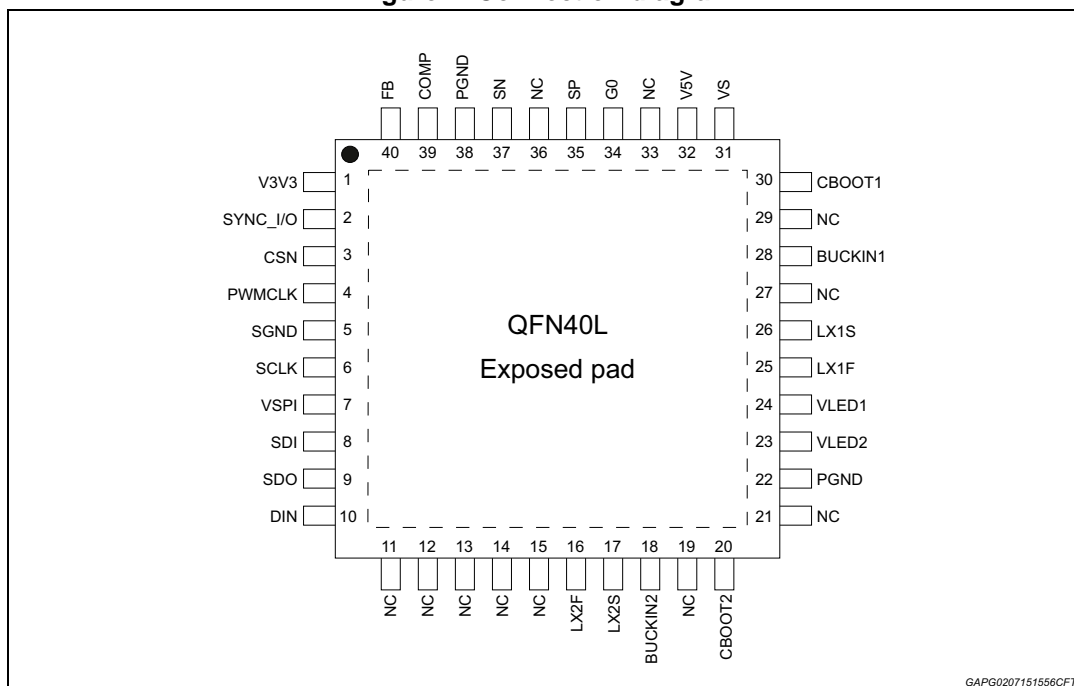


Table 1. Pin functionality

| Pin # | Name     | Function  |
|-------|----------|---|
| 1     | V3V3     | Output of the 3.3 V regulated internal supply. Connect a low ESR capacitor (4.7 $\mu$ F) close to this pin.   |
| 2     | SYNC_I/O | Boost synchronization Input or Output. This pin generates the clock signal for synchronizing another L99LD21 Boost in dual phase configuration.   |
| 3     | CSN      | Chip Select Not (active low) for SPI communication. It is the selection pin of the device. It is a CMOS compatible input.   |
| 4     | PWMCLK   | Clock input for the internal PWM dimming generator.   |
| 5     | SGND     | Signal Ground connection.   |
| 6     | SCK      | Serial Clock for SPI communication. It is a CMOS compatible input.  |
| 7     | VSPi     | Connection to external 3.3 V or 5 V supplies voltage.<br>The external supply powers SPI interface and the I/O signal pins to the microcontroller. It is suggested to connect 100nF capacitor close to this pin. |
| 8     | SDI      | Serial Data Input for SPI communication. Data is transferred serially into the device on SCK rising edge.   |
| 9     | SDO      | Serial Data Output for SPI communication. Data is transferred serially out of the device on SCK falling edge.   |
| 10    | DIN      | Direct input pin.   |
| 16    | LX2F     | Connection to the switching source node of the buck2. This pin must be connected to external free-wheeling diode.   |

Table 1. Pin functionality (continued)

| Pin #   | Name    | Function   |
|---|---------|--|
| 17  | LX2S    | Kelvin connection to the switching source node of the buck2. This pin has to be connected to external bootstrap capacitance. |
| 18  | BUCKIN2 | Connection to the input of the buck channel 2  |
| 20  | CBOOT2  | Connection to the bootstrap capacitor (100nF) of the buck channel 2.   |
| 22, 38  | PGND    | Power Ground connection.   |
| 23  | VLED2   | Connection to the anode of the LED string for read back of the forward voltage of the channel 2.                             |
| 24  | VLED1   | Connection to the anode of the LED string for read back of the forward voltage of the channel 1.                             |
| 25  | LX1F    | Connection to the switching source node of the buck1. This pin must be connected to external free-wheeling diode.            |
| 26  | LX1S    | Kelvin connection to the switching source node of the buck1. This pin has to be connected to external bootstrap capacitance. |
| 28  | BUCKIN1 | Connection to the input of the buck channel 1.   |
| 30  | CBOOT1  | Connection to the bootstrap capacitor (100 nF) of the buck channel 1.  |
| 31  | VS      | Input supply pin of the IC. Connect VS to the battery voltage.   |
| 32  | V5V     | Output of the 5V regulated internal supply. Connect a low ESR capacitor (4.7 $\mu$ F) close to this pin.                     |
| 34  | G0      | Output of the boost gate driver for the external switching mosfet.   |
| 35  | SP      | Positive connection to the boost shunt resistor, in series to the boost switching mosfet.                                    |
| 37  | SN      | Negative connection (Ground) to the boost shunt resistor, in series to the boost switching mosfet.                           |
| 39  | COMP    | Output of the error amplifier of the boost controller. Connect the compensation network between this pin and SGND.           |
| 40  | FB      | Boost output voltage feedback. Connect the FB pin to the boost output voltage, via a resistor divider.                       |
| 11, 12, 13,<br>14, 15, 19,<br>21, 27, 29,<br>33, 36 | NC      | Not connected  |

## 2 Boost controller

### 2.1 General description

The L99LD21 integrates one boost controller, which is based on a fixed frequency, peak current mode architecture. It drives the gate of an external n-channel mosfet in order to step up the VS input voltage to a higher stabilized output voltage.

### 2.2 Frequency selection

The boost controller operates at a fixed frequency which can range from 100 kHz to 450 kHz. The switching frequency is set by a SPI control register (CR#3<9:7>, see [Section 5.4: Registers description](#)).

### 2.3 Output voltage setting

The control loop regulates the voltage at the FB pin to a reference voltage, which value, according table 2, is configurable by the control register CR#3<11:10> (see [Section 5.4: Registers description](#)). Connect the resistor divider tap, top and bottom respectively to the FB pin, to output of the boost controller and to the bottom to SGND.

The resulting boost output voltage is given by:

$$V_{\text{BOOST}} = V_{\text{FB\_REF}}[b_1, b_0] \cdot \left[ 1 + \frac{R_1}{R_2} \right]$$

**Table 2. Reference voltage configuration**

| b1 | b0 | V <sub>FB_REF</sub> [V] |
|----|----|-------------------------|
| 0  | 0  | 0.596                   |
| 0  | 1  | 0.895                   |
| 1  | 0  | 1.242                   |
| 1  | 1  | 1.496                   |

### 2.4 Overvoltage protection

The peak current mode requires a minimum on-time, because of the noise generated right after the turn-on of the switching mosfet. At light load (very low output current), this minimum on-time, in combination with the selected switching frequency is no longer able to regulate the output voltage to the requested voltage. The device enters in overvoltage protection (OVP), in order to prevent an excessive rise of the boost output voltage above the target voltage.

This mode is activated when the voltage on FB pin is higher than the selected internal reference voltage of a specified threshold value ( $V_{FB\_OV\_ON}$ ).

The switching activity is resumed as soon as the voltage on FB pin decreases to the selected internal reference voltage ( $V_{FB\_REF[xx]}$ ).

In case of FB voltage increases above  $V_{FB\_OV\_ON}$ , an output digital flag, called BST\_OVP, is set.

As soon as feedback voltage decreases down to target value ( $V_{FB\_REF[xx]}$ ), the bit is reset after  $t_{BST\_OVP\_RST}$  delay time. This delay time is implemented in order to eliminate the diagnostic ambiguity (toggling of the OVP flag) during permanent no load / light load operation.

BST\_OVP bit is not set in case of boost disabled or boost feedback failure.

## 2.5 Feedback failure protection

L99LD21 is protected in case of boost controller feedback pin failure. More in detail, a specific bit, called BST\_FB\_FAIL, is set in case of feedback pin is shorted to ground.

When this bit is set:

- If device is OFF, boost controller does not start;
- If device is ON in single phase configuration, boost controller is immediately switched OFF;
- If device is ON in dual phase configuration and it is in Active mode: both boost controllers are switched off when the failure is recognized on Master side; only Slave controller is switched off when the failure is recognized on Slave side while the Master is managed by the microcontroller;
- If device is ON in dual phase configuration and it is in Limp Home: both boost controllers are switched off when the failure is recognized on Master side; only Slave controller is switched off when the failure is recognized on Slave side, while the Master is forced to work at minimum duty cycle.

The reset of FB failure bit is demanded to the microcontroller (in Active mode) or to an auto-restart function (in Limp Home) that cyclically clears this bit with a period equal to  $t_{AUTORESTART}$ .

This bit is not set if L99LD21 internal boost controller is not used (in this case, BST\_DIS bit is set).

If left floating, feedback pin will be pulled up internally. In this case, BST\_OVP bit will be set permanently and boost gate driver will be permanently off. Since the feedback pin voltage is in any case high, N\_PWR\_GOOD flag is reset in such condition and shall be ignored.

*Note:* Setting this bit doesn't imply any action on buck converters.

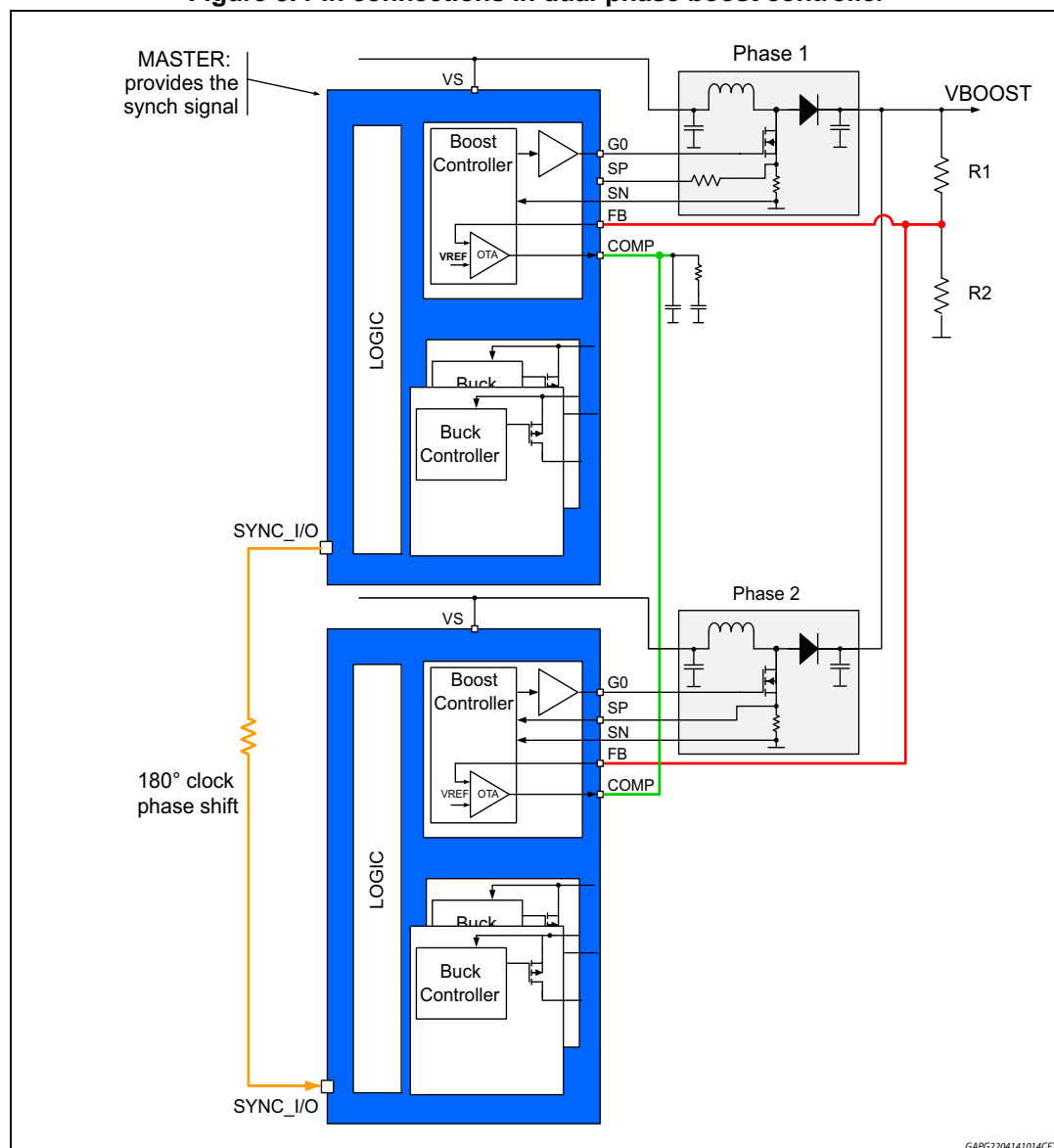
## 2.6 Operation in dual phase interleaved mode

It is possible to combine the boost controllers of two L99LD21, for high power applications, in dual phase configuration. In this configuration, the switching mosfets of the boost controllers are driven at 180° out of phase. By sharing the current between two phases, the conduction losses (which are proportional the square of the conducted current) are reduced and the efficiency of the boost stage increases, in comparison to a single-phase.

The effective switching frequency is doubled and the ripple cancellation effect results in a reduction of the input and output current ripple. This allows small input and output capacitances.

For an operation in dual-phase configuration, FB, COMP and SYNC\_I/O pins must be respectively connected together as shown in [Figure 5](#).

**Figure 5. Pin connections in dual-phase boost controller**



One of the L99LD21 must be configured as the master and the other device must be configured as the slave (see bit <1> on [Table 15: CR#2: Control Register 2](#)). The SYNC\_I/O of the master acts as an output, whilst the slave one respectively as an input. The master boost provides a clock signal to the slave, in order to achieve an interleaved switching activity of the slave boost controller, which is 180° out of phase to that of the master.

For a proper current balancing between the boost phases, the shunt resistors, which are placed in series to the source of the mosfets, and the inductors, must be identical.

## 2.7 Soft start

The L99LD21 features an internal soft start function, which gradually increases the boost mosfet current limit in 8 steps, in order to avoid a voltage overshoot of the boost output. The threshold of the current limitation reaches its nominal value after a specified soft start time ( $t_{SS}$ ).

A soft-start phase is initiated at the activation of the boost controller:

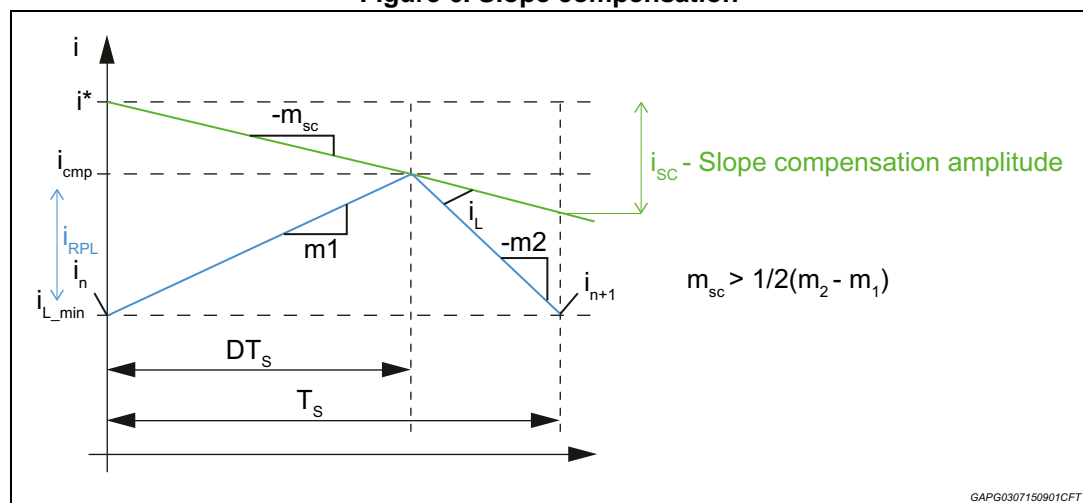
- after leaving standby mode;
- after deactivation of the boost controller due to a VS under voltage;
- after a previous de-activation of the boost by SPI (see bit <1> on [Table 16: CR#3: Control Register 3](#));
- after deactivation of the boost controller due to a BST\_FB\_FAIL.

## 2.8 Slope compensation

Slope compensation is needed to ensure loop stability with all possible values of duty cycle:  $D = T_{ON} / T$  ( $0 < D < 1$ ) especially when duty cycle is greater than 0.5. The slope of the additional ramp is proportional to converter inductor current slope during the turn off phase.

The L99LD21 generates an internal peak current value,  $I_{SLOPE}$ , which is added to the sensing signal at the output of the OTA. The percentage of slope compensation is achieved by choosing a proper value of the  $R_{SC}$  resistor (see [Figure 2](#) for  $R_{SC}$  resistor proper connection).

Figure 6. Slope compensation



## 2.9 Operation together with the buck converters

Right after a power on reset (POR) of the device or after a fault event leading to a latch-off of the boost controller (VS under voltage), a soft start phase is initiated and the boost is activated.



The buck converters activation depends on device status (see [Section 4.1: Operating modes](#)):

- Active mode: in this case, bucks are immediately operative. Their status will depend on DINMAP register configuration (see [Section 4.2.1](#));
- Limp Home:
  - we have to distinguish two different cases:  
Boost Enabled with output voltage higher than 92.5% of final target value. In this case, buck converters are immediately operative according to DIN\_MAP register configuration;  
Boost Disabled or Enabled with output voltage lower than 92.5 % of final target value. In this case, the buck converters are kept disabled for a specified time delay ( $t_{\text{DELAY}}$ ) independently from DINMAP status. Once this time elapses, bucks are operative according to DINMAP register configuration.

On the other hand, when boost and bucks are active and a VS undervoltage fault event occurs, buck converters are immediately disabled while the boost is kept alive for  $t_{\text{DELAY}}$  before being switched off.

## 3 Buck converters

### 3.1 General description

The L99LD21 features two independent buck converters with integrated switching mosfets with forward peak current as high as specified maximum  $I_{Lx\_PEAK}$  (where x indicates Buckx peak current) 1.695 A. They are optimized to deliver a constant current to LED strings.

The  $R_{DS\_ON}$  of the n-channel mosfets can be set programming the appropriate bit in the control register (see bits <3:2> on [Table 14: CR#1: Control Register 1](#)): high  $R_{DS\_ON}$  mode (only one half power stage enabled) or low  $R_{DS\_ON}$  mode (both half power stages enabled).

This feature allows having two different inductor peak current ranges, 0.179 A ÷ 0.849 A or 0.362 A ÷ 1.695 A, respectively for high  $R_{DS\_ON}$  and low  $R_{DS\_ON}$  mode, so achieving the highest of current sense accuracy in the whole current range.

The buck converters are based on constant off-time architecture, which regulates the peak current in each inductor. The monitoring of the inductor peak current is done through integrated senseFETs. This results in a lossless high side current sensing, which does not require any external shunt resistor, and improves the system efficiency.

This architecture provides an inherent cycle-by cycle current limitation and a fast transient response, without any compensation of the control loop.

The average LED current in each LED string is configurable by the SPI, through configuration of the inductor peak current and peak-to-peak current.

The dimming of the LED strings can be realized through the direct input pin (DIN) or through the internal 10-bit PWM dimming generator.

### 3.2 Bootstrap circuit

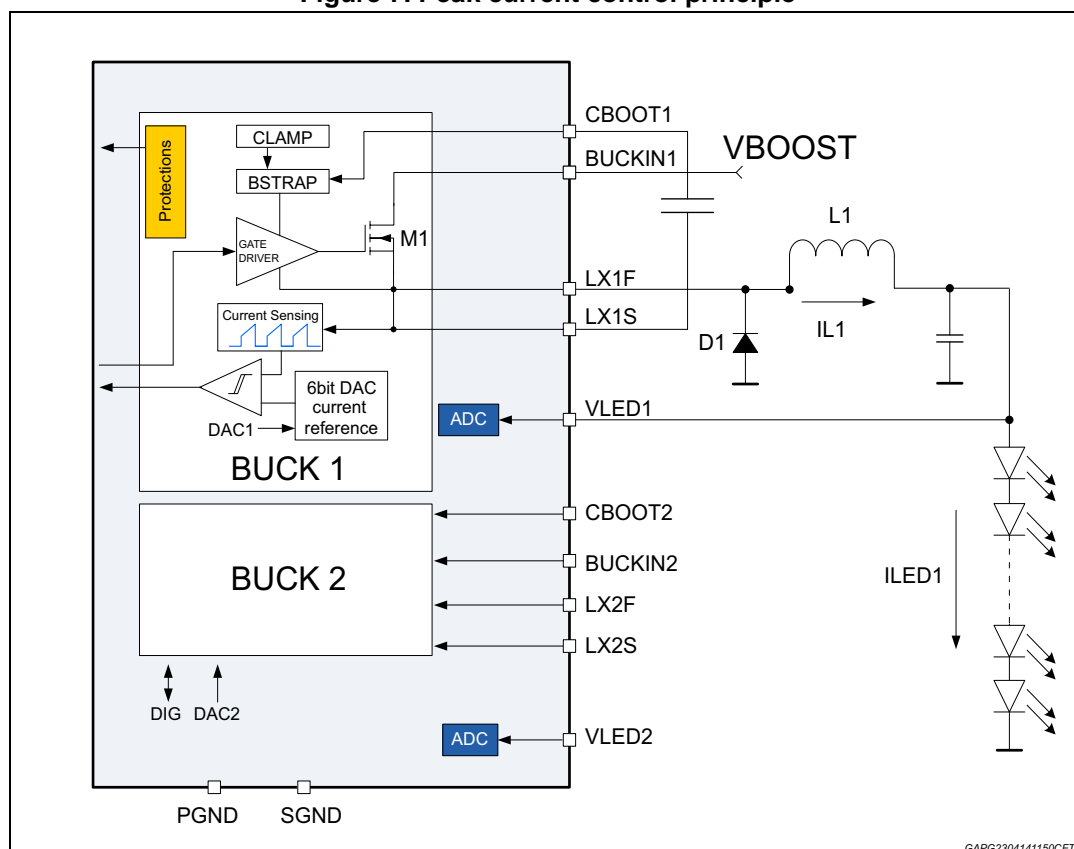
The L99LD21 has built-in high side n-channel switching mosfets, which are driven by gate drivers. Each gate driver uses a bootstrap circuit, consisting of an integrated diode and an external capacitor between the LX1S and CBOOT1 pins, respectively between the LX2S and CBOOT2 pins.

The buck converters impose a minimum off-time ( $T_{OFF\_MIN}$ ) to ensure that the bootstrap capacitor recharges every cycle to a voltage which avoids the switching mosfet to operate in linear mode.  $T_{OFF\_MIN}$  restricts the maximum duty cycle of the buck converters for a given switching frequency. This effect is more pronounced at high switching frequencies and limits the maximum ratio between the buck input voltage ( $V_{BOOST}$ ) and the LED strings' forward voltage. One way to overcome this limitation is reducing switching frequency, by selecting high constant  $V_{LED} \times T_{OFF}$  and/or increase the inductance value.

### 3.3 Peak and average current setting

In buck converters, the inductor is directly connected to the load during the complete switching cycle (see [Figure 7: Peak current control principle](#)). The average inductor current is equal to the average LED string current. Operating in continuous conduction mode (i.e. the inductor current never decays to zero during the off-phase), if the inductor current is tightly controlled, the LED current will be regulated as well.

Figure 7. Peak current control principle



At the beginning of a switching period the MOSFET M1 is turned on, and the inductor current  $I_{L1}$  increases. The mosfet is activated for a minimum on-time  $T_{ON\_MIN}$  in order to avoid that the on-phase is ended up by spurious noise, which is caused by the switch-on.

During mosfet activation, the inductor current,  $I_{L1}$ , increases until reaching a maximum value,  $I_{L1\_PEAK}$ , which is set through a dedicated control register (see bits <23:18> and bits <17:12> on [Table 15: CR#2: Control Register 2](#)). When  $I_{L1}$  reaches its peak value, the switching mosfet is turned off. The mosfet remains off for a time  $T_{OFF}$ , which is derived from the configured constant  $V_{LED1} \times T_{OFF1}$  (see bits <11:8> and bits <7:4> on [Table 15: CR#2: Control Register 2](#)), where  $V_{LED1}$  is the forward voltage of the LED string, which is connected at the output of the buck converter 1.

During  $T_{OFF}$ , the inductor current decreases by:

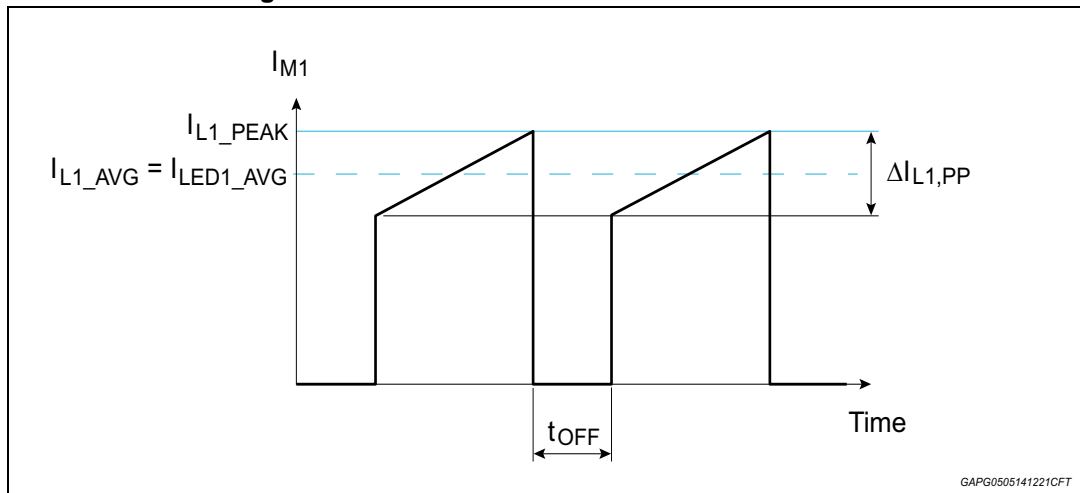
$$\Delta I_{L1\_PP} = \frac{(V_{LED1} - V_{F\_D1})}{L_1} \cdot T_{OFF1} \sim \frac{V_{LED1} \cdot T_{OFF1}}{L_1}$$

where  $\Delta I_{L1\_PP}$  is the inductor peak to peak current and  $V_{F\_D1}$  is the forward voltage of the diode D1. As D1 is a Schottky diode with a low forward voltage,  $V_{F\_D1}$  can be in general neglected, compared to  $V_{LED1}$ .

*Note:* Once the  $V_{LEDxTOFF}$  constant for a given buck converter is selected by SPI, the peak-to-peak inductor current ripple is constant. In particular, it depends neither on the boost voltage nor on the LED forward voltage.

The ripple current through the LED strings is reduced by means of an external capacitor in parallel with the LEDs.

**Figure 8. Inductor and mosfet current waveforms**



Referring to the [Figure 7](#) and [Figure 8](#) the average LED current - valid for both Buck 1 and Buck 2 - is therefore:

$$I_{LED1\_AVG} = I_{L1\_AVG} = I_{L1\_PEAK} * \frac{(\Delta I_{L1\_PP})}{2} = I_{L1\_PEAK} * \frac{(V_{LED} \cdot T_{OFF1})}{2L}$$

where  $I_{L1\_PEAK}^*$  results from  $I_{L1\_PEAK}$  (see [Table 40](#)) corrected with loop delay ( $t_{loop\_delay}$ )

In order to achieve the best accuracy versus input voltage variation during current sensing process, a defined buck input voltage window must be selected, by means of a dedicated control register (see bits <5:4> and bits <3:2> on [Table 16: CR#3: Control Register 3](#)).

### 3.4 Buck converter's blank time

The buck converters have a minimum on-time  $T_{BLANK\_BUCK}$ . Although the inductor's target peak current  $I_{LX\_PEAK}$  is reached before this time has elapsed, the switch is kept on. This delay is used as a leading-edge blank time, in order to avoid a premature end of the switching cycle, which might be caused by the noise, which results from the commutation of the buck's mosfet.

### 3.5 Buck converter's start-up

While the device and the system are protected against short circuit conditions of the buck's output to GND, the device inhibits the detection of the short circuit during the startup phase  $T_{STARTUP}$ .

A startup phase is applied in the following conditions:

- If one of the buck converters is activated for the first time after a power on reset (POR), including buck activation after device wake-up;
- If one of the buck converters has been deactivated for more than  $t_{DELAY}$ ;
- If one of the buck converters has been latched off prior to a Read and Clear command;
- If one of the buck converters is re-activated after a VS under voltage event.

After these events, it is possible that the output capacitors of the buck converters are completely discharged. The charging of the buck output capacitors might lead switching cycles with short on-time (shorter than  $T_{ON\_MIN}$ ), which could potentially lead to a wrong detection of a shorted buck output. The introduction of this start-up phase avoids this wrong diagnostic.

### 3.6 Switching frequency

For a given buck converter, the switching frequency depends on the buck input voltage (output of the boost controller) and the forward voltage of the LED string, which is connected to its output.

In continuous conduction mode,  $T_{OFF}$  is given by:

$$T_{OFF} = (1 - D) \cdot T = \frac{1 - D}{F_{SW}}$$

Where D is the buck converter's duty cycle, T and  $F_{SW}$  are respectively the switching period and frequency.

Neglecting the drop voltage across the mosfet, the inductor's DC resistance and the diode's forward voltage, compared to  $V_{BUCKIN}$  and  $V_{LED}$ , we have:

$$D = \frac{V_{LED}}{V_{BUCKIN}}$$

$$F_{SW} = \frac{1 - \frac{V_{LED}}{V_{BUCKIN}}}{T_{OFF}} = \frac{V_{LED} \cdot \left(1 - \frac{V_{LED}}{V_{BUCKIN}}\right)}{V_{LED} \cdot T_{OFF}}$$

For a given application (given inductance and  $V_{LED}$ ), it is possible to set  $I_{LEDx\_AVG}$  by selecting different combinations of  $I_{Lx\_PEAK}$  and  $V_{LED} \times T_{OFF}$  in order to avoid critical frequency ranges such as the AM radio band.

To avoid buck operation at not allowed  $T_{ON}$  and/or  $T_{OFF}$  times, frequency range has to be kept inside  $F_{SWmin}$  and  $F_{SWmax}$ , where:

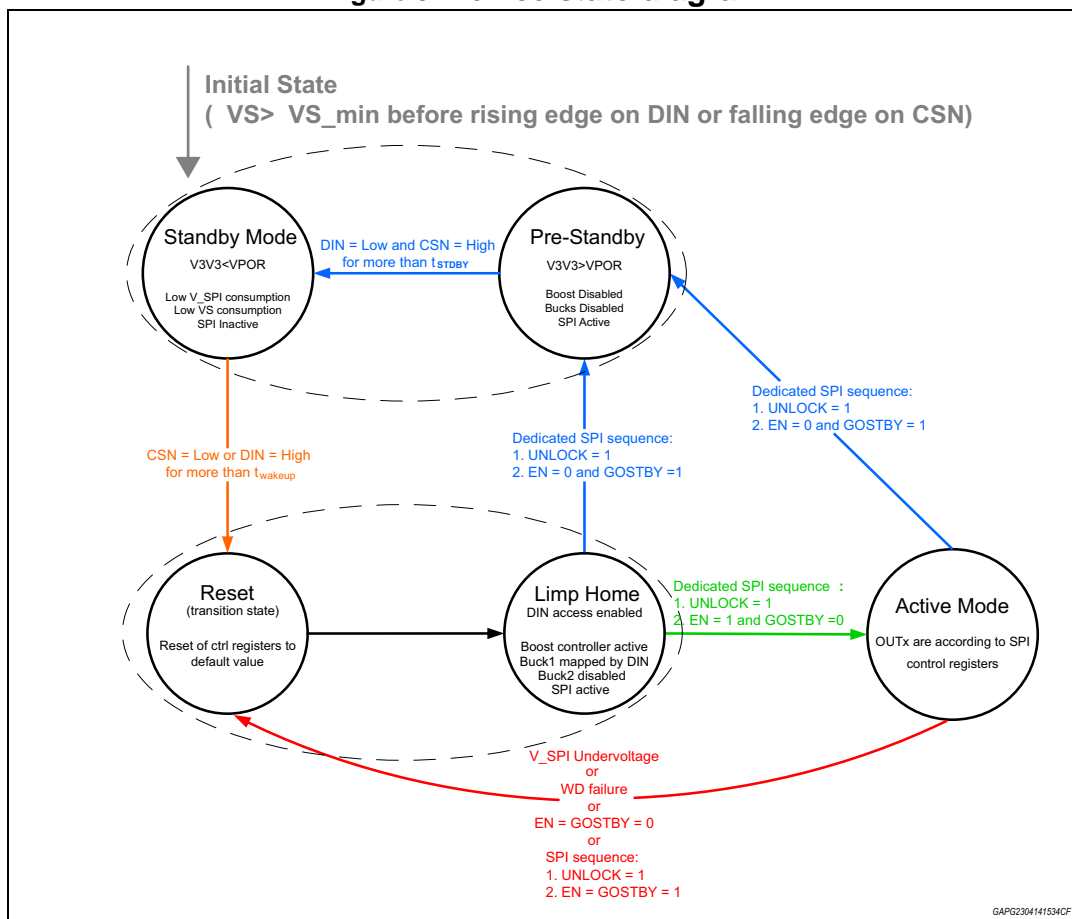
$$F_{SWmin} = 1/(T_{ON\_MAX\_BUCK} + T_{OFF\_MAX\_BUCK})$$

$$F_{SWmax} = 1/(T_{ON\_MIN\_BUCK} + T_{OFF\_MIN\_BUCK})$$

## 4 Functional description

### 4.1 Operating modes

Figure 9. Device state diagram



#### 4.1.1 Standby mode

The pre-requisite for this mode is:

- Device in Pre-Standby mode.

The device enters Standby mode under the following conditions:

- By default, once the device is powered (VS present);
- CSN High and DIN Low for more than t<sub>STDBY</sub>

The Standby mode characteristics are:

- V3V3 < VPOR
- V<sub>SPI</sub> and V<sub>S</sub> low consumption
- SPI inactive

The device leaves this mode if:

- DIN High or CSN Low for a time t > t<sub>WAKEUP</sub>

*Note:*  $V_s$  must be stable above minimum value specified (5.5 V) before rising edge on DIN or falling edge on CSN.

#### 4.1.2 Pre-standby mode

The device enters Pre-standby mode under the following conditions:

- upon the two following consecutive SPI frames setting:
  - UNLOCK = 1
  - (EN, GOSTBY) = (0, 1)

The Pre-standby mode characteristics are:

- $V3V3 > VPOR$
- Boost disabled
- Bucks disabled
- SPI active

The device leaves automatically Pre-standby mode entering standby:

- if CSN High and DIN Low for a time  $t > t_{STDBY}$

#### 4.1.3 Reset mode

The device enters Reset mode under the following conditions:

- By default, once the device leaves Standby mode;
- If device state is Active mode, when one of the following events occur:
  - $V_{SPI}$  under voltage;
  - Watchdog failure
  - One SPI frame setting (EN,GOSTBY) = (0,0)
  - Two consecutive SPI frames setting
    - UNLOCK = 1
    - (EN,GOSTBY) = (1,1)

The Reset mode characteristics are:

- $V3V3 > VPOR$
- All the control and status registers set to their default values
- SPI inactive

The device leaves automatically Reset mode and enters Limp home after 400 ns (typical).

#### 4.1.4 Limp home

The device enters Limp Home automatically 400 ns after Reset mode.

Limp home characteristics are:

- Direct Input access enabled
- Boost active
- Buck1 according DIN
- Buck2 OFF
- SPI active:
  - All SPI write operations must be allowed without any effects on the device behavior.

When the device leaves this mode, it can enter Standby or Active mode.

If the microcontroller sends to the device the following SPI frames sequence:

- The first SPI frame sets UNLOCK bit = 1  
(see bit <1> on [Table 14: CR#1: Control Register 1](#))
- The second consecutive SPI frame sets GOSTBY bit = 1 and EN bit = 0  
(see bit <3> and bit <2> on [Table 15: CR#2: Control Register 2](#))

The device enters Standby mode.

If the microcontroller sends to the device the sequence of the following SPI frames:

- The first SPI frame sets UNLOCK bit = 1;  
(see bit <1> on [Table 14: CR#1: Control Register 1](#))
- The second consecutive SPI frame sets GOSTBY bit = 0 and EN bit = 1.  
(see bit <3> and bit <2> on [Table 15: CR#2: Control Register 2](#))

The device enters Active mode.

In Limp Home, after setting bit 27 on GSB (FE1, functional error bit), an auto restart procedure is implemented: every  $t_{\text{AUTORESTART}}$ , functional error bit eventually set is automatically cleared.

#### 4.1.5 Active mode

The device enters the Active mode if the microcontroller sends the following SPI frames sequence:

- In a first SPI frame set the UNLOCK bit to 1  
(see bit <1> on [Table 14: CR#1: Control Register 1](#))
- In a second frame, set EN bit to 1 and GOSTBY bit to "0"  
(see bit <2> and bit <3> on [Table 15: CR#2: Control Register 2](#))

**Table 3. Operating modes**

| Operating mode   | Entering conditions  | Leaving condition   | Characteristics  |
|------------------|--|---|--|
| Standby mode     | <ul style="list-style-type: none"> <li>– By default, once powered on (VS present);</li> <li>– SPI active and micro sending following consecutive frames:<br/>UNLOCK = 1<br/>(EN,GOSTBY) = (0,1)</li> </ul> | DIN = High for $t_{\text{WAKEUP}}$<br>and/or<br>CSN = Low for $t_{\text{WAKEUP}}$ | <ul style="list-style-type: none"> <li>– <math>V_{3V3} &lt; V_{\text{POR}}</math>;</li> <li>– <math>V_S</math> and <math>V_{\text{SPI}}</math> low consumption;</li> <li>– SPI inactive</li> </ul> |
| Pre-standby mode | <ul style="list-style-type: none"> <li>– Under the following conditions:<br/>Two following consecutive SPI frames setting:<br/>UNLOCK = 1<br/>(EN,GOSTBY) = (0,1)</li> </ul>                               | CSN High and DIN Low for a time $t > t_{\text{STDBY}}$                            | <ul style="list-style-type: none"> <li>– <math>V_{3V3} &gt; V_{\text{POR}}</math></li> <li>– Boost disabled</li> <li>– Bucks disabled</li> <li>– SPI active</li> </ul>                             |



Table 3. Operating modes (continued)

| Operating mode | Entering conditions  | Leaving condition   | Characteristics   |
|----------------|--|---|---|
| Reset mode     | <ul style="list-style-type: none"> <li>– By default, when device leaves Standby mode</li> <li>– Under following condition, when device is in Active mode:<br/> <math>V_{SPI}</math> Under voltage<br/> WD failure;<br/> One SPI frame setting (EN,GOSTBY) = (0,0)<br/> Two consecutive SPI frames setting:<br/> UNLOCK = 1<br/> (EN,GOSTBY) = (1,1)</li> </ul> | Automatic transition after 400 ns   | <ul style="list-style-type: none"> <li>– All registers reset to default values</li> <li>– <math>V3V3 &gt; VPOR</math></li> <li>– SPI inactive</li> </ul>                    |
| Limp Home      | 400 ns after Reset mode  | <ul style="list-style-type: none"> <li>– SPI sequence to enter Active mode:<br/> UNLOCK = 1<br/> (EN,GOSTBY) = (1,0)</li> <li>– SPI sequence to enter Standby mode:<br/> UNLOCK = 1<br/> (EN,GOSTBY) = (0,1)</li> </ul> | <ul style="list-style-type: none"> <li>– Boost controller is active</li> <li>– DIN access enabled: Buck1 is according to DIN; Buck2 is OFF</li> <li>– SPI active</li> </ul> |
| Active mode    | SPI sequence:<br><ul style="list-style-type: none"> <li>– UNLOCK = 1</li> <li>– EN = 1 and GOSTBY = 0</li> </ul>   | <ul style="list-style-type: none"> <li>– <math>V_{SPI}</math> undervoltage</li> <li>– WD failure</li> <li>– SPI sequence to enter Standby mode:<br/> UNLOCK = 1<br/> (EN,GOSTBY) = (0,1)</li> </ul>                     | <ul style="list-style-type: none"> <li>– Boost controller is active</li> <li>– Buck converters are active</li> <li>– SPI is active</li> </ul>                               |

## 4.2 Programmable functions

### 4.2.1 Activation of the buck output

In Active mode, the activation of the Buck converters is performed according to the configuration of control register CR#3<15:14> for Buck1 and CR#3<13:12> for Buck2, as showed in the following table. See [Table 16: CR#3: Control Register 3](#).

Table 4. DIN pin Map for Buck1 and Buck2

| CR#3<15> or CR#3<13> | CR#3<14> or CR#3<12> | Buck1 and Buck2 status                            |
|----------------------|----------------------|---|
| 0                    | 0                    | Buckx always OFF (default for Buck2)              |
| 0                    | 1                    | Buckx attached to internal PWM generator          |
| 1                    | 0                    | Buckx always ON                                   |
| 1                    | 1                    | Buckx controlled by DIN Input (default for Buck1) |

### 4.2.2 PWM dimming

The device allows modifying the brightness of the LEDs string simply managing the average current.

The PWM dimming could be achieved in two different ways:

- Through direct input, DIN
- With integrated PWM generator

### Dimming with direct input

The signal applies to buck1, buck2 or both, depending on DIN mapping bit configuration (see bits <15:14> and bits <13:12> on [Table 16: CR#3: Control Register 3](#)). If the control registers are configured accordingly, one (or both) buck converter(s) are activated and directly controlled by DIN pin.

The default configuration is set in order to allow direct driving only for buck1, whilst buck2 is turned off. In case of limp home function, the default conditions are applied.

PWM control through DIN has to take into account the DIN filter time ( $t_{DIN\_FT}$ , 32  $\mu$ s typical) on rising edge to properly set the desired duty cycle.

### Dimming with integrated PWM generator

This function allows modifying the average current on the LEDs by means of a dedicated control register (see bits <23:14> and bits <13:4> on [Table 14: CR#1: Control Register 1](#)).

This function must be activated setting the right mapping bits configuration inside the control register 3, and in particular, CR#3<15:14> for Buck1 and CR#3<13:12> for Buck2.

To set duty cycle, a 10-bit number must be written in the corresponding register, resulting in a 1024 steps of resolution. The duty cycle is determined through the following equation:

$$DC_{\%} = \frac{N}{1024} \cdot 100$$

Where N is the 10-bit number.

The PWM frequency is depending on the PWM\_CLK input signal with the following equation:

$$PWM\_LF = \frac{PWM\_CLK}{1024}$$

Where PWM\_LF is the LEDs dimming frequency.

If PWM signal fails, an error bit is reported in the STATUS register where PWMCLK fail is located. An internal fallback oscillator is enabled in order to provide a fixed PWM frequency clock signal ( $F_{FALLBACK\_CLK}$ ), whilst no changes is applied on the duty cycle.

Once the external PWM is available again and after a read & clear operation on Status Register 2, the internal clock is disabled and PWM operation continues with the external clock (see [Figure 14](#)).

## 4.3 Protections

### 4.3.1 Temperature warning

The device integrates a temperature warning with two thresholds  $TW_1$  and  $TW_2$  in each buck's mosfet. If the  $T_j$  of the buck mosfet1 or buck mosfet2 rises above  $TW_1$  or  $TW_2$ , the status bit  $TW_{xy}$  is set ( $x = 1$  or  $x = 2$ , it stands for the buck1 or buck2,  $y = 1$  or  $y = 2$ , it stands for the  $TW_1$  or  $TW_2$ ).  $TW_{XY}$  bit is set on the status registers: SR#1<4:3> for Buck1

and SR#2<22:21> for Buck2. Thermal warning is also reported in the Global Status Byte register, and in particular, bit 25 (GW) is set.

If the  $T_j$  drops below the temperature warning reset threshold 1 ( $TW_1 - TW_{1\_HYS}$ ), respectively  $TW_2 - TW_{2\_HYS}$ , the corresponding status bit is automatically reset.

As long as the  $T_j$  does not exceed the over temperature shutdown, the device does not latches off the buck mosfets, even if a temperature warning is detected.

### 4.3.2 Overtemperature shutdown

If the junction temperature of one of the buck mosfets rises above the shutdown temperature  $T_{TSD}$ , an overtemperature event (OVT) is detected. The channel is switched off and the corresponding bit (OVT1 or OVT2) is set in the status register SR#1<5> for Buck1 and SR#2<23> for Buck2.

Overtemperature events are also reported in the Global Status Byte register and in particular bit 27 FE1 is set.

In normal mode the corresponding buck converter is latched off, until the following conditions are fulfilled:

1.  $T_{JX}$  drops below the thermal shutdown reset threshold  $T_{TSD} - T_{TSD\_HYS}$ .
2. Subsequently the microcontroller sends a read and clear command, in order to reset OVT1 or OVT2 bit located in the Status register SR#1<5> or SR#2<23>.

In fail safe mode (Limp Home), the device applies an auto restart of the fault buck converter with a period equal to  $t_{AUTORESTART}$ , provided that the  $T_{JX}$  falls below TSD reset threshold ( $T_{TSD} - T_{TSD\_HYS}$ ).

### 4.3.3 VS under voltage lockout

If the VS supply falls below  $V_{S\_UV}$  (VS under voltage threshold), the boost controller and the buck converters will be deactivated, regardless of the SPI control registers or DIN.

This feature is implemented, in order to avoid an operation of the external mosfet of the boost controller in linear mode, due to a too low gate driver supply.

### 4.3.4 Buck $T_{ON}$ minimum operation

Buck minimum on time operation is detected when the corresponding failure counter counts  $N_{Ton\_min\_fail}$  switching cycles (also nonconsecutive), during which  $I_{LX\_PEAK}$  is reached between  $T_{BLANK\_BUCK}$  and  $T_{ON\_MIN\_BUCK}$ . In normal mode (Active mode), once minimum  $T_{ON}$  operation is validated, flag  $T_{ON\_MIN\_OPx}$  is set and the corresponding Buckx converter is latched off, until the microcontroller sends a frame and clears the corresponding status bit (SR#1<2> and SR#1<1>).

In fail safe mode (Limp Home), once a minimum  $T_{ON}$  violation is validated, the corresponding buck converter is latched off until automatically cleared by an auto-restart procedure, with a period equal to  $t_{AUTORESTART}$ .

The failure counter is not incremented during the startup phase ( $T_{STARTUP}$ ). The failure counter is reset if  $N_{ton\_min\_fail\_reset}$  consecutive pulses are detected with  $T_{ON}$  longer than  $T_{ON\_MIN\_BUCK}$ .

### 4.3.5 Buck output's short circuit to GND

A shorted buck output to GND is detected when LED string voltage ( $V_{LED}$ ) is lower than a specified threshold ( $V_{LED\_SHT}$ ) and the corresponding failure counter counts  $N_{ton\_min\_fail}$  switching cycles (also nonconsecutive), during which  $I_{LX\_PEAK}$  is reached between  $T_{BLANK\_BUCK}$  and  $T_{ON\_MIN\_BUCK}$ . In normal mode (Active mode), once a short circuit is validated, flag  $SHTx$  is set and the corresponding Buckx converter is latched off, until the microcontroller sends a frame and clears the corresponding status bit ( $SR\#1<7>$  and  $SR\#1<6>$ ).

In fail safe mode (Limp Home), once a short circuit is validated, the corresponding buck converter is latched off until automatically cleared by an auto-restart procedure, with a period equal to  $t_{AUTORESTART}$ .

The failure counter is not incremented during the startup phase. The failure counter is reset if  $N_{ton\_min\_fail\_reset}$  consecutive pulses are detected with  $T_{ON}$  longer than  $T_{ON\_MIN\_BUCK}$ .

### 4.3.6 Buck $T_{ON}$ maximum operation

Buck maximum on time operation is detected when switching on time is equal to  $t_{ON\_MAX\_BUCK}$  for two consecutive cycles.

Once maximum  $T_{on}$  operation is validated, flag  $TON\_MAX\_OPx$  is set and the corresponding Buckx converter is temporarily switched off for a  $T_{tonmax\_off}$ .

Then, Buckx is enabled to switch on again while  $TON\_MAX\_OPx$  bit will be latched until a R&C command clears corresponding status bit ( $SR\#2<20>$  or  $SR\#2<19>$ ).

In fail safe mode (Limp Home), once a maximum  $T_{ON}$  violation is validated, the corresponding buck converter is latched off until automatically cleared by an auto-restart procedure, with a period equal to  $t_{AUTORESTART}$ .

### 4.3.7 Buck Open Load detection

If one of the LED strings is disconnected, the converter will charge the output capacitor of the buck converter by regulating the peak current of the switch, until  $V_{LED}$  is equal to the buck input voltage. From this point, since the output capacitor is charged at the maximum possible value, it cannot absorb any current despite the activation of the switch, and the target  $I_{LX\_PEAK}$  cannot be reached.

Upon these conditions, Buckx starts switching at maximum  $T_{on}$ : maximum  $T_{on}$  operation detection (described in [Section 4.3.6](#)) guarantees Open Load failure protection as well.

## 5 SPI functional description

### 5.1 SPI protocol

ST-SPI is a standard used in ST automotive ASSP devices. SPI protocol standardization here described defines a common structure of the communication frames and defines specific addresses for product and status information.

The ST-SPI will allow usage of generic software to operate the devices while maintaining the required flexibility to adapt it to the individual functionality of a particular product. In addition to that, fail safe mechanisms are implemented to protect the communication from external influence and wrong or unwanted usage.

### 5.2 SPI communication

At the beginning of each communication the master can read the content of the <SPI Mode> register (ROM address 10h) of the slave device. This 8 bit register indicates the SPI frame length (32 bit) and the availability of additional features.

Each communication frame consists of a command byte which is followed by 3 data bytes.

The data returned on SDO within the same frame always starts with the <Global Status Byte>. It provides general status information about the device. It is followed by 3 data bytes (i.e. "in-frame-response").

For write cycles the <Global Status Byte> is followed by the previous content of the addressed register.

**Table 5. Command byte (8 bit)**

|      | Operating code |     | Address |    |    |    |    |    |
|------|----------------|-----|---------|----|----|----|----|----|
| Bit  | 31             | 30  | 29      | 28 | 27 | 26 | 25 | 24 |
| Name | OC1            | OC0 | A5      | A4 | A3 | A2 | A1 | A0 |

**Table 6. Data byte 2**

|      | Data byte 2 |     |     |     |     |     |     |     |
|------|-------------|-----|-----|-----|-----|-----|-----|-----|
| Bit  | 23          | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| Name | D23         | D22 | D21 | D20 | D19 | D18 | D17 | D16 |

**Table 7. Data byte 1**

|      | Data byte 1 |     |     |     |     |     |    |    |
|------|-------------|-----|-----|-----|-----|-----|----|----|
| Bit  | 15          | 14  | 13  | 12  | 11  | 10  | 9  | 8  |
| Name | D15         | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

Table 8. Data byte 0

|      | Data byte 0 |    |    |    |    |    |    |    |
|------|-------------|----|----|----|----|----|----|----|
| Bit  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Where:

OCx: Operation Code

Ax : Address

Dx: Data bit

### Command Byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (<Read>, <Write>, <Read and Clear>, <Read Device Information>) and a 6 bit address.

Table 9. Operation code definition

| OC1 | OC0 | Meaning                   |
|-----|-----|---------------------------|
| 0   | 0   | <Write Mode>              |
| 0   | 1   | <Read Mode>               |
| 1   | 0   | <Read and Clear Mode>     |
| 1   | 1   | <Read Device Information> |

The <Write Mode> and <Read Mode> operations allow access to the RAM of the device.

A <Read and Clear Mode> operation is used to read a status register and subsequently clears its content.

The <Read Device Information> allows access to the ROM area which contains device related information.

### Global Status Byte

According to the ST SPI 4.1 standard, the first byte on the SDO pad during each command reports the global status of the chip:

Table 10. Global Status Byte

|      | Global Status Byte |      |      |     |     |    |    |    |
|------|--------------------|------|------|-----|-----|----|----|----|
| Bit  | 31                 | 30   | 29   | 28  | 27  | 26 | 25 | 24 |
| Name | GSBN               | RSTB | SPIE | FE2 | FE1 | DE | GW | FS |

Table 11. Global Status Byte description

| Bit | Name | Description   |
|-----|------|---|
| 31  | GSBN | Global Status Bit Not<br>This bit is a NOR combination of the remaining bits of this register:<br>RSTB nor SPIE nor FE2 nor FE1 nor DE nor GW nor FS  |
| 30  | RSTB | Reset Bit<br>The RSTB indicates a device reset. In case this bit is set, all internal <i>Control Registers</i> are set to default and kept in that state until the bit is automatically cleared by any valid SPI communication. |
| 29  | SPIE | SPI Error<br>The SPIE is a logical OR combination of errors related to a wrong SPI communication (SDI stuck, wrong number of clock, parity check error)   |
| 28  | FE2  | Functional Error 2 (logic OR combination of errors which does not cause parts of the device to be disabled)<br>TOFF1_MAX or TOFF2_MAX or TOFF1_MIN or TOFF2_MIN or<br>TON_MAX_OP1 or TON_MAX_OP2                                |
| 27  | FE1  | Functional Error 1 (logic OR combination of critical errors which cause parts of the device to be disabled)<br>VS_UV or OL1 or OL2 or OVT1 or OVT2 or SHT1 or SHT2 or TON_MIN_OP1 or TON_MIN_OP2 or BST_FB_FAIL                 |
| 26  | DE   | Device error<br>PWMCLK_FAIL or N_PWR_GOOD or BST_OVP  |
| 25  | GW   | Global warning<br>TW11 or TW12 or TW21 or TW22  |
| 24  | FS   | Fail safe<br>If this bit is set, the device is in limp home mode  |

### 5.3 Address mapping

Table 12. RAM memory map

| Address | Name               | Access | Content                                |
|---------|--------------------|--------|--|
| 01h     | Control Register 1 | R/W    | CR#1: 1 <sup>st</sup> Control Register |
| 02h     | Control Register 2 | R/W    | CR#2: 2 <sup>nd</sup> Control Register |
| 03h     | Control Register 3 | R/W    | CR#3: 3 <sup>rd</sup> Control Register |
| 04h     | Control Register 4 | R/W    | CR#4: 4 <sup>th</sup> Control Register |
| 05h     | Status Register 1  | R/C    | SR#1: 1 <sup>st</sup> Status Register  |
| 06h     | Status Register 2  | R/C    | SR#2: 2 <sup>nd</sup> Status Register  |
| 07h     | Status Register 3  | R/C    | SR#3: 3 <sup>rd</sup> Status Register  |

Table 12. RAM memory map (continued)

| Address | Name                       | Access                           | Content   |
|---------|----------------------------|----------------------------------|---|
| 3Eh     | Customer Trimming Register | R/W<br>(W only when EOT bit = 0) | CT: Customer Trimming Register  |
| 3Fh     | Advanced Operation Code    | Clear                            | A R&C operation to this address causes all status registers to be cleared |

Table 13. ROM memory map

| Address | Name            | Access | Content | Comments   |
|---------|-----------------|--------|---------|--|
| 00h     | Company Code    | R      | 00h     | STMicroelectronics   |
| 01h     | Device family   | R      | 02h     | LED product family   |
| 02h     | Device number 1 | R      | 55h     | 'U' in ASCII   |
| 03h     | Device number 2 | R      | 41h     | 'A' in ASCII   |
| 04h     | Device number 3 | R      | 52h     | 'R' in ASCII   |
| 05h     | Device number 4 | R      | 07h     | '7' in hex   |
| 0Ah     | Silicon version | R      | 04h     | Fifth version  |
| 10h     | SPI Mode        | R      | 31h     | Bit7 = 0, burst read is disabled<br>SPI data length = 32 bits<br>Bit6, DL2 = 0<br>Bit5, DL1 = 1<br>Bit4, DL0 = 1<br>Bit3, SPI8 = 0: 8 bit frame option not available<br>Bit2 = 0<br>Parity check is used<br>Bit1, S1 = 0<br>Bit0, S0 = 1 |
| 11h     | WD Type 1       | R      | 4Ah     | A WD is implemented<br>Bit7, WD1 = 0<br>Bit6, WD0 = 1<br>WD period 50 ms = 10 * 5 ms -> WT[5:0] = 0xA<br>Bit5, WT5 = 0<br>Bit4, WT4 = 0<br>Bit3, WT3 = 1<br>Bit2, WT2 = 0<br>Bit1, WT1 = 1<br>Bit0, WT0 = 0                              |
| 13h     | WD bit pos. 1   | R      | 44h     | Bit7, WB1 = 0<br>Bit6, WB2 = 1<br>WBA[5:0], Bit[5:0] = address of the configuration register, where the WD bit is located = 04d = 000100b  |



Table 13. ROM memory map (continued)

| Address | Name                    | Access | Content | Comments   |
|---------|-------------------------|--------|---------|--|
| 14h     | WD bit pos. 2           | R      | D7h     | Bit7, WB1 = 1<br>Bit6, WB0 = 1<br>Bit position of the WD bit within the corresponding configuration register = 23d = 010111b   |
| 20h     | SPI CPHA Test           | R      | 55h     | Predefined by ST - SPI , it is used to verify that the SCK Phase of the SPI master is set correctly  |
| 3Eh     | GSB Options             | R      | 00h     | All bits of GSB are used   |
| 3Fh     | Advanced Operation Code | R      | 00h     | Access to this address provokes a SW reset (all control registers are set to their default values; in addition, all status registers are cleared too).<br><br>Data field should not be all ones, otherwise an SDI stuck occurs |

## 5.4 Registers description

### 5.4.1 Control Register description

#### CR#1: Control Register 1

|       |    |    |    |    |    |    |    |    |    |       |    |    |    |   |   |   |   |   |   |          |          |        |            |
|-------|----|----|----|----|----|----|----|----|----|-------|----|----|----|---|---|---|---|---|---|----------|----------|--------|------------|
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13    | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3        | 2        | 1      | 0          |
| DUTY1 |    |    |    |    |    |    |    |    |    | DUTY2 |    |    |    |   |   |   |   |   |   | HLEDCUR1 | HLEDCUR2 | UNLOCK | Parity bit |

**Address:** 0x01h

**Type:** R/W

Table 14. CR#1: Control Register 1

| Bit   | Default                     | Name     | Description   |
|-------|-----------------------------|----------|---|
| 23÷14 | 1000000000                  | DUTY1    | 10 bit PWM duty cycle selection for Buck1 (from 0 to hex 3FF) Default 50%   |
| 13÷4  | 1000000000                  | DUTY2    | 10 bit PWM duty cycle selection for Buck2 (from 0 to hex 3FF) Default 50%   |
| 3     | Set by OTP<br>(DEF_HLEDCUR) | HLEDCUR1 | [1]: High LED current configuration selected for Buck1 (Low RON, both half power stages enabled)<br>[0]: Low LED current configuration selected for Buck1 (High RON, only one half power stage enabled) |
| 2     |                             | HLEDCUR2 | [1]: High LED current configuration selected for Buck2 (Low RON, both half power stages enabled)<br>[0]: Low LED current configuration selected for Buck2 (High RON, only one half power stage enabled) |

Table 14. CR#1: Control Register 1 (continued)

| Bit | Default | Name       | Description   |
|-----|---------|------------|---|
| 1   | 0       | UNLOCK     | [0]: bits GOSTBY, EN and BST_DIS cannot be set to 1<br>[1]: bits GOSTBY, EN and BST_DIS can be set to 1 with the next SPI frame<br>If UNLOCK = 1, then it is always automatically reset with the next valid SPI frame |
| 0   |         | Parity bit | ODD parity bit check  |

**CR#2: Control Register 2**

|          |    |    |    |    |    |          |    |    |    |    |    |            |    |   |   |            |   |   |   |        |    |    |            |
|----------|----|----|----|----|----|----------|----|----|----|----|----|------------|----|---|---|------------|---|---|---|--------|----|----|------------|
| 23       | 22 | 21 | 20 | 19 | 18 | 17       | 16 | 15 | 14 | 13 | 12 | 11         | 10 | 9 | 8 | 7          | 6 | 5 | 4 | 3      | 2  | 1  | 0          |
| IL1_PEAK |    |    |    |    |    | IL2_PEAK |    |    |    |    |    | VLED_TOFF1 |    |   |   | VLED_TOFF2 |   |   |   | GOSTBY | EN | MS | Parity bit |

**Address:** 0x02h**Type:** R/W

Table 15. CR#2: Control Register 2

| Bit   | Default                                       | Name       | Description   |
|-------|---|------------|---|
| 23÷18 | Set by OTP<br>(see <a href="#">Table 29</a> ) | IL1_PEAK   | Inductor Peak Current selection bits for Buck1  |
| 17÷12 | 100000  | IL2_PEAK   | Inductor Peak Current selection bits for Buck2  |
| 11÷8  | Set by OTP<br>(see <a href="#">Table 30</a> ) | VLED_TOFF1 | Constant VLEDxTOFF Selection bits for Buck1:<br>0000: 10 V*μs;<br>1111: 72 V*μs; see <a href="#">Table 18</a>   |
| 7÷4   | 1111  | VLED_TOFF2 | Constant VLEDxTOFF Selection bits for Buck2:<br>0000: 10 V*μs;<br>1111: 72 V*μs; see <a href="#">Table 18</a>   |
| 3     | 0   | GOSTBY     | Standby Mode Bit:<br>0: Device waked up<br>1: Standby (if EN = 0)<br>GOSTBY can be set to 1 only if UNLOCK = 1; in other words, trying to set this bit to 1 when UNLOCK = 0 will have no effects and it will maintain its previous value.<br>GOSTBY can be reset to 0 also when UNLOCK = 0.<br>To set Standby mode it is necessary to send two consecutive SPI frames, as follows:<br>1 <sup>st</sup> SPI write operation to set UNLOCK bit to 1 (CR#1, bit1)<br>2 <sup>nd</sup> SPI write operation to set GOSTBY bit to 1 and EN bit to 0 |

Table 15. CR#2: Control Register 2 (continued)

| Bit | Default             | Name       | Description  |
|-----|---------------------|------------|--|
| 2   | 0                   | EN         | <p>Active mode Enable Bit:</p> <p>0: Device stays in Limp Home (if GOSTBY = 0). This status is assumed immediately after a wake up (CSN low or DIN High for a time &gt; <math>t_{WAKE\_UP}</math>)</p> <p>1: Device Enabled for Active mode operation (if GOSTBY = 0).</p> <p>EN can be set to 1 only if UNLOCK = 1; in other words, trying to set this bit to 1 when UNLOCK = 0 will have no effects and it will maintain its previous value.</p> <p>EN can be reset to 0 also when UNLOCK = 0.</p> <p>To set Active mode it is necessary to send two consecutive SPI frames as follows:</p> <p>1<sup>st</sup> SPI write operation to set UNLOCK bit to 1 (CR#1, bit1)</p> <p>2<sup>nd</sup> SPI write operation to set GOSTBY bit to 0 and EN bit to 1</p> |
| 1   | Set by OTP (DEF_MS) | MS         | <p>Master/Slave bit</p> <p>0: Device is Master (pin SYNC_IO is an output, providing a 180° phase shifted replica of internal Boost clock)</p> <p>1: Device is Slave (pin SYNC_IO is an input and it is used as a clock for the Boost)</p>  |
| 0   |                     | Parity bit | ODD parity bit check   |

## CR#3: Control Register 3

|     |    |    |    |     |    |    |    |          |          |         |          |    |    |   |          |         |   |         |   |         |            |   |   |
|-----|----|----|----|-----|----|----|----|----------|----------|---------|----------|----|----|---|----------|---------|---|---------|---|---------|------------|---|---|
| 23  | 22 | 21 | 20 | 19  | 18 | 17 | 16 | 15       | 14       | 13      | 12       | 11 | 10 | 9 | 8        | 7       | 6 | 5       | 4 | 3       | 2          | 1 | 0 |
| PH1 |    |    |    | PH2 |    |    |    | DIN_MAP1 | DIN_MAP2 | BST_REF | BST_FREQ |    |    |   | PWM_SYNC | B_IN_W1 |   | B_IN_W2 |   | BST_DIS | Parity bit |   |   |

Address: 0x03h

Type: R/W

Table 16. CR#3: Control Register 3

| Bit   | Default | Name     | Description  |
|-------|---------|----------|--|
| 23÷20 | 0000    | PH1      | 4 bit phase selection for Buck1:<br>Phase shift = PH1 * 360 / 16   |
| 19÷16 | 0000    | PH2      | 4 bit phase selection for Buck2:<br>Phase shift = PH1 * 360 / 16   |
| 15÷14 | 11      | DIN_MAP1 | Buck1 DIN map (see <a href="#">Table 19</a> )  |
| 13÷12 | 00      | DIN_MAP2 | Buck2 DIN map (see <a href="#">Table 19</a> )  |
| 11÷10 | 11      | BST_REF  | <p>Boost Reference Voltage<sup>(1)</sup></p> <p>11: VFB_REF[11]</p> <p>10: VFB_REF[10]</p> <p>01: VFB_REF[01]</p> <p>00: VFB_REF[00]</p> |

Table 16. CR#3: Control Register 3 (continued)

| Bit | Default                    | Name       | Description   |
|-----|----------------------------|------------|---|
| 9÷7 | 011                        | BST_FREQ   | Boost Frequency Clock selection bits (see <a href="#">Table 20</a> )  |
| 6   | 0                          | PWM_SYNC   | PWMSYNC:<br>0: PWM Counter not reset;<br>1: PWM Counter Reset (note that this bit is automatically reset after counter reset)   |
| 5÷4 | 00                         | B_IN_W1    | Buck Input Voltage Window for Buck1 (see <a href="#">Table 21</a> )   |
| 3÷2 | 00                         | B_IN_W2    | Buck Input Voltage Window for Buck2 (see <a href="#">Table 21</a> )   |
| 1   | Set by OTP<br>(DEF_BSTDIS) | BST_DIS    | BST_DIS can be set to 1 only if UNLOCK = 1; in other words, if the $\mu\text{C}$ tries to set this bit to 1 when UNLOCK = 0 it maintains its previous value.<br>BST_DIS can be reset to 0 also when UNLOCK = 0<br>0: Boost enabled<br>1: Boost disabled:<br>For disabling the boost It is necessary to send two distinct SPI frame as follows:<br>1 <sup>st</sup> SPI Register write: set UNLOCK bit to 1<br>2 <sup>nd</sup> SPI Register write: set BST_DIS to 1 |
| 0   |                            | Parity bit | ODD parity bit check  |

1. See [Table 2](#).

#### CR#4: Control Register 4

|         |          |    |        |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |            |
|---------|----------|----|--------|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|------------|
| 23      | 22       | 21 | 20     | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0          |
| WD_TRIG | Reserved |    | Unused |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | Parity bit |

**Address:** 0x04h

**Type:** R/W

Table 17. CR#4: Control Register 4

| Bit   | Default | Name       | Description  |
|-------|---------|------------|--|
| 23    | 0       | WD_TRIG    | In order to keep device in Active mode, this bit must be cyclically toggled within a period equal to $t_{WD}$ to refresh the watchdog. |
| 22÷21 | 00      | Reserved   | Note: when writing on this register, bit 21 and 22 must be set to 00   |
| 20÷1  |         | Unused     |  |
| 0     |         | Parity bit | ODD parity bit check   |

Table 18. Constant VLED x TOFF selection

| VLED_TOFF | Constant VLED x TOFF [V x $\mu$ s] |
|-----------|------------------------------------|
| 0000      | 10                                 |
| 0001      | 12                                 |
| 0010      | 14                                 |
| 0011      | 16                                 |
| 0100      | 18                                 |
| 0101      | 20                                 |
| 0110      | 22                                 |
| 0111      | 24                                 |
| 1000      | 28                                 |
| 1001      | 32                                 |
| 1010      | 36                                 |
| 1011      | 40                                 |
| 1100      | 48                                 |
| 1101      | 56                                 |
| 1110      | 64                                 |
| 1111      | 72                                 |

Table 19. DIN map table for Buck Cell X

| DIN_MAP X | Status of Buck Cell X |
|-----------|-----------------------|
| 00        | Always OFF            |
| 01        | PWM dimming           |
| 10        | Always ON             |
| 11        | Controlled by DIN     |

Table 20. Boost clock selection

| BST_FREQ | Boost clock [kHz] |
|----------|-------------------|
| 000      | 100               |
| 001      | 151.5             |
| 010      | 200               |
| 011      | 250               |
| 100      | 303               |
| 101      | 357               |
| 110      | 400               |
| 111      | 454.5             |

Table 21. Buck input voltage window

| B_IN_W | Buck In voltage range [V] |
|--------|---------------------------|
| 00     | 10÷25                     |
| 01     | 25÷40                     |
| 10     | 40÷50                     |
| 11     | 50÷60                     |

## 5.4.2 Status Register description

### SR#1: Status Register 1

|          |    |    |    |    |    |    |    |          |    |    |    |    |    |   |   |      |      |      |      |      |             |             |            |
|----------|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|------|------|------|------|------|-------------|-------------|------------|
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7    | 6    | 5    | 4    | 3    | 2           | 1           | 0          |
| VLED1,ON |    |    |    |    |    |    |    | VLED2,ON |    |    |    |    |    |   |   | SHT1 | SHT2 | OVT1 | TW12 | TW11 | TON_MIN_OP1 | TON_MIN_OP2 | Parity bit |
| R/C      |    |    |    |    |    |    |    |          |    |    |    |    |    |   |   |      |      |      | R    |      | R/C         |             |            |

**Address:** 0x05h

**Type:** R, R/C

**Table 22. SR#1: Status Register 1**

| Bit   | Default  | Name     | Description   | Access |
|-------|----------|----------|---|--------|
| 23÷16 | 00000000 | VLED1,ON | ADC conversion related to VLED1 (ranging from 0 V to 52.5 V), sampled during on time of Buck1.<br>Note that in case of Buck1 controlled by DIN pin or by SPI, the ADC is continuously refreshed during on-state, while, if controlled by internal PWM dimming generator, ADC refresh occurs only once per period just before the end of each PWM on-cycle.                      | R/C    |
| 15÷8  | 00000000 | VLED2,ON | ADC conversion related to VLED2 (ranging from 0 V to 52.5V), sampled during on time of Buck2.<br>Note that in case of Buck2 controlled by DIN pin or by SPI, the ADC is continuously refreshed during on-state, while, if controlled by internal PWM dimming generator, ADC refresh occurs only once per period just before the end of each PWM on-cycle.                       | R/C    |
| 7     | 0        | SHT1     | VLED1 short circuit detection.<br>This bit is set when TON_MIN_OP1 is set too but only if, at the same instant, average VLED1 voltage is lower than 1.5V.<br>When SHT1 = 1, Buck1 is disabled until a read and clear command of this bit has been acknowledged.<br>In LHM, an auto restart procedure cyclically clears this bit with a period equal to $t_{\text{AUTORESTART}}$ | R/C    |
| 6     | 0        | SHT2     | VLED2 short circuit detection.<br>This bit is set when TON_MIN_OP2 is set too but only if, at the same instant, average VLED2 voltage is lower than 1.5V.<br>When SHT2 = 1, Buck2 is disabled until a read and clear command of this bit has been acknowledged.   | R/C    |

Table 22. SR#1: Status Register 1 (continued)

| Bit | Default | Name        | Description  | Access |
|-----|---------|-------------|--|--------|
| 5   | 0       | OVT1        | <p>Overtemperature for Buck1<br/>(set when <math>T_j \geq T_{TSD}</math> for more than <math>t_{OVT}</math>);<br/>If this bit is set:</p> <ul style="list-style-type: none"> <li>– in Active mode: Buck1 is latched OFF; reset is performed by a R&amp;C command, which will be successful only if <math>T_j &lt; T_{TSD} - T_{TSD\_HYS}</math> (typ 140 °C). Then Buck1 is allowed to turn on again.</li> <li>– in LHM, after setting an OVT1, an auto restart procedure is implemented: every <math>t_{AUTORESTART}</math> OVT1 bit is automatically cleared and, if <math>T_j &lt; T_{TSD} - T_{TSD\_HYS}</math>, then Buck1 is allowed to turn on again, otherwise OVT1 bit is set again.</li> </ul> | R/C    |
| 4   | 0       | TW12        | <p>Thermal warning 2 for Buck1.<br/>This bit is set if <math>T_j \geq TW_2</math>.<br/>This is a read only and real time bit.<br/>When Buck1 temperature decreases under a second threshold (<math>T_j &lt; TW_2 - TW_{2\_HYS}</math>), this bit is cleared.</p>   | R      |
| 3   | 0       | TW11        | <p>Thermal warning 1 for Buck1.<br/>This bit is set if <math>T_j \geq TW_1</math>.<br/>This is a read only and real time bit.<br/>When Buck1 temperature decreases under a second threshold (<math>TW_1 - TW_{1\_HYS}</math>), this bit is cleared.</p>  | R      |
| 2   | 0       | TON_MIN_OP1 | <p>Operation at minimum on-time for Buck1.<br/>This bit is set when Buck1 runs at an on-time shorter than <math>t_{ON\_MIN\_BUCK}</math> for more than 32 (even not consecutive) cycles.<br/>When TON_MIN_OP1 = 1, Buck1 is disabled until a read and clear command of this bit has been acknowledged.<br/>In LHM, an auto restart procedure cyclically clears this bit with a period equal to <math>t_{AUTORESTART}</math>.</p>   | R/C    |
| 1   | 0       | TON_MIN_OP2 | <p>Operation at minimum on-time for Buck2.<br/>This bit is set when Buck2 runs at an on-time shorter than <math>t_{ON\_MIN\_BUCK}</math> for more than 32 (even not consecutive) cycles.<br/>When TON_MIN_OP2 = 1, Buck2 is disabled until a read and clear command of this bit has been acknowledged.</p>   | R/C    |
| 0   |         | Parity Bit  | ODD parity bit check   |        |



**SR#2: Status Register 2**

|      |      |      |             |             |             |           |           |         |       |           |           |           |           |            |         |             |        |        |   |   |   |            |   |
|------|------|------|-------------|-------------|-------------|-----------|-----------|---------|-------|-----------|-----------|-----------|-----------|------------|---------|-------------|--------|--------|---|---|---|------------|---|
| 23   | 22   | 21   | 20          | 19          | 18          | 17        | 16        | 15      | 14    | 13        | 12        | 11        | 10        | 9          | 8       | 7           | 6      | 5      | 4 | 3 | 2 | 1          | 0 |
| OVT2 | TW22 | TW21 | TON_MAX_OP1 | TON_MAX_OP2 | PWMCLK_FAIL | VSPI_FAIL | WD_STATUS | WD_FAIL | VS_UV | TOFF_MIN1 | TOFF_MIN2 | TOFF_MAX1 | TOFF_MAX2 | N_PWR_GOOD | BST_OVP | BST_FB_FAIL | DIN_ST | Unused |   |   |   | Parity bit |   |
| R/C  | R    |      | R/C         |             |             | R         |           | R/C     |       |           |           | R         |           |            |         | R/C         | R      |        |   |   |   |            |   |

**Address:** 0x06h**Type:** R, R/C**Table 23. SR#2: Status Register 2**

| Bit | Default | Name        | Description  | Access |
|-----|---------|-------------|--|--------|
| 23  | 0       | OVT2        | Overtemperature for Buck2 (set when $T_j \geq T_{TSD}$ for more than $t_{OVT}$ );<br>if this bit is set Buck2 is latched OFF; reset is performed by a R&C command, which will be successful only if $T_j < T_{TSD} - T_{TSD\_HYS}$ . Then Buck2 is allowed to turn on again.   | R/C    |
| 22  | 0       | TW22        | Thermal warning 2 for Buck2.<br>This bit is set if $T_j \geq TW_2$ .<br>This is a read only and real time bit.<br>When Buck2 temperature decreases under a second threshold ( $T_j < TW_2 - TW_{2\_HYS}$ ), this bit is cleared.   | R      |
| 21  | 0       | TW21        | Thermal warning 1 for Buck2.<br>This bit is set if $T_j \geq TW_1$ .<br>This is a read only and real time bit.<br>When Buck2 temperature decreases under a second threshold ( $TW_1 - TW_{1\_HYS}$ ), this bit is cleared.   | R      |
| 20  | 0       | TON_MAX_OP1 | Operation at maximum on-time for Buck1.<br>This bit is set when Buck1 runs at an on-time equal to $t_{ON\_MAX\_BUCK}$ for two consecutive cycles.<br>Every time this event occurs, Buck1 is temporarily switched off for a $t_{TON\_MAX\_OFF}$ time, then is enabled to switch on again.<br>Instead, TON_MAX_OP1 bit will be latched until a R&C.<br>In LHM, an auto restart procedure cyclically clears this bit with a period equal to $t_{AUTORESTART}$ . | R/C    |
| 19  | 0       | TON_MAX_OP2 | Operation at maximum on-time for Buck2.<br>This bit is set when Buck2 runs at an on-time equal to $t_{ON\_MAX\_BUCK}$ for two consecutive cycles.<br>Every time this event occurs, Buck2 is temporarily switched off for a $t_{TON\_MAX\_OFF}$ time, then is enabled to switch on again.<br>Instead, TON_MAX_OP2 bit will be latched until a R&C.  | R/C    |

Table 23. SR#2: Status Register 2 (continued)

| Bit   | Default | Name        | Description   | Access |
|-------|---------|-------------|---|--------|
| 18    | 0       | PWMCLK_FAIL | When this bit is set, a PWM Clock Fail is detected.<br>This occurs $F_{PWMCLK} \leq F_{PWMCLK\_FAIL}$ . In this case PWMCLK signal is bypassed by an internal fall back PWM frequency clock (having a frequency equal to $F_{FALLBACK\_CLK}$ ). PWMCLK normal operation will be restored after a R&C operation, when PWMCLK frequency $F_{PWMCLK} > F_{PWMCLK\_FAIL}$ . | R/C    |
| 17    | 0       | VSPI_FAIL   | VSPI failure bit<br>0: VSPI (external SPI Supply) present<br>1: VSPI not present (VSPI voltage lower than $V_{SPI\_UV}$ ): device goes to Limp Home Mode  | R      |
| 16÷15 | 00      | WD_STATUS   | Watchdog status bit: see <a href="#">Table 25</a>   | R      |
| 14    | 0       | WD_FAIL     | Watchdog failure bit:<br>0: watchdog OK;<br>1: watchdog failure in Active mode<br>When this bit is set, the device goes in Limp Home Mode   | R/C    |
| 13    | 0       | VS_UV       | VS undervoltage bit<br>0: $V_S > V_{S\_UV}$ ;<br>1: $V_S \leq V_{S\_UV}$  | R      |
| 12    | 0       | TOFF_MIN1   | Minimum off-time operation for Buck1<br>0: Off-time $\geq t_{OFF\_MIN\_BUCK}$<br>1: Off-time $< t_{OFF\_MIN\_BUCK}$   | R      |
| 11    | 0       | TOFF_MIN2   | Minimum off-time operation for Buck2<br>0: Off-time $\geq t_{OFF\_MIN\_BUCK}$<br>1: Off-time $< t_{OFF\_MIN\_BUCK}$   | R      |
| 10    | 0       | TOFF_MAX1   | Maximum off-time operation for Buck1:<br>0: Off-time $< t_{OFF\_MAX\_BUCK}$<br>1: Off-time $\geq t_{OFF\_MAX\_BUCK}$  | R      |
| 9     | 0       | TOFF_MAX2   | Maximum off-time operation for Buck2:<br>0: Off-time $< t_{OFF\_MAX\_BUCK}$<br>1: Off-time $\geq t_{OFF\_MAX\_BUCK}$  | R      |
| 8     | 0       | N_PWR_GOOD  | This bit reflects the status of signal boost power good (negative)<br>1: Output Boost voltage not reaching 92.5% of its target value<br>0: Output Boost voltage has reached 92.5% of its target value   | R      |
| 7     | 0       | BST_OVP     | Boost Overvoltage Protection.<br>This bit is set when $V_{FB} > V_{FB\_OV\_ON}$ for more than $t_{BST\_OVP}$ while is reset when $V_{FB} < V_{FB\_OV\_OFF}$ for more than $t_{BST\_OVP\_RST}$ .<br>If $BST\_DIS = 1$ then $BST\_OVP$ is not set.<br>If $BST\_FB\_FAIL = 1$ then $BST\_OVP$ is not set.  | R      |

Table 23. SR#2: Status Register 2 (continued)

| Bit | Default | Name        | Description   | Access |
|-----|---------|-------------|---|--------|
| 6   | 0       | BST_FB_FAIL | <p>Boost feedback pin failure.</p> <p>This bit is set when FB pin is shorted to ground.</p> <p>When this bit is set:</p> <ul style="list-style-type: none"> <li>– if Boost is in off-state, then it will not be allowed to start up;</li> <li>– if Boost is in on-state, then it will immediately switched OFF;</li> <li>– in both cases, no clock is delivered through SYNC_IO pin;</li> <li>– in addition, in Limp Home mode COMP pin will be pulled down.</li> </ul> <p>If BST_DIS = 1, BST_FB_FAIL bit will not be set.</p> <p>When BST_FB_FAIL = 1, Boost is disabled until a read and clear command of this bit has been acknowledged.</p> <p>In LHM, an auto restart procedure cyclically clears BST_FB_FAIL bit with a period equal to <math>t_{\text{AUTORESTART}}</math>.</p> | R/C    |
| 5   | 0       | DIN_ST      | <p>Direct input status bit.</p> <p>Filtered replica of logical level at DIN pin.</p> <p>Filtering time is equal to <math>t_{\text{DIN\_ST}}</math>.</p>   | R      |
| 4÷1 | 0000    | Unused      |   |        |
| 0   |         | Parity Bit  | ODD Parity Bit Check  |        |

**SR#3: Status Register 3**

|           |    |    |    |    |    |    |    |           |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |            |
|-----------|----|----|----|----|----|----|----|-----------|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|------------|
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |            |
| VLED1,OFF |    |    |    |    |    |    |    | VLED2,OFF |    |    |    |    |    |   |   | Unused |   |   |   |   |   |   |   | Parity bit |
| R/C       |    |    |    |    |    |    |    |           |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |            |

**Address:** 0x07h**Type:** R/C**Table 24. SR#3: Status Register 3**

| Bit   | Default  | Name       | Description   | Access |
|-------|----------|------------|---|--------|
| 23÷16 | 00000000 | VLED1,OFF  | ADC conversion related to VLED1 (ranging from 0 V to 52.5 V), sampled during off-time of Buck1.<br>Note that in case of Buck1 controlled by DIN pin or by SPI, the ADC is continuously refreshed during off-state, while, if controlled by internal PWM dimming generator, ADC refresh occurs only once per period just before the end of each PWM off-cycle. | R/C    |
| 15÷8  | 00000000 | VLED2,OFF  | ADC conversion related to VLED2 (ranging from 0 V to 52.5 V), sampled during off-time of Buck2.<br>Note that in case of Buck1 controlled by DIN pin or by SPI, the ADC is continuously refreshed during off-state, while, if controlled by internal PWM dimming generator, ADC refresh occurs only once per period just before the end of each PWM off-cycle. | R/C    |
| 7÷1   | 0000000  | Unused     |   |        |
| 0     |          | Parity Bit | ODD Parity Bit Check  |        |

**Table 25. Watchdog status**

| WD_STATUS | WD timer status |
|-----------|-----------------|
| 00        | [0...24%]       |
| 01        | [24% ... 50%]   |
| 10        | [50% ... 74%]   |
| 11        | [74% ... 100%]  |

### 5.4.3 Customer test and trimming registers description

#### CT: Customer Trimming Register

|              |    |    |             |    |          |    |               |    |        |            |     |          |    |   |   |   |   |   |   |   |   |            |   |
|--------------|----|----|-------------|----|----------|----|---------------|----|--------|------------|-----|----------|----|---|---|---|---|---|---|---|---|------------|---|
| 23           | 22 | 21 | 20          | 19 | 18       | 17 | 16            | 15 | 14     | 13         | 12  | 11       | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1          | 0 |
| CTM_TRIM_COD |    |    | DEF_HLEDCUR |    | DEF_DAC1 |    | DEF_VLEDTOFF1 |    | DEF_MS | DEF_BSTDIS | EOT | Reserved |    |   |   |   |   |   |   |   |   | Parity bit |   |

**Address:** 0x3Eh

**Type:** R/W

Write operation allowed only when CTM\_TRIM\_COD = 100 and EOT = 0

**Table 26. CT: Ctm Trimming Register**

| Bit   | Default     | Name          | Comment  |
|-------|-------------|---------------|--|
| 23÷21 | 000         | CTM_TRIM_COD  | Operation Code for Trimming Operation:<br>011: Execute blank check read<br>100: Execute selected bit burning<br>010: Execute margin mode read<br>011: Execute blank check read<br>111: Execute end of trimming<br>001: Execute standard read |
| 20÷19 | 00          | DEF_HLEDCUR   |  |
| 18÷17 | 00          | DEF_DAC1      |  |
| 16÷15 | 00          | DEF_VLEDTOFF1 |  |
| 14    | 0           | DEF_MS        |  |
| 13    | 0           | DEF_BSTDIS    |  |
| 12    | 0           | EOT           | End of Ctm Trimming  |
| 11÷1  | 00000000000 | —             | Reserved   |
| 0     |             | Parity Bit    | ODD Parity Bit Check   |

## 5.4.4 Customer test and trimming procedure description

### General description

The writing procedure is performed connecting the two terminals of the anti-fuse capacitor at 15 V and ground respectively. This is achieved by providing 15V on VS battery pin.

After this phase, the capacitor is burnt and behaves like a resistance; its value (the residual resistance) strictly depends on the effectiveness of the burning procedure. During physical reading operation, the residual resistance is compared with a fixed threshold. If the residual resistance is greater than threshold a bit 0 is given, and the OTP cell is considered unwritten, otherwise a bit 1 is given and the OTP cell is considered written.

Blank check reading is executed to verify that all anti-fuses are unwritten after fabrication, while margin mode, usually performed immediately after the burning process, is used to verify if burned cells are properly written. Executing a blank-check reading after all writing operations have been completed allows verifying that unwritten cells haven't been degraded by burning processes.

### Recommended test flow

In [Figure 10](#) and in [Table 28](#) the recommended testing procedure is shown and described.

Testing procedure starts with a blank check read, to verify that all anti-fuse rows are unwritten. After this operation, it is possible to select the bits to be written and to start programming. Writing operation should be performed up to 3 times. At the end of programming, a reading procedure should be performed in Margin Mode.

At the end of the test, it is strongly recommended executing a blank-check read in order to verify that unwritten cells haven't been degraded.

[Table 27](#) summarizes the writing test conditions.

**Table 27. Writing test conditions**

| Symbol   | Parameter                     | Conditions | Min | Typ | Max | Unit |
|----------|-------------------------------|------------|-----|-----|-----|------|
| VS       | 15 V supply                   |            |     | 15  |     | V    |
| $I_{HV}$ | HV current during programming |            |     |     | 28  | mA   |
| —        | Temperature                   |            | -40 | 27  | 150 | °C   |
| —        | External capacitance          |            | 2   | 5   | 10  | nF   |

*Note:* An external capacitance must be applied between VS and GROUND pins.

Figure 10. Testing flow chart

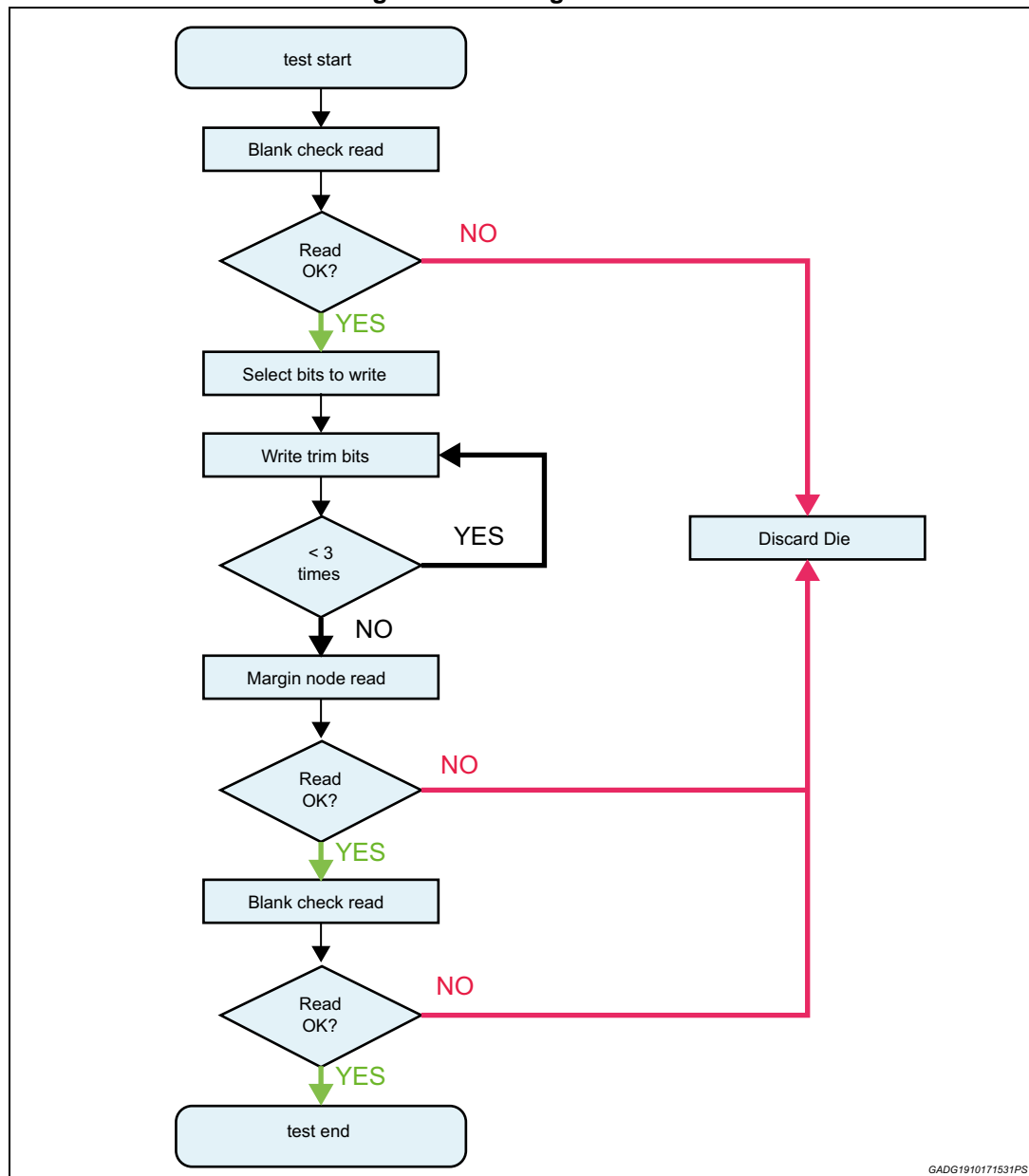


Table 28. Testing procedure description

| Step                   | Description  | Action   | SPI Frames (binary, unless otherwise specified)   |
|------------------------|--|--|---|
| Blank Check (load)     | In this step, antifuses are compared with a higher resistance than the standard one - to be sure they are initially unburned. Their content is loaded into bits (20÷13) of CTM register.   | Send an SPI write to CTM   | 00 111110 011<br>00000000000000000000             |
| Blank Check (read)     | During previous step, the result of Blank Check Read is loaded into bits (20÷13) of CTM register. A read operation is required this result.  | Send an SPI read for customer trimming register and analyze the SDO frame received from device   | 01 111110 000<br>000000000000000000001            |
| Blank Check (decision) | A decision must be taken, based on the previous result. If antifuses were damaged, device must be discarded, otherwise the flow can proceed.   | If the answer to previous SPI read is different from <b>xx0000xx</b> , then device must be discarded   | -   |
| Select bits to write   | Desired setting for default values of some control bits must be chosen. Let's assume that the chosen 8 bit word is: <i>ctm</i> , corresponding to the 8 bits of CTM from 20 to 13 (DEF_HLEDCUR + DEF_DAC1 + DEF_VLEDTOFF1 + DEF_MS + DEF_BSTDIS).  | Select 8 bit word to write ( <i>ctmd</i> )   | -   |
| Burn (X3)              | In this step, selected word (i.e. <i>ctmd</i> ) must be written in the OTPs. <b>This step must be repeated three times.</b> It is recommended to wait the completion of a burn operation before starting the following one. Time required to burn one word depends on the number of fuses to be burned and it is equal to: <b>2.85 <math>\mu</math>s + 401 <math>\mu</math>s * &lt;number of selected bits&gt;</b> | Prepare the right external setup (see Table 27, "Writing test conditions").<br>Send an SPI write to CTM. Selected word must be placed in bits (20÷13) of CTM.<br>Last bit depends on odd parity check. | 00 111110 100<br>[ <i>ctmd</i> ]0000000000000000x |
| End Of Trimming (X3)   | In this step, end of trimming antifuse is burned. <b>This step must be repeated three times.</b> It is recommended to wait the completion of a burn operation before starting the following one. Time required to burn one bit is almost equal to: <b>404<math>\mu</math>s</b>   | Send an SPI write to CTM   | 00 111110 111<br>000000000000000000001            |



Table 28. Testing procedure description (continued)

| Step                         | Description  | Action   | SPI Frames (binary, unless otherwise specified) |
|------------------------------|--|--|---|
| Margin Mode (load)           | In this step, antifuses are compared with a lower resistance than the standard one - to be sure selected bits are properly burned. Their content is loaded into CTM register.      | Send an SPI write to CTM   | 00 111110 010<br>00000000000000000000           |
| Margin Mode (read)           | During previous step, the result of MM Read is loaded into the most significant 16 bits of each corresponding trimming register. A read operation is required to read this result. | Send an SPI read for customer trimming register and analyze the SDO frame received from device   | 01 111110 000<br>00000000000000000001           |
| Margin Mode (decision)       | A decision must be taken, based on the previous result. If antifuses were not correctly burned after three steps, then device must be discarded, otherwise the flow can proceed.   | If the answer to SPI read operation is different from:<br><b>xxxxxxx</b><br><b>[ctm]100000000000</b><br><b>x</b> , then device must be discarded.<br>Last bit depends on odd parity check. | -   |
| Final Blank Check (load)     | In this step, antifuses are compared with a higher resistance than the standard one - to be sure unselected bits are really unburned. Their content is loaded in CTM register.     | Send an SPI write to CTM   | 00 111110 011<br>00000000000000000000           |
| Final Blank Check (read)     | During previous step, the result of Blank Check Read is loaded into bits (20÷13) of CTM register. A read operation is required for each of them to read this result.               | Send an SPI read for customer trimming register and analyze the SDO frame received from device   | 01 111110 000<br>00000000000000000001           |
| Final Blank Check (decision) | A decision must be taken, based on the previous result. If antifuses were damaged, device must be discarded, otherwise the flow can proceed.                                       | If the answer to SPI read operation is different from: <b>xxxxxxx</b><br><b>[ctm]100000000000</b><br><b>x</b> , then device must be discarded.<br>Last bit depends on odd parity check.    | -   |

Table 29. Default peak current selection for Buck Cell 1

| DEF_DAC1 | DAC1 (default value) | $I_{L1\_Peak}$ [A]<br>(HLED_CUR1 = 1) | $I_{L1\_Peak}$ [A]<br>(HLED_CUR1 = 0) |
|----------|----------------------|---------------------------------------|---------------------------------------|
| 00       | 100000               | 0.809                                 | 0.402                                 |
| 01       | 000000               | 0.362                                 | 0.179                                 |
| 10       | 110001               | 1.235                                 | 0.632                                 |
| 11       | 111111               | 1.695                                 | 0.849                                 |

Table 30. Default VLEDxTOFF Selection for Buck Cell 1

| DEF_VLEDTOFF1 | VLED_TOFF1           |
|---------------|----------------------|
| 00            | 1111 (72 V* $\mu$ s) |
| 01            | 1011 (40 V* $\mu$ s) |
| 10            | 0101 (20 V* $\mu$ s) |
| 11            | 0000 (10 V* $\mu$ s) |

## 6 Electrical specifications

### 6.1 Absolute maximum ratings

Stressing the device above the rating listed in the [Table 31](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 31. Absolute maximum ratings**

| Symbol  | Parameter  | Value                     | Unit |
|---|--|---------------------------|------|
| $V_S$   | Battery supply voltage                               | -0.3 to 40                | V    |
| $V_{SPI}$   | Supply voltage of the SPI interface                  | -0.3 to 6.5               | V    |
| $V_{5V}$  | 5V Voltage Regulator Capacitor Output                | -0.3 to 6.5               | V    |
| $V_{3V3}$   | 3.3V Voltage Regulator Capacitor Output              | -0.3 to 4.6               | V    |
| $V_{CSN}, V_{SDI}, V_{SCK}$                         | SPI pins voltage                                     | -0.3 to 6.5               | V    |
| $V_{SDO}$   | SPI pin voltage                                      | -0.3 to $V_{SPI} + 0.3$   | V    |
| $V_{CBOOT1}, V_{CBOOT2}$                            | Buck-related high voltage pins                       | -0.3 to 65                | V    |
| $V_{CBOOT1}-V_{LX1},$<br>$V_{CBOOT2}-V_{LX2}$       | Buck MOSFET overdrive                                | -0.3 to 4.6               | V    |
| $V_{BUCKIN1}, V_{BUCKIN2},$<br>$V_{LED1}, V_{LED2}$ | Buck input and output pins voltage                   | -0.3 to 62                | V    |
| $V_{LX1}, V_{LX2}$                                  | Buck switching node pins voltage                     | -1.0 to 62                | V    |
| $I_{VLEDx}$   | $V_{LEDx}$ pins maximum injected current             | 0.1                       | mA   |
| $V_{DIN}$   | Direct input pin voltage                             | -0.3 to 6.5               | V    |
| $V_{PWMCLK}$  | Clock input pin (for internal PWM dimming generator) | -0.3 to 6.5               | V    |
| $V_{SYNC\_I/O}$                                     | Boost synchronization I/O pin                        | -0.3 to $V_{3V3} + 0.3$   | V    |
| $V_{G0}$  | Boost gate driver pin voltage                        | -0.3 to $V_{5V} + 0.3$    | V    |
| $V_{SP}$  | Boost sense positive pin voltage                     | $-0.3 \div V_{3V3} + 0.3$ | V    |
| $V_{SN}$  | Boost sense negative pin voltage                     | $-0.3 \div 1$             | V    |
| $V_{COMP}$  | Boost compensation network pin voltage               | $-0.3 \div V_{3V3} + 0.3$ | V    |
| $V_{FB}$  | Boost feedback pin voltage                           | $-0.3 \div V_{3V3} + 0.3$ | V    |
| $T_j$   | Junction operating temperature                       | -40 to 150                | °C   |
| $T_{STG}$   | Storage temperature                                  | -55 to 150                | °C   |

## 6.2 ESD protection

Table 32. ESD protection

| Parameter                         | Value | Unit |
|-----------------------------------|-------|------|
| All pins <sup>(1)</sup>           | ±2    | kV   |
| All output pins <sup>(2)</sup>    | ±4    | kV   |
| All pins (Charge Device Model)    | ±500  | V    |
| Corner pins (Charge Device Model) | ±750  | V    |

1. HBM (human body model, 100 pF, 1.5 kΩ) according to MIL 883C, Method 3015.7 or EIA/JESD22A114-A.

2. HBM with all none zapped pins grounded, output pins are VS, DIN, VLED1, VLED2.

## 6.3 Thermal characteristics

Table 33. QFN40L 6x6 thermal resistance

| Symbol              | Parameter  | Min | Typ | Max | Unit |
|---------------------|--|-----|-----|-----|------|
| $R_{thj-amb}^{(1)}$ | Thermal resistance junction to ambient (JEDEC JESD 51-2) | —   | 32  | —   | °C/W |
| $R_{thj-board}$     | Thermal resistance junction to board (JEDEC JESD 51-8)   | —   | 11  | —   | °C/W |
| $R_{thj-case}$      | Junction-to-case thermal resistance                      | —   | 7.2 | —   | °C/W |

1. Device mounted on four layers 2s2p PCB (thermally enhanced, slug included).

Table 34. Thermal characteristics

| Symbol         | Parameter                            | Min | Typ | Max | Unit |
|----------------|--------------------------------------|-----|-----|-----|------|
| $T_{J\_OP}$    | Operating junction temperature       | -40 |     | 150 | °C   |
| $TW_1$         | Junction temperature warning 1       | 120 | 130 | 140 | °C   |
| $TW_{1\_HYS}$  | Temperature warning 1 hysteresis     |     | 30  |     | °C   |
| $TW_2$         | Junction temperature warning 2       | 130 | 140 | 150 | °C   |
| $TW_{2\_HYS}$  | Temperature warning 2 hysteresis     |     | 10  |     | °C   |
| $T_{TSD}$      | Junction thermal shutdown            | 155 | 165 | 175 | °C   |
| $T_{TSD\_HYS}$ | Junction thermal shutdown hysteresis |     | 25  |     | °C   |

## 6.4 Electrical characteristics

$5.5\text{ V} < V_S < 24\text{ V}$ ,  $-40\text{ }^{\circ}\text{C} < T_J < 150\text{ }^{\circ}\text{C}$ , unless otherwise specified.

The device is still operative and functional at higher temperatures (up to  $175\text{ }^{\circ}\text{C}$ ).

*Note: Parameters limits at higher temperatures than  $150\text{ }^{\circ}\text{C}$  may change respect to what is specified as per the standard temperature range.*

*Device functionality at high temperature is guaranteed by characterization.*

### 6.4.1 Supply

**Table 35. Supply**

| Symbol          | Parameter                               | Test conditions   | Min  | Typ  | Max  | Unit          |
|-----------------|---|---|------|------|------|---------------|
| $V_{SPI}$       | Digital I/O supply voltage              |   | 3.0  |      | 5.5  | V             |
| $V_{SPI,UV}$    | $V_{SPI}$ under voltage                 |   | 2.0  | 2.5  | 3.0  | V             |
| $I_{SPI,STBY}$  | $V_{SPI}$ standby current               | Device in standby mode<br>$V_{SPI} = 5.0\text{ V}$  |      | 1    | 2    | $\mu\text{A}$ |
| $I_{SPI,Q}$     | $V_{SPI}$ quiescent current             | Device operating<br>$V_{SPI} = 5.0\text{ V}$  |      |      | 3    | mA            |
| $V_S$           | Operating $V_S$ supply voltage          |   | 5.5  |      | 24   | V             |
| $V_{S,UV,L}$    | $V_S$ under voltage shutdown low limit  | $V_{SPI} = 5\text{ V}$ ; Ramp on $V_S$ from $5.5\text{ V}$ to $4.4\text{ V}$  | 4.5  |      | 5    | V             |
| $V_{S,UV,H}$    | $V_S$ under voltage shutdown high limit | $V_{SPI} = 5\text{ V}$ ; Ramp on $V_S$ from $4.4\text{ V}$ to $5.85\text{ V}$   |      | 5.3  | 5.6  | V             |
| $V_{S,UV,HYST}$ | $V_S$ under voltage hysteresis          |   |      | 0.5  |      | V             |
| $I_S$           | $V_S$ operating current                 | $V_S = 13.5\text{ V}$ ;<br>Boost ON at $F_{SW} = 250\text{ KHz}$ ;<br>Buck1 and Buck2 ON;<br>$V_{BUCKIN1} = V_{BUCKIN2} = V_{BOOST} = 25\text{ V}$<br>$I_{OUT1} = I_{OUT2} = 250\text{ mA}$ |      | 30   |      | mA            |
| $I_{S,Q}$       | $V_S$ quiescent current                 | $V_{SPI} = 5\text{ V}$ , $V_S = 13.5\text{ V}$ ; Boost and buck disabled  |      | 7    | 16   | mA            |
| $I_{S,STBY}$    | $V_S$ standby current                   | Device in standby mode;<br>$V_S = 13.5\text{ V}$  |      | 6    | 10   | $\mu\text{A}$ |
| $V_{POR,H}$     | Power-on reset high state               | Ramp on $V3V3$ from $3.3\text{ V}$ to $2\text{ V}$  | 2.7  | 2.8  | 2.9  | V             |
| $V_{POR,L}$     | Power-on reset low state                | Ramp on $V3V3$ from $2\text{ V}$ to $3.3\text{ V}$  | 2.65 | 2.75 | 2.85 | V             |
| $V_{POR,HYST}$  | Power-on reset hysteresis               |   |      | 0.05 |      | V             |
| $V_{3V3}$       | Output voltage of $3V3$ LDO             | $V_S = 13\text{ V}$ , $C_{out} = 220\text{ nF}$   | 3.1  | 3.3  | 3.5  | V             |

## 6.4.2 Boost controller

**Table 36. Boost gate driver**

| Symbol         | Parameter                             | Test conditions   | Min                | Typ | Max      | Unit |
|----------------|---------------------------------------|---|--------------------|-----|----------|------|
| $t_{G0}$       | Gate driver output rise and fall time | $V_S = 13\text{ V}$ ; $CG0 = 4.7\text{ nF}$ ; $VGS\_G0$ rising from 10% ÷ 90%   |                    | 25  | 75       | ns   |
|                |                                       | $V_S = 13\text{ V}$ ; $CG0 = 4.7\text{ nF}$ ; $VGS\_G0$ falling from 90% ÷ 10%  |                    | 25  | 75       | ns   |
| $V_{G0\_H}$    | Gate driver High output voltage       |   | $0.9 \cdot V_{5V}$ |     | $V_{5V}$ | V    |
| $V_{G0\_L}$    | Gate driver Low output voltage        |   |                    |     | 0.3      | V    |
| $V_{5V}$       | Output Voltage of 5V LDO              | $V_S = 13\text{ V}$ ; $C_{out} = 4.7\text{ }\mu\text{F}$ ,<br>External maximum load current:<br>$I_{load} = 10\text{ mA}$ | 4.75               | 5   | 5.25     | V    |
| $I_{5V}^{(1)}$ | Current capability of 5V LDO          | $V_S = 13\text{ V}$<br>Output of 5V LDO connected to ground   | 30                 | 45  | 60       | mA   |

1.  $I_{5V} = Q_{tgate} \times F_{boost\_sw}$  (external MOSFET total gate charge multiplied by boost switching frequency).

**Table 37. Boost controller**

| Symbol               | Parameter  | Test conditions   | Min | Typ | Max | Unit |
|----------------------|--|---|-----|-----|-----|------|
| $F_{BOOST\_SW\_MAX}$ | Boost maximum operative switching frequency  | CR#3<9:7> (000)b ÷ (111)b                                     |     | 450 |     | kHz  |
| $F_{BOOST\_SW\_MIN}$ | Boost minimum operative switching frequency  | CR#3<9:7> (000)b ÷ (111)b                                     |     | 100 |     | kHz  |
| $F_{BOOST\_STEP}$    | Boost Switching Frequency Step   |   |     | 50  |     | kHz  |
| $F_{BOOST\_ACC}$     | Boost Switching Frequency accuracy   | $T = 125\text{ }^\circ\text{C}$                               | -5  |     | 5   | %    |
| $V_{BOOST\_LIM}$     | Boost maximum current sense differential voltage (SP, SN pin) for current limitation | $V_S = 13\text{ V}$<br>Boost enabled                          | 350 | 390 | 430 | mV   |
| $t_{BOOST\_MIN}$     | Minimum boost on-time  | $V_S = 13\text{ V}$ ; SP pin = 3.3 V<br>Boost enabled         |     | 200 | 600 | ns   |
| $D_{BOOST\_MAX}$     | Boost maximum duty cycle   | $V_S = 13\text{ V}$ ; SP pin = 0 V<br>Boost enabled           |     | 90  |     | %    |
| $V_{5V\_DROP}$       | Min voltage drop of 5V LDO respect to $V_S$ :<br>$V_{5V\_DROP} = (V_S - V_{5V})$     | $I(5V5) = -1\text{ mA}$                                       |     | 0.1 | 0.3 | V    |
| $t_{SS}$             | Soft start duration  | Guaranteed by scan and frequency oscillator (20 MHz, typical) |     | 8   |     | ms   |

Table 37. Boost controller (continued)

| Symbol      | Parameter   | Test conditions   | Min | Typ  | Max | Unit             |
|-------------|---|---|-----|------|-----|------------------|
| $G_M$       | Error amplifier trans conductance gain              | $V_{FB} - V_{FB\_REF}[11] = \pm 35 \text{ mV}$ ;<br>$V_{COMP} = 1.5 \text{ V}$ ; $V_S = 13 \text{ V}$ ;<br>$I_{OUT} = \pm 20 \mu\text{A}$ |     | 570  |     | $\mu\Omega^{-1}$ |
| $I_{COMP}$  | Trans conductance amplifier Output current          | Sourcing into COMP pin;<br>$V_{FB} = 3.3 \text{ V}$ ; $V_S = 13 \text{ V}$  |     | 110  |     | $\mu\text{A}$    |
|             |   | Sinking from COMP pin;<br>$V_{FB} = 0 \text{ V}$ ; $V_S = 13 \text{ V}$   |     | -110 |     | $\mu\text{A}$    |
| $G_{LA}$    | Gain of linear amplifier                            | $V_S = 13 \text{ V}$ ; $V_{SP} = 250 \text{ mV}$ ;<br>$V_{SN} = 0 \text{ V}$  |     | 4.25 |     | V/V              |
| $I_{SLOPE}$ | Slope compensation current value injected to SP pin |   |     | 20   |     | A/s              |

Table 38. Boost controller reference voltage

| Symbol                  | Parameter                                 | BOOSTREF [1:0]                      | Min    | Typ                            | Max    | Unit |
|-------------------------|---|-------------------------------------|--------|--------------------------------|--------|------|
| $V_{FB\_REF}[00]$       | Boost feedback reference voltage          | [0,0]                               |        | 0.596                          |        | V    |
| $V_{FB\_REF}[01]$       |   | [0,1]                               |        | 0.895                          |        | V    |
| $V_{FB\_REF}[10]$       |   | [1,0]                               |        | 1.242                          |        | V    |
| $V_{FB\_REF}[11]$       |   | [1,1]                               |        | 1.496                          |        | V    |
| $V_{FB\_REF\_ACC}$      | Boost feedback reference voltage accuracy | all configuration                   | -2     |                                | 2      | %    |
| $V_{FB\_OV\_ON}$        | Boost OV activation threshold             | [1,1]                               | Typ-3% | $1.03 * V_{FB\_REF}[11]$       | Typ+3% | V    |
|                         |   | [x,x]                               |        | $1.05 * V_{FB\_REF}[xx]^{(1)}$ |        |      |
| $V_{FB\_OV\_OFF}$       | Boost OV de-activation threshold          | [x,x]                               |        | $V_{FB\_REF}[xx]$              |        | V    |
| $V_{BST\_FB\_FAIL\_TH}$ | Boost feedback pin failure - threshold    | Ramp on FB pin from 1 V down to 0 V |        | 90                             | 130    | mV   |

1. "xx" <> "11".

### 6.4.3 Buck

Table 39. Buck converter power stage

| Symbol                                       | Parameter                                | Test conditions  | Min   | Typ | Max  | Unit |
|--|--|--|-------|-----|------|------|
| $V_{\text{BUCKIN1}}$<br>$V_{\text{BUCKIN2}}$ | Buck input voltage range                 |  | $V_S$ |     | 60   | V    |
| $I_{\text{Lx\_PEAK}}$                        | Accuracy of the inductor peak current    | Low RDSon Mode;<br>$T_j \geq 25\text{ }^\circ\text{C}$   | -4.5  |     | 4.5  | %    |
|  |  | Low RDSon Mode;<br>$T_j < 25\text{ }^\circ\text{C}$<br>DAC code $\geq 26$  | -6    |     | 6    | %    |
|  |  | High RDSon Mode;<br>$T_j \geq 25\text{ }^\circ\text{C}$<br>DAC code $\geq 26$  | -4.5  |     | 4.5  | %    |
|  |  | High RdsOn Mode;<br>$T_j \geq 25\text{ }^\circ\text{C}$<br>DAC code $< 26$   | -6    |     | 6    | %    |
|  |  | High RdsOn Mode;<br>$T_j < 25\text{ }^\circ\text{C}$<br>DAC code $\geq 26$   |       |     |      |      |
| $V_{\text{LED\_SHT}}$                        | Buck short circuit activation threshold  | Ramp on $V_{\text{LEDx}}$ from 52.5 V to 0 V   | 1.2   | 1.7 | 2.2  | V    |
| $R_{\text{DSon}}$                            | Buck MOSFET $R_{\text{DSon}}$            | High $R_{\text{DS\_ON}}$ mode;<br>$V_{\text{BUCKINx}} = 45\text{ V}$ ;<br>$I_{\text{OUT}} = 350\text{ mA}$ ; $T_j = 25\text{ }^\circ\text{C}$  |       |     | 800  | mΩ   |
|  |  | Low $R_{\text{DS\_ON}}$ mode;<br>$V_{\text{BUCKINx}} = 45\text{ V}$ ;<br>$I_{\text{OUT}} = 700\text{ mA}$ ; $T_j = 25\text{ }^\circ\text{C}$   |       |     | 400  | mΩ   |
| $R_{\text{DSon}}$                            | Buck MOSFET $R_{\text{DSon}}$            | High $R_{\text{DS\_ON}}$ mode;<br>$V_{\text{BUCKINx}} = 45\text{ V}$ ;<br>$I_{\text{OUT}} = 350\text{ mA}$ ; $T_j = 150\text{ }^\circ\text{C}$ |       |     | 1300 | mΩ   |
|  |  | Low $R_{\text{DS\_ON}}$ mode;<br>$V_{\text{BUCKINx}} = 40\text{ V}$ ;<br>$I_{\text{OUT}} = 700\text{ mA}$ ; $T_j = 150\text{ }^\circ\text{C}$  |       |     | 650  | mΩ   |
| $(dV_{\text{Lx}}/dt)_{\text{ON}}$            | LX Turn on voltage slope                 |  |       | 2.4 |      | V/ns |
| $(dV_{\text{Lx}}/dt)_{\text{OFF}}$           | LX Turn off voltage slope                |  |       | 2.4 |      | V/ns |
| $t_{\text{Blank\_Buck}}$                     | Buck Blanking Time                       |  |       | 200 |      | ns   |
| $t_{\text{STARTUP}}$                         | Buck startup phase duration              |  |       | 400 |      | μs   |
| $N_{\text{ton\_min\_fail}}$                  | Number of failure counter cycle          |  |       | 32  |      |      |
| $N_{\text{ton\_min\_fail\_reset}}$           | Reset of number of failure counter cycle |  |       | 10  |      |      |



Table 39. Buck converter power stage (continued)

| Symbol                  | Parameter   | Test conditions  | Min   | Typ  | Max   | Unit       |
|-------------------------|---|--|-------|------|-------|------------|
| $t_{TONMAX\_OFF}$       | Buck off time after detection of two consecutive $T_{ON\_MAX}$ operation  |  |       | 64   |       | $\mu s$    |
| $t_{DELAY}$             | Time delay before: to switch on Buckx (Boost Disable or No power good); to switch off Boost ( $V_S$ undervoltage)           |  |       | 10   |       | ms         |
| $t_{LOOP\_DELAY\_BUCK}$ | Buck loop delay   |  |       | 190  |       | ns         |
| $t_{ON\_MIN\_BUCK}$     | Operative Buck converter minimum on-time  |  | 400   |      |       | ns         |
| $t_{ON\_MAX\_BUCK}$     | Operative Buck converter maximum on-time  |  |       | 20   |       | $\mu s$    |
| $t_{OFF\_MIN\_BUCK}$    | Operative Buck converter minimum off-time   |  | 500   |      |       | ns         |
| $t_{OFF\_MAX\_BUCK}$    | Operative Buck converter maximum off-time   |  |       | 10   |       | $\mu s$    |
| $I_{Lx\_Peak}$          | Inductor Peak Current Reference Range (see <a href="#">Table 40</a> and figures <a href="#">11</a> and <a href="#">12</a> ) | Low $I_{Lx\_PEAK}$ current range; High $R_{DS(on)}$ mode   | 0.179 |      | 0.849 | A          |
|                         |   | High $I_{Lx\_PEAK}$ current range; Low $R_{DS(on)}$ mode   | 0.362 |      | 1.695 |            |
| VLED_RES                | VLED input impedance  |  |       | 425  |       | k $\Omega$ |
| ADC_RES                 | ADC resolution  |  |       | 8    |       | bits       |
| ADC_CONV_TIME           | VLED1 ADC refresh time  | Full conversion of 8 bits<br>$V_S = 13.5\text{ V}$<br>$V_{SPI} = 5\text{ V}$<br>$V_{LEDx} = 10\text{ V}$ |       | 3.6  |       | $\mu s$    |
|                         | VLED2 ADC refresh time  |  |       |      |       |            |
| ADC_FS                  | ADC full scale for VLED measurement   |  |       | 52.5 |       | V          |
| ADC_INL                 | ADC Integral Non Linearity  |  | -2    |      | 2     | LSB        |
| ADC_DNL                 | ADC Differential Non Linearity  |  | -2    |      | 2     | LSB        |

Note: The values shown in the [Table 40](#) are in accordance to the CR#2<23:18> and CR#2<17:12> configuration; see [Section 5.4](#)

Table 40. Inductor peak current selection

| DAC code | DAC code 5 | DAC code 4 | DAC code 3 | DAC code 2 | DAC code 1 | DAC code 0 | IL_PEAK [A]<br>Low RDSON | IL_PEAK [A]<br>High RDSON |
|----------|------------|------------|------------|------------|------------|------------|--------------------------|---------------------------|
| 0        | 0          | 0          | 0          | 0          | 0          | 0          | 0.362                    | 0.179                     |
| 1        | 0          | 0          | 0          | 0          | 0          | 1          | 0.369                    | 0.183                     |
| 2        | 0          | 0          | 0          | 0          | 1          | 0          | 0.376                    | 0.186                     |
| 3        | 0          | 0          | 0          | 0          | 1          | 1          | 0.384                    | 0.19                      |
| 4        | 0          | 0          | 0          | 1          | 0          | 0          | 0.392                    | 0.194                     |
| 5        | 0          | 0          | 0          | 1          | 0          | 1          | 0.401                    | 0.198                     |
| 6        | 0          | 0          | 0          | 1          | 1          | 0          | 0.41                     | 0.203                     |
| 7        | 0          | 0          | 0          | 1          | 1          | 1          | 0.419                    | 0.208                     |
| 8        | 0          | 0          | 1          | 0          | 0          | 0          | 0.429                    | 0.213                     |
| 9        | 0          | 0          | 1          | 0          | 0          | 1          | 0.44                     | 0.218                     |
| 10       | 0          | 0          | 1          | 0          | 1          | 0          | 0.451                    | 0.223                     |
| 11       | 0          | 0          | 1          | 0          | 1          | 1          | 0.462                    | 0.229                     |
| 12       | 0          | 0          | 1          | 1          | 0          | 0          | 0.474                    | 0.235                     |
| 13       | 0          | 0          | 1          | 1          | 0          | 1          | 0.487                    | 0.243                     |
| 14       | 0          | 0          | 1          | 1          | 1          | 0          | 0.499                    | 0.248                     |
| 15       | 0          | 0          | 1          | 1          | 1          | 1          | 0.513                    | 0.255                     |
| 16       | 0          | 1          | 0          | 0          | 0          | 0          | 0.527                    | 0.261                     |
| 17       | 0          | 1          | 0          | 0          | 0          | 1          | 0.542                    | 0.269                     |
| 18       | 0          | 1          | 0          | 0          | 1          | 0          | 0.557                    | 0.276                     |
| 19       | 0          | 1          | 0          | 0          | 1          | 1          | 0.572                    | 0.284                     |
| 20       | 0          | 1          | 0          | 1          | 0          | 0          | 0.588                    | 0.292                     |
| 21       | 0          | 1          | 0          | 1          | 0          | 1          | 0.598                    | 0.297                     |
| 22       | 0          | 1          | 0          | 1          | 1          | 0          | 0.615                    | 0.305                     |
| 23       | 0          | 1          | 0          | 1          | 1          | 1          | 0.632                    | 0.314                     |
| 24       | 0          | 1          | 1          | 0          | 0          | 0          | 0.649                    | 0.322                     |
| 25       | 0          | 1          | 1          | 0          | 0          | 1          | 0.668                    | 0.332                     |
| 26       | 0          | 1          | 1          | 0          | 1          | 0          | 0.686                    | 0.34                      |
| 27       | 0          | 1          | 1          | 0          | 1          | 1          | 0.706                    | 0.35                      |
| 28       | 0          | 1          | 1          | 1          | 0          | 0          | 0.725                    | 0.36                      |
| 29       | 0          | 1          | 1          | 1          | 0          | 1          | 0.745                    | 0.37                      |
| 30       | 0          | 1          | 1          | 1          | 1          | 0          | 0.766                    | 0.38                      |
| 31       | 0          | 1          | 1          | 1          | 1          | 1          | 0.787                    | 0.39                      |

Table 40. Inductor peak current selection (continued)

| DAC code | DAC code 5 | DAC code 4 | DAC code 3 | DAC code 2 | DAC code 1 | DAC code 0 | IL_PEAK [A]<br>Low RDSON | IL_PEAK [A]<br>High RDSON |
|----------|------------|------------|------------|------------|------------|------------|--------------------------|---------------------------|
| 32       | 1          | 0          | 0          | 0          | 0          | 0          | 0.809                    | 0.402                     |
| 33       | 1          | 0          | 0          | 0          | 0          | 1          | 0.831                    | 0.413                     |
| 34       | 1          | 0          | 0          | 0          | 1          | 0          | 0.853                    | 0.424                     |
| 35       | 1          | 0          | 0          | 0          | 1          | 1          | 0.877                    | 0.436                     |
| 36       | 1          | 0          | 0          | 1          | 0          | 0          | 0.9                      | 0.447                     |
| 37       | 1          | 0          | 0          | 1          | 0          | 1          | 0.924                    | 0.46                      |
| 38       | 1          | 0          | 0          | 1          | 1          | 0          | 0.938                    | 0.471                     |
| 39       | 1          | 0          | 0          | 1          | 1          | 1          | 0.963                    | 0.483                     |
| 40       | 1          | 0          | 1          | 0          | 0          | 0          | 0.987                    | 0.496                     |
| 41       | 1          | 0          | 1          | 0          | 0          | 1          | 1.013                    | 0.509                     |
| 42       | 1          | 0          | 1          | 0          | 1          | 0          | 1.039                    | 0.521                     |
| 43       | 1          | 0          | 1          | 0          | 1          | 1          | 1.066                    | 0.535                     |
| 44       | 1          | 0          | 1          | 1          | 0          | 0          | 1.093                    | 0.549                     |
| 45       | 1          | 0          | 1          | 1          | 0          | 1          | 1.12                     | 0.562                     |
| 46       | 1          | 0          | 1          | 1          | 1          | 0          | 1.148                    | 0.576                     |
| 47       | 1          | 0          | 1          | 1          | 1          | 1          | 1.177                    | 0.59                      |
| 48       | 1          | 1          | 0          | 0          | 0          | 0          | 1.205                    | 0.605                     |
| 49       | 1          | 1          | 0          | 0          | 0          | 1          | 1.235                    | 0.62                      |
| 50       | 1          | 1          | 0          | 0          | 1          | 0          | 1.265                    | 0.635                     |
| 51       | 1          | 1          | 0          | 0          | 1          | 1          | 1.295                    | 0.65                      |
| 52       | 1          | 1          | 0          | 1          | 0          | 0          | 1.326                    | 0.665                     |
| 53       | 1          | 1          | 0          | 1          | 0          | 1          | 1.357                    | 0.681                     |
| 54       | 1          | 1          | 0          | 1          | 1          | 0          | 1.389                    | 0.696                     |
| 55       | 1          | 1          | 0          | 1          | 1          | 1          | 1.421                    | 0.713                     |
| 56       | 1          | 1          | 1          | 0          | 0          | 0          | 1.453                    | 0.729                     |
| 57       | 1          | 1          | 1          | 0          | 0          | 1          | 1.486                    | 0.746                     |
| 58       | 1          | 1          | 1          | 0          | 1          | 0          | 1.52                     | 0.762                     |
| 59       | 1          | 1          | 1          | 0          | 1          | 1          | 1.554                    | 0.78                      |
| 60       | 1          | 1          | 1          | 1          | 0          | 0          | 1.588                    | 0.797                     |
| 61       | 1          | 1          | 1          | 1          | 0          | 1          | 1.623                    | 0.814                     |
| 62       | 1          | 1          | 1          | 1          | 1          | 0          | 1.658                    | 0.832                     |
| 63       | 1          | 1          | 1          | 1          | 1          | 1          | 1.695                    | 0.849                     |

Figure 11. IL\_PEAK vs DAC code - Low  $R_{dson}$

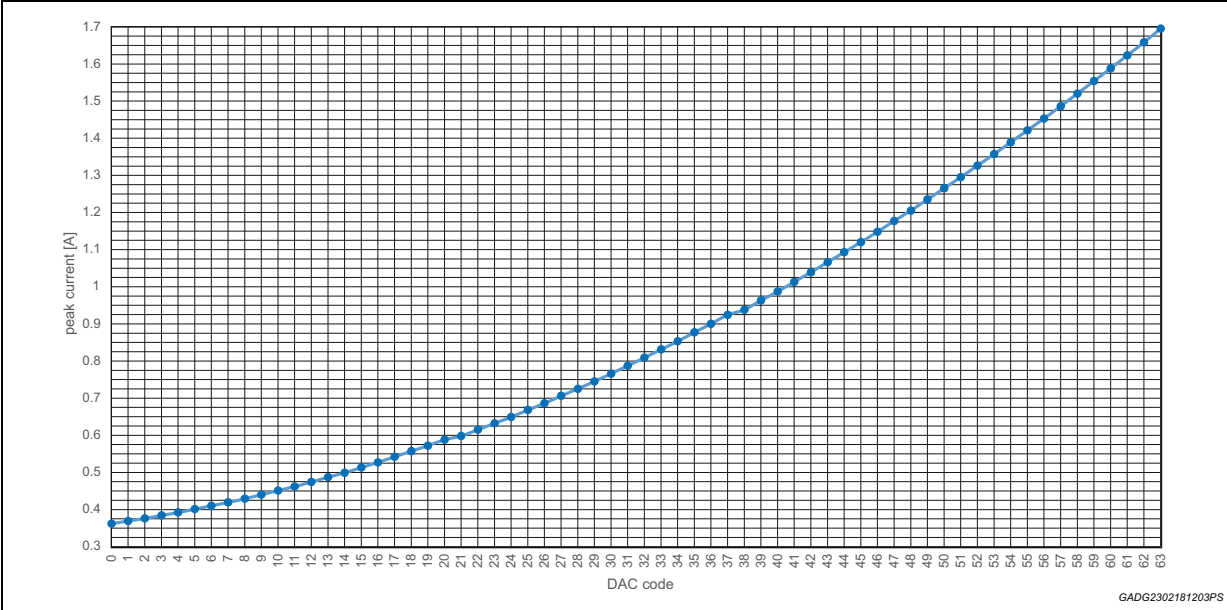


Figure 12. IL\_PEAK vs DAC code - High  $R_{dson}$

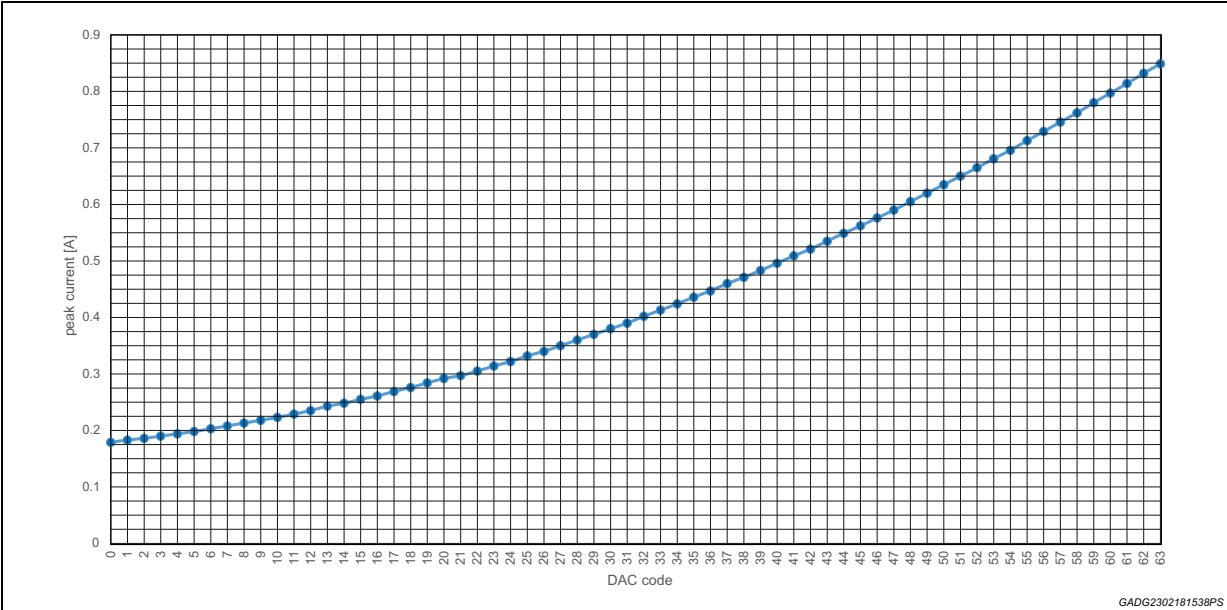
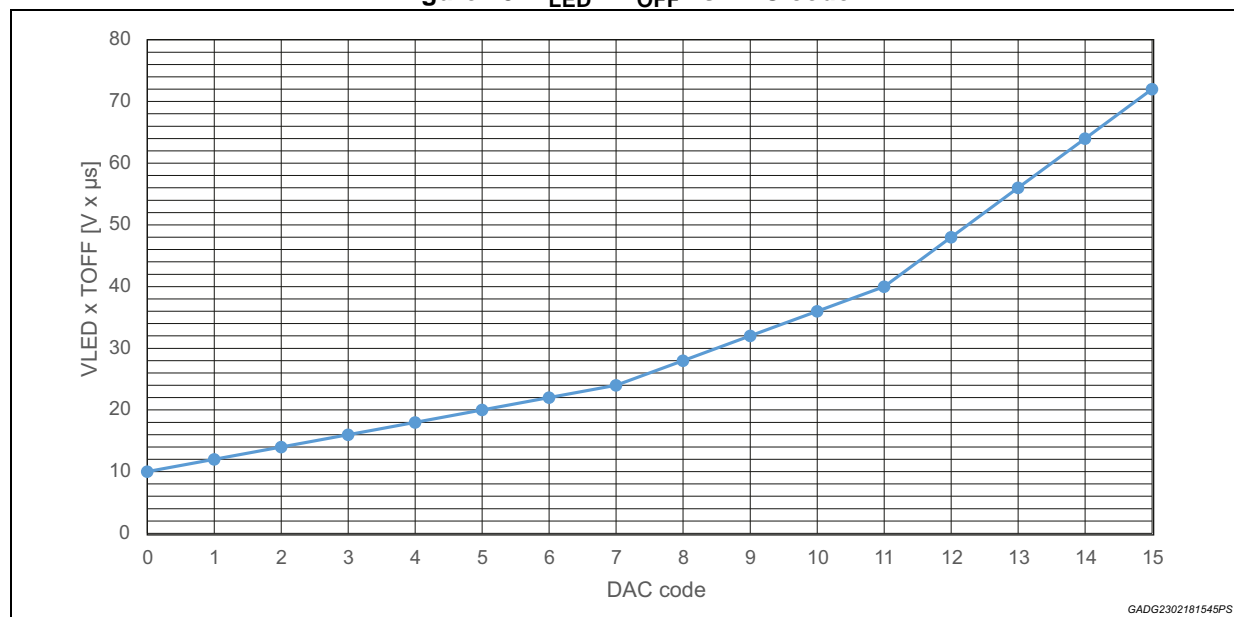


Table 41. VLEDxTOFF constants

| Symbol                         | Parameter  | Test conditions                                 | Min  | Typ | Max | Unit |
|--------------------------------|--|---|------|-----|-----|------|
| VLEDxTOFF1<br>OR<br>VLEDxTOFF2 | Constant product led<br>output voltage off time<br>(see <a href="#">Figure 13</a> -<br>parameter vs DAC<br>code) | CR#2<11:8> OR CR#2<7:4> = [0000]b               | —    | 10  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [0001]b               | —    | 12  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [0010]b               | —    | 14  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [0011]b               | —    | 16  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [0100]b               | —    | 18  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [0101]b               | —    | 20  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [0110]b               | —    | 22  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [0111]b               | —    | 24  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [1000]b               | —    | 28  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [1001]b               | —    | 32  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [1010]b               | —    | 36  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [1011]b               | —    | 40  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [1100]b               | —    | 48  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [1101]b               | —    | 56  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [1110]b               | —    | 64  | —   | V*μs |
|                                |  | CR#2<11:8> OR CR#2<7:4> = [1111]b               | —    | 72  | —   | V*μs |
| VLEDxTOFFx                     | Accuracy   | $V_{LED\_SHTmin} \leq V_{LEDx} \leq 5\text{ V}$ | -13  | —   | 13  | %    |
|                                |  | $5\text{ V} < V_{LEDx} \leq 7\text{ V}$         | -9.5 | —   | 9.5 |      |
|                                |  | $V_{LEDx} > 7\text{ V}$                         | -8   | —   | 8   |      |

Figure 13.  $V_{LED} \times T_{OFF}$  vs DAC code

## 6.4.4 SPI

Table 42. SPI signal description

| Symbol   | Parameter                       | Test conditions           | Min             | Typ           | Max             | Unit          |
|----------|---------------------------------|---------------------------|-----------------|---------------|-----------------|---------------|
| CSN      | Chip Select Not                 | High State                | $0.7 * V_{3V3}$ | —             | $V_{3V3}$       | V             |
|          |                                 | Low State                 | —               | —             | $0.3 * V_{3V3}$ |               |
| SCK      | Serial Clock                    | High State                | $0.7 * V_{3V3}$ | —             | $V_{3V3}$       | V             |
|          |                                 | Low State                 | —               | —             | $0.3 * V_{3V3}$ |               |
| SDI      | Serial data Input               | High State                | $0.7 * V_{3V3}$ | —             | $V_{3V3}$       | V             |
|          |                                 | Low State                 | —               | —             | $0.3 * V_{3V3}$ |               |
| SDO      | Serial data Output - High State | $I_{OUT} = -1 \text{ mA}$ | $V_{SPI-0.5}$   | $V_{SPI-0.2}$ | —               | V             |
|          | Serial data Output - Low State  | $I_{OUT} = 1 \text{ mA}$  | —               | 0.2           | 0.5             |               |
| $I_{LK}$ | Output leakage current          | —                         | -1              | —             | 1               | $\mu\text{A}$ |

Note: See also [Chapter 5: SPI functional description](#).

Table 43. SPI timings

| Symbol          | Parameter                                 | Test conditions  | Min | Typ | Max | Unit          |
|-----------------|---|--|-----|-----|-----|---------------|
| $T_{sck}$       | Serial clock (SCK) period                 |  | 250 |     |     | ns            |
| $T_{Hsck}$      | SCK high time                             |  | 100 |     |     | ns            |
| $T_{Lsck}$      | SCK low time                              |  | 100 |     |     | ns            |
| $T_{rise\_in}$  | CSN, SCK, SDI rise time                   | $F_{sck} = 4 \text{ MHz}$                                  |     |     | 25  | ns            |
| $T_{fall\_in}$  | CSN, SCK, SDI fall time                   | $F_{sck} = 4 \text{ MHz}$                                  |     |     | 25  | ns            |
| $T_{Hcsn}$      | CSN high time                             |  | 6   |     |     | $\mu\text{s}$ |
| $T_{Scsn}$      | CSN setup time, CSN low before SCK rising |  | 100 |     |     | ns            |
| $T_{Ssck}$      | SCK setup time, SCK low before CSN rising |  | 100 |     |     | ns            |
| $T_{Ssdi}$      | SDI setup time before SCK rising          |  | 25  |     |     | ns            |
| $T_{hold\_sdi}$ | SDI hold time                             |  | 25  |     |     | ns            |
| $T_{csn\_v}$    | CSN falling until SDO valid               | $C_{out} = 50 \text{ pF};$<br>$I_{out} = \pm 1 \text{ mA}$ |     |     | 100 | ns            |
| $T_{csn\_v}$    | CSN rising until SDO tristate             | $C_{out} = 50 \text{ pF};$<br>$I_{out} = \pm 4 \text{ mA}$ |     |     | 100 | ns            |
| $T_{sck\_v}$    | SCK falling until SDO valid               | $C_{out} = 50 \text{ pF}$                                  |     |     | 60  | ns            |
| $T_{Rsdo}$      | SDO rise time                             | $C_{out} = 50 \text{ pF};$<br>$I_{out} = -1 \text{ mA}$    |     | 50  | 100 | ns            |

Table 43. SPI timings (continued)

| Symbol            | Parameter       | Test conditions  | Min | Typ | Max | Unit |
|-------------------|-----------------|--|-----|-----|-----|------|
| $T_{Fsd0}$        | SDO fall time   | $C_{out} = 50 \text{ pF};$<br>$I_{out} = 1 \text{ mA}$ |     | 50  | 100 | ns   |
| $T_{csn\_low\_t}$ | CSN low timeout |  | 20  | 35  | 50  | ms   |

### 6.4.5 Direct input

Table 44. Direct Input pin limits

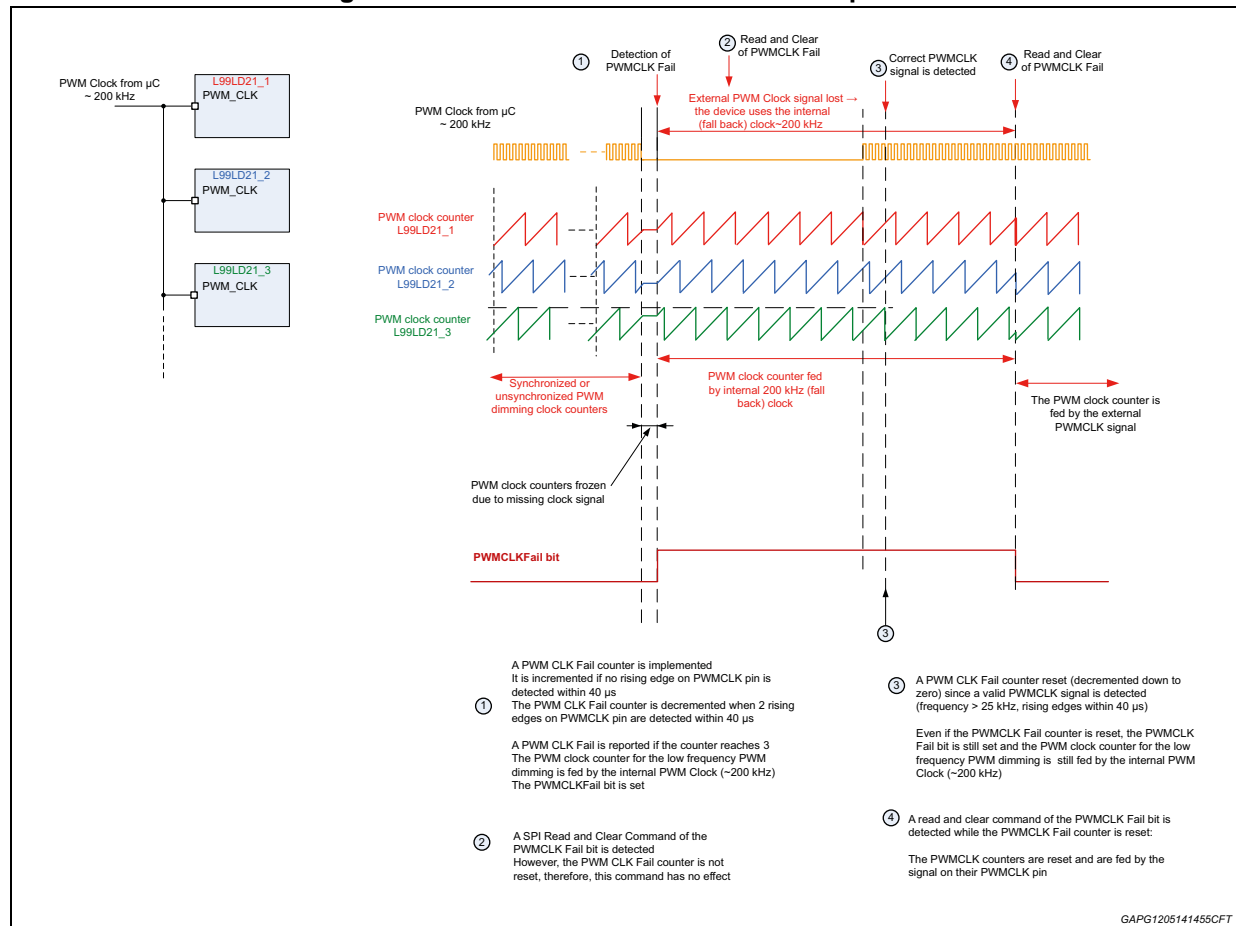
| Symbol       | Parameter          | Test conditions | Min          | Typ | Max          | Unit |
|--------------|--------------------|-----------------|--------------|-----|--------------|------|
| $V_{DIN\_L}$ | DIN Low threshold  |                 |              | —   | $0.3 * V3V3$ | V    |
| $V_{DIN\_H}$ | DIN High threshold |                 | $0.7 * V3V3$ | —   | V3V3         | V    |

## 6.4.6 PWM dimming

Table 45. PWMCLK and Fall back PWM description

| Symbol              | Parameter                             | Test conditions | Min             | Typ | Max             | Unit |
|---------------------|---------------------------------------|-----------------|-----------------|-----|-----------------|------|
| $V_{PWMCLK\_L}$     | PWMCLK low threshold                  |                 |                 |     | $0.3 * V_{3V3}$ | V    |
| $V_{PWMCLK\_H}$     | PWMCLK high threshold                 |                 | $0.7 * V_{3V3}$ |     | $V_{3V3}$       | V    |
| $F_{PWMCLK}$        | PWMCLK input frequency range          |                 | 102400          |     | 409600          | Hz   |
| $F_{PWMCLK\_FAIL}$  | PWMCLK frequency fail detection range |                 | 0               |     | 26500           | Hz   |
| $F_{FALLBACK\_CLK}$ | Fall back PWM frequency clock         |                 | 190             | 200 | 210             | KHz  |

Figure 14. PWM clock failure and reset sequence





## 6.4.7 Digital timings

Table 46. Digital timings description

| Symbol                | Parameter  | Test conditions  | Min | Typ  | Max | Unit    |
|-----------------------|--|--|-----|------|-----|---------|
| $t_{WD}$              | Watchdog timeout period  |  | 45  | 50   | 55  | ms      |
| $t_{CSN\_TIMEOUT}$    | CSN timeout  |  | 90  | 115  | 140 | ms      |
| $t_{AUTORESTART}$     | Autorestart time in limp home mode   |  | 45  | 50   | 55  | ms      |
| $t_{VS,UV}$           | VS undervoltage filter time  |  |     | 32   |     | $\mu s$ |
| $t_{DIN\_FT}^{(1)}$   | DIN Filter time  |  |     | 32   |     | $\mu s$ |
| $t_{DIN\_ST}$         | DIN status information time  |  |     | 12.8 |     | $\mu s$ |
| $t_{SKEW}$            | Timing skew for DIN  |  |     |      | 2.5 | $\mu s$ |
| $t_{VSPI\_FT}$        | VSPI Filtering Time  |  |     | 32   |     | $\mu s$ |
| $t_{WAKE\_UP}$        | Time for a complete wake up ( $V_{3V3} > V_{POR\_L}$ )   | CSN low or DIN high for $t > t_{WAKEUP}$<br>Cap on V3V3 = 4.7 $\mu F$<br>$V_{3V3} > 3 V$ |     | 190  |     | $\mu s$ |
| $t_{STDBY}$           | Time needed for a transition to standby mode ( $V_{3V3} < V_{POR\_L}$ )                              | DIN low<br>Cap on V3V3 = 4.7 $\mu F$<br>$V_{3V3} < 2.5 V$                                |     | 1.6  |     | ms      |
| $t_{OVT}$             | Filtering time for overtemperature (OVT bit will be set if $T_j > T_{TSD}$ for more than $t_{OVT}$ ) | guaranteed by frequency oscillator (20 MHz typical) and scan                             |     | 1.2  |     | $\mu s$ |
| $t_{BST\_OVP}$        | BST_OVP flag set filtering time  |  |     | 32   |     | $\mu s$ |
| $t_{BST\_OVP\_RST}$   | BST_OVP flag reset filtering time  |  |     | 10   |     | ms      |
| $t_{BOOST\_FB\_FAIL}$ | BST_FB_FAIL flag set filtering time  |  |     | 1.6  |     | $\mu s$ |

1. Digital timings guaranteed by scan. WD and autorestart timings limits added to give indication on application cases.

## 7 Package and PCB thermal data

### 7.1 QFN-40L 6x6 thermal data

Figure 15. QFN-40L 6x6 on four-layers PCB

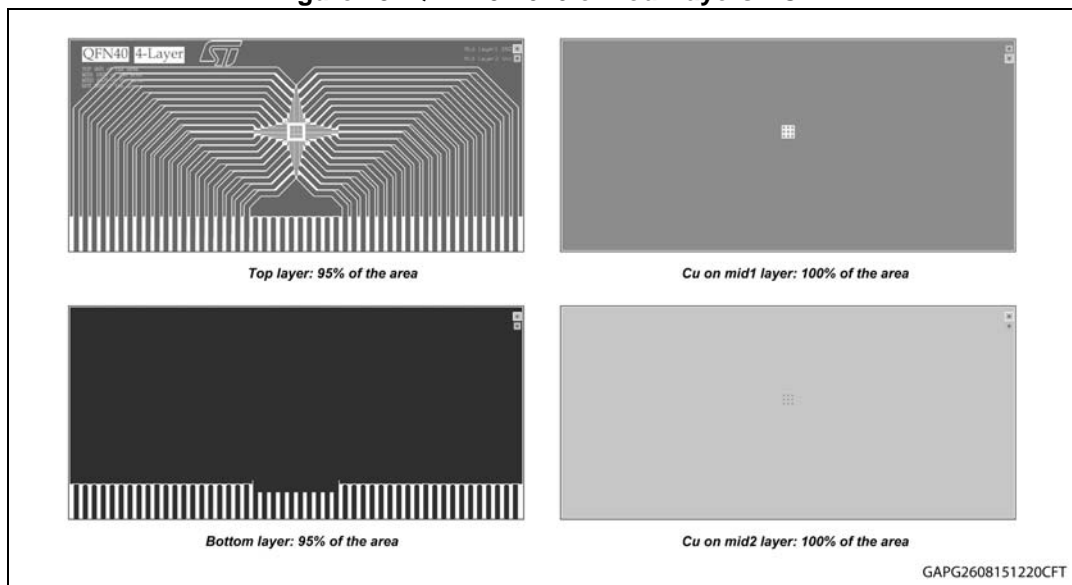


Table 47. PCB properties

| Dimension                       | Value              |
|---------------------------------|--------------------|
| Board finish thickness          | 1.6 mm +/- 10%     |
| Board dimension                 | 129 mm x 60 mm     |
| Board Material                  | FR4                |
| Copper thickness (outer layers) | 0.070 mm           |
| Copper thickness (inner layers) | 0.035 mm           |
| Thermal vias separation         | 1.2 mm             |
| Thermal via diameter            | 0.3 mm +/- 0.08 mm |
| Copper thickness on vias        | 0.025 mm           |

## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK® is an ST trademark.

### 8.1 QFN-40L 6x6 package information

Figure 16. QFN-40L 6x6 package dimensions

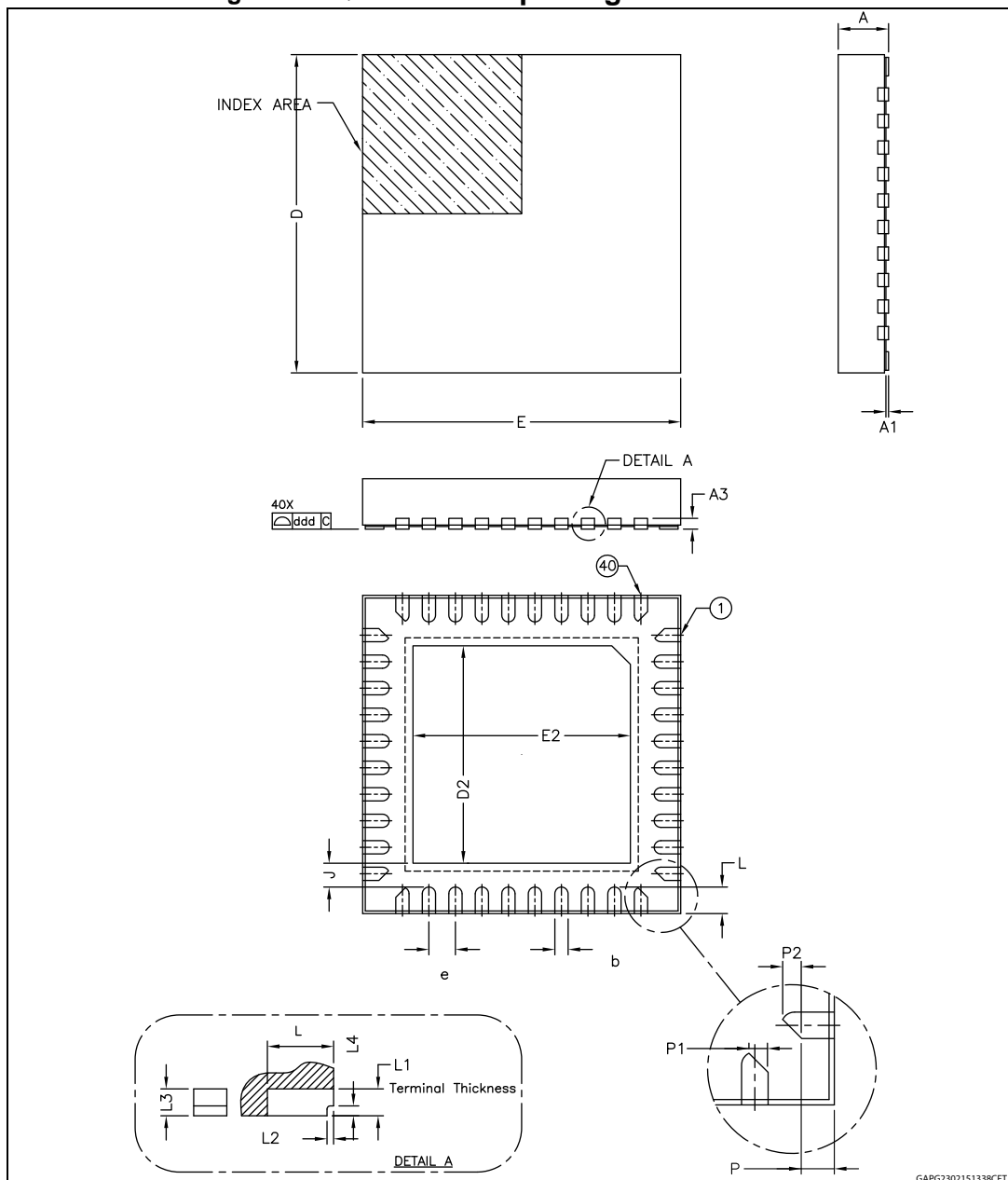


Table 48. QFN-40L 6x6 mechanical data

| Symbol | Min  | Typ   | Max  |
|--------|------|-------|------|
| A      | 0.85 | 0.95  | 1.05 |
| A1     | 0    |       | 0.05 |
| A3     |      | 0.20  |      |
| b      | 0.20 | 0.25  | 0.30 |
| D      | 5.85 | 6.00  | 6.15 |
| E      | 5.85 | 6.00  | 6.15 |
| D2     | 3.95 | 4.10  | 4.25 |
| E2     | 3.95 | 4.10  | 4.25 |
| e      |      | 0.50  |      |
| J      |      | 0.45  |      |
| L      | 0.40 | 0.50  | 0.60 |
| L1     |      | 0.20  |      |
| L2     |      | 0.05  |      |
| L3     |      | 0.20  |      |
| L4     |      | 0.075 |      |
| P      |      | 0.31  |      |
| P1     |      | 0.18  |      |
| P2     |      | 0.18  |      |
| ddd    |      | 0.08  |      |

## 9 Order codes

**Table 49. Device summary**

| Package     | Order code |               |
|-------------|------------|---------------|
|             | Tube       | Tape and reel |
| QFN-40L 6x6 | L99LD21Q6  | L99LD21Q6TR   |

## Appendix A Glossary

**Table 50. Glossary**

| Acronym | Description                           |
|---------|---------------------------------------|
| μC      | Microcontroller                       |
| ADC     | Analog / Digital converter            |
| ASSP    | Application Specific Standard Product |
| CPHA    | Clock Phase                           |
| CPOL    | Clock Polarity                        |
| CSN     | Chip select not (normal low) (SPI)    |
| CTRL    | Control register                      |
| FE      | Functional Error                      |
| FS      | Fail Safe                             |
| GE      | Device Error                          |
| GSB     | Global Status Byte                    |
| GSBN    | Global Status Bit Not                 |
| GW      | Global Warning                        |
| I/O     | Input /Output pins                    |
| DIN     | Direct input                          |
| LH      | Limp Home                             |
| LSB     | Least Significant Bit                 |
| MCU     | Mirocontroller                        |
| SDI     | SPI Data Input (slave)                |
| SDO     | SPI Data Onput (slave)                |
| MSB     | Most Significant Bit                  |

## Revision history

**Table 51. Document revision history**

| Date        | Revision | Changes   |
|-------------|----------|---|
| 03-Jul-2015 | 1        | Initial release.  |
| 28-Sep-2015 | 2        | <p>Updated <a href="#">Features</a> and <a href="#">Description</a></p> <p>Updated following sections:</p> <ul style="list-style-type: none"> <li>– <a href="#">Chapter 1: Introduction</a></li> <li>– <a href="#">Section 1.1: Typical application</a></li> <li>– <a href="#">Section 2.3: Output voltage setting</a></li> <li>– <a href="#">Section 2.4: Overvoltage protection</a></li> </ul> <p>Added <a href="#">Section 2.5: Feedback failure protection</a></p> <p>Updated following sections:</p> <ul style="list-style-type: none"> <li>– <a href="#">Section 2.6: Operation in dual phase interleaved mode</a></li> <li>– <a href="#">Section 2.7: Soft start</a></li> <li>– <a href="#">Section 2.8: Slope compensation</a></li> <li>– <a href="#">Section 2.9: Operation together with the buck converters</a></li> <li>– <a href="#">Section 3.1: General description</a></li> <li>– <a href="#">Section 3.3: Peak and average current setting</a></li> <li>– <a href="#">Section 3.4: Buck converter's blank time</a></li> <li>– <a href="#">Section 3.5: Buck converter's start-up</a></li> <li>– <a href="#">Section 3.6: Switching frequency</a></li> <li>– <a href="#">Section 4.1: Operating modes</a></li> <li>– <a href="#">Section 4.1.4: Limp home</a></li> <li>– <a href="#">Section 4.2.2: PWM dimming</a></li> <li>– <a href="#">Section 4.3.1: Temperature warning</a></li> <li>– <a href="#">Section 4.3.2: Overtemperature shutdown</a></li> </ul> <p>Added following sections:</p> <ul style="list-style-type: none"> <li>– <a href="#">Section 4.3.4: Buck <math>T_{ON}</math> minimum operation</a></li> <li>– <a href="#">Section 4.3.6: Buck <math>T_{ON}</math> maximum operation</a></li> <li>– <a href="#">Section 4.3.7: Buck Open Load detection</a></li> </ul> <p>Removed "Open load" section</p> <p>Updated following sections:</p> <ul style="list-style-type: none"> <li>– <a href="#">Chapter 5: SPI functional description</a></li> <li>– <a href="#">Section 6.1: Absolute maximum ratings</a></li> <li>– <a href="#">Chapter 6.3: Thermal characteristics</a></li> <li>– <a href="#">Chapter 6.4: Electrical characteristics</a></li> </ul> <p>Added <a href="#">Chapter 7: Package and PCB thermal data</a></p> <p>Added <a href="#">Section 8.1: QFN-40L 6x6 package information</a></p> <p>Updated <a href="#">Chapter 9: Order codes</a></p> |

Table 51. Document revision history (continued)

| Date        | Revision | Changes   |
|-------------|----------|---|
| 13-Mar-2018 | 3        | <p>Datasheet status promoted from preliminary data to production data.<br/> Removed in cover page the image of the TQFP-48 package.<br/> Updated:</p> <ul style="list-style-type: none"> <li>– Features and description in cover page;</li> <li>– <i>Section 1: Introduction on page 8;</i></li> <li>– <i>Figure 1: Functional block diagram on page 9;</i></li> <li>– <i>Figure 2: Typical application schematic on page 10</i></li> <li>– <i>added Figure 3: Application diagram on page 10;</i></li> <li>– <i>removed TQFP48 connection diagram;</i></li> <li>– <i>removed column “TQFP48” on Table 1: Pin functionality;</i></li> <li>– <i>Section 2.5: Feedback failure protection;</i></li> <li>– <i>Section 2.7: Soft start;</i></li> <li>– <i>Section 3.1: General description on page 18;</i></li> <li>– <i>Section 3.3: Peak and average current setting</i></li> <li>– <i>Section 4.1.1: Standby mode;</i></li> <li>– <i>Section 4.1.2: Pre-standby mode;</i></li> <li>– <i>Section 4.2.2: PWM dimming</i></li> <li>– <i>Table 13: ROM memory map;</i></li> <li>– <i>Section 5.4.1: Control Register description;</i></li> <li>– <i>Section 5.4.2: Status Register description;</i></li> <li>– <i>Section 5.4.3: Customer test and trimming registers description;</i></li> <li>– <i>Section 5.4.4: Customer test and trimming procedure description;</i></li> <li>– <i>Section 6: Electrical specifications</i></li> <li>– <i>removed “TQFP-48L thermal data” in Section 7: Package and PCB thermal data;</i></li> <li>– <i>removed “TQFP-48L package information” in Section 8: Package information;</i></li> <li>– <i>removed reference to TQFP48 package in Section 9: Order codes.</i></li> </ul> |
| 10-May-2018 | 4        | Updated equation in <i>Section 2.3: Output voltage setting</i> . Updated <i>Table 37</i> .  |
| 25-Jul-2018 | 5        | Updated <a href="#">Figure 9: Device state diagram</a> .  |



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