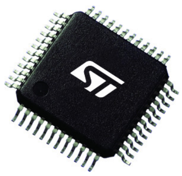
L9966

Datasheet

FlexInput IC for automotive applications



TQFP48 (7x7 mm)

Features

- AEC-Q100 qualified
- 12 V and 24 V systems compatible (operating battery supply voltage 5.5 V-36 V)
- Programmable interface with 15 total inputs:
  - 12 for connection to external analog loads (with connection to VVAR, VDD5 and clamped battery VPRE, with resistance measurement)
    - 4 with also λ sensor functionality
    - 4 with also SENT functionality
  - 3 for connection to external digital switches (with connection to VPRE)
- Programmable pull-up/down current sources
- Integrated precise resistance measurements
- 12-bit ADC for voltage measurements
- 15-bit ADC for resistance measurements
- Variable reluctance sensor / Hall sensor Interface
- 1 analog output channel + 4 digital output channels
- SPI interface for device configuration and data communication
- Overtemperature protection
- Thermal resistance $R_{th(j-c)}$ = 3 K/W

Product status link
L9966

Product summary	
Order code	L9966CB-TR
Package	TQFP48
Packing	Tape and reel

Description

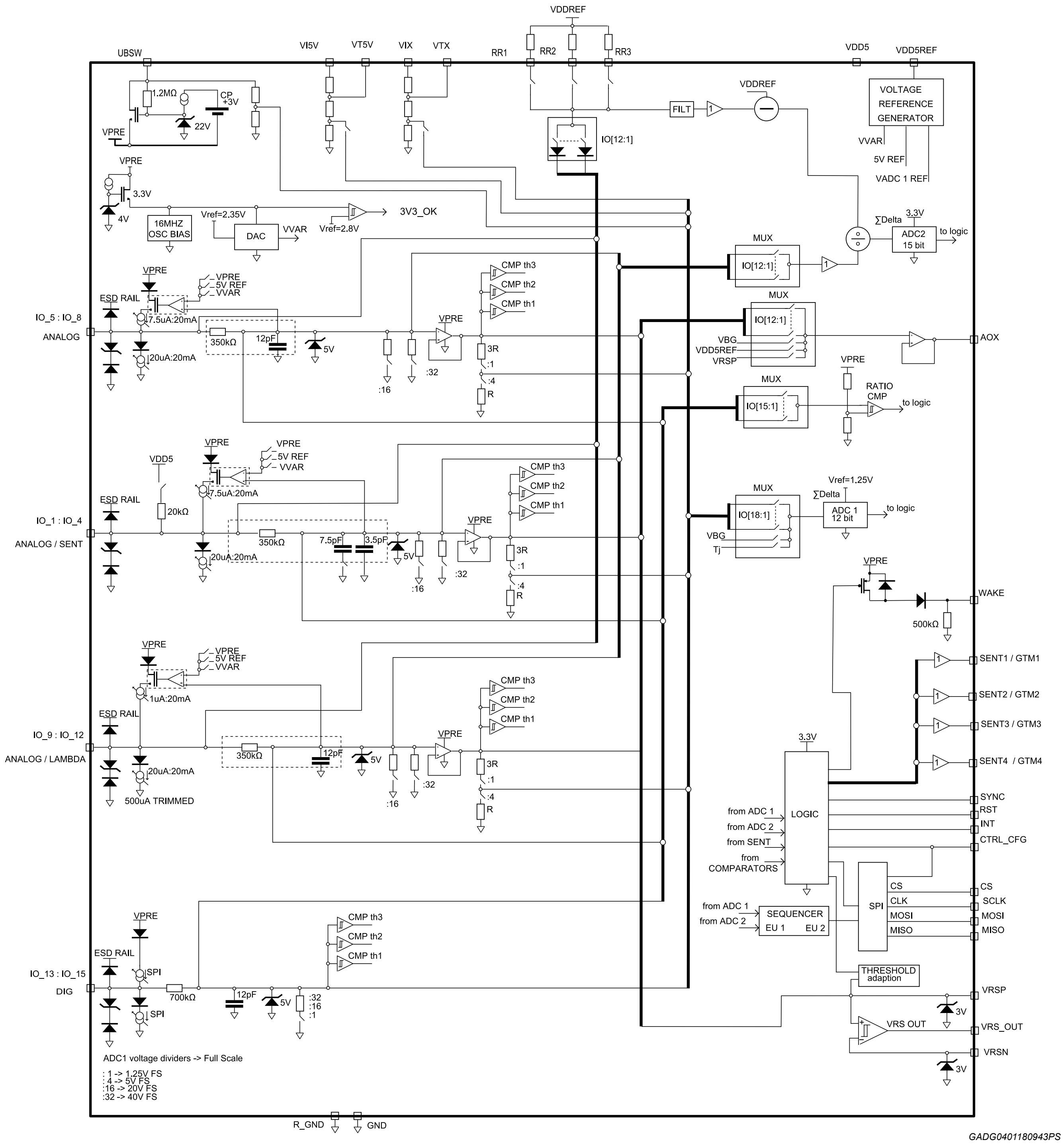
The L9966 is an automotive grade IC designed to be used as sensors interface. Up to 15 channels are available for analog sensing, resistance measurement and digital sensing (e.g. temperature, lambda, pressure, position sensors).

The L9966 allows replacing a number of discrete components and it gives the possibility to change the sensors across different applications without modifying the PCB hardware.

Target applications are Engine Control Units and Body/Chassis Modules.

1 Block diagram

Figure 1. **Block diagram**



2 Pin description

Figure 2. Pin connection diagram

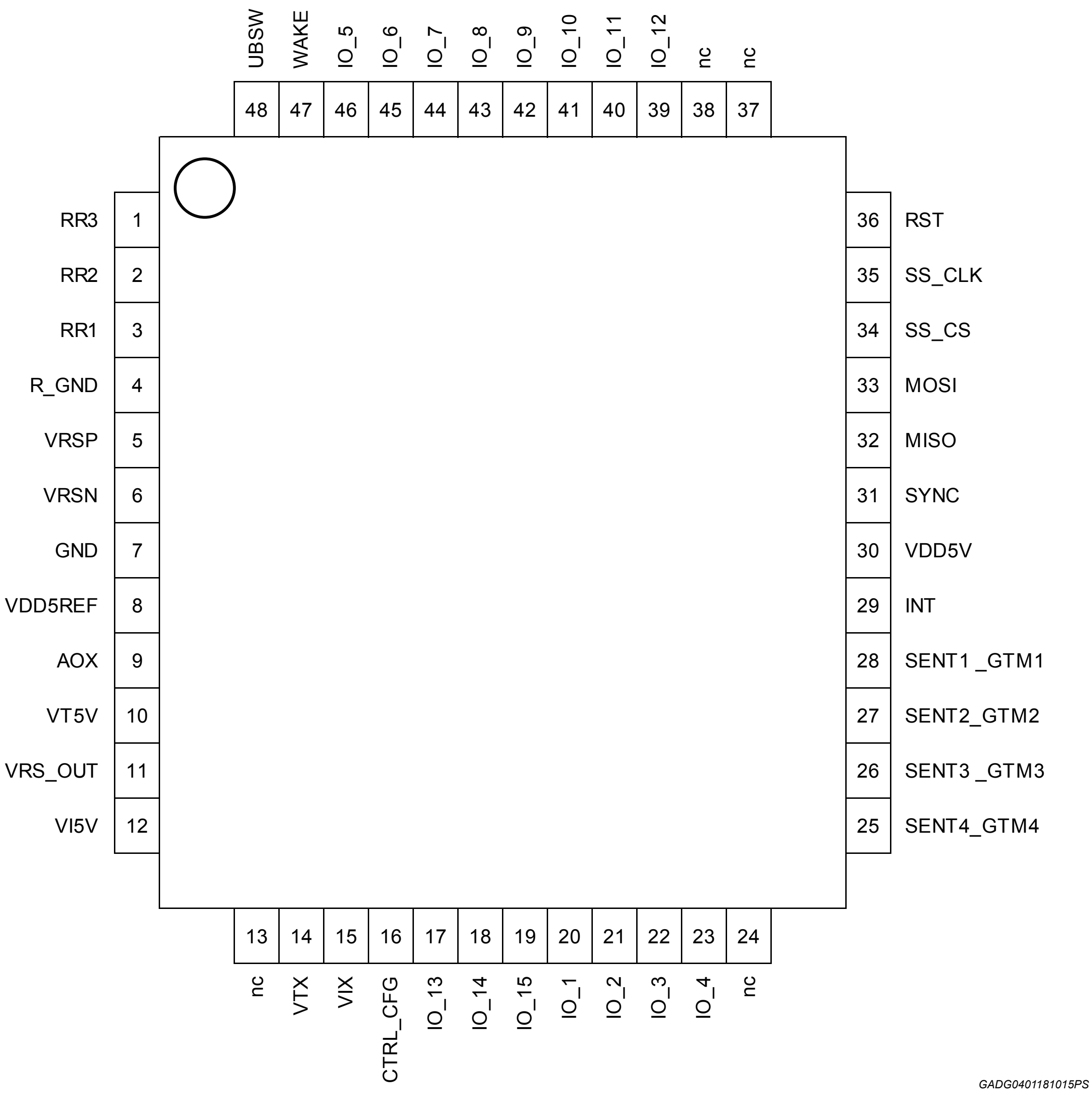


Table 1. Pin description

Pin-Nr.	Pin-name	Description	Pin-class (1)
1	RR3	Reference Pullup Resistor 3 for R-Measurement	I
2	RR2	Reference Pullup Resistor 2 for R-Measurement	I
3	RR1	Reference Pullup Resistor 1 for R-Measurement	I
4	R_GND (2)	Reference Ground for high accuracy signals	I
5	VRSP	Positive variable reluctance sensor input	A
6	VRSN	Negative variable reluctance sensor input	A
7	GND	Ground for supply voltage	S

Pin-Nr.	Pin-name	Description	Pin-class [1]
8	VDD5REF	Positive reference to both ADC	I
9	AOX	Analog output for input channel x	I
10	VT5V	Ratiometric Voltage output VI5V	I
11	VRS_Out	Digital Output of Variable reluctance sensor	I
12	VI5V	Input Voltage	I
13	nc	Not connected	-
14	VTX	Ratiometric Voltage output VIX	I
15	VIX	Input Voltage	I
16	CTRL_CFG	Input to control current source / Configuration input to select SPI Address-Mux during Reset	I
17	IO_13	Flexible Input and current output 13	D
18	IO_14	Flexible Input and current output 14	D
19	IO_15	Flexible Input and current output 15	D
20	IO_1	Flexible Input and current output 1 / SENT1	A
21	IO_2	Flexible Input and current output 2 / SENT2	A
22	IO_3	Flexible Input and current output 3 / SENT3	A
23	IO_4	Flexible Input and current output 4 / SENT4	A
24	nc	Not connected	-
25	SENT4_GTM4	Digital Output for SENT 4 channel / GTM_TO_SENT_4	I
26	SENT3_GTM3	Digital Output for SENT 3 channel r/ GTM_TO_SENT_3	I
27	SENT2_GTM2	Digital Output for SENT 2 channel / GTM_TO_SENT_2	I
28	SENT1_GTM1	Digital Output for SENT 1 channel / GTM_TO_SENT_1	I
29	INT	Interrupt (result status for controller)	I
30	VDD5V	5 V Power supply	I
31	SYNC	Digital input to synchronize sequencer start	I
32	MISO	Communication interface clock for Master-IN/ Slave-OUT	I
33	MOSI	Communication interface for Master-OUT/ Slave-IN	I
34	CS	Communication interface chip select	I
35	SCLK	Communication interface clock	I
36	RST	Reset	I
37	nc	Not connected	-
38	nc	Not connected	-
39	IO_12	Flexible Input and current output 12 / LAMBDA	A
40	IO_11	Flexible Input and current output 11 / LAMBDA	A
41	IO_10	Flexible Input and current output 10 / LAMBDA	A
42	IO_9	Flexible Input and current output 9 / LAMBDA	A
43	IO_8	Flexible Input and current output 8	A
44	IO_7	Flexible Input and current output 7	A
45	IO_6	Flexible Input and current output 6	A
46	IO_5	Flexible Input and current output 5	A
47	WAKE	Output for wake-up	I

Pin-Nr.	Pin-name	Description	Pin-class [1]
48	UBSW	Battery supply	S

1. see ***Pin-class legend***.
2. *R_GND is the ground reference for ADC1, ADC2, VDD5REF voltage divider, input channel voltage dividers. In case R_GND connection to ground on the PCB is lost, R_GND is referenced one diode voltage drop above GND.*

Pin-class legend:

I: ECU Internal Pins: connection to other electrical components on the ECU (Local pins).

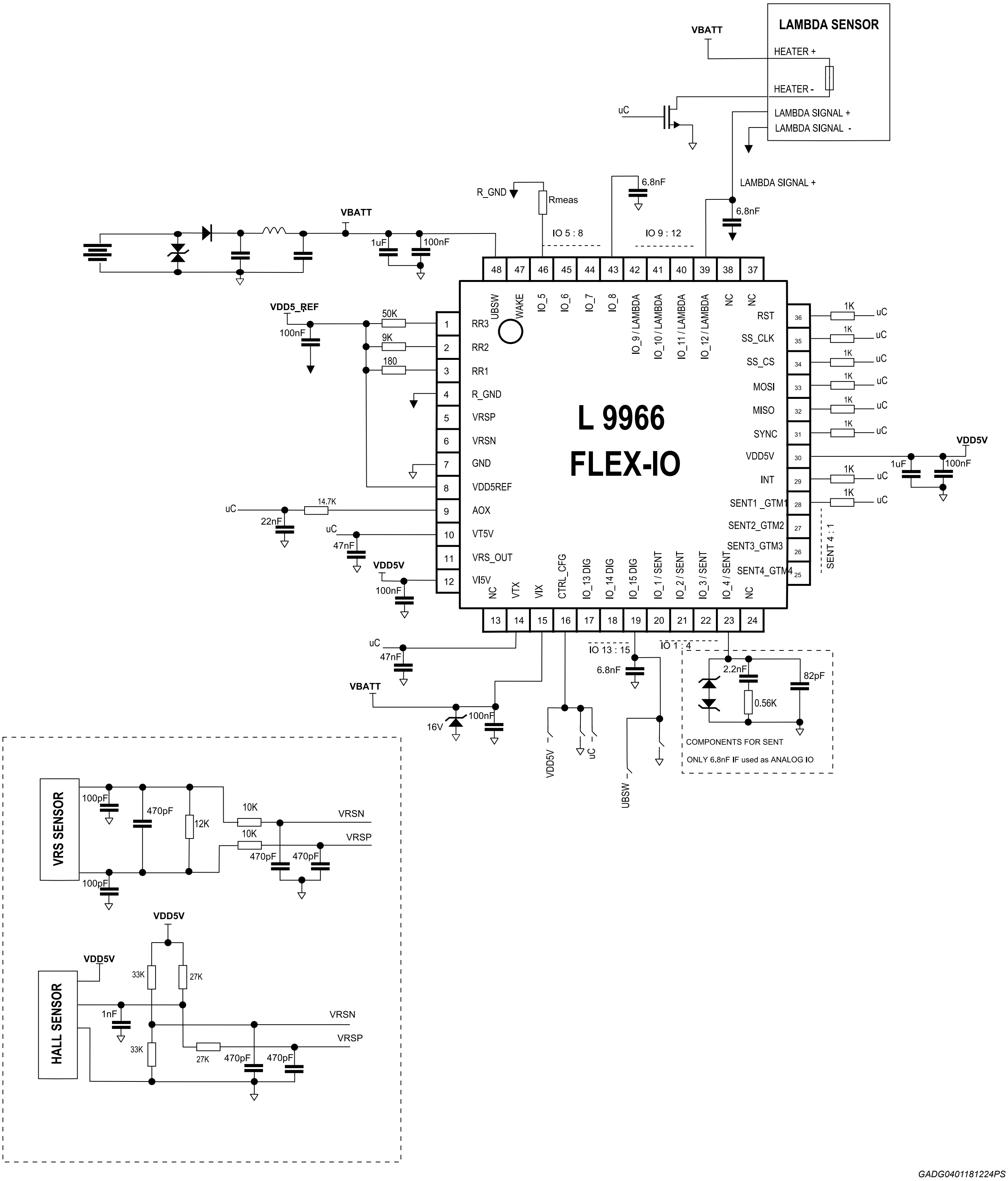
S: Supply Pins: connection to supply sources with protected battery supply (Local pins except UBSW that is a global pin).

A: Analog Inputs: connection to external ECU pins (Global pin).

D: Digital Inputs: connection to external ECU pins (Global pin).

3 Application circuit

Figure 3. Application circuit



In case some functions are not used in the application, the following configurations reported in Table 2. Configuration of unused functions are recommended:

Table 2. Configuration of unused functions

Unused function	Pin	Recommended connection
Resistor measurement	RR1, RR2, RR3	VDD5 or OPEN
Variable Reluctance Sensor	VRSP, VRSN / VRSOUT	Short to GND or OPEN / OPEN
Auxiliary analog output	AOX	RC load / Open if not addressed (R_AOX=0000 in SWITCH_ROUTE register)
Sync pulse	SYNC	Short to GND
Input voltage and ratiometric output voltage	VI5V/VIX	Short to GND
	VT5V/VTX	Open or short to GND
Input voltage	VI5V/VIX	OPEN
	VT5V/VTX	Used as voltage sense
Ratiometric output voltage	VI5V/VIX	Used as voltage sense
	VT5V/VTX	OPEN
SENT/GTM	SENTx_GTMx	OPEN
Interrupt	INT	OPEN
Wake	WAKE	OPEN

4 Input structure

The L9966 hosts 15 different input channels. These channels can be connected to different types of external loads, such as switches, sensors or resistors.

The input structure allows down to -3 V negative input voltage:

- to withstand ground shifts between the ECU ground and the chassis ground where the input signal source is referenced to
- limited to the SENT inputs, to withstand the RF noise without clamping effect that could distort the input signal.

The input structure allows down to -30 V transient on the SENT IO[4:1] pins only if UBSW is no greater than 24 V max. The input protection uses a DPI (Direct Power Injection) filter to avoid rectifying effects in case of HF disturbance on the line.

On the ECU, the input line must be equipped with a discrete ESD capacitor. The value of this capacitor is 6.8 nF. Exceptions to this are the SENT inputs (IO1/2/3/4 pins), because the SAE SENT standard allows max. 100 pF, with an additional 2.2 nF / 560 Ω RC combination. Therefore, SENT inputs have to be additionally protected by TVS (Transient Voltage Suppressor) on the ECU, if necessary.

5 Device operation

The L9966 can enter several operating ranges according to the UBSW voltage, RST pin level, channel state (for polling) and internal fault conditions.

5.1 Absolute maximum rating

The component withstands all the following stimuli without any damage or latch-up. Exceeding any of these values for extended period may lead to component damage.

All voltages are related to GND.

Table 3. Absolute maximum rating

Pin Name	Pin Class	Pin Direction	Min Voltage	Max Voltage	Max Pin Current
IO_1 … IO_12	A	IO	-3 V(1)	58 V	30 mA
IO_13 … IO_15	D	IO	-3 V	58 V	30 mA
UBSW	S	S	-0.3 V	58 V	400 mA
VDD5	I	S	-0.3 V	5.5 V	100 mA
VDD5REF	I	I	-0.3 V	5.5 V	1 mA
VI5V	I	I	-0.3 V	5.5 V	1 mA
VIX	I	I	-0.3 V	36 V	1 mA
VT5V	I	O	-0.3 V	5.5 V	1 mA
VTX	I	O	-0.3 V	36 V	1 mA
RR1 … RR3	I	I	-0.3 V	5.5 V	25 mA
CS, SCLK, MOSI, MISO	I	IO	-0.3 V	5.5 V	5 mA
CTRL_CFG	I	I	-0.3 V	5.5 V	1 mA
INT	I	O	-0.3 V	5.5 V	1 mA
WAKE	I	O	-0.3 V	58 V	20 mA
RST	I	I	-0.3 V	5.5 V	1 mA
SYNC	I	I	-0.3 V	5.5 V	5 mA
AOX	I	O	-0.3 V	5.5 V	1 mA
GND	S	S	0	0	1 A
R_GND	I	I	-0.3 V	0.3 V	1 mA
VRSP, VRSN	A	I	-0.3 V	3.6 V	20 mA
VRSout	I	O	-0.3 V	5.5 V	1 mA
SENT1-4	I	O	-0.3 V	5.5 V	1 mA

1. *IO[4:1] allows down to -30 V transient in case UBSW no greater than 24 V max.*

5.2 Latch-up trials

Latch-up tests performed according to JEDEC 78 class 2 Level A.

5.3 ESD trials

ESD requirements for the stand-alone component (without any external circuits).

Table 4. ESD

Parameter	Value	Unit
ESD according to the Human Body Model (HBM), Q100-002 for global pins; (100 pF/1.5 kΩ)	±4000	V
ESD according to the Human Body Model (HBM), Q100-002 for all pins; (100 pF/1.5 kΩ)	±2000	V
ESD according to the Charged Device Model (CDM), Q100-011 Corner pins	±750	V
ESD according to the Charged Device Model (CDM), Q100-011 All pins	±500	V

5.4 Operating voltage ranges

Table 5. Supply operating ranges summarizes the different operating ranges where different functionalities of the FlexInput are guaranteed. It is assumed that the junction temperature range for proper functionality goes from -40 °C up to 150 °C, unless otherwise specified.

Table 5. Supply operating ranges

Operation Range	UBSW (V)	VDD5 (V)	Remark
Load Dump	36 – 58		Parameters can be out of tolerance (if RST='1'), system is not damaged for pulse duration of 500 ms, 10 time in life.
Jump start	0 – 48		Parameter can be out of tolerance (if RST='1'), system is not damaged for pulse duration of 60 s, 10 time in life.
Normal	7.5 – 36	4.85 – 5.15	All parameters in spec. with VDD5_REF = 5 V(1)
Low Batt	5.5 – 7.5	4.85 – 5.15	All parameters in spec. with VDD5_REF = 5 V(1) Current sources can be out of tolerance, but still non-zero. Resistance measurement is guaranteed for UBSW-V(IO)>1.5 V that means if UBSW = 5.5 V → IOx<4 V
Normal, Low VDD5	7.5 – 36	4 – 4.85	All parameters in spec. Digital and AOX output buffers still working, voltages limited by VDD5 voltage. 5 V_REF, VVAR and VADCxREF are scaled down to VDD5 voltage.
Low Batt, Low VDD5	5.5 – 7.5	4 – 4.85	All parameters in spec. Current sources can be out of tolerance, but still non-zero. Digital and AOX output buffers still working, voltages limited by VDD5 voltage. 5V_REF, VVAR and VADCxREF are scaled down. Resistance measurement is guaranteed for UBSW-V(IO)>1.5V that means if UBSW = 5.5 V → IOx<4 V
Low Batt – 3V3 digital fault	3V3_FLT – 5.5	>4	Configuration data is kept; Input buffer is not able to reach 5 V full range; VRS and SPI functionalities are in spec for UBSW down to 4.5 V. SPI (frequency is not guaranteed) still run down to POR. All analog functions are still on but parameters are out of tolerance. VRS hysteresis features are not guaranteed in case UBSW is < 4.5 V.
3V3 digital fault	VPOR – 3V3_FLT	>4	If 3V3_FLT = 1 all functions switched off. Only internal charge pump kept on to guarantee no reset of internal logic
Low Batt	< VPOR		Device in OFF mode

1. *The parameters depending on VDD5_REF are: ADC1 accuracy, pull-up voltage 5V and VVAR. They will have the same tolerance in addition as VDD5_REF.*

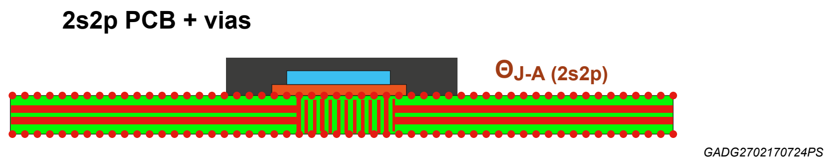
5.5 Temperature ranges and thermal data

Table 6. Temperature ranges and thermal data

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
T_j (1)	Operating junction temperature	–	-40	–	150	°C	–
T_{stg}	Storage temperature	–	-55		150	°C	–
$R_{Th\ j\text{-}a}$ (2)	Thermal resistance junction-to-ambient	–	–	31	–	°C/W	Homogeneous internal power distribution (3)
$R_{Th\ j\text{-}cb}$ (2)	Thermal resistance junction-to-case-bottom	–	–	3	–	°C/W	Homogeneous internal power distribution

1. *All parameters are guaranteed, and tested, in the temperature range T_j -40 to 150 °C unless otherwise specified.*
2. *Not subject to production test, guaranteed by design.*
3. *$R_{Th\ j\text{-}a}$ value is retrieved according to Jedec JESD51-2,-5,-7 guideline with a 2s2p board.*

Figure 4. 2s2p PCB with thermal vias



Note: In "2s2p", the "s" suffix stands for "Signal" and the number before indicates how many PCB layers are dedicated to signal wires. The "p" suffix stands for "Power" and the number before indicates how many PCB layers are dedicated to power planes.

5.6 Operating modes

The state machine operation is summarized in the state diagram of Figure 5. Every time RST pin rises, the IC enters INIT mode, remaining for PB (blanking time); once this time has expired, if a fault is detected the IC enters FAULT mode, NORMAL mode otherwise. Only once NORMAL mode is entered, the IC is fully running and SPI gets ready to process commands.

Figure 5. Operating mode state diagram

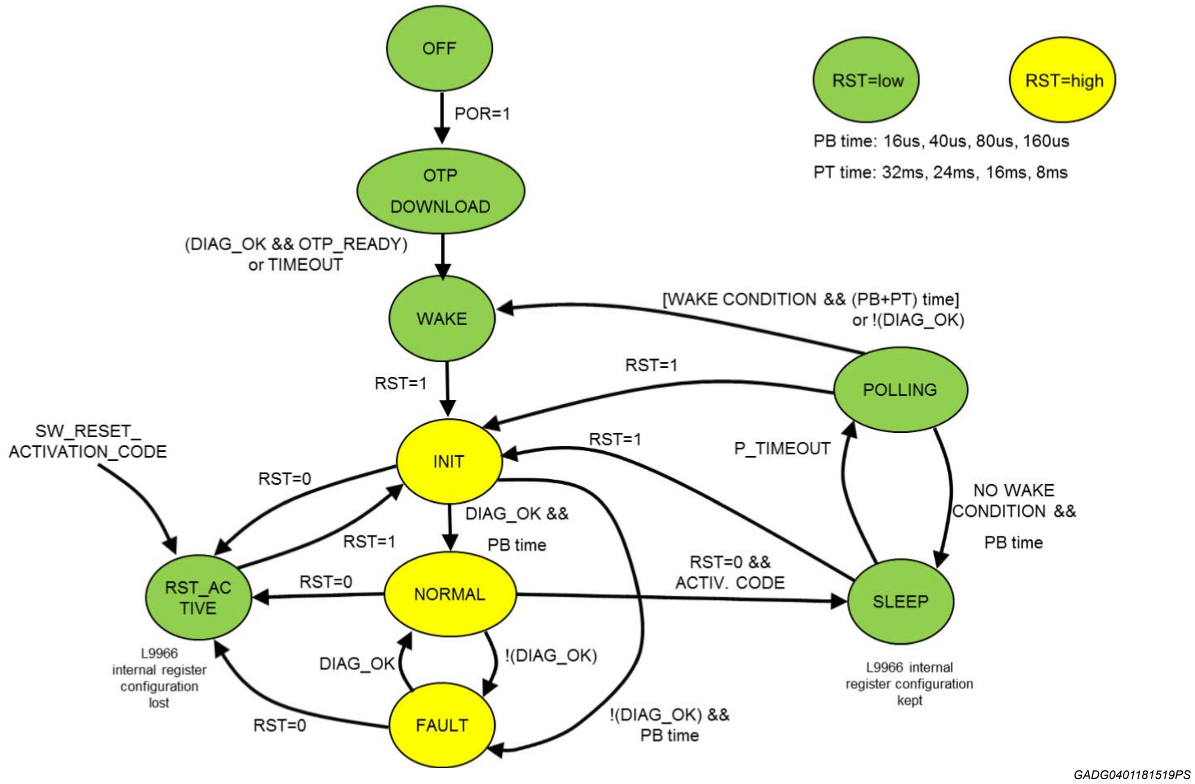


Table 7. Transition between operation modes

From	To	Description
OFF	EEPROM_download	FSM (Finite State Machine) changes from OFF to EEPROM_download in case a rising edge of POR is detected (supply on in terms of internal 3V3 internal supply is stable).
EEPROM_download	WAKE	FSM changes from EEPROM_download to WAKE when EEPROM (NVM, Not volatile memory) is ready (trimming bit saved in memory). Based on data validity a trimming fault flag can be asserted. In case of fault detection, in terms of DIAGNOSTIC not OK or CALIB_FLT/ TRIM_FLT detection (available on GEN_STATUS register) after a timeout (NVM_timeout) the IC moves anyway in WAKE status. WAKE output pin and WAK_UP_FLG in GEN_STATUS register are asserted high. Once read, the WAK_UP_FLG is cleared and the WAKE pin goes to zero.
WAKE	INIT	FSM changes from WAKE to INIT in case a rising edge of RST is detected During this transition, status of CTRL_CFG pin is latched to determine SPI chip address.
INIT	NORMAL	FSM changes from INIT to NORMAL when diagnostic check is ok for PB time.
INIT	FAULT	FSM changes from INIT to FAULT when diagnostic check is not ok for at least PB time_TIMEOUT.

From	To	Description
NORMAL	FAULT	FSM changes from NORMAL to FAULT when overtemperature (if not masked) or internal 3V3 supply fault event happens. In FAULT SPI runs and internal reference voltage are still on.
FAULT	NORMAL	FSM changes from FAULT to NORMAL when fault event is solved.
NORMAL	SLEEP	FSM changes from NORMAL to SLEEP when writing an activation code 3 times to the WAK_CONFIG register and then RST pin goes to 0. In SLEEP, the device configuration is kept.
SLEEP	POLLING	FSM changes from SLEEP to POLLING once the PT_timeout time has expired.
POLLING	SLEEP	FSM changes from POLLING to SLEEP if wake up sources don't change their value for at least PB time since POLLING mode was entered.
POLLING	WAKE	FSM changes from POLLING to WAKE when a wake-up event is detected for at least the sum of the 2 timeouts PB+PT (wake-up sources are detected to have changed their values). PT is polling timeout.
Any RST-low mode	INIT	FSM changes to INIT in case a rising edge of RST is detected.
Any RST-high mode	RST_ACTIVE	FSM power control comes back to RST_ACTIVE when RST pin goes to 0 during NORMAL, FAULT, INIT. In RST_ACTIVE, the device configuration is lost. A deglitch filter on RESET pin prevents anomalous entering in RST_ACTIVE mode. RST deglitch filter in sleep =16 μs RST deglitch filter in normal mode = 1 μs
Any mode	OFF	FSM power control leads to OFF if UBSW falls below POR level.

In Figure 6 and Figure 7 are reported an example of power up and power down sequence.

In Figure 6: UBSW rises and as a consequence VPRE and 3V3 internal supply rise too. POR is an internal threshold of 3V3 regulator that enables the internal reference circuit, which guarantees that the digital blocks are correctly supplied.

Assertion of 3V3_ok signal guarantees that the internal analog blocks are correctly supplied.

WAKE signal is asserted once the EEPROM download is succeeded or the internal NVM_timeout is elapsed.

A possible application scenario is WAKE high which wakes an external 5 V power supply which feeds VDD5 and VDD5REF and manages the RST de-assertion. Once the RST is de-asserted, the IC moves in normal operating mode.

Figure 6. Example of power up sequence

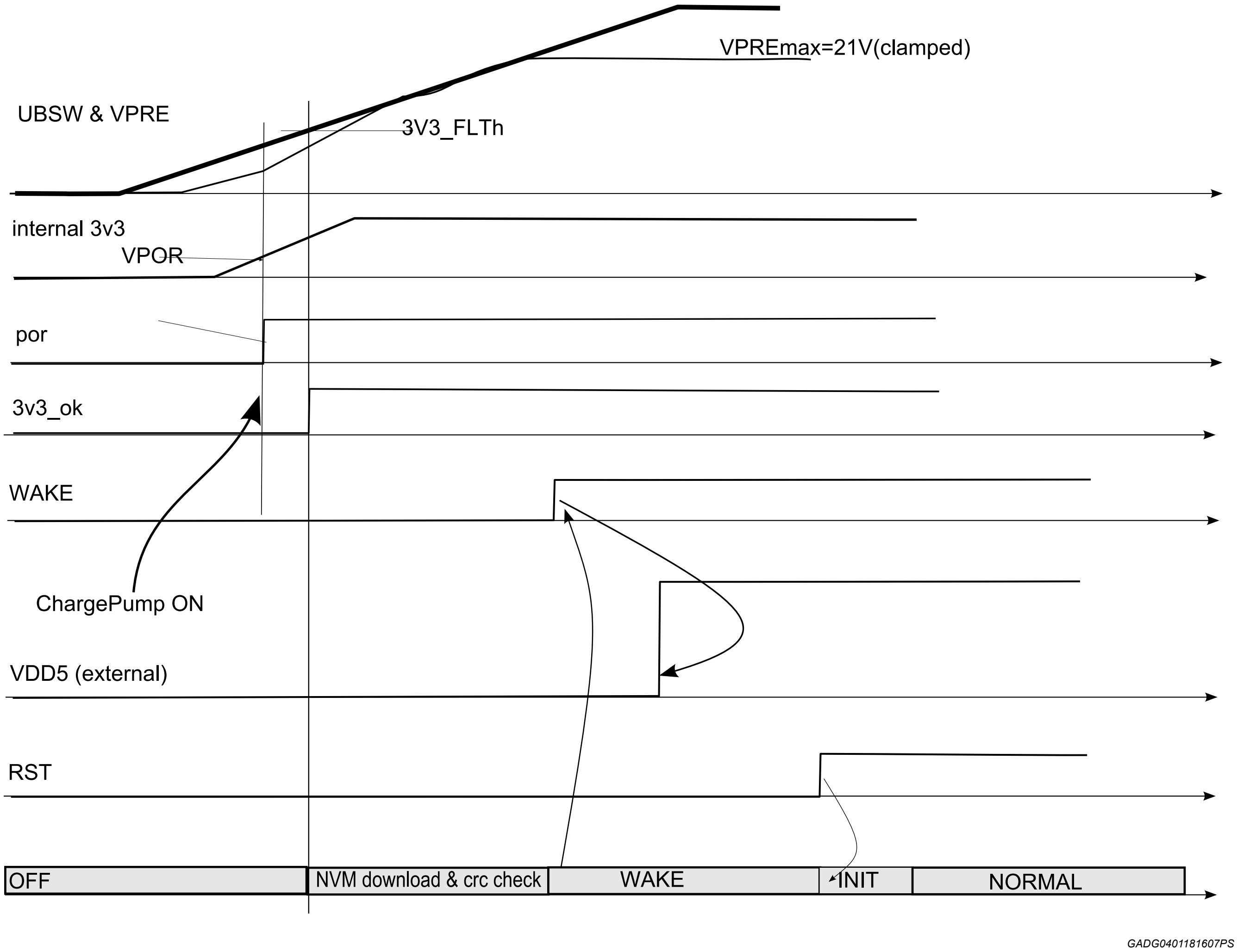
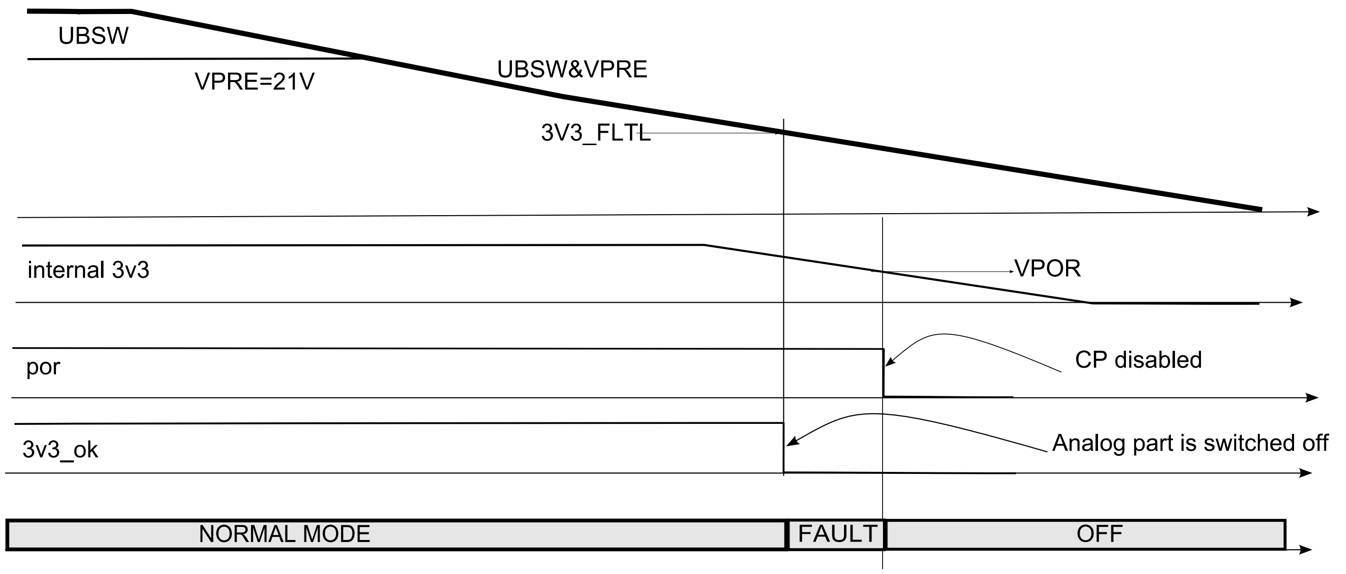


Figure 7 shows a power down sequence without SLEEP-POLLING phase: UBSW falls down to 3V3_FLT assertion and POR.

If 3V3_FLT is set, the internal power blocks are switched off, while SPI is still running. Further lowering of UBSW determines POR and consequently the reset of the device.

Figure 7. **Example of power down sequence**



For the state evolutions which involve a timeout expiration, two separate timers are taken into account:

- PB: blanking timeout, 160 µs by default;
- PT: polling timeout, 16 ms by default.

Both of them have a default value that can be modified, once the SPI is able to operate, setting the appropriate values in PB[1:0] and PT[1:0] fields inside WAK_CONFIG register.
Every time the system exits from POR or RST_ACTIVE, the two timeouts reset to their default values.
Current consumption in each device status is summarized in next Table 8.

Table 8. **Current consumption**

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.							
V3V3	Internal 3V3	Design info – analog and digital supply voltage range	3	-	3.55	V	-
I_{RST_ACTIVE}	Current consumption during RST	RST pin low, UBSW = 12 V	-	210	300	µA	UBSW
		RST pin low, UBSW = 12 V CTRL_CFG connected to GND or VDD5 (not floating) and CS kept H	-	-	30	µA	UBSW
I_{SLEEP}	SLEEP current consumption	SLEEP mode (no current sources activated and no WAKE SOURCE defined) and UBSW = 12 V. CTRL_CFG connected to GND or VDD5 (not floating) and CS kept H	-	75	130	µA	UBSW
$I_{SLEEP\text{-}POLLING}$	Average SLEEP - POLLING current consumption	POLLING mode (only one WAKE SOURCE defined and configured as PULL DOWN), 32 ms PT TIME, 16 µs PB TIME and UBSW = 12 V. CTRL_CFG connected to GND or VDD5 (not floating) and CS kept H	-	75	130	µA	UBSW
I_{NORMAL}	NORMAL current consumption	NORMAL mode, no active current sources	-	24	30	mA	UBSW
I_{VDD5}	VDD5	NORMAL mode, without SPI and SENTx_GTMx activity	-	5	10	mA	VDD5

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$I_{VDD5REF}$	VDD5REF	NORMAL mode	-	50	100	µA	VDD5REF
MAIN_OSC	MAIN_OSC	NORMAL mode oscillator frequency	-9%	16	+9%	MHz	-
LOW_SPEED_OSC	LOW SPEED OSC	SLEEP mode low power, low speed oscillator frequency	-40%	1	+40%	MHz	-
NVM_timeout	NVM timeout	Guaranteed by design	-40%	3.125	+40%	ms	-

5.6.1 Software reset

Configuration bit can be cleared by entering RST_ACTIVE mode, or alternatively, by issuing a SOFT_RESET command procedure. The procedure is a sequence of 3 separate SPI write operations with activation codes specified in the register description in Section 16.18 SOFT_RST_CMD. Only consecutive write accesses are allowed: any write or read access in-between will reset the activation code. After procedure completion the device moves back in NORMAL mode.

5.7 Chip status

The status of the chip can be read in the GEN_STATUS register. In particular CFG_CHK[1:0] bit in GEN_STATUS are configured to default ‘10’ after power-up. User can write any different code during NORMAL mode to understand later if a new POR or a reset event has occurred (POLLING does not impact these two bits).

The device is equipped with an overtemperature protection that could be masked. When not masked, as soon as the overtemperature is detected, the OT_FLT bit sets to ‘1’ and the device goes to the FAULT mode. When masked setting OT_MASK = ‘1’, the fault bit is set, but the device will not enter FAULT mode.

Overtemperature diagnostic is active at power up after trimming bits have been downloaded from internal EEPROM; in case a fault of the download procedure is detected, such a function is disabled and an eventual overtemperature is not detected.

An internal voltage comparator is implemented on the internal supply reference (3V3_ref) to monitor its proper range. In case of fault, the 3V3_FLT bit is set and the device goes to the FAULT mode. Once the fault is no longer persisting and the bit is read, the bit itself is cleared.

At the POWER up, as soon as UBSW is recognized higher than VPOR, the device downloads the EEPROM content; the internal FSM, before reaching the WAKE state, waits until 3V3_FLT is de-asserted. Once the EEPROM content has been downloaded into the internal registers, a consistency check of data is performed; result of this check is CALIB_FLT, which takes into account an eventual fault of calibration data for ADC1 and ADC2, and TRIM_FLT flag, which takes into account the consistency of data used for trimming.

When UBSW falls down, once 3V3_FLT is asserted, the analog section is no more guaranteed to properly operate. Bandgap reference, main oscillator, voltage monitoring, logic section (SYNC, RST, INT) and SPI keep working allowing the possibility to read the internal status of 3V3 signal. Internal current generators, VRS, GTM, AOX blocks are switched off; the configuration is still kept until UBSW goes below VPOR, that generates a POR event.

Parameters that determine fault condition for the device are defined in Table 9.

Table 9. Chip status electrical parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, T_{j-max} = 150 °C unless otherwise specified.							
V_{POR}	POR threshold H to L	Battery POR threshold	-	-	2.5	V	UBSW
	POR threshold L to H	Battery POR threshold Design info	4.5	-	-	V	UBSW
3V3_FLTh	3V3_FLT higher threshold, By design	If internal 3V3 > 3V3_FLTh => 3V3_FLT = ‘0’; POR is not activated Design info	2.8	-	3.2	V	UBSW

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
3V3_FLTI	3V3_FLT lower threshold	If internal 3V3 < 3V3_FLTI => 3V3_FLT = ‘1’; POR is not activated	2.75	-	3.15	V	UBSW
RST_hi	RST input logic high voltage		1.5	-	1.7	V	RST
RST_lo	RST input logic low voltage	-	1.2	-	1.4	V	RST
RST_hys	RST input voltage hyst	-	200	-	315	mV	RST
RST_pu	RST pull up to VDD5V	-	65	100	140	kΩ	RST
RST_degl_filt	RST deglitch filter	-	-20%	1	+20%	µs	RST
OT	Overtemperature	OT_FLT set, TRIM_FLT = 0	170	180	190	°C	-
OT_hys	Overtemperature hysteresis	-	-	10	-	°C	-
OT_de	Overtemperature deglitch	Guaranteed by scan	-	100	-	µs	-

5.8 Polling operation: WAKE and SLEEP modes

SLEEP mode is enabled by sending 3 consecutive specific 32 bits SPI frames. The specific three SPI frames are intended to avoid any unintentional SLEEP mode activation. Each frame needs a separate chip-select signal. Once the SPI sequence has been sent, RST pin has to be driven low to enter SLEEP. In case the RST pin is not driven low, the device stays in NORMAL mode and as soon as a new SPI command is received, the SPI sequence previously sent to enter SLEEP mode is invalidated.

After the FlexInput has entered SLEEP mode, the ADC, SPI, VRS, pull up and pull down current generators and sequencer are stopped. VDD5 is no longer necessary (0-5.5 V). In SLEEP mode the current sources are not enabled, however they keep their configuration. The chip is supplied by UBSW (permanent supply).

The average current consumption in SLEEP / POLLING mode, $I_{SLEEP\text{-}POLLING}$ is defined in Table 8. Current consumption.To save current consumption, current sources are pulsed in SLEEP / POLLING mode.

A pulsed current source is normally switched off, but it will be switched on for the time the chip reads the inputs. Besides, the main oscillator is stopped and a second one takes over with reduced performances, in order to guarantee the operation of the POLLING mechanism.

The pulse switch on depends on the configurable polling blanking time PB[1:0] in WAK_CONFIG register. Default value is 160 µs.

The digital level of all 15 inputs is read (polled) every (m+1)*8 ms, where m is selected in PT[1:0] in WAK_CONFIG register. WAK_MSK register defines which IOx are selected as WAKE SOURCES.

With respect to the IOx selected in WAK_MSK register, only the channels having CIS[3:0]=”0000”, MODE=”1”, PullUp/PullDown configuration SEL = “001”(PullUp to battery/HiZ) or SEL = “100”(PullDown/HiZ) will act as WAKE SOURCES; all the other IO configured through a different SEL selection will be ignored.

During polling, IOx defined as WAKE SOURCES are checked against the value they had before entering SLEEP mode. These values have been stored in SLEEP_CONFIG register.

The check lasts for a PB time. At the end of PB time, if no WAKE SOURCE has changed its value, the chip goes back to SLEEP mode. Otherwise, if at least one WAKE SOURCE has changed its value, this starts the verification that the new status lasts for a longer PT time.

During PT time, the WAKE SOURCES can be as in one of the three below scenarios.

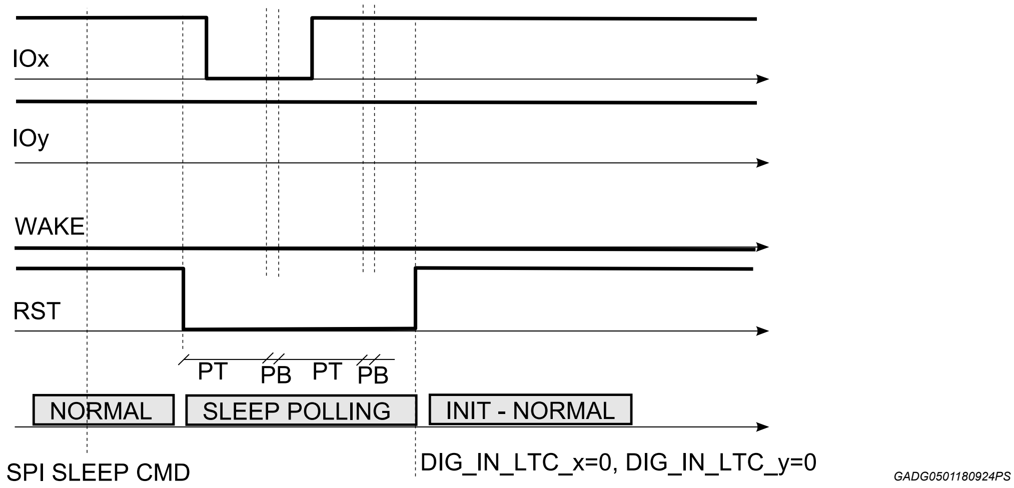
Scenario 1

Once the new status is detected, the WAKE SOURCES return at their PRE_SLEEP value before PB+PT time elapses.

The IC returns back in SLEEP mode as shown in Figure 8;

IC only moves in INIT once RST pin is released (no wake pin assertion)

Figure 8. **WAKE SOURCE returns at its PRE_SLEEP value**

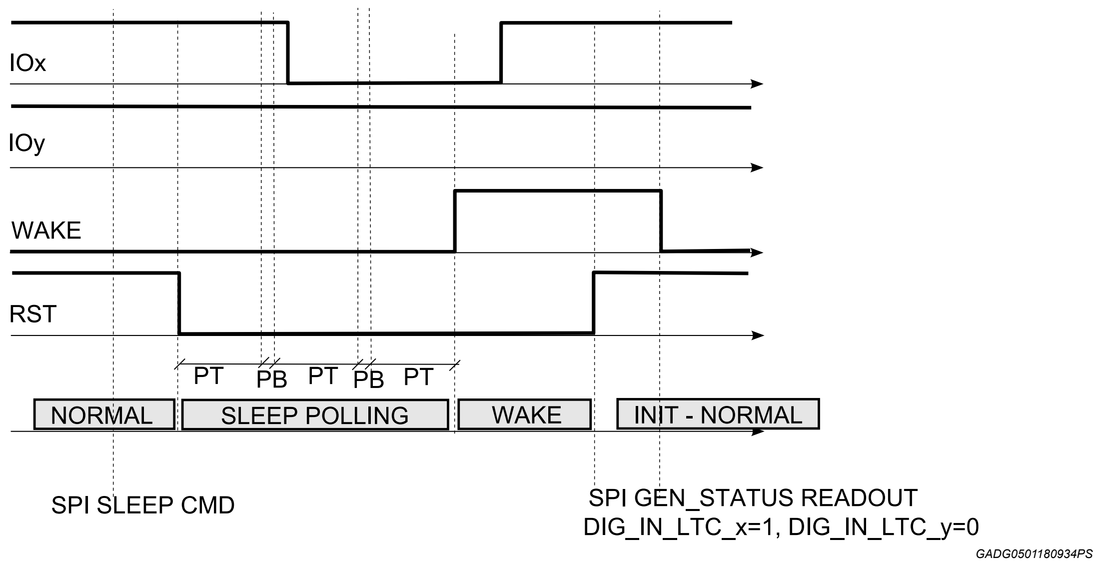


Scenario 2

Once the new status is detected, the WAKE SOURCES maintain the new value for PB+PT time.

This determines WAKE EVENT as shown in Figure 9. WAKE SOURCE determines a WAKE EVENT.

Figure 9. **WAKE SOURCE determines a WAKE EVENT**



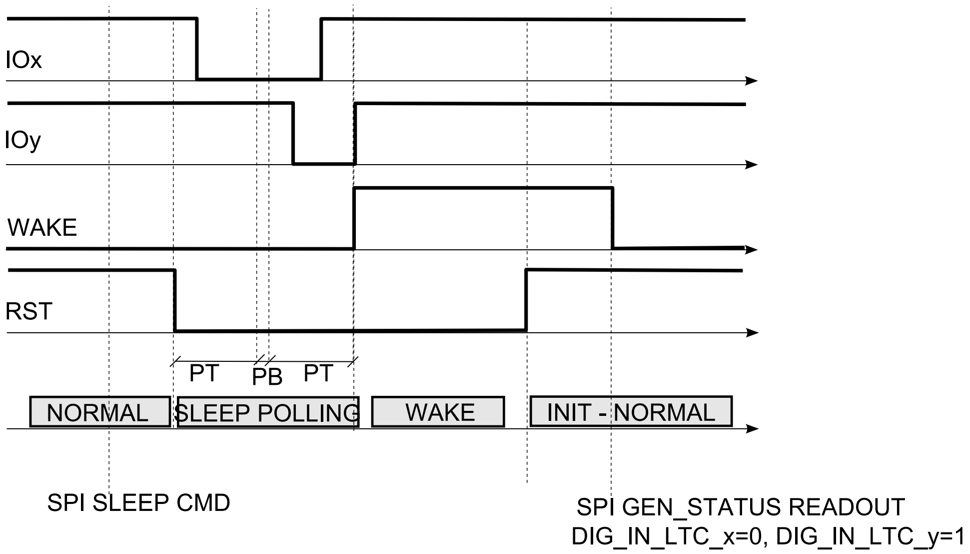
Scenario 3

Once a new status is detected on some WAKE SOURCES, in PB+PT time their values return at their PRE-SLEEP ones while other WAKE SOURCES change their status.

Even if the events separately last for less than a PB+PT time, if their combination lasts for at least PB+PT time, this determines a WAKE EVENT, as shown in Figure 10.

The WAKE SOURCE latched as responsible for the WAKE EVENT is the one asserted as soon as PT expires.

Figure 10. **Combination of two consecutive WAKE SOURCES determines a WAKE EVENT**



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Once the WAKE EVENT is recognized, the IC enters WAKE mode.

If at the end of the sum of the 2 timeouts (PB+PT), the state is still different from the one recorded in SLEEP_CONFIG register, the DIG_IN_STAT_LTC will be written with the XOR of all and only the IO configured as WAKE SOURCES (WAK_MSK register) which changed their value during polling: ‘1’ means the status changed, ‘0’ means no change. Then the IC enters in WAKE mode, the WAKE pin is asserted high and the WAK_UP_FLG in GEN_STATUS is set.

Figure 11. **SLEEP-POLLING operation example**

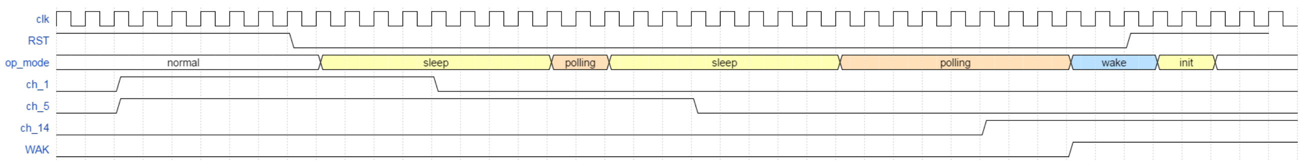

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Figure 11 shows a SLEEP mode scenario. In this case, CH5 and CH14 are configured as WAKE SOURCES with SEL = "001" and "100" respectively. When the RST is driven low, the device enters SLEEP mode.

- During the first sleep period, CH1 changes its value from ‘1’ to ‘0’. Nonetheless, after polling blanking time, only CH5 and CH14 are checked against their original value, then device re-enters immediately sleep mode.
- At second sleep-polling cycle, CH5 changes its value from ‘1’ to ‘0’. After the Polling timeout PT has expired, device enters WAKE mode. Only after RST is driven high again, the device re-enters INIT mode for diagnostic checks and finally NORMAL mode.

It is forbidden to use UTh_ratio to detect an eventual WAKE EVENT.

5.9 SLEEP mode

To enter SLEEP mode, the following steps must be done:

1. Select which channel should be polled in SLEEP mode to detect the wake-up event. This is done by setting the corresponding bit in WAK_MSK register. Only IO properly configured through SEL bit can be defined as WAKE UP sources; the IO with SEL bit not properly configured for the function is ignored in WAK_MSK register and the corresponding bit remains by default.

2. Activation of SLEEP Mode. This is done by writing an activation code 3 times to the WAK_CONFIG register. PB[1:0] are used to configure the PB time during the polling mode. PT[1:0] are used to configure the P_TIMEOUT. Only consecutive write accesses are allowed. Any write or read access in-between will reset the activation code.

Once IC enters in SLEEP mode, in order to save current consumption, the main oscillator is stopped and a low power, lower frequency oscillator takes over, in order to guarantee the correct operation of the POLLING operations.

6 Current Sources

The FlexInput is equipped with a set of programmable and configurable current sources that can pull up or pull down the input line.

The pull up current sources can pull up the input line to three different levels:

- VPRE, the internal clamped high voltage rail
- 5V_REF, the internal generated 5 V rail
- VVAR, the internal generated and programmable variable voltage level

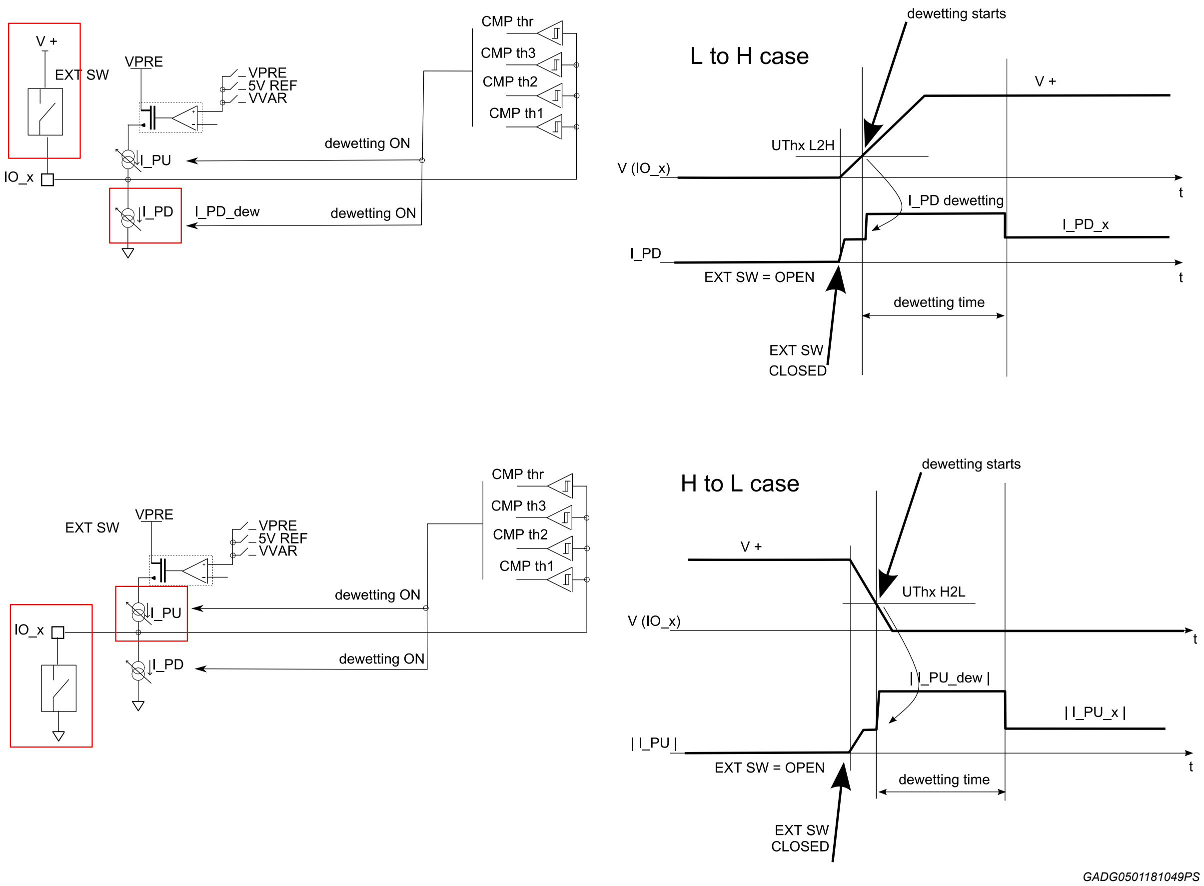
The strength of the current and the voltage limit (pull up only) can be configured by register CURR_SRC_CTRL_x for the channel configuration and DWT_VOLT_SRC_LSF_CTRL for VVAR output voltage setting.

The current sources can be controlled in order to configure a dewetting function. Both dewetting current and actuation time are selectable via SPI; dewetting time (DWT[2:0] bit of DWT_VOLT_SRC_LSF_CTRL register) is shared among the channels while current value setting (CV_DW_1, CV_DW_0 bit of CURR_SRC_CTRL_x registers) is specific for each one.

The dewetting function is disabled by default. If enabled, the dewetting function is triggered according to the following conditions, see Figure 12:

- If IO_x is configured as pull up, then a falling edge on IO_x detected by the comparator will start dewetting.
- If IO_x is configured as pull down, then a rising edge on IO_x detected by the comparator will start dewetting.

Figure 12. Dewetting activation



After that the configured dewetting time is expired, the current turns back to the value defined in the CURR_SRC_CTRL_x registers bit CV[2:0].

For the IOx configured with dewetting enabled, every time the IC moves from SLEEP to NORMAL an automatic dewetting is performed.

6.1 Pull-down current programming

Pull down current generators are implemented as controlled current generator with back to back diode to avoid damaging when the FlexInput input is being brought below ground.

Pull Down current values are reported in Table 10.

IOx saturation voltages are reported in Table 11.

Table 10. Pull Down Current

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.							
Ipd_7	Pull down current	Current source code [CV2,CV1,CV0]=111	16	20	24	mA	IO1-15
Ipd_6	Pull down current	Current source code [CV2,CV1,CV0]=110	8	10	12	mA	IO1-15
Ipd_5	Pull down current	Current source code [CV2,CV1,CV0]=101	4	5	6	mA	IO1-15
Ipd_4	Pull down current	Current source code [CV2,CV1,CV0]=100	0.8	1	1.2	mA	IO1-15
Ipd_3	Pull down current	Current source code [CV2,CV1,CV0]=011	390	500	610	µA	IO1-15
Ipd_2	Pull down current	Current source code [CV2,CV1,CV0]=010	71	100	120	µA	IO1-4
Ipd_2	Pull down current	Current source code [CV2,CV1,CV0]=010	80	100	120	µA	IO5-15
Ipd_1	Pull down current	Current source code [CV2,CV1,CV0]=001	14	20	26	µA	IO1-15
Ipd_0	Pull down current	Current source code [CV2,CV1,CV0]=000	480	600	720	µA	IO1-15

Table 11. Saturation voltages

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.							
VPDsat5-15(1)	Pull down saturation range	Pull down current not guaranteed if voltage on IO is below VPDsat	-	-	200	mV	IO5-15
VPDsat1-4(1)	Pull down saturation range	Pull down current not guaranteed if voltage on IO is below VPDsat	-	-	200(2)	mV	IO1-4
VPDsat5-15	Pull down saturation range	Output current is guaranteed to be at least 10% of the nominal value (e.g. > 1.6mA for Ipd_7)	200	-	700	mV	IO5-15
VPDsat1-4	Pull down saturation range	Output current is guaranteed to be at least 10% of the nominal value (e.g. > 1.6mA for Ipd_7)	200 (2)	-	800	mV	IO1-4
VPDsat1-4	Pull down saturation range	Output current is guaranteed to be within nominal range	800	-	-	mV	IO1-4
VPDsat5-15	Pull down saturation range	Output current is guaranteed to be within nominal range	700	-	-	mV	IO5-15
IPDlkg	Output leakage current	Input voltage: 0V to VPRE	-	-	200	nA	IO1-15
DELTA_Ipd_x	Delta Output current	V(IO)>VPRE, x = 0..4	-	-	+1	mA	IO1-4
		V(IO)>VPRE, x = 5,6	-	-	+3	mA	IO1-4
		V(IO)>VPRE, x = 7	-	-	+8	mA	IO1-4
DELTA_Ipd_x	Delta Output current	V(IO)>VPRE, x = 0..4	-	-	+0.5	mA	IO5-15
		V(IO)>VPRE, x = 5	-	-	+1.5	mA	IO5-15
		V(IO)>VPRE, x = 6	-	-	+1.5	mA	IO5-15
		V(IO)>VPRE, x = 7	-	-	+2	mA	IO5-15

1. *Once defined the IPD, if the IO voltage is decreasing, the Pull Down current value is guaranteed down to VPDsat. In case of IO shorted to GND, the voltage on the pin tries to be increased up to VPDsat.*
2. *In case 20 µA is selected ,minimum voltage to guarantee current is 750 mV , below 750 mV current may be zero.*

6.2 Pull-up current programming

Internal pre-regulated voltage (VPRE) is implemented to protect internal circuitry against high voltage UBSW: VPRE value with respect to UBSW is reported in Table 12.

Table 12. Pre-regulated voltages value

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, T_{j-max} = 150 °C unless otherwise specified.							
VPRE_L	Internal pre-regulated voltage	UBSW <20 V (115 mA @ 150 °C: 5 channels with 20 mA each)	UBSW-0.2 UBSW-025	-	UBSW	V	IO1-12 IO13-15
VPRE_H	Internal pre-regulated voltage clamp	UBSW >22 V	20	21	22	V	IO1-15

The pull up current sources are implemented as current generators supplied from VPRE.

That means the 5V_REF and VVAR current sources are obtained from VPRE through a voltage limitation. The VVAR voltage is adjusted by register DWT_VOLT_SRC_LSF_CTRL bit VVAR_V[4:0].

Every time the pull up voltage reference is changed, in order to avoid overshoot, it is recommended to switch first in HiZ. For IO[12:9] any VVAR modification automatically leads to a switch in HiZ.

Pull up regulated voltage values are VPRE over the ones reported in Table 13. Regulated voltages value.

In case of IO[15:13] the only possible pull up is to VPRE; the other pull up voltage, VVAR or 5V_REF, are automatically redirected to VPRE

Table 13. Regulated voltages value

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, T_{j-max} = 150 °C unless otherwise specified.							
5V_REF	5 V voltage level	Tested at open load, UBSW > 7.5 V	-2%	5	+2%	V	IO1-12
5V_REF_drop	5 V voltage drop	Tested at open load, 5.5 V < UBSW < 7.5 V	0	0.75	1	V	IO1-12
VVAR	Variable voltage source range		0.8	-	1.9	V	IO1-12
VVAR_acc	Variable voltage source accuracy		-50	-	+50	mV	IO1-12
VVAR_step	Variable voltage source step		45	50	55	mV	IO1-12
5V_REF_dly	5V_REF delay time	From enable to start of rising front, digital delay not effecting	-	-	150	µs	IO1-12
5V_REF_rise	5V_REF rise time	From 20% to 80% Tested at open load, current source=Ipu_7 (Voltage slope on IO depends on current selected, and load on the IO)	-	-	200	µs	IO1-12
VVAR_dly	VVAR delay time	From enable to start of rising front	-	-	120	µs	IO1-12
VVAR_rise	VVAR rise time	From 20% to 80% Tested at open load, current source = Ipu_7 (Voltage slope on IO depends on current selected, and load on the IO)	-	-	200	µs	IO1-12
VPRE_dly	VPRE delay time	From enable to start of rising front, digital delay not effecting	-	-	150	µs	IO1-15
VPRE_rise	VPRE rise time	From 20% to 80% of VPRE_H.	-	-	200	µs	IO1-15

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
		Tested at open load, current source = Ipu_7 (Voltage slope on IO depends on current selected and load on the IO)					

Internal back to back diode is implemented on each FlexInput channel to avoid pulling up of UBSW by FlexInput short to a high external source.

Pull-up voltage for digital channels is limited to VPRE only: neither 5V_REF nor VVAR voltage limitations are applied on digital IOs. Conversely, all three of them (VPRE, 5V_REF and VVAR) can be applied to the analog channels.

Output load is 6.8 nF (+/-20%), ESR max = 1 Ω + external wiring and sensor capacitance. On pins which can be routed to SENT sensors, the load can also be 82 pF//(2.2 nF+560 Ω) + wire and sensor capacitance.

Pull Up current values are reported in Table 14. IOx saturation voltages with respect to VPRE are reported in Table 15.

Table 14. Pull up current value

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.							
Ipu_7	Pull up current	Current source code [CV2,CV1,CV0]=111, pull-up current to VPRE (to 5V_REF or VVAR only for IO1-12)	-20%	20	+20%	mA	IO1-15
Ipu_6	Pull up current	Current source code [CV2,CV1,CV0]=110, pull-up current to VPRE (to 5V_REF or VVAR only for IO1-12)	-20%	10	+20%	mA	IO1-15
Ipu_5	Pull up current	Current source code [CV2,CV1,CV0]=101, pull-up current to VPRE (to 5V_REF or VVAR only for IO1-12)	-20%	5	+20%	mA	IO1-15
Ipu_4	Pull up current	Current source code [CV2,CV1,CV0]=100, pull-up current to VPRE (to 5V_REF or VVAR only for IO1-12)	-20%	1	+20%	mA	IO1-15
Ipu_3	Pull up current	Current source code [CV2,CV1,CV0]=011, pull-up current to VVAR 5V_REF, VPRE	-20%	500	+20%	uA	IO1-8
Ipu_3_lambda(1)	Pull up current	Current source code [CV2,CV1,CV0]=011,pull-up current to VVAR, 5V_REF, VPRE	450	500	550	µA	IO9-12
Ipu_3_lambda1	Pull up current	Current source code [CV2,CV1,CV0]=011, pull-up current to VPRE	-20%	500	+20%	µA	IO13- 15
Ipu_2	Pull up current	Current source code [CV2,CV1,CV0]=010, pull-up current to VPRE (to 5V_REF or VVAR only for IO1-12)	-20%	250	+20%	µA	IO1-15
Ipu_1	Pull up current	Current source code [CV2,CV1,CV0]=001, to VPRE (5V_REF or VVAR in case IO[8:1])	-20%	20	+20%	µA	IO1-8; IO13-15
Ipu_1	Pull up current	Current source code [CV2,CV1,CV0]=001 to VPRE, 5V_REF or VVAR	16	20	22	µA	IO9-12
Ipu_0	Pull up current	Current source code [CV2,CV1,CV0]=000 pull-up current to 5V_REF, VPRE	-21%	7.5	+21%	µA	IO1-12
Ipu_0	Pull up current	Current source code [CV2,CV1,CV0]=000 pull-up current to VPRE(2)	-25%	7.5	+25%	µA	IO13-15
Ipu_0_lambdaVVAR	Pull up current	Current source code [CV2,CV1,CV0]=000 pull-up current to VVAR	-50%	1	+50%	µA	IO1-12

1. *Ipu_3_lambda IO9-12 is the reference current for trimming.*
2. *In case of minimum current selection on IO[15:13], pull up voltage reaches VPRE only in case of UTh2 or UTh_ratio is configured.*

The above current ranges can be guaranteed only if sufficient headroom is available with respect to the pull-up reference voltage. In case of VPRE, Table 15. Pull up saturation voltage shows the different voltage ranges and the relative current capability.

In case 5V_REF or VVAR are selected, the above current ranges are guaranteed for all voltage ranges from 0V to 5V_REF or VVAR.

Maximum total output current through pull up IO has to be limited to 100 mA, that means five IO channels switched on at the same time with 20 mA nominal current or 10 IO with channels switched on at the same time with 10 mA nominal current.

This is related to max power dissipation. Maximum junction temperature is of 150 °C.

Table 15. Pull up saturation voltage

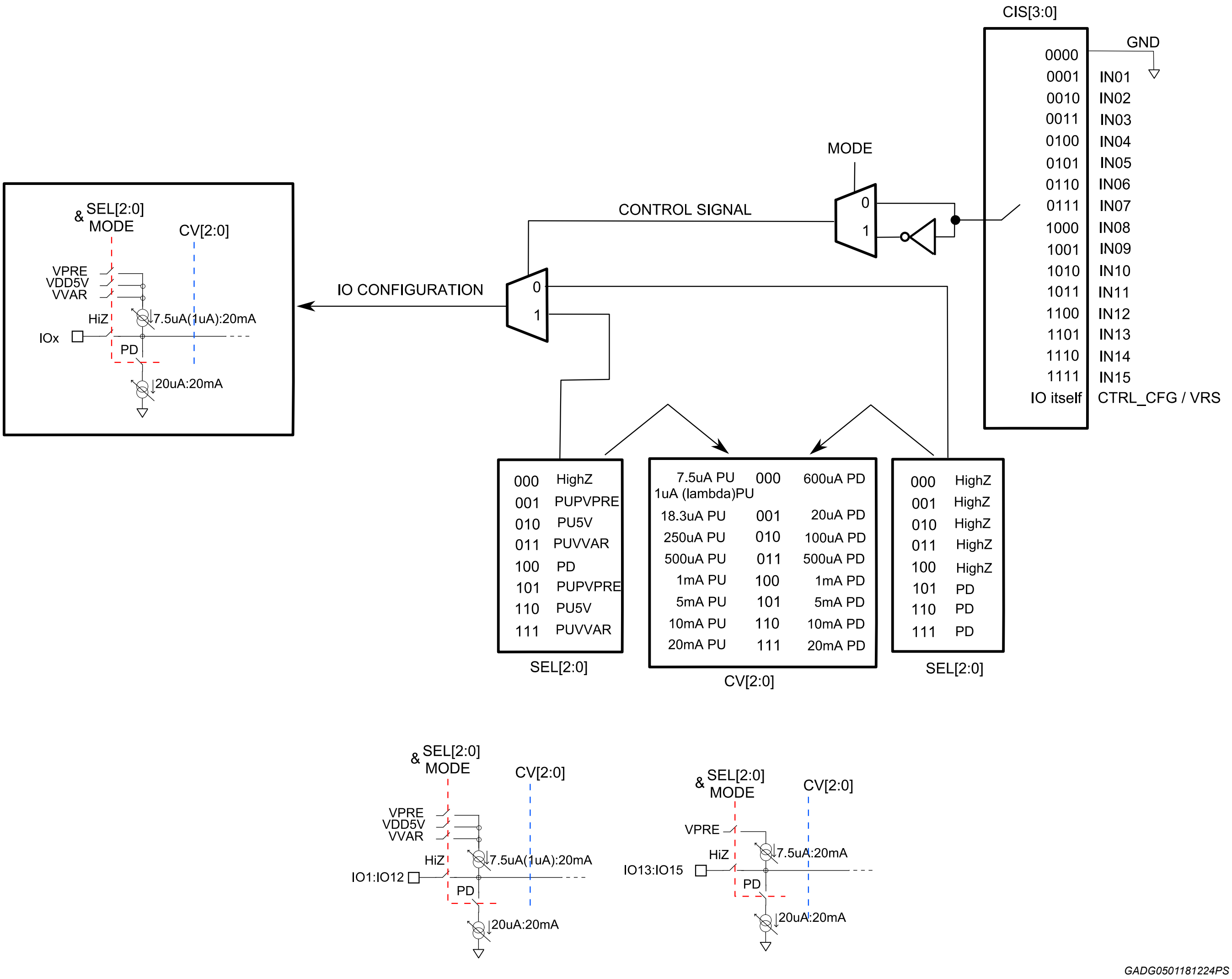
Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.							
VPUsat	Pull up voltage range	Output current is guaranteed to be non-zero	VPRE-0.2	-	-	V	IO5-15
VPUsat	Pull up voltage range	Output current is guaranteed to be non-zero	VPRE-0.25	-	-	V	IO1-4
VPUsat [(1)]	Pull up voltage range	Output current is guaranteed to be at least 10% of the nominal value (e.g. > 1.6 mA for Ipu_7)	VPRE*90%	-	VPRE-0.2	V	IO5-15
VPUsat[(1)]	Pull up voltage range	Output current is guaranteed to be at least 10% of the nominal value (e.g. > 1.6 mA for Ipu_7)	VPRE*80%	-	VPRE-0.25	V	IO1-4
VPUsat	Pull up voltage range, Ipu_x x>1	Output current is guaranteed to be within nominal range	-	-	VPRE*90%	V	IO5-15
VPUsat	Pull up voltage range, Ipu_x x>1	Output current is guaranteed to be within nominal range	-	-	VPRE*80%	V	IO1-4
VPUsat	Pull up voltage range Ipu_0, Ipu_1	Output current is guaranteed to be within nominal range	-	-	VPRE-1.5	V	IO1-15
IPUlkg	Output leakage current	Input voltage: 0 V to UBSW (input channel disabled)	-		200	nA	IO1-15

1. *In case of I_pu_0 and I_pu_1, VPUsat max is limited to VPRE-1.5 V because low drop circuit is not implemented for I_pu_0 and I_pu_1. It means that with UBSW=7.5 V current is guaranteed with VIO <=6 V*

6.3 Control of current source

For IO[4:1] if R20K_SENT_x =0 the control of current source is as reported below; if R20K_SENT_x =1, the internal current sources are kept off and the internal R = 20 kΩ pull up is connected to VDD5.

Figure 13. IOx configuration diagram



For each input, the correspondent current source is driven according to CURR_SRC_CTRL_x register in the following ways:

1. CV[2:0] bits define the current source value
2. CIS[3:0] bits define which signal controls the IOx current source configuration.

In case CIS[3:0] = 0000, no comparator is used as reference and the channel being set is controlled as always having a low level input.

In case CIS[3:0] = IOy, different from the IOx, IOy status (defined by its input comparator) selects the direction of the current source, according to SEL[2:0] and MODE bit setting. If the current source (IOx) is controlled by another IOy, the delay time depends on whether pull up or pull down voltage is set.

In case of pull up to VDD5 the delay is 5V_REF_dly, in case of pull up to VVAR the delay is VVAR_dly, as specified in Table 13.

In case CIS[3:0] selects the same channel being set (e.g. CIS[3:0] = 0011 and x = 3), an auxiliary source is selected: either the VRS or CTRL_CFG pins control the current source on channel x, based on AUX_Even/Odd channel bit in register SWITCH_ROUTE.

SEL[2:0] bits define if the current source is connected either to a pull up (and to which pull up voltage value level among VPRE, 5V_REF and VVAR) or pull down source or high impedance. The choice of the connection is defined through these 3 bits in conjunction with MODE bit that defines the “non-inversion / inversion” mode. In case of IO[15:13], only PU-VPRE is possible and any PU to 5V_REF or VVAR is automatically redirected to VPRE.

VVAR value is set through VAR_V[4:0] in DWT_VOLT_SRC_LSF_CTRL register. Every writing access to DWT_VOLT_SRC_LSF_CTRL has impact on IOx configuration. For IO[12:9], the configuration is automatically reset: in case LSF_MD_x=1, default configuration is 250 µA PU VDD5; in case LSF_MD_x=0, default configuration is HiZ. IO[8:1] maintain their configuration and V(IOx) changes according to a new VVAR value set.

MODE bit defines the non-inversion / inversion mode of the controlling input channel. MODE = 0 (Non Inv): the configuration is done assigning to the control source a ‘1’ if the control source signal is high, a ‘0’ if the control source signal is low. MODE = 1 (Inv): the configuration is done assigning to the control source a ‘0’ if the control source signal is high, a ‘1’ if the control source is low.

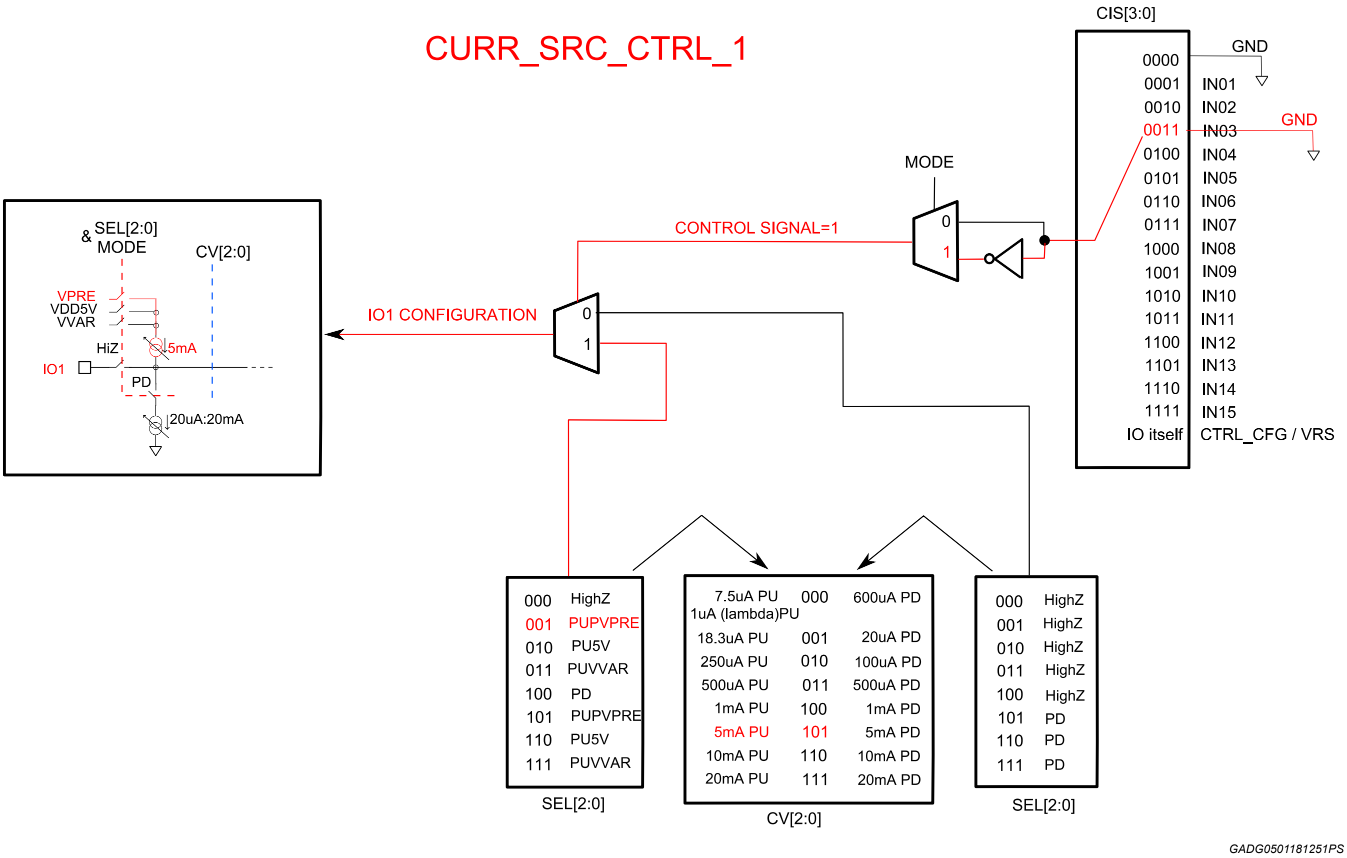
In Table 16 the IOx setting based on SEL, MODE and the control signal is reported (see Figure 13): control signal is considered as it is if MODE=0; it is considered its negated value if MODE=1

Table 16. IOx stage configuration

CURR_SRC_CTRL_x						
SEL[2:0]	MODE = 0			MODE = 1		
	input signal	control signal	PU (VDD5, VPRE, VVAR) PD or HiZ	input signal	control signal	PU (VDD5, VPRE, VVAR) PD or HiZ
000	H	1	HiZ	H	0	HiZ
001	H	1	Pu_VPRE	H	0	HiZ
010	H	1	Pu_5V_REF	H	0	HiZ
011	H	1	Pu_VVAR	H	0	HiZ
100	H	1	Pd	H	0	HiZ
101	H	1	Pu_VPRE	H	0	Pd
110	H	1	Pu_5V_REF	H	0	Pd
111	H	1	Pu_VVAR	H	0	Pd
000	L	0	HiZ	L	1	HiZ
001	L	0	HiZ	L	1	Pu_VPRE
010	L	0	HiZ	L	1	Pu_5V_REF
011	L	0	HiZ	L	1	Pu_VVAR
100	L	0	HiZ	L	1	Pd
101	L	0	Pd	L	1	Pu_VPRE
110	L	0	Pd	L	1	Pu_5V_REF
111	L	0	Pd	L	1	Pu_VVAR

Figure 14 shows an example of configuration of CURR_SRC_CTRL_1 register in order to drive IO1 with 5 mA PU to VPRE being MODE=1 and IO1 driven by IO3 which is here stuck at GND.

Figure 14. IOx configuration: IO1 driven through IO3 (stuck @ GND), Pull Up to VPRE, 5 mA, MODE=1



6.4 Binary Lambda mode

IO[12:9] present additional capabilities for the use of binary lambda sensors. By setting LSF_MDx(x = 9:12) in DWT_VOLT_SRC_LSF_CTRL, it is possible to activate binary lambda mode to control PU5V/PUVVAR configuration through the control source defined in CIS[3:0].

Every writing access to DWT_VOLT_SRC_LSF_CTRL has impact on IOx configuration. For IO[12:9], the configuration is automatically reset: in case LSF_MD_x=1, default configuration is 250 µA PU VDD5; in case LSF_MD_x=0, default configuration is HiZ.

The only selectable currents when binary lambda mode is active are reported in Table 17.

Table 17. Lambda IO current values

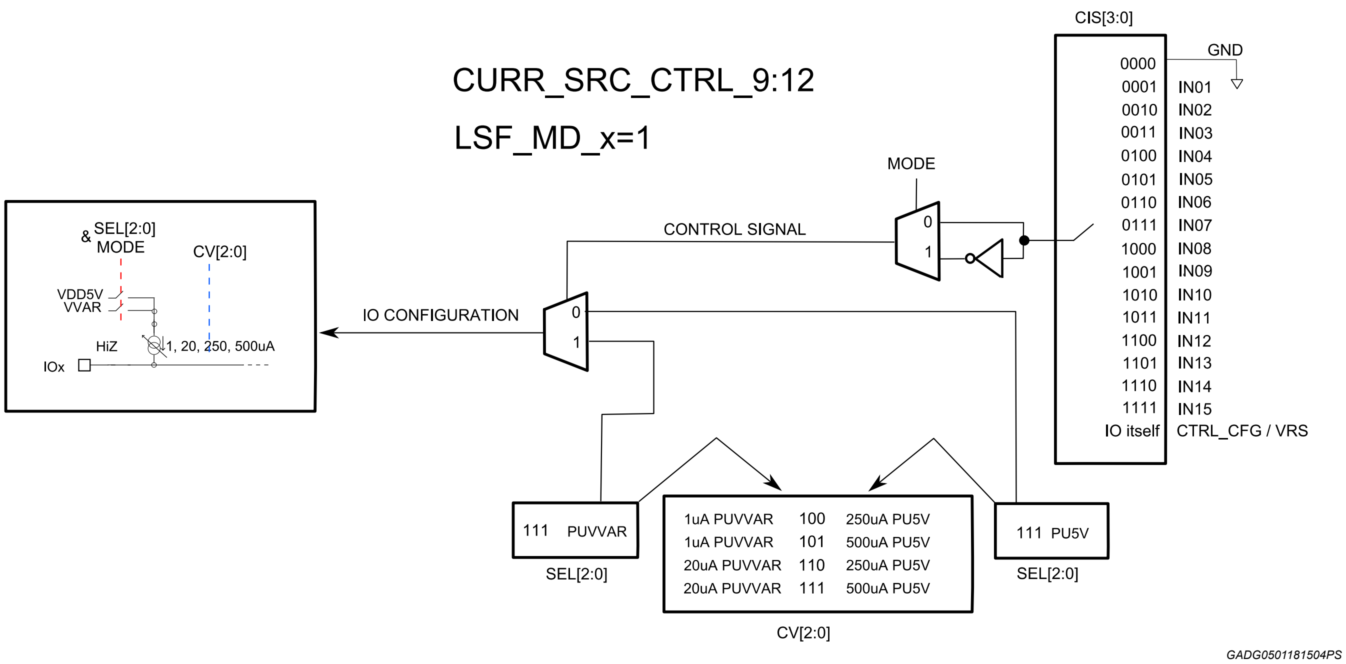
Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.							
Ipu_7_VVAR	Pull up current	Current source code [CV2,CV1,CV0]=111, pull-up current to VVAR	16	20	22	µA	IO9-12
Ipu_6_VVAR	Pull up current	Current source code [CV2,CV1,CV0]=110, pull-up current to VVAR	16	20	22	µA	IO9-12
Ipu_5_VVAR	Pull up current	Current source code [CV2,CV1,CV0]=101, pull-up current to VVAR	-50%	1	+50%	µA	IO9-12
Ipu_4_VVAR	Pull up current	Current source code [CV2,CV1,CV0]=100, pull-up current to VVAR	-50%	1	+50%	µA	IO9-12
Ipu_7_5V	Pull up current	Current source code [CV2,CV1,CV0]=111, pull-up current to 5V_REF	-10%	500	+10%	µA	IO9-12
Ipu_6_5V	Pull up current	Current source code [CV2,CV1,CV0]=110, pull-up current to 5V_REF	-20%	250	+20%	µA	IO9-12
Ipu_5_5V	Pull up current	Current source code [CV2,CV1,CV0]=101, pull-up current to 5V_REF	-10%	500	+10%	µA	IO9-12
Ipu_4_5V	Pull up current	Current source code [CV2,CV1,CV0]=100, pull-up current to 5V_REF	-20%	250	+20%	µA	IO9-12

In Table 18 and Figure 15 the IOx setting is reported, when binary lambda mode is active, based on SEL, MODE and the control signal (see Figure 15): control signal is considered as it is if MODE=0; it is considered its negated value if MODE=1

Table 18. Lambda IO stage configuration in LSF mode

CURR_SRC_CTRL_x, LSF_MD=1						
SEL[2:0]	MODE = 0			MODE = 1		
	input signal	control signal	PU (VDD5, VPRE, VVAR) PD or HiZ	input signal	control signal	PU (VDD5, VPRE, VVAR) PD or HiZ
111	H	1	Pu_VVAR	H	0	Pu_5V_REF
111	L	0	Pu_5V_REF	L	1	Pu_VVAR

Figure 15. Lambda IO stage configuration in LSF mode



6.4.1 Active discharge

When binary lambda channel switches from PullUp 5V to PullUp VVAR, corresponding IO requires a rapid discharge to operate correctly.

This can be achieved by enabling the active discharge bit ACTIVE_DSCHRG_EN_CHx(x=9:12) in ACTIVE_DSCHRG_LSF_CTRL register.

An example is reported in Figure 16. In this case IO5 controls IO9 configured as lambda IO with active discharge on.

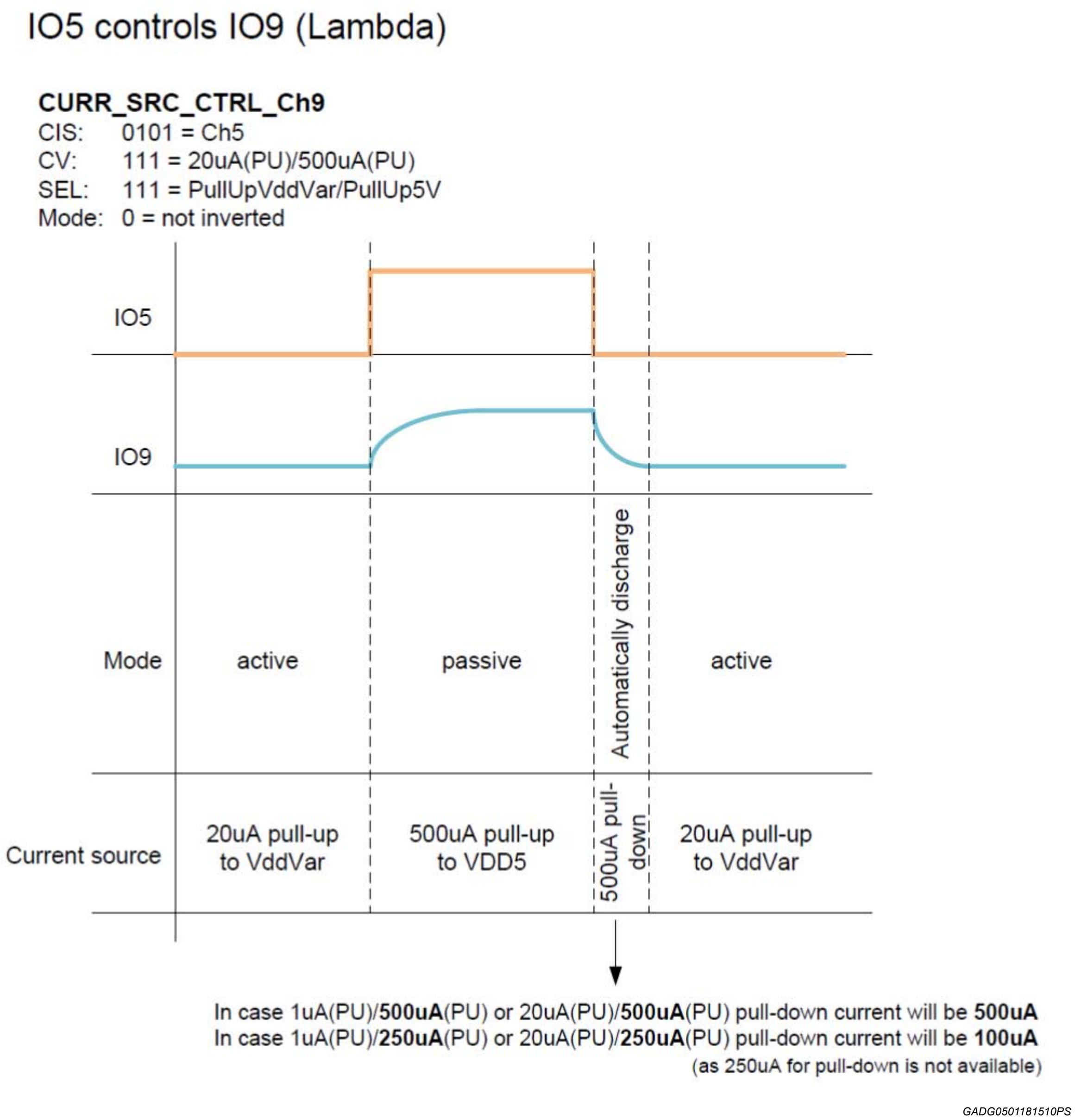


Figure 16. **Active discharge function**

The active discharge is performed by the PullDown sink for a duration configurable in ACTIVE_DSCHRG_TIM[3:0], see Table 20. The sink current is selected as shown in Table 19.

In Table 19 is reported the Pull Up current values when binary lambda mode is active, and the Pull Down current value when Active discharge based on SEL, MODE and the control signal (see Figure 13): control signal is considered as it if MODE=0; it is considered at its negated value if MODE=1.

Table 19. **Lambda IO stage configuration in LSF mode**

LSF_MD_x=1 SEL[2:0]=111 CV[2:0]	Current Value Pullup VDD5V	Current Value Pullup Vvar	Active Discharge Current Value Pull Down
111	500 µA	20 µA	500 µA
110	250 µA	20 µA	100 µA

LSF_MD_x=1 SEL[2:0]=111 CV[2:0]	Current Value Pullup VDD5V	Current Value Pullup Vvar	Active Discharge Current Value Pull Down
101	500 µA	1 µA	500 µA
100	250 µA	1 µA	100 µA

Table 20. **Lambda IO LSF mode active discharge**

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
ACT_DIS_TIM	Active discharge time	LSF_MD=1, ACT_DSCHRG_EN_CHx=1	-	ACTIVE_DSCHRG_TIM[3:0]		ms	IO9-12
ACT_DIS_TIM_RES	Active discharge time resolution	LSF_MD=1, ACT_DSCHRG_EN_CHx=1	-	-	1	ms	IO9-12

7 Multiplexing switches

The FlexInput has different type of integrated switches to connect the input channels to the desired functionality. These functionalities are:

- Integrated ADC for voltage measurement (with 4 different full-scale voltage ranges)
- Integrated ADC for resistance measurement (with 3 different resistance ranges, according to the 3 external pull-up reference resistances)
- AOX output to provide an analog output signal of the input line
- SENTx_GTMx output pins to provide the SENT signals to an external SENT decoder
- SENTx_GTMx outputs to provide a digital output signal of the input line
- Ratiometric analog comparator

The switches are controlled by register SWITCH_ROUTE, CURR_SRC_CTRL_X and SC_CONF/SQNCR_CMD registers.

The sequencer, if used, can anyhow take control of the switches settings connecting the input lines to the 2 integrated ADCs for voltage and resistance measurements.

7.1 Channels routing to SENTx_GTMx output buffers

Channel comparator output can be read with a SPI on DIG_IN_STAT register or routing the channel state to SENTx_GTMx buffers.

By default at power-up, IO15 is routed on SENT4_GTM4 while the others SENTx_GTMx outputs are kept in HiZ. Once an IOx is configured as SENT through SWITCH_ROUTE register, the corresponding SENTx_GTMx buffer is automatically programmed to output the SENT signal. An eventual previous configuration of the same SENTx_GTMx as GTM is overwritten.

Routing input channel comparators to SENTx_GTMx (x=1:4) requires:

- Disabling SENT_x functionality by writing RSENT_x = ‘0’ in SWITCH_ROUTE register (in case the SENT functionality was enabled)
- Configure the routed channel by writing SENTx_GTM_ROUTE[4:1] in GTM_TO_SENT_ROUTE_1_2 (for SENT 1/2) or in GTM_TO_SENT_ROUTE_3_4 (for SENT 3/4)

It is possible to put the SENTx_GTMx output buffers in high impedance configuring SENTx_GTM_ROUTE[4:1] = "0000" in GTM_TO_SENT_ROUTE_1_2/3_4 register.

8 ADC converter

Two sigma delta time continuous converters are implemented.

ADC1(VOLT) is a general purpose 1.25 V full scale, 12 bits ∑Δ converter used for input voltage measurement while ADC2(RES) is a dedicated 15 bits ∑Δ converter used for resistance measurement function on the 12 FlexInput analog input pins.

It is possible to access to ADC resource in two different ways: in single conversion mode (SC) or through a sequential approach (sequencer), which is equipped with 2 execution units (EU1, EU2).

A new conversion can be requested once the running conversion is completed. In case the condition is violated the algorithm can be blocked and a reset (hardware or software) is required to re-engage the procedure.

Should either IOx settings or ADCx configuration change while conversion is running, the first result after the new setting is unreliable: configuration registers are not locked.

ADC_TIMING register is used to configure settling time both for voltage and for resistance measurements. The settling time step resolution is respectively 8 μs for voltage measurement and 200 μs for resistance measurement.

Resistance measurement settling time is selectable independently for each of the RRx reference pins.

Once a single conversion or a complete sequencer cycle ends, an interrupt pulse can be generated on INT pin (if not masked). The behaviour of INT pin is defined in the register SQNCR_INT_MSK_FLG over the bit CFG_EU2, CFG_EU1 and CFG_SC. Bits INT_EU2, INT_EU1, INT_SC indicate flag which unit generated the interrupt, also in case the interrupt on INT pin is masked.

In order to avoid any noise injection on the internal nets that impacts the accuracy both for ADC1 and ADC2, no ratiometric comparator has to be connected on the IOx where the ADCs measurement is on going. To be noted that ratiometric comparator sweeps through all channels but it is effectively connected only to the IOx which have been selected for UTh_ratio.

No problem instead if the absolute comparators are used (see Section 12 Voltage comparators).

In case CALIB_FLT=1 in GEN_STATUS register, it is recommended to disable the calibration, that means configure CALIB_SEL=0 in the same register.

8.1 ADC1: voltage measurement

Purpose of this ADC is to achieve voltage measurement over all the 12 analog input pins, 3 ECU internal voltage monitors (UBSW, VI5V, VIX), internal junction temperature, internal BandGap and 3 digital input pins.

The ADC circuitry implements an input time-continuous filtering structure intended to filter out HF noise and to avoid aliasing effects, see Table 21.

Table 21. ADC analog constant time

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, T_{j-max} = 150 °C unless otherwise specified.							
ADC1tau_1_4_low	ADC input analog filter constant time	SENTx_GTM_ROUTEx=0x0 and RSENTx=0	-45%	4.4	+45%	μs	IO1-4
ADC1tau_1_4_high	ADC input analog filter Tau for SENT config	SENTx_GTM_ROUTEx≠0x0 or RSENTx≠0	-40.1%	1.235	+40.1%	μs	IO1-4
ADC1tau_5_12	ADC input analog filter constant time	-	-45%	4.20	+45%	μs	IO5-12
ADC1tau_13_15	ADC input analog filter constant time	-	-50%	8.4	+50%	μs	IO13-15
ADC1df	ADC input analog filter damping factor	-	-	20dB/dec	-	-	IO1-15

The FlexInput also implements different input voltage dividers to adapt the ADC to different input ranges. The input impedance of the channel is strongly dependent on the selected full-scale.

There are 4 different input ranges for the ADC conversion of analog inputs and 3 for the digital inputs. The default selection of the input full scale for the analog channels is 5 V, while for digital channels it is 1.25 V. Regardless of the programmed full scale range on a channel, each time the ADC1 conversion is over, the full scale range of the channel goes back to its default state.

Note: *An overshoot to VPRE occurs in case it is requested a voltage conversion with 20 V or 40 V full scale range on IO configured as PullUp at 5V_REF or VVAR.*

When converting on the digital inputs, the CTR[1:0] in the CURR_SRC_CTRL register have to be set to UTh2 or UTh_ratio thresholds.

Every time the full scale range in the ADC voltage moves from the default value (5 V, div factor 4) to a different one, a settling time (see Table 22) is automatically added to the configurable setting time (CT_AD[2:0] in ADC_TIMING register) to allow the signal to reach a steady value.

ADC1 reference voltage is ratiometric with 5 V_REF voltage, so no absolute internal reference is used for ADC1 conversion. Digital out is $V_{in}/V_{fullrange}$ represented over 12 bits.

Table 22 shows the contributors to the accuracy of the overall conversion, from input signal to digital readout. Two parts are considered: the input voltage dividers, with their accuracy, and the ADC block, with its accuracy. To get the overall accuracy of conversion, both these contributors must be taken into account.

In order to reach the best accuracy with the full range of 5 V, calibration has to be activated by setting CALIB_SEL to ‘1’. Calibration feature is guaranteed in case calibration fault CALIB_FLT flag in GEN_STATUS register is not set.

By default the calibration is disabled (CALIB_SEL = ‘0’): the status of the CALIB_FLT flag should be verified, then the calibration eventually enabled or kept disabled accordingly.

Table 22. ADC1 parameters

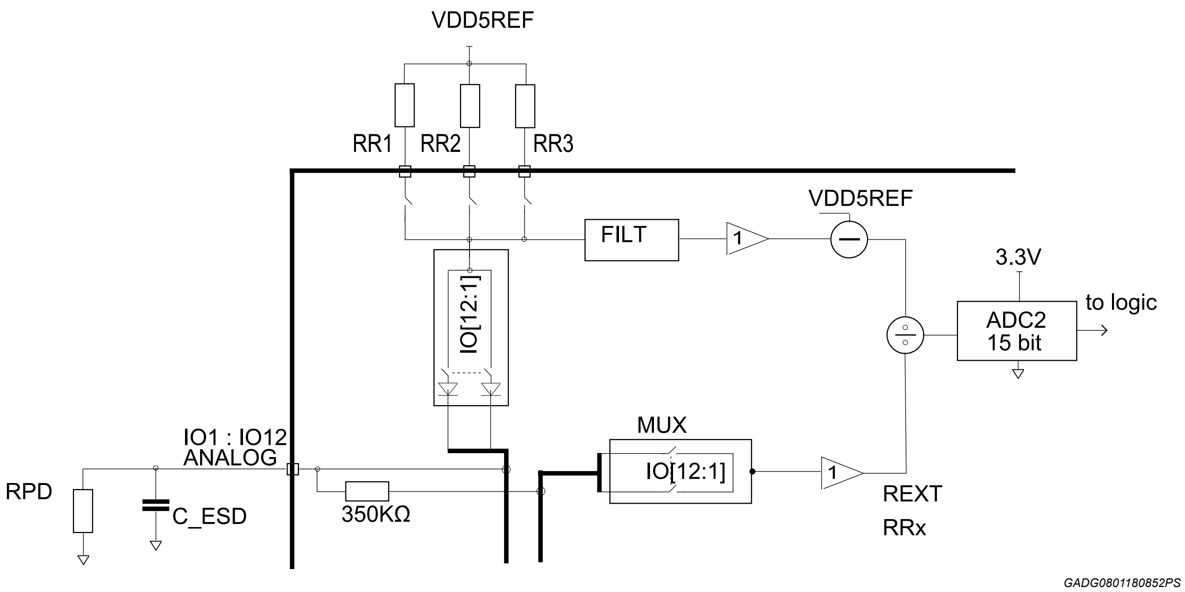
Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.							
ADC1res	ADC resolution	-	-	12	-	bit	-
ADC1range_1_25	ADC input range	Full range: 1.25 V, buffer structure	0.03	-	1.23	V	IO 1-15
ADC1range_5	ADC input range	Full range: 5 V	0.05	-	4.95	V	IO 1-12
ADC1range_20	ADC input range	Full range: 20 V	0.45	95%FR=18.3+-3%		V	IO 1-4
				95%FR=19.0+-3%		V	IO5-15
ADC1range_40	ADC input range	Full range: 40 V	0.8	95%FR=38.9+-3%		V	IO 1-15
ADC1err	ADC block error	With calibration Design info (1LSB = 1.22 mV)	-	-	4	LSB	-
ADC1err_a_1_25	ADC1 total measurement error on analog inputs	Including all error contributions (VDD5REF excl.) While no ratiometric comparator running Full range 1.25 V (1LSB = 0.3 mV)	-	-	40	LSB	IO 1-12
ADC1err_a_5	ADC1 total measurement error on analog inputs	Including all error contributions (VDD5REF excl.) While no ratiometric comparator running Full range 5 V (1LSB = 1.22 mV) CALIB_FLT=0 and CALIB_SEL=1, with ADC1tau_1_4_low selected	-	-	10	LSB	IO 1-12
ADC1err_a_5_no_calib	ADC1 total measurement error on analog inputs	Including all error contributions (VDD5REF excl.) While no ratiometric comparator running Full range 5 V (1LSB = 1.22 mV) CALIB_SEL=0	-	-	64	LSB	IO 1-12
ADC1err_a_20	ADC1 total measurement error on analog inputs	Including all error contributions (VDD5REF excl.) While no ratiometric comparator running Full range 20 V (1LSB = 5 mV)	-	-	90	LSB	IO 1-12

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
ADC1err_a_40	ADC1 total measurement error on analog inputs	Including all error contributions (VDD5REF excl.) While no ratiometric comparator running Full range 40 V (1LSB = 10 mV)	-	-	90	LSB	IO 1-12
ADC1err_d_1_25	ADC1 total measurement error on digital inputs	Including all error contributions (VDD5REF excl.) While no ratiometric comparator running Full range 1.25 V (1LSB = 0.3 mV)	-	-	100	LSB	IO 13-15
ADC1err_d_20	ADC1 total measurement error on digital inputs	Including all error contributions (VDD5REF excl.) While no ratiometric comparator running Full range 20 V (1LSB = 5 mV)	-	-	100	LSB	IO 13-15
ADC1err_d_40	ADC1 total measurement error on digital inputs	Including all error contributions (VDD5REF excl.) While no ratiometric comparator running Full range 40 V (1LSB = 10 mV)	-	-	100	LSB	IO 13-15
AFlexInputZ_1_25	Analog FlexInput input Impedance	Full range: 1.25 V	>>10M	-	-	Ω	IO 1-12
AFlexInputZ_5	Analog FlexInput input Impedance	Full range: 5 V	>>10M	-	-	Ω	IO 1-12
AFlexInputZ_20	Analog FlexInput input Impedance	Full range: 20 V	>200K	-	-	Ω	IO 1-12
AFlexInputZ_40	Analog FlexInput input Impedance	Full range: 40 V	>200K	-	-	Ω	IO 1-12
DflexInputZ_1_25	Digital FlexInput input Impedance	Full range: 1.25 V	>500K	-	-	Ω	IO 13-15
DflexInputZ_20	Digital FlexInput input Impedance	Full range: 20 V	>500K	-	-	Ω	IO 13-15
DflexInputZ_40	Digital FlexInput input Impedance	Full range: 40 V	>500K	-	-	Ω	IO 13-15
ADC1settl_1_25	ADC settling time	Full range: 1.25 V Not to be programmed, already embedded in the logic	-9%	4	+9%	µs	IO 1-15
ADC1settl_5	ADC settling time	Full range: 5 V Not to be programmed, already embedded in the logic	-9%	1.5	+9%	µs	IO 1-12
ADC1settl_20	ADC settling time	Full range: 20 V Not to be programmed, already embedded in the logic	-9%	15	+9%	µs	IO 1-15
ADC1settl_40	ADC settling time	Full range: 40 V Not to be programmed, already embedded in the logic	-9%	10	+9%	µs	IO 1-15
ADC1settl	ADC settling time	UBSW, VI5V, VIX, internal bandgap	-9%	1.5	+9%	µs	-
ADC1conv	ADC conversion time	Not considering ADCsettl	-9%	40	+9%	µs	IO 1-15

8.2 ADC2: resistance measurement

The device implements a dedicated function to perform high precision resistance measurements connected between analog input pin IO[12:1] and ground. In Figure 17 a simplified circuit is reported..

Figure 17. **Simplified circuit for resistance measurement**



A wide measurement range is allowed by selecting the pull-up external reference resistors.

Digital out is RPD/RRx represented over 15 bits fixed point number (4 bits integer, 11 bits fractional). The result from the SPI register needs then to be divided by 2048.

$$RPD = \frac{ADC2\_RESULT}{2048} * RRx$$

In order to reach the best accuracy, calibration of ADC, both ADC1 and ADC2, has to be activated by setting CALIB_SEL to ‘1’. Calibration feature is guaranteed in case calibration fault CALIB_FLT flag in GEN_STATUS register is not set.

By default the calibration is disabled (CALIB_SEL = ‘0’): the status of the CALIB_FLT flag should be verified, then the calibration eventually enabled or kept disabled accordingly.

Depending on the selected external pull-up resistance RRx, a specific settling time has to be considered (see Table 23. ADC2 parameters). Bit CT_PUx[3:0] in ADC_TIMING register can be used to set the proper settling time for each pull up resistance selected (RRx).

Best accuracy is achieved when RPD/RRx is close to 1.

Table 23. **ADC2 parameters**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.						
RMEASrange	Resistance measurement range	-	50		400K	Ω
RMEASacc_L	Total resistance measurement accuracy	0.1<RPD/RRx<8 50 to 2K, RRx = 470 Ω Excl. external pull-up RRx precision No ratiometric comparator running CALIB_FLT=0 and CALIB_SEL=1	-	-	1.5	%
RMEASacc_M	Total resistance measurement accuracy	0.1<RPD/RRx<8 2K to 30K, RRx = 9 kΩ Excl. external pull-up RRx precision No ratiometric comparator running CALIB_FLT=0 and CALIB_SEL=1	-	-	1.5	%

Symbol	Parameter	Condition	Min	Typ	Max	Unit
RMEASacc_H	Total resistance measurement accuracy	0.1<RPD/RRx<8 30K to 400K, RRx = 50 kΩ Excl.external pull-up RRx precision No ratiometric comparator running CALIB_FLT=0 and CALIB_SEL=1	-	-	1.5	%
RMEASacc_L	Total resistance measurement accuracy	0.1<RPD/RRx<8 50 to 2K, RRx = 470 Ω Excl. external pull-up RRx precision No ratiometric comparator running CALIB_SEL=0	-	-	10	%
RMEASacc_M	Total resistance measurement accuracy	0.1<RPD/RRx<8 2K to 30K, RRx = 9 kΩ Excl. external pull-up RRx precision No ratiometric comparator running CALIB_SEL=0	-	-	10	%
RMEASacc_H	Total resistance measurement accuracy	0.1<RPD/RRx<8 30K to 400K, RRx = 50 kΩ Excl.external pull-up RRx precision No ratiometric comparator running CALIB_SEL=0	-	-	10	%
RMEASacc_LL	Total resistance measurement accuracy	0.01<RPD/RRx<0.1 No ratiometric comparator running CALIB_FLT=0 and CALIB_SEL=1	-	-	19	%
RMEASacc_HH	Total resistance measurement accuracy	8<RPD/RRx<16 No ratiometric comparator running (regardless CALIB_SEL)	-	-	10	%
Rsw_mux_force_1_4	Internal switch impedance	IO[4:1] pins	-	72	125	Ω
Rsw_mux_force_5_12	Internal switch impedance	IO[12:5] pins	-	75	125	Ω
RMEASsettl time	Resistance measurement settling time	Design info With 6.8 nF and RRx = 470 Ω	-	-	50	µs
RMEASsettl time	Resistance measurement settling time	Design info With 6.8 nF and RRx = 9 kΩ	-	-	400	µs
RMEASsettl time	Resistance measurement settling time	Design info With 6.8nF and RRx = 50 kΩ	-	-	1.8	ms
ADC2conv	ADC conversion time	-	-9%	80	+9%	µs
ADC2res	ADC resolution	-		15		bit
ADC2range	ADC input range	RPD/RRx[1]	0.01		16	Ω/Ω

1. 0.01<RPD/RRx<0.1 the measurement can be performed but the accuracy is degraded.

In order to reach the best accuracy, calibration has to be activated setting CALIB_SEL. Calibration feature is guaranteed in case calibration fault CALIB_FLT flag in GEN_STATUS register is not set.

9 Measurement approaches

9.1 Single conversion (SC)

Once the single conversion mode is selected, the FlexInput performs a single shot voltage conversion (ADC1) or a resistance measurement (ADC2).

The single conversion command parameters are set through the SC_CONF register.

Single conversion is defined through the following parameters:

- Type of measurement (voltage or resistance) via R_VOLT_MEAS_SELECT bit – SC_CONFIG register;
- Full scale range (voltage measurement) or RRx (resistance measurement) via PUPx_DIV[1:0] – SC_CONFIG register. If either UBSW, VI5V or VIX is measured, the correspondent full scale range is 1.25 V and the partitioning is defined in Section 11 Voltage dividers and internal signals
- channel to be converted through ADC_MUX[4:0] – SC_CONFIG register:
  – for voltage measurement: one of the 15 IO channels (both analog and digital) or UBSW, VI5V, VIX, internal junction temperature T_j = 0.133ADCdec-261.043, only OT is guaranteed see Table 9. Chip status electrical parameters. or the internal bandgap voltage reference (BG)
  – for resistance measurement: one of the 12 IOx analog channels only
  – in case of invalid code selection, the ADC will run the conversion anyhow, but the result is meaningless
- Start the conversion through ADC_RUN bit – SC_CONFIG register. This bit can be only written to 1 in order to start the conversion and it is automatically reset once the conversion ends.
- ADC settling time in ADC_TIMING register

Single conversion result is available in a dedicated register, SC_RESULT.

The result is written on:

- A 12 bits field ADC[11:0] in case of voltage measurement; a flag NEW_RSLT_FLG is also set in case new conversion result is available. This flag is reset once the register is read, but the result on the register is still kept.
- A 15 bits field ADC[14:0] in case of resistance measurement. Once the register is read, it is automatically reset, 0x0 value indicates the measurement has been already read.

9.2 Sequencer

The sequencer controls the scheduled execution of analog-to-digital conversions on ADC1 (voltage measurement) and ADC2 (resistance measurement).

As showed in Figure 18, sequencer operates as 3 execution units (EU1, EU2, SC) that fetch conversion requests from registers and passes them to ADCs according to a priority mechanism.

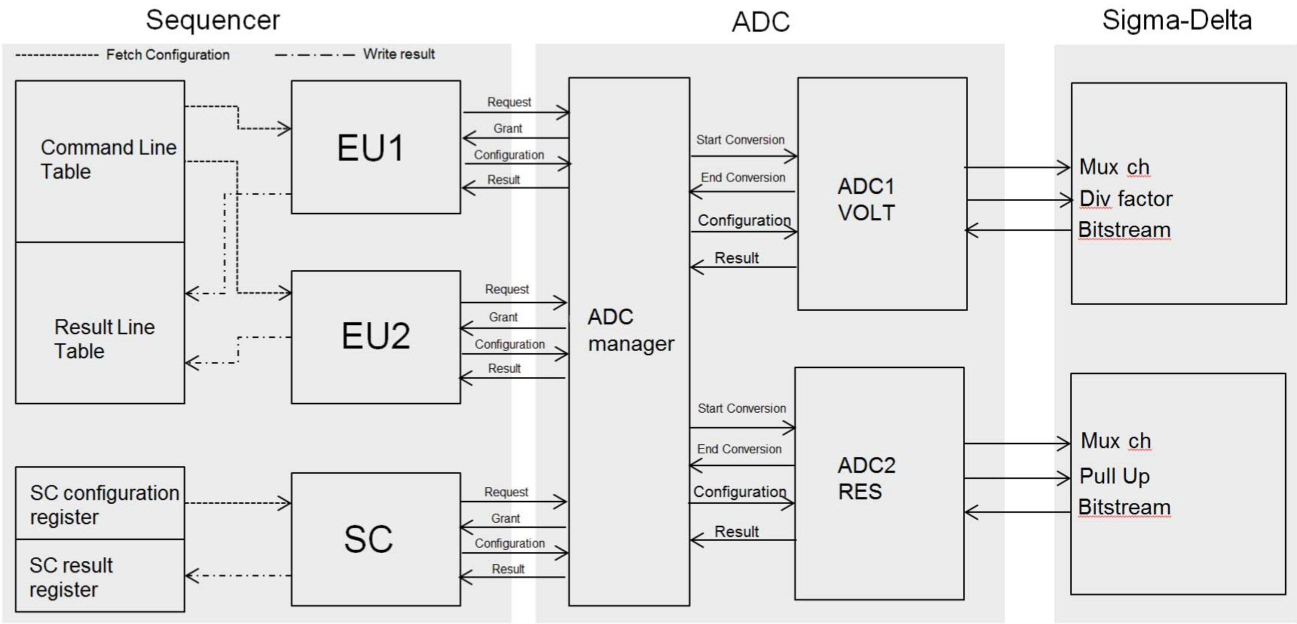
Execution units EU1 and EU2 are able to perform a sequence of ADC conversions. The sequence is programmed as per the following:

- register SQNCR_CTRL, to set the sequence start line address on the different SQNCR_CMD[15:1] registers (INIT_PC_EUx[3:0]) and to enable the sequence start. Sequencer start is triggered in two ways. The first is SPI setting of EUx_EN bit, the second is through SYNC pin, toggling once EUx_SYNC_EN bit is set. In this last case EUx_EN bit is automatically set with a rising edge of the SYNC pin occurs.
- registers SQNCR_CMD[15:1] to instruct the sequencer about the conversions to process and the next line to be addressed.

Sequences can be configured as one of the following:

- Closed loop: configuration is such that the last step points back to any of the previous lines of the sequence, thus forming a closed continuous loop.
- Open loop: configuration is such that the last sequence step points to ENDLOOP code on NXT_PC (code ‘0000’). ENDLOOP condition occurs and sequence stops.

Figure 18. **ADC conversion chain**



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In order to start the sequencer correctly, INIT_PC_EUx[3:0] field in SQNCR_CTRL register has to be properly filled, for both EUx, with the first sequence lines. By default, in fact, INIT_PC_EUx[3:0] points to the ENDLOOP. The sequencer is blocked if it starts (through SYNC signal if EUx_SYNC_EN =1 or SPI if EUx_EN=1) with INIT_PC_EUx[3:0] = ENDLOOP.

Once the sequencer runs (EUx_EN=1) any write access to SQNCR_CTRL register is ignored, avoiding any unpredictable operation sequence.

In case the sequencer is running, any modification in its configuration requires the sequencer to be stopped resetting EUx_SYNC_EN and EUx_EN in SQNCR_CTRL register.

9.2.1 Sequencer channels addressing

The sequencer can use both the ADC1 for voltage measurements and ADC2 for resistance measurements.

Each input channel measurement is configurable through a dedicated register SQNCR_CMD_x [x=1:15] . The measurement results are instead readable in the register SQNCR_RESULT_x [x=1:15]. Table 24 shows the addresses for configuration and result lines.

For ADC1, the meaningful input channels are:

- all the analog channels IO[12:1]
- UBSW, VI5V and VIX pins.

For ADC2, the meaningful input channels are:

- all the analog channels IO[12:1]

UBSW, VI5V and VIX pins can be fed into ADC2, but the results are meaningless.

Table 24. **Channel addressing**

	Description
0xC1	Configuration Analog Channel 1
0xC2	Configuration Analog Channel 2
0xC3	Configuration Analog Channel 3
0xC4	Configuration Analog Channel 4
0xC5	Configuration Analog Channel 5
0xC6	Configuration Analog Channel 6
0xC7	Configuration Analog Channel 7
0xC8	Configuration Analog Channel 8
0xC9	Configuration Analog Channel 9
0xCA	Configuration Analog Channel 10
0xCB	Configuration Analog Channel 11
0xCC	Configuration Analog Channel 12
0xCD	Configuration UBSW
0xCE	Configuration VI5V
0xCF	Configuration VIX
0xE1	Result Analog Channel 1
0xE2	Result Analog Channel 2
0xE3	Result Analog Channel 3
0xE4	Result Analog Channel 4
0xE5	Result Analog Channel 5
0xE6	Result Analog Channel 6
0xE7	Result Analog Channel 7
0xE8	Result Analog Channel 8
0xE9	Result Analog Channel 9
0xEA	Result Analog Channel 10
0xEB	Result Analog Channel 11
0xEC	Result Analog Channel 12
0xED	Result UBSW
0xEE	Result VI5V
0xEF	Result VIX

Sequencer configuration Channel x:

SQNCR_CMD_x is used for the following channel-specific settings:

- Type of measurement (voltage or resistance) via R_VOLT_MEAS_SELECT bit
- Full scale range (voltage measurement selected) or RRx (resistance measurement selected) via PUPx_DIV[1:0]. If either UBSW, VI5V or VIX is measured, the correspondent full scale range is 1.25 V and the partitioning is defined in Section 11 Voltage dividers and internal signals
- Next line to be processed through NXT_PC[3:0]. NXT_PC is ‘0000’ is intended as ENDLOOP condition. When the ENDLOOP is reached, the sequencer stops.

Result ADC channel x:

Sequencer results are fed into internal buffers then, before reading SQNCR_RESULT_x registers, a copy command has to be issued.

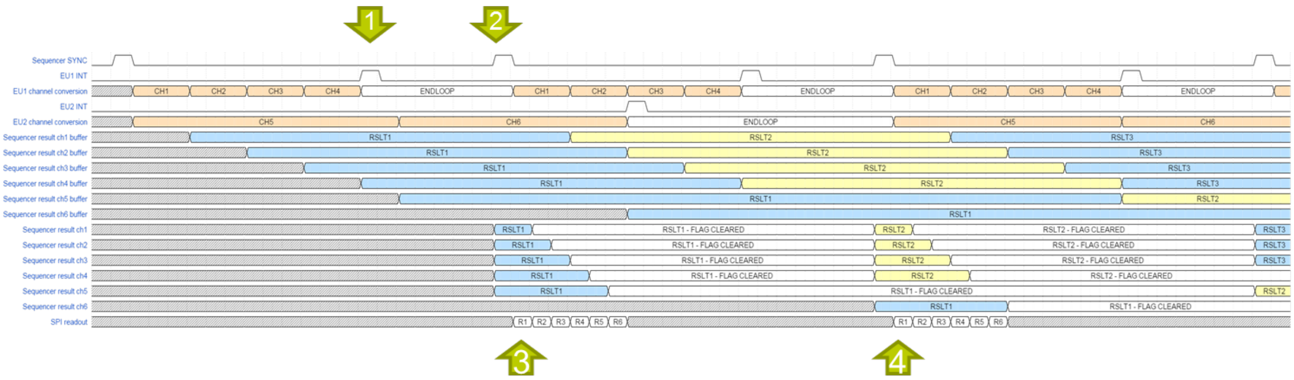
Copy command can be issued by the two following options:

- SPI reading access on SQNCR_RSLT_COPY_CMD register
- SYNC pin trigger, provided that it is configured to be used for copy command operation, setting SYNC_CMD_EN in SQNCR_CTRL register.

SPI reading access on SQNCR_RSLT_COPY_CMD register always issues a copy command even in case SYNC_CMD_EN is set.

Buffering operation:

Figure 19. **SEQUENCER flow example**



GADG0801181136PS

The Figure 19 is an example of the sequencer using two EUs: EU1 has a sequence from CH1 to CH4, EU2 from CH5 to CH6. SYNC toggling has enabled the copy command. EU1 measures voltages (ADC1) while EU2 resistance (ADC2).

1. When EU1 completes its loop, interrupt is generated (see Section 9.3 Interrupt generation).
2. To read results, it is necessary to wait for the rising edge of SYNC filtered pulse, so that results are copied to the SPI registers.
3. At readout, results are read with the “new result flag”, except for the CH6 result which is not available yet. After readout, NEW_RESULT flag is cleared.
4. At next SYNC pulse, new results from EU1 are available. For EU2, only new result from CH6 is available, CH5 is read with its NEW_RESULT flag cleared.

L9966 allows distinguishing whether data reported in SQNCR_RESULT_x register has been already read. In case of voltage measurement bit SQNCR_RESULT_x[14] is set (clear on read bit). For resistance measurement, instead, the whole content of the SQNCR_RESULT_x is reset once read.

Table 25 describes the copy command according to the availability of a new result and SPI readout operation occurred before the copy command.

Table 25 is referenced to each sequencer line; the copy command action has effect on all the 15 internal buffer result registers at the same time. Nonetheless, the NEW_RESULT flag is handled for each result individually, as the SPI readout operation is individual for each line.

Table 25. **Copy CMD effect**

SPI readout	New measurement data available	Copy command effect
No readout	No	Overwrite SPI register with buffer content (same data) NEW_RESULT flag set

SPI readout	New measurement data available	Copy command effect
No readout	Yes	Copy of buffer content (with new data) NEW_RESULT flag set
Readout	No	Overwrite SPI register with buffer content (same data) NEW_RESULT flag not set
Readout	Yes	Copy of buffer content (with new data) NEW_RESULT flag set

9.2.2 Sequencer execution control

Sequencer starting phase is defined in SQNCR_CTRL register through EUx_EN or EUx_SYNC_EN bit:

- EUx_EN = ‘1’ allows sequencer starting (see Section 9.2.3 Priority mechanism for conflict management); EUx_EN = ‘0’ stops the correspondent EUx as soon as the running ADC conversion is completed.
- EUx_SYNC_EN = ‘1’ allows correspondent EUx starting synchronous with the rising edge of the external SYNC signal. In case SYNC rising edge occurs while the sequencer is running, SYNC toggle is ignored.

In case of open loop sequence, once the specific EUx is over, EUx_EN bit is automatically reset; EUx_EN bit is otherwise always kept enabled.

Execution flows steps:

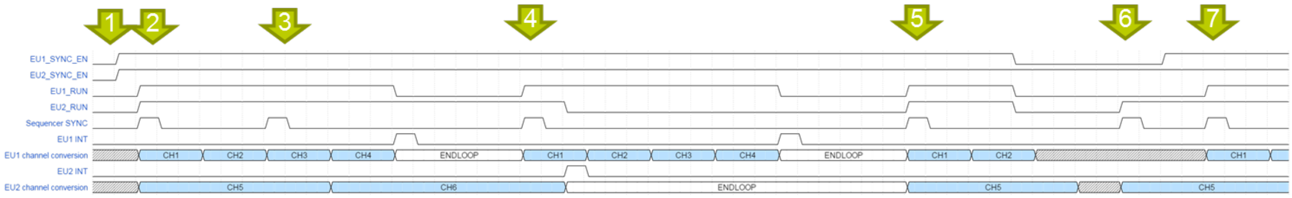
1. The execution unit EUx is started by setting the run bit EUx_EN=’1’ (by SPI command or by SYNC). Following steps run only if EUx_EN bit is kept to ‘1’, otherwise the correspondent EUx will stop without asserting the INT pin to flag the end of conversion.
2. As a first step, the EUx reads the control data on register SQNCR_CTRL.
3. The EUx waits for the requested ADC to be available.
4. The EUx sets the ADC according to the configuration written in the first SQNCR_CMDx being chosen.
5. The EUx starts the ADC conversion and waits till the conversion is finished.
6. The EUx moves the ADC data to the internal buffer result register corresponding to the pointed channel.
7. The EUx reads the next buffer line address (SQNCR_CMDx). If the sequencer is configured to run closed sequences, the EUx starts over with step 2, else it stops.
8. If not masked (register SQNCR_INT_MSK_FLG), an interrupt is generated on INT pin each time a closed sequence starts over or the ENDLOOP condition occurs (see Section 9.3 Interrupt generation).

Once running, the sequencer is not stopped abruptly. If EUx_EN are asynchronously written to zero the eventual ADCx ongoing conversion is completed then the execution unit EUx stops with no INT assertion.

In Figure 20 a possible scenario of sequencer being controlled by the SYNC pin is shown.

1. Before starting the sequencer, both EU1 and EU2 are configured to be triggered by the SYNC pin.
2. As soon as the filtered SYNC pulse rising edge is detected, both EUx start.
3. SYNC pulse occurs while both EUx are running -> SYNC toggle ignored.
4. SYNC pulse occurs when EU1_EN has reached its ENDLOOP condition (EU1_EN=0) whereas EU2 is still running -> EU1 starts a new loop, EU2 ignores the SYNC toggle.
5. SYNC pulse is detected once both EUs have completed their sequence -> both start a new run.
6. EU1 and EU2 are stopped via SPI, writing EU1_EN, EU2_EN and EU1_SYNC_EN to ‘0’. Being EU2_SYNC_EN set, a new SYNC toggle starts EU2 only.
7. EU1_SYNC_EN is set again: next SYNC toggle restarts EU1, while EU2 keeps on running.

Figure 20. **SYNC controlled sequencer example**



GADG0801181212PS

The input voltage on SYNC is evaluated with a comparator, see Table 26. The digital signal after the comparator is filtered for time duration $t_{SYNC\text{-}glitch}$ before triggering the sequencer. The trigger event is a rising edge on filtered SYNC pulse.

Table 26. **SYNC pin parameters**

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.							
VinH	SYNC input high level	-	-	1.7	2.3	V	SYNC
VinL	SYNC input low level	-	1.2	1.4	-	V	SYNC
Vhys	SYNC input hysteresis	-	0.23	-	0.6	V	SYNC
$t_{SYNC\text{-}glitch}$	SYNC input filter time	-	4.2	4.7	5.2	µs	SYNC
RPD	SYNC input pull-down	-	60	105	150	kΩ	SYNC

9.2.3 Priority mechanism

The two EUx work in parallel with shared resources (ADC resistance and ADC voltage). The EU has access to the selected ADC as soon as it is no more engaged by the other EU or the SC. In case more than one EU has a request to the same ADC, the ADC manager applies the following priority rules:

- Priority HIGH: Single Conversion Module
- Priority MEDIUM: Execution Unit 1
- Priority LOW: Execution Unit 2

In case of continuous loop programmed, EU1 loses its priority for one clock cycle every time its sequence is completed (that means INT is generated, see Section 9.3 Interrupt generation) and Figure 21 INT_EU1 in SQNCR_INT_MSK_FLG is set leaving to EU2 the opportunity to proceed with an eventual pending request on ADC_x.

Table 27 and Figure 21 report an example of ADC priority management in case of conflict in the access to one ADCx through the sequencer flow:

EU1 performs CH1, CH2 CH3, CH4 voltage conversion, then points back to CH1 and generates the interrupt.

EU2 performs resistance measurement on CH11, CH12, voltage measurement on VI5V, VIX then points back to CH11 and generates the interrupt.

SC voltage measurement on CH5 occurs while EU1 is running.

At cursor 1, EU1 completes the sequence and thus loses priority for one clock cycle. In that moment, neither EU2 nor SC are requesting ADC1, then EU1 restarts the sequence with CH1 conversion right after.

At cursor 2, EU2 has already completed ADC2 conversions on CH11 and CH12 and has a pending request for ADC1. As soon as EU1 ends the sequence, EU2 can take over, performing ADC1 conversion on VI5V. At conversion end, EU1 regains priority and restarts with CH1.

At cursor 3, SC on ADC1 CH5 occurs. Since SC has the highest priority, it will immediately take over once ADC1 is available (CH3 conversion is over). At the end of SC, EU1 gains access to ADC1 with CH4 until the end of the loop.

At cursor 4, EU1 loses the priority and thus EU2 can perform ADC1 conversion on VIX and complete its sequence.

Table 27. **Example of sequencer priority case**

	Address	NEXT_PC	PUP_DIV	_VOLT_MEAS_SE
Line CH1	0xC1	Line CH2	Pup_5V	VOLT
Line CH2	0xC2	Line CH3	Pup_5V	VOLT
Line CH3	0xC3	Line CH4	Pup_5V	VOLT
Line CH4	0xC4	Line CH1	Pup_5V	VOLT
Line CH5	0xC5			
Line CH6	0xC6	-	-	-
Line CH7	0xC7	-	-	-
Line CH8	0xC8	-	-	-
Line CH9	0xC9	-	-	-
Line CH10	0xD0	-	-	-
Line CH11	0xD1	Line CH12	RR1	RES
Line CH12	0xD2	Line VI5V	RR2	RES
Line UBSW	0xD3	-	-	-
Line VI5V	0xD4	Line VIX	Pup_5V	VOLT
Line VIX	0xD5	Line CH11	Pup_5V	VOLT

Figure 21. **Example of sequencer priority case**

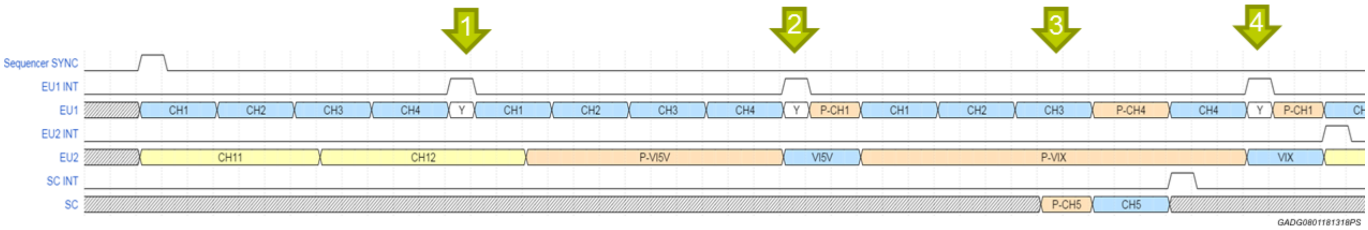


Figure 22 shows a scenario where SC request occurs while EU1 is running last sequence step and EU2 is also waiting to access to the shared ADC1. At cursor 2, EU1 reaches the end of the loop and SC, with highest priority level, is immediately served. EU2 has to wait EU1 reaching next end loop to be served, at cursor 3.

Figure 22. **Example of sequencer priority case**

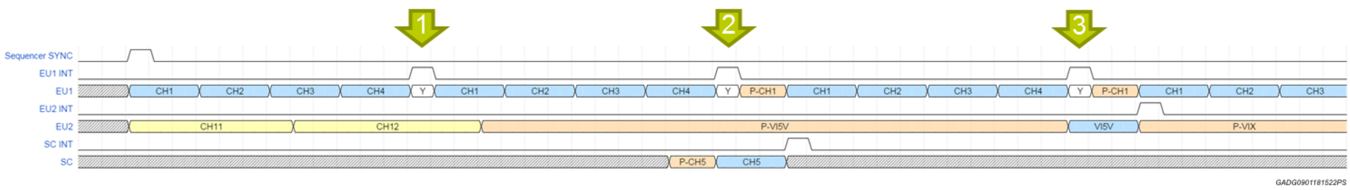


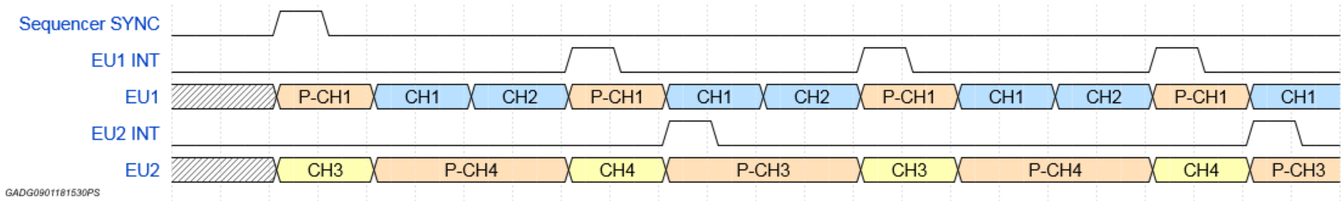
Figure 23 shows the case where EU1 and EU2 require the same ADC in the first sequence command line. The case is:

- EU1 requires ADC1 to measure IO1 and IO2 in loop and INT_EU1_CONF=IO1
- EU2 requires ADC1 to measure IO3 and IO4 in loop and INT_EU2_CONF=IO3

Both EUx are enabled through SYNC signal and both are in LOOP (the last command line points back to the first one).

As SYNC pin rises, EU2 starts performing ADC1 conversion on IO3 while EU1 waits for the yield. At the end of the conversion, EU1 gains priority and starts running with IO1. Once EU1 loop is completed, it loses priority for one clock cycle, EU2 can take over, performing ADC1 conversion on IO4. The procedure runs up to EUx_EN is forced 0.

Figure 23. **Example of sequencer priority case**



Every time the sequencer starts with an ADC conflict in the first line, EU2 takes the priority then the mechanism proceeds as described in the above scenarios.

9.3 Interrupt generation

Every time an EUx/SC loop reaches an interrupt condition, a pulse on INT pin can be generated.

EU_x/SC interrupt on INT pin can be masked by writing corresponding CFG_EU[2:1]/CFG_SC to ‘1’ in the SQNCR_INT_MSK_FLG.

As the interrupt is asserted, a flag is set on INT_EU[2:1]/INT_SC on the SQNCR_INT_MSK_FLG; such a flag is not masked by CFG_EU[2:1]/CFG_SC and gets cleared after being read.

Interrupt condition

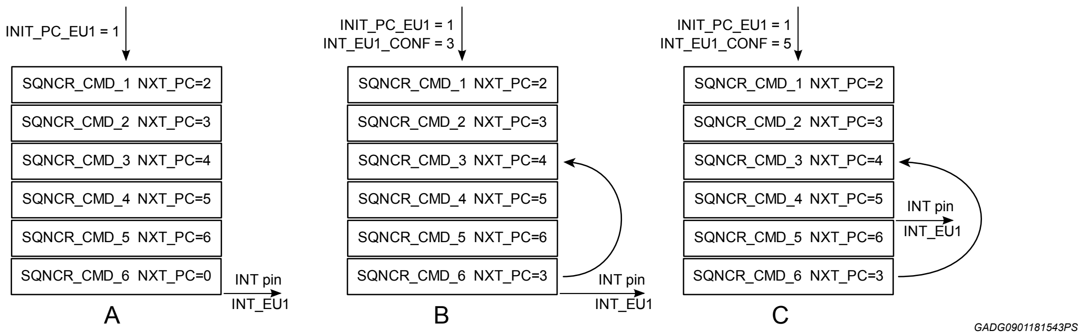
Provided that no interrupt mask is enabled, the conditions that can lead to the generation of the interrupt are the following.

For EUx, there are two possible cases: open loop and closed loop condition. In **open loop condition**, EUx completes the last step conversion then points to ENDLOOP determining the interrupt generation, as shown in **A** next figure. In **closed loop condition** instead, INT generation depends on what is programmed in INT_EUx_CONF[3:0] field of the SQNCR_INT_MSK_FLG register.

Note: INT_EUx_CONF are write only fields, any read back returns 0000.

INT is generated every time EUx has processed the SQNCR_CMD_x line whose NEXT_PC points to the same line selected in INT_EUx_CONF[3:0] field, as shown in B and C of the following figure.

Figure 24. **Interrupt condition open/closed loop INT generation**



A	open loop, INT generation
B	closed loop and INT generation in case the last SQNCR line points back to the same line of INT_EU1_CONF
C	closed loop and INT generation in case the last SQNCR line points back to a different line in respect of the one of INT_EU1_CONF

In case of single conversion (SC), once it is completed, the interrupt is generated.

10 SENT Interface

FlexInput implements 4 channels to filter SENT signals and provides them to an external decoder through SENTx_GTMx x=1:4 output pins. The output buffers are push-pull. IO[4:1] inputs are configured as analog input at the power-up. SENTx_GTMx are configured either as SENT or GTM via the SWITCH_ROUTE register. At power up IO15 is routed on SENT4_GTM4 in GTM mode, while the other SENTx_GTMx outputs are kept in HiZ. When a whatever pin of IO[4:1] is configured as SENT through SWITCH_ROUTE register, the corresponding SENTx_GTMx buffer is automatically programmed in SENT mode and an eventual previous configuration as GTM is overwritten.

This function includes a 2-stage filter and the possibility to connect a pull-up input structure.

Externally a matching impedance net is required as reported in Figure 25 and Table 28. The SENT input and filter circuitry fulfil SAE J2716 Rev. 4 standard requirements.

To fulfil SAE J2716 input stage of each IOx x=1:4 is equipped with an internal resistor (RPU) of 20kohm connected to VDD5. The RPU can be independently connected to the IOx via SPI command, through 20kPU_x, x=1:4 bit in GTM_TO_SENT_ROUTE_x_y register.

In case 20kPU_x bit is set, the IOx configuration defined in CURR_SRC_CTRL_x, x=1:4 is reset to the default value: CV[2:0]=000, CV_DW[1:0]=00, SEL[2:0]=000. MODE=0 and CIS[3:0]=0000. The correspondent IO is consequently tight to VDD5 through the internal 20kohm; the current flowing through the IO depends on the external load.

In this configuration, current through the IO is limited both in case of short to ground or short to UBSW.

The modification on 20kPU_x bit set, from ‘1’ to ‘0’, determines the reset at default value of any previous configuration in CURR_SRC_CTRL_x related to the IOx whose 20kPU_x bit was reset.

Digital sampling may be disabled by reg GTM_TO_SENT_ROUTE_1_2 bit[10:11] and GTM_TO_SENT_ROUTE_3_4 bit[10:11]. In this way no digital sampling will effect output signal.

Figure 25. SENT input structure

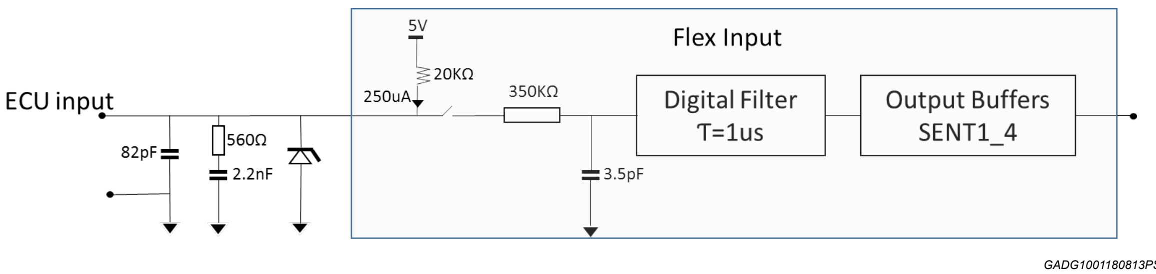


Table 28. SENT interface electrical parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, T_{j-max} = 150 °C unless otherwise specified.							
Stage1tau	First stage time constant	-	0.74	-	1.73	µs	IO1-4
Stage2tau	Second stage time constant	-	0.6	-	1.4	µs	IO1-4
V_{oL}	Output low voltage	I_{load} = |2 mA|	-	-	0.5	V	SENT1-4
V_{oH}	Output high voltage	I_{load} = |2 mA|	VDD5-0.5	-	-	V	SENT1-4
$t_{SENT-rise}$	Output rise time (100 pF load)	From 20% to 80%, design info	9	-	40	ns	SENT1-4
$t_{SENT-fall}$	Output fall time (100 pF load)	From 80% to 20% design info	16	-	30	ns	SENT1-4
t_{dist}	Distorsion time	Difference between delay (IO →SENTx) in the rising and falling edge with fast analog filter	-	-	2.95	µs	SENT1-4

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
jitter HL	Jitter between two consecutive HL SENT_OUT transitions	-	-	-	210	ns	SENT1-4
jitter LH [(1)]	Jitter between two consecutive LH SENT_OUT transitions	-	-	-	210	ns	SENT1-4
RPU	Pull up resistor in SENT mode		10	20	55	kΩ	IO1-4
OPEN_LOAD_drop vs VDD5	VDD5-V(IOx) in OPEN LOAD, SENT mode		0	0.1	0.5	V	IO1-4

1. *For 3µs nominal clock tick including clock accuracy. For higher clock tick times these values can be increased proportionally*

In case one of IO[4:1] is programmed as SENT, the analog input filter time is automatically changed to ADC1tau_1_4_high reported in Table 21. ADC analog constant time.

11 Voltage dividers and internal signals

The device implements different voltage dividers to scale the system voltage rails (UBSW, VI5V, VIX) to a suitable level for the integrated ADC1.

The full range of the ADC1 is 1.25V

In Table 29 the voltage divider ratios parameters are listed. The chosen voltage divider is set simply based on the voltage pin being converted, regardless of the configuration of PUP_DIV[1:0] in SC_CONF or SQNCR_CMDx registers.

Table 29. Voltage dividers and internal signals electrical parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.							
RatioBatt	Voltage divider ratio to ADC1	UBSW input range 40 V 95%FR=39.22+-3.5%	-3.5%	33	+3.5%	V/V	UBSW
RatioIX	Voltage divider ratio to ADC1	VIX input range 25 V 95%FR=24.95 V	-3%	21	+3%	V/V	VIX
RatioT5V	Voltage divider ratio to ADC1	VI5V input range 5 V 95%FR=4.87 V	-3%	4.1	+3%	V/V	VI5V
RatioBG	Voltage divider ratio to ADC1	Bandgap reference ratio Design info	-3%	1.975	+3%	V/V	-
ADC1err_UBSW	ADC1 total measurement error	Including all error contributions (VDD5REF excl.) UBSW input range 42 V (1LSB=10 mV)	-	-	144	LSB	UBSW
ADC1err_VIX	ADC1 total measurement error	Including all error contributions (VDD5REF excl.) VIX input range 27 V (1LSB=7 mV)	-	-	110	LSB	VIX
VIX_range	VIX input range	VIX input range	0.75		25	V	VIX
ADC1err_VI5V	ADC1 total measurement error	Including all error contributions (VDD5REF excl.) VI5V input range 5.15 V (1LSB=1.3 mV)	-	-	80	LSB	VI5V
VI5V_range	VI5V input range	VI5V input range	0.15	-	5	V	VI5V
ADC1err_BG	ADC1 total measurement error	Including all error contributions (VDD5REF excl.) (1LSB=0.3 mV)	-	-	100	LSB	-
RatioX	Voltage divider to VIX and VTX	VIX/VTX ratio	-2%	5.85	+2%	V/V	VIX, VTX
Ratio5V	Voltage divider to VT5V and VT5V	VI5V/VT5V ratio	-1%	1.04	+1%	V/V	VI5V, VT5V
VT5V output	Divider output impedance	-	-50%	48k	+50%	Ω	VT5V
VTX output	Divider output impedance	-	-45%	58k	+45%	Ω	VTX
VI5V input	Divider input impedance	-	-50%	97k	+50%	Ω	VI5V
VIX input	Divider input impedance	-	-45%	135k	+45%	Ω	VIX
V therm	Thermal sensor voltage	Design info (-40 °C)	-	0.5	-	V	-
V therm	Thermal sensor voltage	Design info (27 °C)	-	0.65	-	V	-
V therm	Thermal sensor voltage	Design info (150 °C)	-	0.89	-	V	-

To save power consumption, the voltage dividers are switched off when the device enters SLEEP or RST_ACTIVE mode.

When the conversion is requested on UBSW, VI5V, VIX or VBG the proper voltage divider is automatically applied. In case the internal bandgap voltage reference is to be converted, no voltage divider is used.

12 Voltage comparators

The device allows the programming of configurable thresholds for the voltage comparators.

There are two types of comparators, one absolute with 3 selectable thresholds and one ratiometric to VPRE. The status of the comparators selected (CTR[1:0] in CURR_SRC_CTRL_x register) for each IOx is either available on DIG_IN_STAT register or SENTx_GTMx digital outputs, if properly routed.

A particular focus has to be put on digital IO[13:15]: UTh1 and UTh3 selection inserts on IOx a resistance path towards GND which causes a voltage partitioning during ADC voltage measurements or in case of pull up current set with CV[2:0]=000. UTh2 and UTh_ratio do not affect performances on digital IOx.

12.1 Absolute comparators

The absolute comparators can be programmed, for each IOx, with three thresholds, reported in Table 30.

Table 30. Absolute comparators threshold values

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, T_{j-max} = 150 °C unless otherwise specified.							
Vth1_L2H	Voltage comparator threshold 1(absolute)	-	-	3.15	3.5	V	IO1-15
Vth1_H2L	Voltage comparator threshold 1(absolute)	-	2.2	2.64	-	V	IO1-15
Vth2_L2H	Voltage comparator threshold 2(absolute)	-	-	1.864	2.2	V	IO1-15
Vth2_H2L	Voltage comparator threshold 2(absolute)	-	0.8	1.162	-	V	IO1-15
Vth3_L2H	Voltage comparator threshold 3 (absolute)	-	-	5.33	6.0	V	IO1-15
Vth3_H2L	Voltage comparator threshold 3 (absolute)	-	3.5	4.62	-	V	IO1-15
Vhys	Vth1, Vth2, Vth3 voltage comparator hysteresis	-	0.39	0.64	1.0	V	IO1-15

The threshold for each IOx is defined through CTR[1:0] of CURR_SRC_CTRL_x register

12.2 Ratiometric comparator

There is only one ratiometric comparator continuously sweeping all the IOx, regardless of their configuration. For the IOx with UTh_ratio selected (CTR[1:0] in CURR_SRC_CTRL_x register), the status of the comparator itself is either available on DIG_IN_STAT register or SENTx_GTMx digital outputs, if properly routed

Table 31. Ratiometric comparator parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, T_{j-max} = 150 °C unless otherwise specified.							
Vth4H	Voltage comparator threshold 4 (ratiometric to VPRE) VPRE is load affected	-	VPRE(min)*66%-0.11	VPRE*66%	VPRE(max)*80%	V	IO1-15
Vth4L	Voltage comparator threshold 4 (ratiometric to VPRE) VPRE is load affected	-	VPRE(min)*33%-0.11	VPRE*33%	-	V	IO1-15
T_sw	Switching time among two consecutive IOx	-	-9%	40	+9%	µs	IOx-IOx+1
T_cycle	One cycle sweep time	-	-9%	600	+9%	µs	IO1-15

The ratio comparator sweeps between all IOx; it takes T_sw time to move between two consecutive channels, for a total sweeping time of T_cycle, see Table 31.

Although ratiometric comparator sweeps through all channels, only the channels which have been selected for UTh_ratio are connected to it through the analog multiplexer.

13 SPI interface

For SPI communication an in-frame protocol is used. This means the complete SPI transmission is finished within one CS low phase. The requested data is transmitted to the master in the same SPI frame. Furthermore, the SPI interface offers a burst feature for read and write commands.

The SPI interface is designed to work up to a clock frequency (SCLK) of 10 MHz

13.1 SPI interface characteristics

1. During active reset conditions the SPI is driven into its default state. When reset becomes inactive, the state machine enters into a wait state for the next instruction. During active reset conditions the output MISO is high impedance (HiZ).
2. If the signal at CS is inactive (high), the state machine is forced to enter the wait state waiting for instructions. CS is kept inactive when RST is active low.
3. During active (low) state of the CS, the falling edge of the serial clock signal SCLK is used to latch the input data at MOSI (this corresponds to MCU SPI peripheral configuration CPOL=0; CPHA=1). Output data at MISO is driven with the rising edge of SCLK. Further processing of the data according to the instruction (i.e. modification of internal registers) is triggered by the rising edge of the CS signal.
4. Chip address: In order to support two L9966 working on a fully shared SPI bus, each frame has to contain the chip address, reported on the two MSB of each instruction byte. To avoid a bus conflict the output MISO remains at HiZ during the addressing phase of the frame: if the chip address does not match, the frame is ignored and MISO remains HiZ, even in case the instruction bit should match a valid instruction. A frame with not matching chip address is ignored and does not generate any Transfer Failure Message.
5. Check byte: Simultaneously to the receipt of an SPI instruction the FlexInput transmits a check byte via the output MISO to the controller. This byte indicates regular or irregular operation of the SPI. It contains an initial fixed bit pattern and a flag indicating an eventual invalid instruction of the previous access.
6. On a read access the data bit at the SPI input MOSI are rejected/ignored, but parity check is always performed.
7. Invalid access. An access is invalid, if one of the following conditions are fulfilled:
   - An unused/invalid instruction code is detected. An instruction code is not valid when its address doesn’t exist.
   - In case the previous transmission was not completed (CS went inactive too early)
   - The parity bit of either MOSI instruction (PAR_MOSI_INST) or MOSI data (PAR_MOSI_DATA) frame is wrong.

   If an invalid instruction is detected, no modifications on registers of the FlexInput will be performed. In case an unused instruction code occurred, the expected answer is collected with PAR_MISO_DATA = ‘1’ and all data bit at 1; the resulting word, transmitted after having sent the check byte, is then 0xFFFF.
8. In order to guarantee SPI proper operation, CS signal must remain de-asserted for at least $t_{SPICS\text{-}high}$ in between two consecutive SPI accesses. During this time, the eventual SPI configuration/command becomes effective and the L9966 gets ready for a new SPI exchange.

A write access is internally suppressed (i.e. internal registers will not be affected) in all cases where the number of falling edges of SCLK applied to the SPI input is not equal to 32 at the rising (inactive) edge of CS (respectively 16*(m+1) clock pulses in burst mode, where m indicates the burst packets sent).

For each of the invalid access types reported above, a Transfer Failure bit (TRANS_F) is set and can be read on MISO at next SPI transaction. On top of all the cases reported above, de-assertion of RST with CS asserted (low) determines the setting of TRANS_F bit in first SPI frame.

In Figure 26. Write access (32 bits frame) and Figure 27. Read access (32 bits frame) are reported SPI frame examples:

Figure 26. **Write access (32 bits frame)**

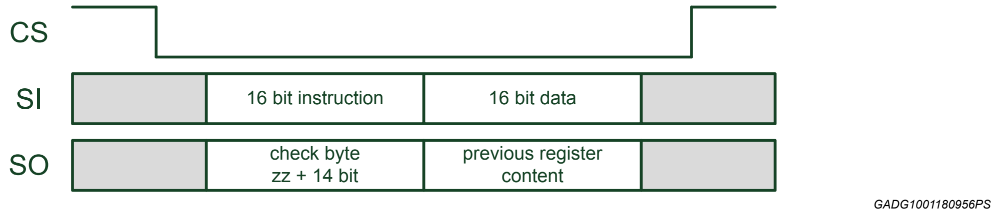
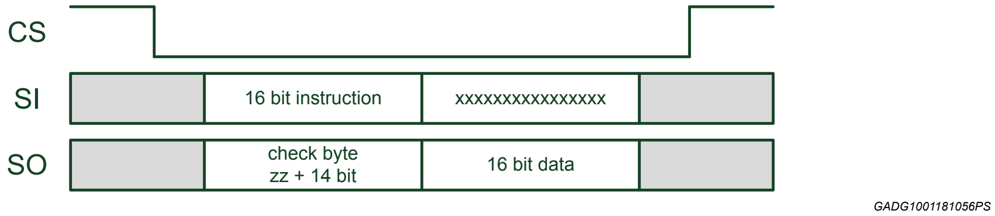


Figure 27. **Read access (32 bits frame)**



13.2 Address multiplexing

The chip features hardware configurable address multiplexing which allows 2 ICs sharing all the SPI bus, CS line included.

The first two bits of the SPI frame are used to address the chip. The MSB is always '1' while the second address bit depends on the level of the CTRL_CFG pin, latched during the transition from WAKE to INIT at power up, see Table 32. CTRL_CFG hardware address.

In case of open, the CTRL_CFG pin is internally pulled up, see Table 33. CTRL_CFG electrical parameters.

Table 32. **CTRL_CFG hardware address**

Bit 31	Bit 30	Chip address
1	0 (CTRL_CFG pin low)	10
1	1 (CTRL_CFG pin high)	11

The chip does not shift out any bit on MISO line unless the correct address is decoded.

Table 33. **CTRL_CFG electrical parameters**

Symbol	parameter	condition	Min	Typ	Max	Unit
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.						
VinH	CTRL_CFG input voltage levels	-	-	-	2	V
VinL	CTRL_CFG input voltage levels	-	0.8	-	-	V
Vhys	CTRL_CFG input voltage hysteresis	-	0.15	-	0.5	V
CTRL_CFG_pu	CTRL_CFG pull up to 3V3	-	50	100	150	kΩ

13.3 SPI mode

L9966 SPI is implemented as per the following: CPHA = 1 / CPOL = 0

Communication starts with a falling edge on CS; during this phase the SCLK line must be low.

With the following rising edges of SCLK line the MISO data is shifted out from the internal shift register while the MOSI data is latched in on the following falling edges.

13.4 Frame definition

The FlexInput chip implements a 32 bits in-frame SPI protocol, see the following tables.

Table 34. Complete 32 bits frame

<table>
<tr><th rowspan="2"></th><th colspan="16">Instruction</th><th colspan="16">Data</th></tr>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>MOSI</td><td>1</td><td>CTRL_CFG</td><td>R/W</td><td>CLK_MON</td><td colspan="8">Register Address</td><td>X</td><td>X</td><td>X</td><td>PAR_MOSI_INSTR</td><td>PAR_MOSI_DATA</td><td colspan="15">write data or ignored if R/W=0</td></tr>
<tr><td rowspan="2">MISO</td><td rowspan="2">Z</td><td rowspan="2">Z</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">TRANSF_F</td><td colspan="8" rowspan="2">Register Address (blind echo)</td><td>PAR_MISO_DATA</td><td colspan="15">read data or previous content of register in case of write</td></tr>
<tr><td colspan="16">0xFFFF in case of wrong instruction code</td></tr>
</table>

Table 35. 16 bits instruction word

	Instruction															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOSI	1	CTRL_CFG	R/W	CLK_MON	Register Address								X	X	X	PAR_MOSI_INSTR
MISO	Z	Z	1	0	1	0	1	TRANS_F	Register Address (blind echo)							

Table 36. **16 bits data word**

	Data															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	PAR_MOSI_DATA	write data or ignored if R/W=0														
MISO	PAR_MISO_DATA	read data or previous content of register in case of write														
	0xFFFF in case of wrong instruction code															

Table 37. **MOSI bit**

Bit	Function/Meaning
[31:30]	Chip Address Either “10” or “11” (depending on CTRL_CFG level during reset)
[29]	Read/Write command 0: read 1: write
[28]	Clock monitoring 0: off (burst mode) • Data will be written to a register after a complete reception of 16 CLK cycles. Only the last frame will be discarded if the number of CLK cycles is different from 16*(m+1) 1: on (one frame transferred) • Data will be written to a register only when 32 CLKs have been detected. Frame will be otherwise discarded.
[27:20]	Register address[7:0]
[19:17]	Don’t care
[16]	PAR_MOSI_INST Odd parity bit of instruction computed over bit[31:16]
[15]	PAR_MOSI_DATA Odd parity bit of instruction computed over bit[15:0]
[14:0]	Write data / ignored if bit[29] = 0

Table 38. **MISO bit**

Bit	Function/Meaning
[31:30]	HiZ
[29:25]	Fixed bit pattern (10101)
[24]	Transfer Failure Message TRANS_F = 0: previous transfer was recognized as valid

Bit	Function/Meaning
	TRANS_F = 1: previous transfer was recognized as not valid (only if chip address is recognized)
[23:16]	Blind address echo
[15]	PAR_MISO_DATA Odd parity bit of data computed over [15:0] ‘1’ in case of wrong instruction code detected
[14:0]	read data or previous content of register in case of write access '7FFFhex' in case of wrong instruction code detected

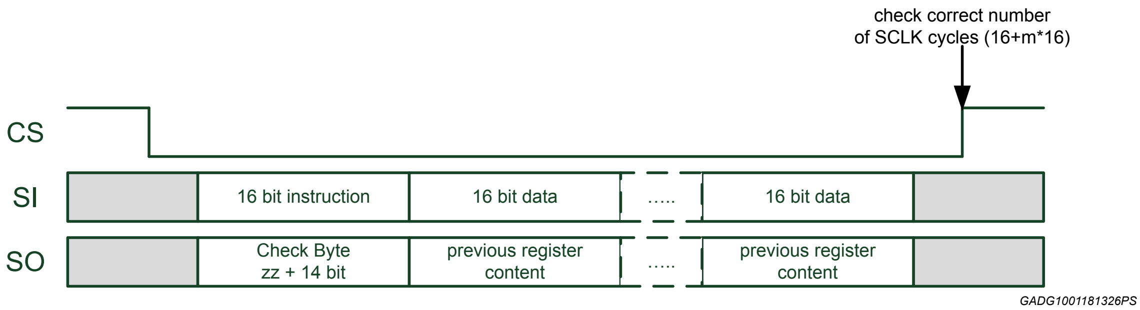
13.5 Burst mode

The burst mode has the advantage to transfer more data in less time: only one 16 bits instruction has to be sent during the transfer. As long as the CS is low and a clock is provided, data can be transferred. The burst mode can be used for both write and read access of registers.

A write access in burst mode (bit[29]=1, see Figure 28. Write burst mode frames) consists of:

- first 16 bits instruction on MOSI line
- following m*16 bits data to be written in the consecutively addressed registers on MOSI line
- first check byte + TRANS_F + blind echo of register address on MISO line
- following m*16 bits previous register content on MISO line

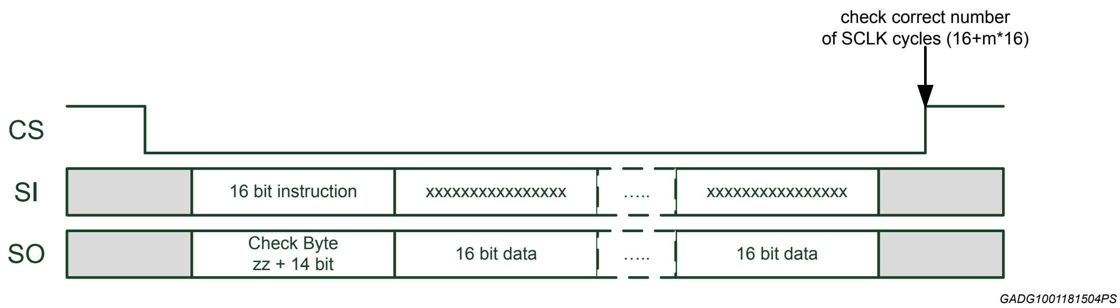
Figure 28. **Write burst mode frames**



A read access in burst mode (bit[29]=0, see Figure 29. Read burst mode frames) consists of:

- first 16-bit instruction on MOSI line
- following m*16 bit don’t care on MOSI line
- first check byte + TRANS_F + blind echo of register address on MISO line
- m*16 bit data corresponding to the content of consecutively addressed registers on MISO line

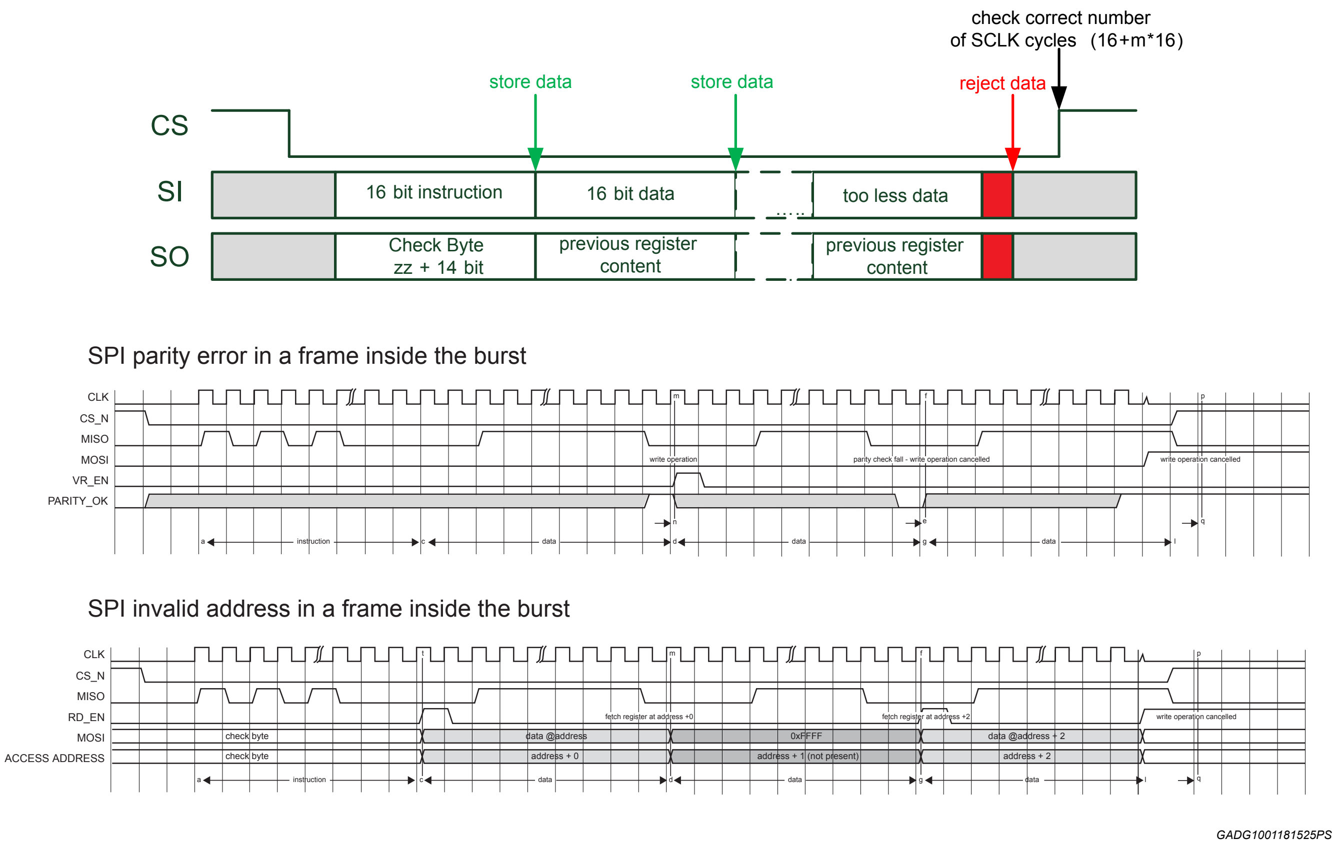
Figure 29. **Read burst mode frames**



In the 16-bit instruction a “start” register address is present. As long as the CS signal keeps low and the SCLK is running, 16-bit data is either sampled on MOSI line (write access) or shifted out on MISO line (read access). The next register gets selected automatically after each 16 clock cycles on SCLK. In case of write access after each complete 16 SCLK cycles the data is written into the register, no input buffer present.

A correct SCLK cycles number check is done after CS rising: the SCLK count must be a multiple of 16*(m+1) where m is the number of frames transferred during the burst mode. During burst, each valid 16-bit word is considered as data and latched inside the addressed register: eventually, if the last bits sent on SPI bus don't belong to a packet of 16 bits, these are discarded, see Figure 30. Burst mode error handling. In case of a parity error within one of the 16 SCLK transmissions, the following part of the burst will be completely rejected, including the wrong frame. These two errors (too many bits or parity errors) set the TRANS_F bit at the next SPI transfer.

Figure 30. Burst mode error handling



When the instruction is initialized with an invalid address, the whole SPI access is invalidated and TRANS_F flag bit is set at the next SPI transfer.

As it is shown in the picture, it is allowed to perform a SPI burst operation with incremental address going through an invalid address. Operation on not existing register is discarded.

Note: When burst mode is not active (SPI CLK_MON=1), a write SPI access composed by 16 bit valid instruction word + 16(1+2k) valid data word (k > 0) does not flag TRANS_F bit. The frame is recognized as valid and a command composed by the first 16 instruction bit + the last 16 data bit is issued.*

13.6 SPI parameters

Figure 31. SPI timing

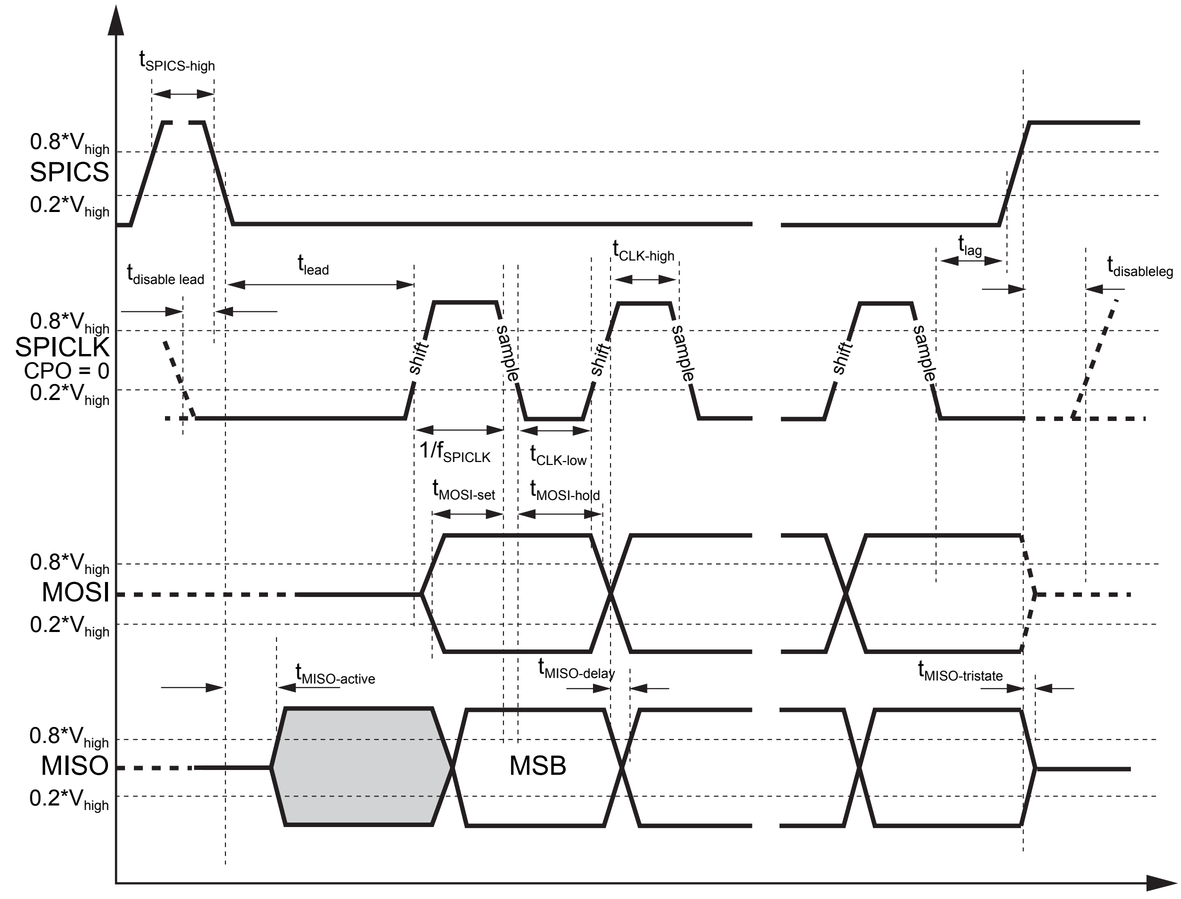


Table 39. SPI electrical parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.							
CS_hi	CS input logic high voltage	-	1.75	-	-	V	CS
CS_lo	CS input logic low voltage	-	-	-	0.75	V	CS
CS_hys	CS input voltage hyst	-	0.2	-	0.5	V	CS
CS_pu	CS pull up to 3V3	-	50	100	150	kΩ	CS
SCLK_hi	SCLK input logic high voltage		1.75	-	-	V	SCLK
SCLK_lo	SCLK input logic low voltage	-	-	-	0.75	V	SCLK
SCLK_hys	SCLK input voltage hyst	-	0.2	-	0.5	V	SCLK
SCLK_pd	SCLK pull down to GND	-	50	100	150	kΩ	SCLK
MOSI_hi	MOSI input logic high voltage	-	1.6	-	2.3	V	MOSI
MOSI_lo	MOSI input logic low voltage	-	1.2	-	1.9	V	MOSI
MOSI_hys	MOSI input voltage hyst	-	0.2	-	0.6	V	MOSI
MOSI_pd	MOSI pull down to GND	-	50	100	150	kΩ	MOSI

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
MISO_Voh	MISO Output high voltage level	I_{load} = |2 mA|	VDD5-0.5	-	-	V	MISO
MISO_Vol	MISO Output low voltage level	I_{load} = |2 mA|	-	-	0.5	V	MISO
f_{SPICLK}	SCLK frequency	-	-	10	-	MHz	-
$t_{CLK\text{-}high/low}$	SCLK high/low time	-	45	-	-	ns	-
t_{lead}	CS to SCLK delay	-	180	-	-	ns	-
t_{lag}	SCLK to CS delay	-	45	-	-	ns	-
$t_{disablelead}$	SCLK disable lead time	-	10	-	-	ns	-
$t_{disablelag}$	SCLK disable lag time	-	10	-	-	ns	-
$t_{MOSI\text{-}set}$	MOSI to SCLK delay	-	10	-	-	ns	-
$t_{MOSI\text{-}hold}$	SCLK to MOSI delay	-	10	-	-	ns	-
$t_{MISO\text{-}delay}$	SCLK to MISO delay, $C_L \leq 90$ pF	-	-	-	30	ns	-
$t_{MISO\text{-}delay}$	SCLK to MISO delay, $C_L = 25$ pF (Design info)	-	-	-	20	ns	-
$t_{MISO\text{-}delay}$	SCLK to MISO delay, $C_L = 200$ pF (Design info)	-	-	-	75	ns	-
$t_{MISO\text{-}active}$	CS to MISO active delay, $C_L \leq 90$ pF	-	-	-	30	ns	-
$t_{MISO\text{-}valid}$	CS to MISO valid delay, $C_L \leq 90$ pF	-	-	-	40	ns	-
$t_{MISO\text{-}tristate}$	CS to MISO tristate delay, $C_L \leq 90$ pF	-	-	-	30	ns	-
$t_{SPICS\text{-}high}$	CS high time	-	400	-	-	ns	-
$I_{MISO\_tristate}$	MISO leakage current	-	-10		10	µA	-
V_{inH}	CS, MOSI, SCLK input voltage levels and hysteresis (1)	-	-	-	2	V	-
V_{inL}	CS, MOSI, SCLK input voltage (1)	-	0.8	-	-	V	-

1. *SPI input pin capacitance < 10 pF.*

13.7 SPI chip ID

The SPI Chip ID is ‘5A’ hex to identify L9966 via SPI data in DEV_ID register; in order to track device revision, other two registers are available:

- HW_REV register: tracks major silicon revisions starting from rev A = 1, rev B = 2, rev C = 3 and so on.
- DEV_V register: tracks minor silicon (as localized metal fixing) revisions starting from rev AA = 1, rev AB = 2, rev AC = 3 and so on.

14 Output

14.1 Analog output AOX

AOX buffer is a rail to rail buffer capable of outputting the analog IO[12:1] voltage to AOX output pin through an internal analog multiplexer. The channel being fed to the AOX output is selected by RAOX[3:0] bit on the SWITCH_ROUTE register. The default state of the AOX is HiZ with no connection to any IO channel.

Table 40. AOX electrical parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.							
V_{outH}	Output high level	Input 0 V to 5 V I_{load} |200 µA|	VDD5-0.1	-	-	V	AOX
V_{outL}	Output low level	Input 0 V to 5V I_{load} |200 µA|	-	-	0.1	V	AOX
AOXerr	AOX input/output offset error	Input voltage range 0.04 V – (VDD5-20 mV), outside this range offset is 13 mV (1)	-5	-	+5	mV	AOX

1. Guaranteed by design.

AOX pin output voltage follows the input voltage with AOXerr offset in range defined in Table 40. AOX electrical parameters.

The AOX pin is designed to drive an RC low pass filter with 10 kΩ min resistor followed by a capacitor towards ground.

Bandwidth is limited by FlexInput analog IO input filter time constant ADC1tau_1_12 (see Table 21. ADC analog constant time).

In addition to the analog IO[12:1] the following internal voltages can be routed on AOX for ASIC functionality monitoring: internal Band Gap, ADCx reference voltage, VRSP, see Table 41. Signal routed on AOX.

Table 41. Signal routed on AOX

Symbol	Parameter	Condition	Min	Typ	Max	Unit
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.						
VBG_INT	Internal band gap	Design info	-5%	1.24	5%	V
VREF	ADCx reference voltage	Design info 5V_REF = 5 V	-1%	1.25	1%	V
VRSP	VRSP voltage gain	RAOX[3:0] = 0xF	-2%	1	2%	V/V

14.2 Digital outputs SENTx_GTMx

SENTx_GTMx buffers can be configured for digital signal routing; in such a case the buffers can be configured as output for digital signal routing. In such case the state of the comparators properly programmed for each IOx will set the output state..

Digital routing to SENTx_GTMx buffer is configured through GTM_TO_SENT_ROUTE_1_2 and GTM_TO_SENT_ROUTE_3_4 registers. By default, SENT4_GTM4 is connected to IO15, while the remaining buffers are in HiZ.

Once an Input channel is routed on SENTx_GTMx, the output depends on the thresholds selected for that specific IOx, either absolute or ratiometric.

In case of ratiometric comparator selected for one or more IOx, the ratiometric comparator sweeps between all IOx with a total sweeping time of T_cycle, see Section 12.2 Ratiometric comparator; the IOx digital conversion is updated every T_cycle time.

In case of absolute comparators, each IOx has a dedicated absolute comparator, the IOx digital conversion is immediately updated.

In both cases SENTx_GTMx is the result of the IOx comparison with the threshold selected, that in turn is reported for each IO in DIG_IN_STAT register, as described in Section 12 Voltage comparators.

When SENTx_GTMx is not assigned to any channel (SENTx_GTM_ROUTE_x=0), the output pin is in HiZ.

Table 42. SENTx_GTMx electrical parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.							
SENToutH	Output high level	I_{load} = |2 mA|	VDD5-0.5	-	-	V	SENTx/GTMx
SENToutL	Output low level	I_{load} = |2 mA|	-		0.5	V	SENTx/GTMx
SENTout_HiZ	Tri-state impedance		-	>1M	-	Ω	SENTx/GTMx
Delay time HL	Delay time rising edge (covered by filter time test)	IOx as per default config; IOx routed on GTMy	-	-	10	µs	SENTx/GTMx
Delay time LH	Delay time falling edge (covered by filter time test)	IOx as per default config; IOx routed on GTMy	-	-	10	µs	SENTx/GTMx

In case one or more IO[4:1] are configured as SENT, output of signal processing chains are automatically routed on SENTx_GTMx regardless of any possible existing configuration in GTM_TO_SENT_ROUTE_1_2 or GTM_TO_SENT_ROUTE_3_4.

In case of IO1:4, it is possible to:

- select the fast or slow filter through AN_FIL_x in GTM_TO_SENT_ROUTE_x_y register
- Insert or not the 1 µs digital filter through DIG_FIL_x in SWITCH_ROUTE register
- route the absolute comparator output directly on SENTx_GTMx through DIG_BP_x in GTM_TO_SENT_ROUTE_x_y register, in this case no digital sampling is performed.

14.3 INT output

The INT output pin is used to generate an interrupt in order to flag the end of single conversion or the end of command list programmed for both EU1 and EU2 (NEXT_PC either reached END LOOP or INT_EUx_CONF[3:0]). INT flag is managed through SQNCR_INT_MSK_FLG register: it is possible to selectively enable / disable the toggle on INT pin while the flag generation is never inhibited.

Output Type: Push-pull, see Table 43. INT electrical parameters.

Table 43. INT electrical parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.							
INToutH	Output high level	I_{load} = |2 mA|	VDD5-0.5	-	-	V	INT
INToutL	Output low level	I_{load} = |2 mA|	-	-	0.5	V	INT
INTtoggle	INT toggle time	-	-9%	16	+9%	µs	INT

14.4 WAKE output

The WAKE output pin and WAK_UP_FLG are set high at the end of Power up cycle, as showed in Figure 5. Operating mode state diagram.

Both WAKE output and WAK_UP_FLG go back to zero by reading the GEN_STATUS register.

Moreover, it is used also in polling mode. If a WAKE event is detected in polling, both WAKE pin and WAK_UP_FLG bit are asserted.

WAKE output stage is supplied from VPRE. WAKE output is tolerant against short to battery. The pin has an internal passive pull-down structure to prevent any floating condition in case no external pull-down is mounted.

Type: pull up open drain, see Table 44. WAKE electrical parameters.

Table 44. WAKE electrical parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.							
WAKEoutH	Output high level	I_{load} = |2 mA|	VPRE-1.3	-	-	V	WAKE
WAKERPD	Passive pull-down	-	300k	-	800k	Ω	WAKE

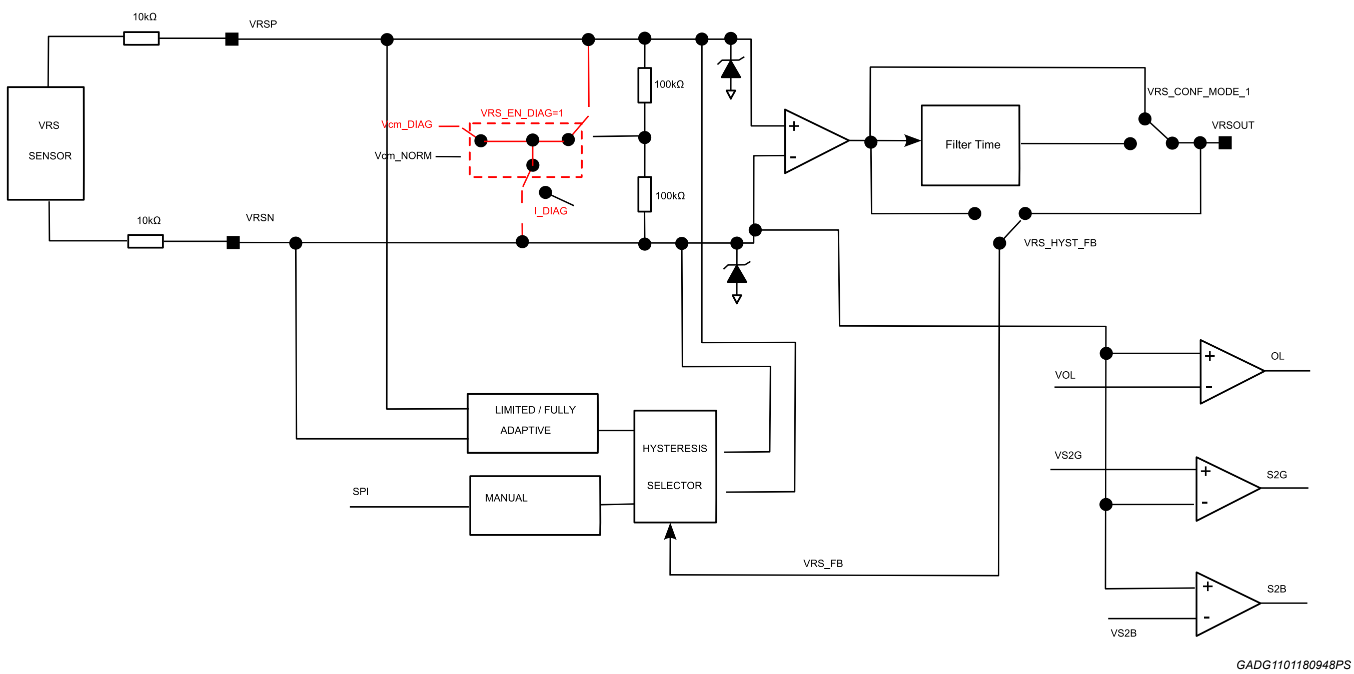
15 Inductive sensor interface

The interface handles signals coming from inductive sensors or Hall Effect sensors. The interface feeds the digital signal to microcontroller that extracts flying wheel rotational position, angular speed and acceleration.

15.1 VRS interface

VRS interface runs either in normal mode to convert the input differential voltage or in diagnostic mode to detect eventual short to ground, short to battery or open condition at sensor pins. In order to guarantee a better coverage, VRSP pin can be routed on AOX pin. Figure 32. VRS interface block diagram shows the main parts inside VRS block and, in red, the internal connection in case of active diagnostic mode.

Figure 32. **VRS interface block diagram**



Operating mode is defined in VRS register through VRS_EN_DIAG bit: when VRS_EN_DIAG=0, VRS block is set in normal mode; when VRS_EN_DIAG=1 the VRS diagnosis mode is activated.

VRSP or VRSN pins are equipped with a clamp at V_{clampH} and V_{clampL}.

In case of activation of clamp both on VRSP and VRSN, it is guaranteed by design that VRSP voltage is higher than VRSN.

Table 45. **VRS electrical parameters**

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, T_{j-max} = 150 °C unless otherwise specified.							
VCM_norm	Input common mode voltage level	Open load	1	1.6	2.2	V	VRSP/VRSN
V_{clampH}	Input signal high clamping voltage NORMAL state	NORMAL state, max input current 20 mA	3.1	3.3	3.5	V	VRSP/VRSN
V_{clampH_OFF}	Input signal high clamping voltage OFF condition	OFF condition	-	-	3	V	VRSP/VRSN
V_{clampL}	Input signal low clamping voltage	Max input current 20 mA	-1.5	-0.6	-0.3	V	VRSP/VRSN

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
V_{clampL_OFF}	Input signal low clamping voltage OFF condition	Max input current 20 mA	-1.5	-0.6	-0.3	V	VRSP/VRSN
Rin CM	Input impedance	Equivalent resistance between VRSP/N and Vcm_NORM (1)	60	100	140	kΩ	VRSP/VRSN
IBVRS	Input leakage current	VRSP/N = Vcm_NORM otherwise Rin_CM is measured	-	-	1	µA	VRSP/VRSN
V_{oh}	Output high voltage level	I_{load} = |2 mA|	VDD5-0.5	-	-	V	VRS_OUT
V_{ol}	Output low voltage level	I_{load} = |2 mA|	-	-	0.5	V	VRS_OUT
Tdfalling	Delay between zero crossing of the voltage differential VRSP and VRSN to VRS_out	VRS_CONF_MODE[1]='0' (no Filter Time inserted)	-	-	1	µs	VRS_OUT
Tdrising	Delay between zero crossing of the voltage differential VRSP and VRSN to VRS_out	Vdiff period = 4ms VRS_CONF_MODE[1]=1 and VRS_SEL=1 (fully adaptive filter selected)	-	-	150	µs	VRS_OUT
VCM_diag	Diagnosis VRSP voltage	VRSP open, diag mode	0.9	1.1	1.3	V	VRSP
Idiag	Diagnosis current	VRSP open, VRSN short to GND, diag mode	45	60	75	µA	VRSP/VRSN
VOL	Open load threshold	Diag mode	2.65	2.80	3.0	V	VRSP/VRSN
VS2G	Short to ground threshold	Diag mode	1.15	1.25	1.35	V	VRSP/VRSN
VS2B	Short to battery threshold	Diag mode (=VclampH)	3.1	3.3	3.5	V	VRSP/VRSN

1. Guaranteed by design.

15.2 VRS - Normal mode

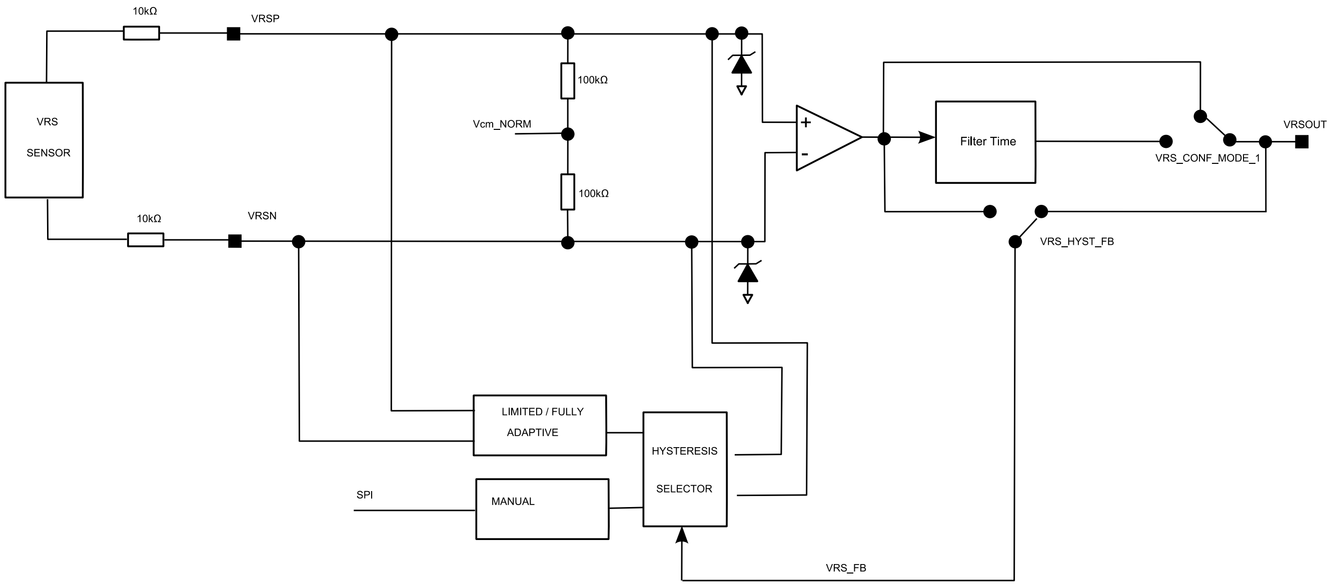
The VRS normal mode is set with VRS_EN_DIAG=0.

In Normal mode, the circuit can be configured as the one reported in Figure 33. VRS block diagram - Normal operating mode. It allows decoding the VRS signal while flying wheel is in rotation.

Due to high variability of the input signal (±200 V), the input is clamped in the range [VclampH:VclampL] if the IC is supplied or to VCLAMPH_OFF if the IC is not supplied; current through VRSP and VRSN is limited by external resistor on each pin in order to allow the analog circuitry processing the signal itself. Moreover, the sensor input pins have an input common mode, VCM_norm.

The preconditioned input signal is then processed by a zero-crossing comparator, which toggles at each transition of the input signal.

Figure 33. **VRS block diagram - Normal operating mode**



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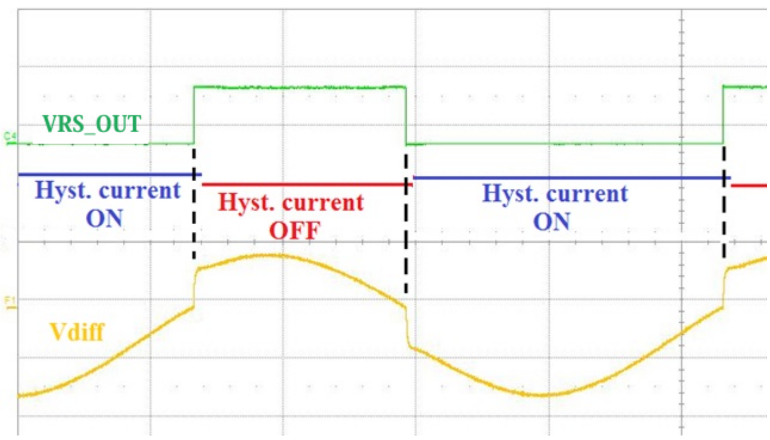
To avoid spurious commutations of the zero crossing comparator, a hysteresis mechanism is implemented. L9966 is able to sink a hysteresis current which generates a voltage drop across the external resistors. The voltage levels related to the hysteresis function shown hereafter are calculated considering an external series resistance of 10kΩ on VRSP and 10kΩ on VRSN pins.

As reported in Figure 34. Hysteresis application, the Vdiff (VRSP-VRSN) input differential signal exhibits some steps at each zero crossing:

- when the output of the zero crossing comparator is high, the hysteresis current is kept OFF;
- when the output of the zero crossing comparator is low, the hysteresis current is switched ON.

This approach applies the hysteresis current only on the transition HL of the VRS_OUT signal.

Figure 34. **Hysteresis application**



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The output of the zero crossing comparator can be further processed by a filtering circuit or directly routed to VRS_OUT.

15.2.1 VRS normal mode configurations

L9966 integrates two main configurable architectures: VRS_A and VRS_B. These architectures are selected in VRS register, VRS_SEL bit.

Once VRS_A (VRS_SEL=1) or VRS_B (VRS_SEL=0) has been configured, hysteresis and filtering strategy are defined through VRS_CONF_MODE[1:0] bit in the same VRS register:

- VRS_CONF_MODE[1] defines filtering function (OFF/ON and if ON, its time value)
- VRS_CONF_MODE[0] defines the hysteresis (manual or adaptive)

The next two tables summarize the parameters of VRS_A and VRS_B architecture; the two configurations are:

- In VRS_B limited adaptive and SPI configuration, it is possible to force the default hysteresis value (HI1) by setting MIN_HYST_FORCE bit in VRS register.
- In VRS_A fully adaptive and SPI configuration, it is possible to force the default hysteresis value (HI3) by setting MIN_HYST_FORCE bit in VRS register.

Entering in normal mode, in order to properly initialize the VRS block, it is recommended to have the first VRS_OUT toggles with low HIx value – manual mode (default condition) and then configure VRS block itself.

Table 46. VRS_A hysteresis and filter time definition

VRS_SEL (A config.)	VRS_CONF_ MODE[1:0]	Filter		Hyst		MIN_HYST_FORCE
1	00	OFF	0 µs	Manual	Ref to VRS_A – Manual Hysteresis	Active
1	01	OFF	0 µs	Full adaptive	Ref. to VRS_A – Fully Adaptive Hysteresis	Active
1	10	ON	T(n-1)/32	Manual	Ref to VRS_A – Manual Hysteresis	Active
1	11	ON	T(n-1)/32	Full adaptive	Ref. to VRS_A – Fully Adaptive Hysteresis	Active

Table 47. VRS_B hysteresis and filter time definition

VRS_SEL (B config.)	VRS_CONF_ MODE[1:0]	Filter		Hyst		MIN_HYST_FORCE
0	00	OFF	0 µs	Manual	Ref. to VRS_B – Manual Hysteresis	Active
0	01	OFF	0 µs	Limited adaptive	Ref. to VRS_B –Limited Adaptive Hysteresis	Active
0	10	ON	2.5 µs	Manual	Ref. to VRS_B – Manual Hysteresis	Active
0	11	ON	2.5 µs	Limited adaptive	Ref. to VRS_B –Limited Adaptive Hysteresis	Active

In case a change of VRS_SEL bit within the normal operating mode occurs (1->0 or 0->1) with hysteresis current active, this leads to the change of the hysteresis not synchronized with any VRS_OUT zero crossing.

15.2.2 VRS_A – Manual Hysteresis

To set the manual hysteresis on VRS_A configuration, bit VRS_CONF_MODE[0] has to be configured at ‘0’. Hysteresis value is manually set through VRS_HYST_CONF[2:0] of VRS register according to Table 48. VRS_A hysteresis value. Such hysteresis is fixed until a new SPI programming occurs.

Default hysteresis current after exiting reset is HI3.

New SPI current value is updated during HYST CURRENT OFF phase that means the output comparator is high.

The following hysteresis value ranges include also the error given by the temperature behavior of the leakage currents on the input pins.

Table 48. **VRS_A hysteresis value**

Hysteresis current [HI]	Value			Unit	Correspondent value on 20 kΩ ext. resistor	Unit
	Min	Typ	Max			
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.						
HI1	4.5	6	7.5	µA	120	mV
HI2	9.5	11.5	13.5	µA	230	mV
HI3	16.5	20	23.5	µA	400	mV
HI4	42	52.5	63	µA	1050	mV
HI5	64	80	97	µA	1600	mV
No Hyst	-	-	-	-	-	-

15.2.3 VRS_A – Fully adaptive hysteresis

To set the adaptive hysteresis on VRS_A configuration, bit VRS_CONF_MODE[0] has to be set to ‘1’. In this configuration, VRS input differential signal is fed into a peak detector circuit and then quantized on 5 different voltage levels, based on 4 PVi thresholds (see Table 49. Peak voltage value ranges). Default hysteresis current after exiting reset is HI3.

Table 49. **Peak voltage value ranges**

Peak Voltage [PVi]	Min	Typ	Max	Unit
UBSW = 7.5 V:36 V, VDD5V = 4.85 V:5.15 V, $T_{j\text{-}max}$ = 150 °C unless otherwise specified.				
PV1	650	900	1100	mV
PV2	1200	1500	1650	mV
PV3	1800	2100	2350	mV
PV4	2450	2800	3050	mV

The quantized output is sent to a logic block (Hysteresis Selection Table) that chooses the proper hysteresis value (HIi) depending on the input peak voltage (PVi), see Table 50. Peak voltage range correspondence with hysteresis selection.

Table 50. **Peak voltage range correspondence with hysteresis selection**

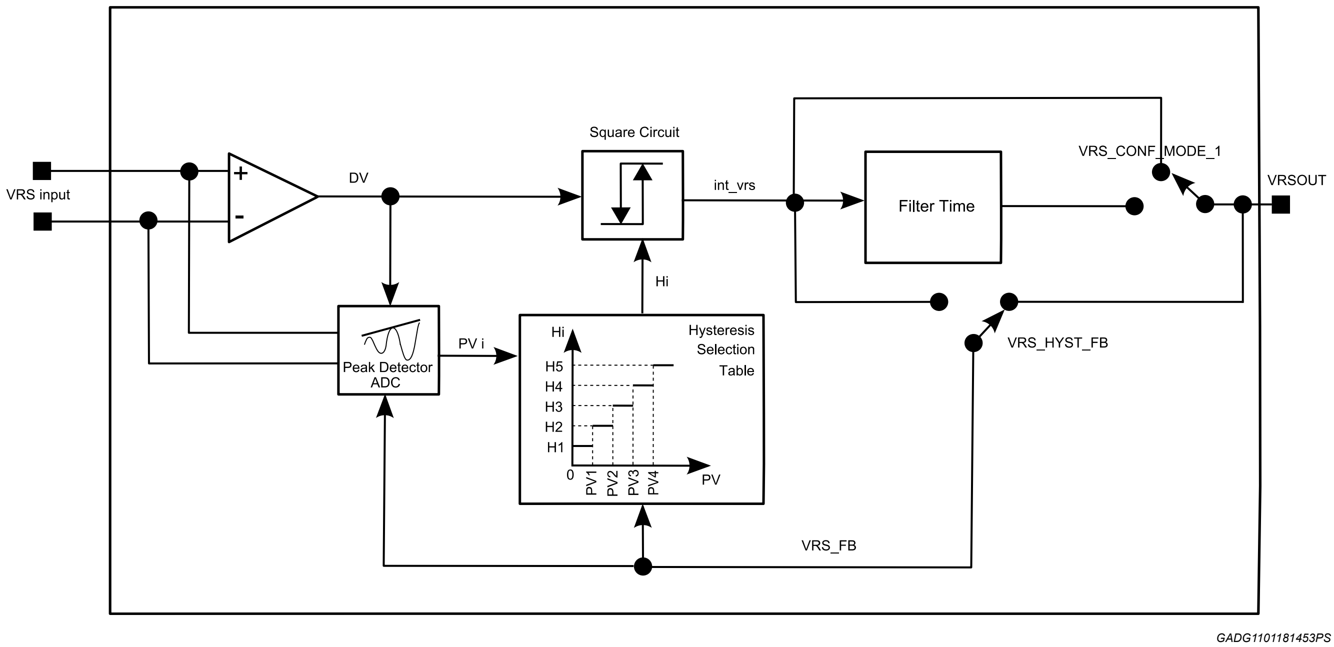
Input Peak Voltage Range	Selected Hysteresis (HIi)
0 - PV1	HI1
PV1 – PV2	HI2
PV2 – PV3	HI3
PV3 – PV4	HI4
> PV4	HI5

Peak detector and Hysteresis Selection Table circuits are enabled by VRS_OUT signal according to VRS_HYST_FB bit value in the VRS SPI register that establishes if the feedback signal is before or after the filter time.

VRS input differential voltage is continuously acquired: its max value, reached while VRS_OUT signal is high (hysteresis current off), is latched through the peak detector. Peak detector, in turn, defines the hysteresis current value. Hysteresis current is turned on as soon as the VRS_OUT falls to zero and it is switched OFF at next VRS_OUT rising edge.

Based on the hysteresis current, the signal is processed by a square circuit which processes the output signal of the comparator, see Figure 35. VRS_A fully adaptive hysteresis.

Figure 35. **VRS_A fully adaptive hysteresis**



15.2.4 VRS_A – Adaptive Filter Time

In VRS_A mode, it is possible to enable the filter time on the output of the zero crossing comparator through the bit VRS_CONF_MODE[1] of VRS register.

Once enabled, the most suitable internal filter based on the input signal frequency is determined.

According to VRS previous output period, filter time value is updated as per the following:

$$Tfilter(n) = \frac{Tperiod(n-1)}{32}$$

Should the value of the previous period be lower than 80 µs, the filter time would be saturated at 2.5 µs fixed value.The starting filter time period at power on reset is 125 µs. This is also the max filter time value that means if the period of input differential signal is greater than 4 ms, the filter time applied is no greater than 125 µs.

- VRS_OUT rising edge: the transition depends on the hysteresis crossing of differential signal Vdiff; VRS output is set if Vdiff remains asserted and stable for a period longer than Tfilter;

Through VRS_FE_FILT_EN bit in VRS register, it is possible to configure two different strategies for the filtering algorithm:

- VRS OUT falling edge: the transition depends on the zero crossing of differential signal Vdiff:
  - VRS_FE_FILT_EN = 1: VRS_OUT is deasserted when the signal is low and remains stable for at least T_{filter}, see Figure 36. VRS_FE_FILT_EN = 1
  - VRS_FE_FILT_EN = 0: VRS_OUT is de-asserted at first zero crossing transition of differential signal and next eventual commutations are ignored for T_{filter} time, see Figure 37. VRS_FE_FILT_EN = 0.

Figure 36. **VRS_FE_FILT_EN = 1**

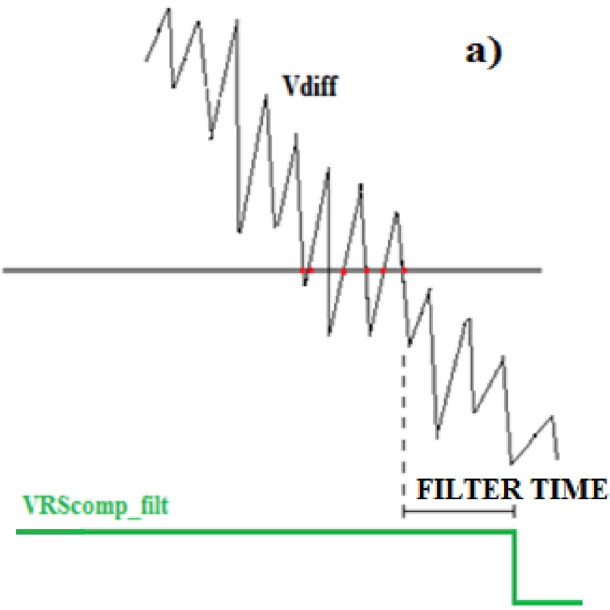


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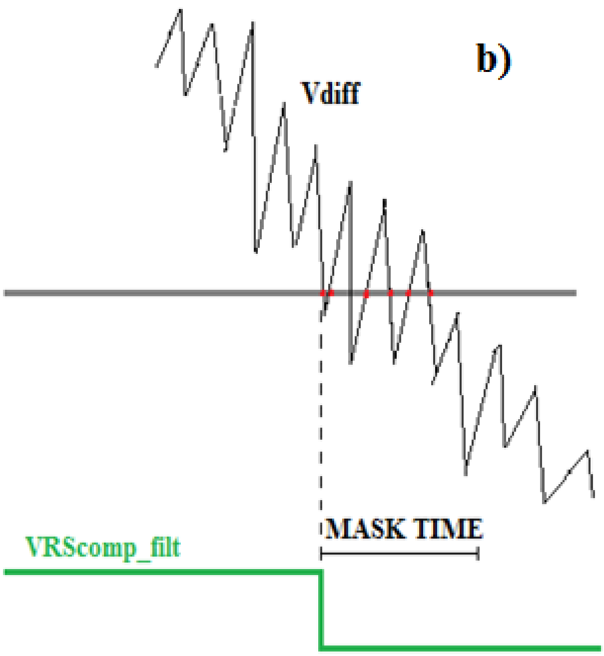
Figure 37. **VRS_FE_FILT_EN = 0**



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15.2.5 VRS_B – Manual Hysteresis

To set the manual hysteresis on VRS_B configuration, bit VRS_CONF_MODE[0] has to be set to ‘0’. Hysteresis value is manually set through VRS_HYST_CONF[2:0] of VRS register according to Table 48. VRS_A hysteresis value. Such hysteresis is fixed until a new SPI programming occurs.

Default hysteresis current after exiting reset is HI1.

Once a new value is defined, new hysteresis threshold is applied after the second VRS_OUT HL transition and until the next rising edge of the VRS input differential voltage occurs.

15.2.6 VRS_B –Limited Adaptive Hysteresis

To set the limited adaptive hysteresis on VRS_B configuration, bit VRS_CONF_MODE[0] has to be set to ‘1’. In this mode, user programs a hysteresis threshold through VRS_HYST_CONF[2:0] bit in VRS register and the internal logic selects a hysteresis based on input signal peak value (see Section 15.2.3 VRS_A – Fully adaptive hysteresis): the maximum of these two values is actually applied.

Default hysteresis current after exiting reset is HI1.

Once a new value is defined, new hysteresis threshold is applied after the first or the second VRS_OUT HL transition depending on LIM_ADAP_DOUBLE_EDGE bit in VRS register, if the bit has been fixed “0” the new hysteresis value is applied after the first VRS_OUT HL transition (default), otherwise after the second.

Current hysteresis value is active until the next rising edge of the VRS input differential voltage occurs.

When VRS_B architecture is selected, it is possible to force the hysteresis current to its minimum value through HYST_MIN_FORCE of VRS register regardless of the content of VRS_HYST_CONF [1,0] bit.

Default hysteresis current after exiting reset is HI1.

15.2.7 VRS_B – Fixed Filter Time

In VRS_B configuration, it is possible to enable the filter time on the output of the zero crossing comparator through the bit VRS_CONF_MODE[1] of VRS register. This configuration allows defining the internal filter time at a fixed value of 2.5 µs, active on both rising and falling edges of VRS output. The starting filter time period at power on reset is 125 µs.

As per VRS_A architecture, VRS_FE_FLT_EN allows configuring the same two different strategies for the filtering algorithm (see Section 15.2.4 VRS_A – Adaptive Filter Time).

15.3 VRS Diagnostic Mode

The diagnostic mode is selected through VRS_EN_DIAG = ‘1’ in VRS register. This mode provides feedback to detect faulty conditions either on VRSP or VRSN.

To be noted that diagnostic results are not reliable while the flying wheel is rotating.

If a fault is detected in DIAG mode, VRS correct functionality is not guaranteed.

Based on three comparators, it is possible to detect an open load fault condition, a short to ground or a short to battery fault condition. Fault bit VRS_FAULT[1:0] of VRS register are consequently set.

Once a fault has been detected being the diagnostic active (VRS_EN_DIAG=1) if the faulty condition is stable, DIAG_CLEAR_CMD set does not clear VRS_FAULT[1:0] field; if the faulty condition is solved, a write SPI access with DIAG_CLEAR_CMD=1 clears VRS_FAULT[1:0] field in terms of internal device register; only through another SPI access (either write or read access) determines VRS_FAULT[1:0] reset in SPI VRS register.

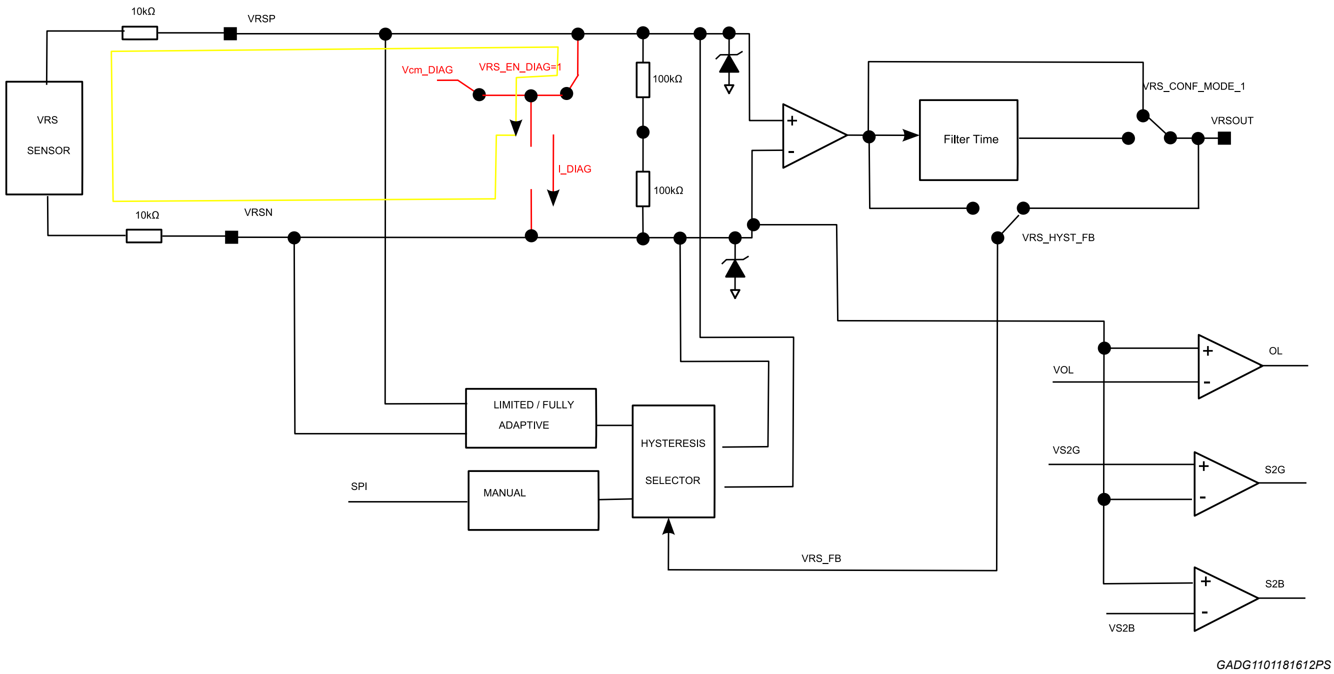
Once a fault has been detected (VRS_EN_DIAG=1), the reset of VRS_FAULT[1:0] field because of the diagnostic has been switched off, requires three SPI accesses:

- The first one to switch off the diagnostic and any DIAG_CLEAR_CMD set in the same frame is ignored
- Once the diagnostic is switched off, DIAG_CLEAR_CMD set determines the reset of VRS_FAULT[1:0] field in the internal register;
- The next SPI access (W or R) shows on SPI that VRS_FAULT[1:0] field in VRS register has been cleared

Figure 38. VRS block diagram - Diagnostic operating mode - Current path shows the circuit used in Diagnostic mode.

When VRS diagnostic mode is activated, VRSP is fixed at Vcm_DIAG and IDIAG current generator is enabled ; the current path is the one in yellow in Figure 38. VRS block diagram - Diagnostic operating mode - Current path.

Figure 38. **VRS block diagram - Diagnostic operating mode - Current path**



As additional feature VRSP can be routed to AOX to have a monitor of VRSP in case the sensor is not running.

15.4 Application circuit

Sensor sketch and parameters are reported in Figure 39. Sensor sketch and Table 51. VRS sensor parameters.

Figure 39. **Sensor sketch**

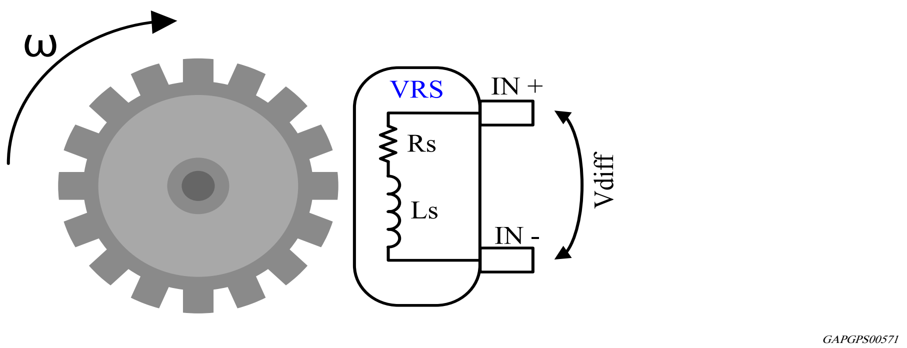


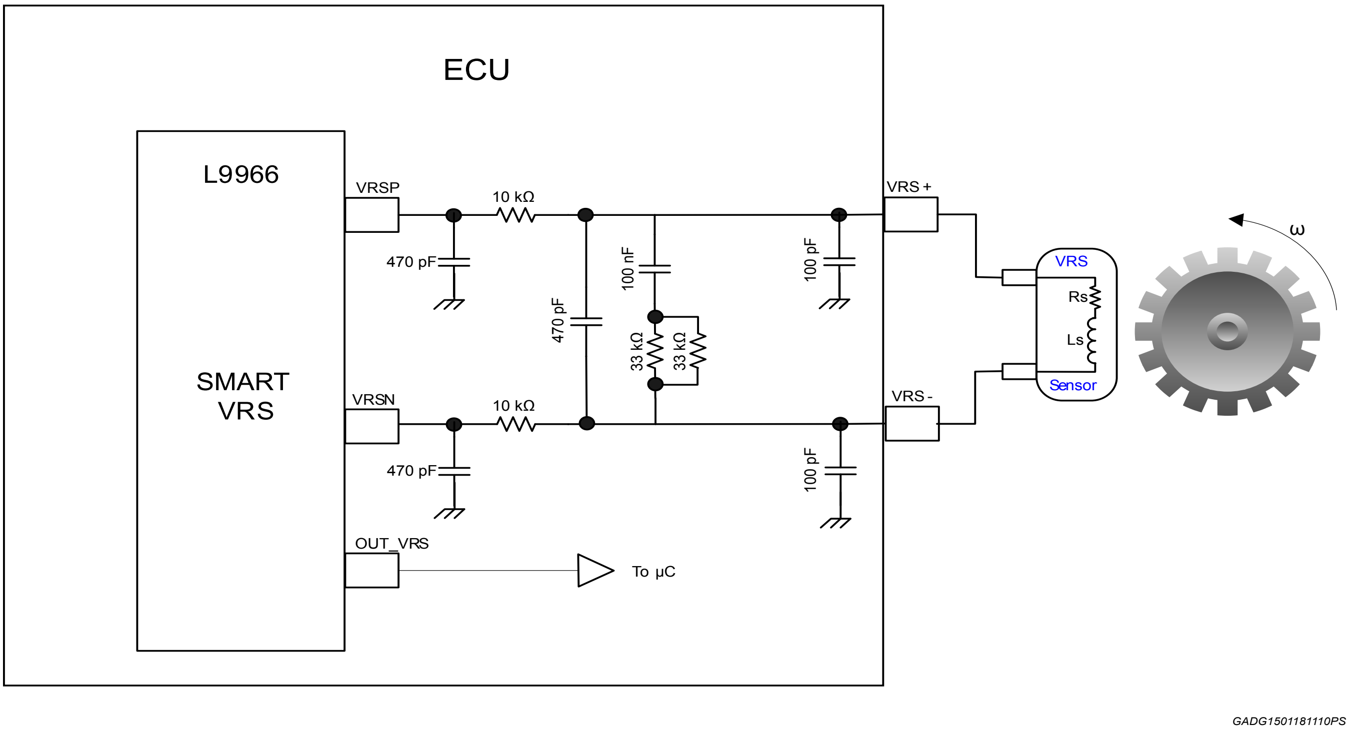
Table 51. **VRS sensor parameters**

Symbol	Parameter	Min	Typ	Max	Unit
Rs	Sensor resistance	300	600	1000	Ω
Ls	Sensor inductor	-	250	-	mH
Vdiff	Sensor output voltage	-200	-	+200	V
Tout	Output period	100	-	5000	μs

The interface handles signals coming from magnetic pick-up sensors, see Figure 40. Variable reluctance sensor (VRS), or Hall Effect sensors with two possible configurations, as per Figure 41. Hall effect sensor configuration 1 and Figure 42. Hall effect sensor configuration 2.

The interface feeds the digital signal to microcontroller that extracts flying wheel rotational position, angular speed and acceleration.

Figure 40. Variable reluctance sensor (VRS)



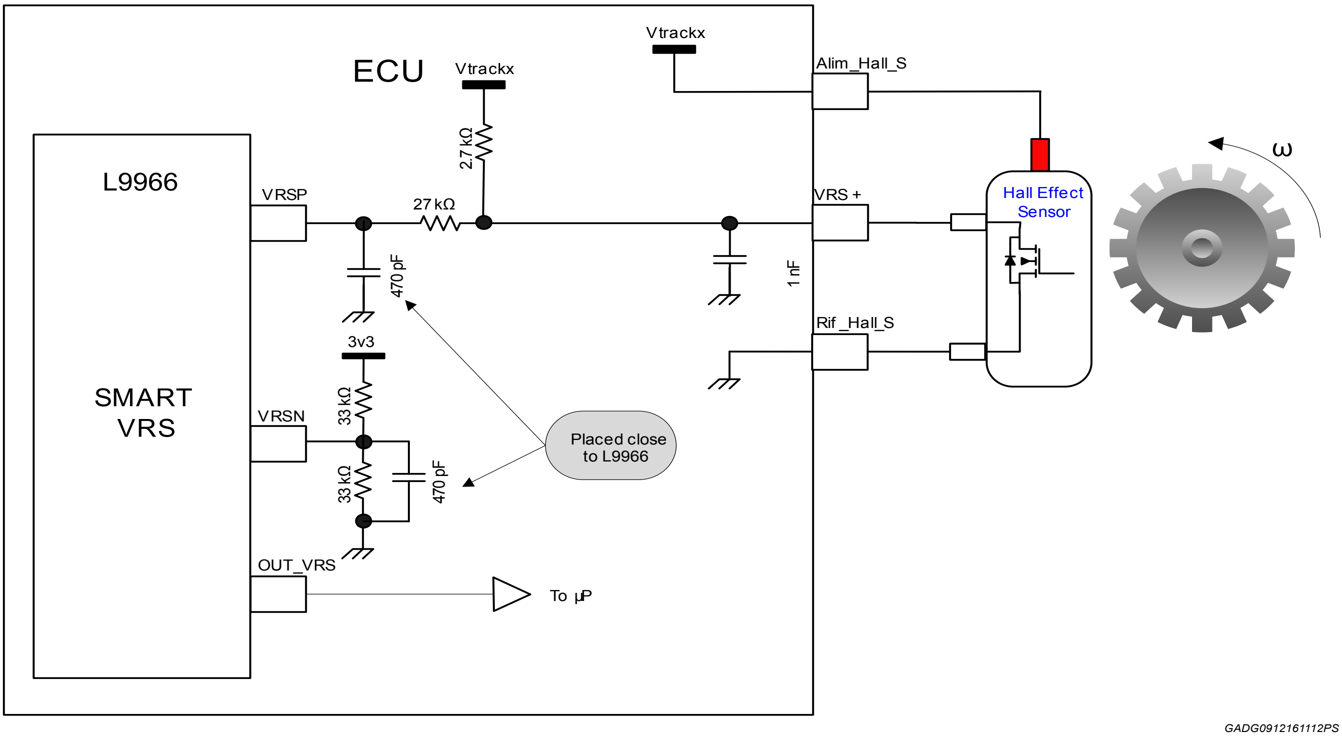


Figure 41. Hall effect sensor configuration 1

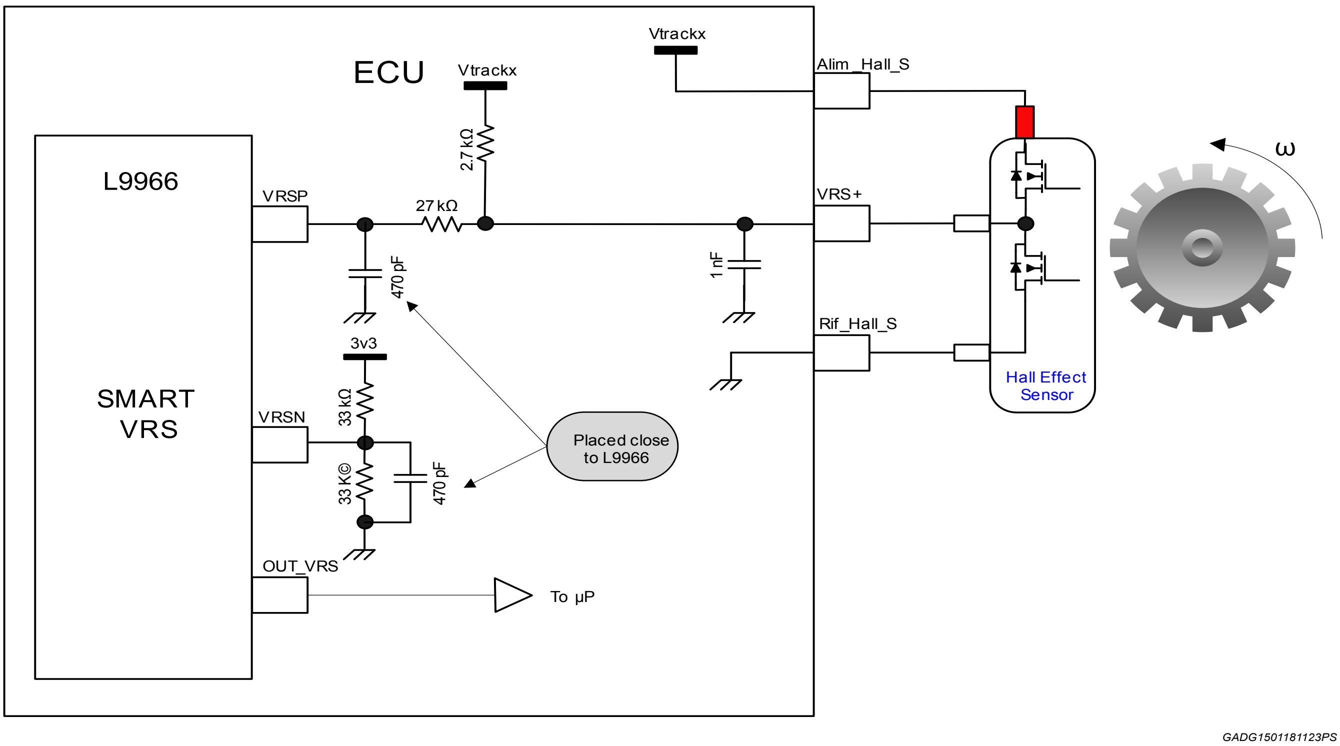


Figure 42. Hall effect sensor configuration 2

16 SPI register map

16.1 GEN_STATUS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	CFG_CHK_1	CFG_CHK_0	RESERVED						CALIB_SEL	CALIB_FLT	TRIM_FLT	OT_MASK	WAK_UP_FLG	3V3_FLT	OT_FLT
-	RW	RW							RW	R	R	RW	CR		

R = Read
W = Write
CR = Clear on Read

Address: 00000_0001
Description: General status register

Table 52. **GEN_STATUS register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:13]	Configuration Check Default value indicates device configuration is lost	10	PORn RSTn
[12:7]	RESERVED		
[6]	CALIB_SEL ADC calibration selection: 0: raw ADC result 1: calibrared ADC result	0	PORn RSTn
[5]	CALIB_FLT 0: no fault 1: Fault condition	0	PORn
[4]	TRIM FLT 1: Fault condition	0	PORn
[3]	OT_MASK Overtemperature fault mask 1: Enabled 0: Disabled	0	PORn RSTn
[2]	WAK_UP Wake up event 0: no fault 1: Entered wake up event state	1	PORn

Range	Field name/description	Reset Value	Reset Event
[1]	3V3_FLT 3V3 voltage supply fault 0: no fault 1: Fault condition	0	PORn
[0]	OT_FLT Overtemperature fault 0: no fault 1: Fault condition	0	PORn

16.2 DEV_V

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	RESERVED							VER_ID_7	VER_ID_6	VER_ID_5	VER_ID_4	VER_ID_3	VER_ID_2	VER_ID_1	VER_ID_0
-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 0b0000_0010

Description: Device version register

Table 53. **DEV_V register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:8]	Reserved	0	PORn
[7:0]	VER_ID_[7:0] Device Version ID It is incremented for each minor change in the same hardware revision	n n= 1 for x**A**, n=2 for x**B**	PORn

16.3 HW_REV

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	RESERVED							HW_REV_7	HW_REV_6	HW_REV_5	HW_REV_4	HW_REV_3	HW_REV_2	HW_REV_1	HW_REV_0
-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 0b0000_0011

Description: Hardware revision

Table 54. **HW_REV register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:8]	Reserved	0	PORn
[7:0]	HW_REV_[7:0] Hardware revision ID It is incremented for each silicon major change	m m=1 for **A**x m=2 for **B**x	PORn

16.4 DEV_ID

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	RESERVED							DEV_ID_7	DEV_ID_6	DEV_ID_5	DEV_ID_4	DEV_ID_3	DEV_ID_2	DEV_ID_1	DEV_ID_0
-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 0b0000_0100

Description: Device identification register

Table 55. **DEV_ID register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:8]	Reserved	0	PORn
[7:0]	DEV_ID Device ID	01011010	PORn

16.5 CURR_SRC_CTRL_[1:4]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	CIS_3	CIS_2	CIS_1	CIS_0	CTR_1	CTR_0	CV_2	CV_1	CV_0	CV_DW_1	CV_DW_0	SEL_2	SEL_1	SEL_0	MODE_INV
-	RW (R20K_SENT_x = 0), R (R20K_SENT_x = 1)				RW		RW (R20K_SENT_x = 0), R (R20K_SENT_x = 1)								RW

Address: 0b0010_0001 up to 0b0010_0100

Description: Current source control register

Table 56. **CURR_SRC_CTRL_[1:4] register bit description (when R20K_SENT_x = 0)**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:11]	CIS[3:0]: Control channel selection (read/write field) 0000: Force to 0 0001: Channel 1 …. CIS == x: Select VRS or CTRL_CFG according to bit AUX_EVENCH or AUX_ODDCH 1111: Channel 15	0000	PORn RSTn
[10:9]	CTR: Comparator threshold 00: Uth1 01: Uth2 10: Uth3 11: Uth Ratiometric	00	PORn RSTn
[8:6]	CV[2:0] Current source value 000: 7.5 µA (PU) - 1 µA (PU-VVAR) - 600uA(PD) 001: 20 µA (PU) - 20 µA (PD) 010: 250 µA (PU) - 100 µA (PD) 011: 500 µA (PU) - 500 µA (PD) 100: 1 mA (PU) - 1 mA (PD) 101: 5 mA (PU) - 5 mA (PD) 110: 10 mA (PU) - 10 mA (PD) 111: 20 mA (PU) - 2 0 mA (PD)	000	PORn RSTn
[5:4]	CV_DW: Current source value during dewetting phase 00: 5 mA 01: 10 mA 10: 20 mA 11: current source value as from CV[2:0]	11	PORn RSTn
[3:1]	SEL[2:0]: Pull-up/pull-down selection (CS=Control Signal) 000: HighZ (CS=1) - HighZ (CS=0)	000	PORn RSTn

Range	Field name/description	Reset Value	Reset Event
	001: PullUPVPRE (CS=1) - HighZ (CS=0) 010: PullUp 5V_REF (CS=1) - HighZ (CS=0) 011: PullUpVVAR (CS=1) - HighZ (CS=0) 100: PullDown (CS=1) - HighZ (CS=0) 101: PullUPVPRE (CS=1) - PullDown (CS=0) 110: PullUp 5V_REF (CS=1) - PullDown (CS=0) 111: PullUpVVAR (CS=1) - PullDown (CS=0) IO[15:13] PU only to VPRE; VVAR or 5V_REF automatically redirected to VPRE		
[0]	MODE Invert control channel polarity to obtain CONTROL SIGNAL 0: not inverted 1: inverted	0	PORn RSTn

Table 57. CURR_SRC_CTRL_[1:4] register bit description (when R20K_SENT_x = 1)

Range	Field name/description	Reset Value	Reset Event
[15]	Parity		
[14:11]	CIS[3:0]: 0000 (read only field)	0000	PORn RSTn
[10:9]	CTR: Comparator threshold 00: Uth1 01: Uth2 10: Uth3 11: Uth Ratiometric	00	PORn RSTn
[8:6]	CV[2:0]: 000 (read only field)	000	PORn RSTn
[5:4]	CV_DW[1:0]: 11 (read only field)	11	PORn RSTn
[3:1]	SEL[2:0]=000 (read only field)	000	PORn RSTn
[0]	MODE=0 (read only field)	0	PORn RSTn

16.6 CURR_SRC_CTRL_[5:8]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	CIS_3	CIS_2	CIS_1	CIS_0	CTR_1	CTR_0	CV_2	CV_1	CV_0	CV_DW_1	CV_DW_0	SEL_2	SEL_1	SEL_0	MODE
-	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: 0b0010_0101 up to 0b0010_1000

Description: Current source control register

Table 58. CURR_SRC_CTRL_[5:8] register bit description

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:11]	CIS[3:0]: Control channel selection (read/write field) 0000: Force to 0 0001: Channel 1 …. CIS == x: Select VRS or CTRL_CFG according to bit AUX_EVENCH or AUX_ODDCH 1111: Channel 15	0000	PORn RSTn
[10:9]	CTR: Comparator threshold 00: Uth1 01: Uth2 10: Uth3 11: Uth Ratiometric	00	PORn RSTn
[8:6]	CV[2:0] Current source value 000: 7.5 µA (PU) - 1uA (PU-VVAR) - 600uA(PD) 001: 20 µA (PU) - 20 µA (PD) 010: 250 µA (PU) - 100 µA (PD) 011: 500 µA (PU) - 500 µA (PD) 100: 1 mA (PU) - 1mA (PD) 101: 5 mA (PU) - 5mA (PD) 110: 1 0mA (PU) - 10mA (PD) 111: 2 0mA (PU) - 20mA (PD)	000	PORn RSTn
[5:4]	CV_DW: Current source value during dewetting phase 00: 5 mA 01: 10 mA 10: 20 mA 11: current source value as from CV[2:0]	11	PORn RSTn
[3:1]	SEL[2:0]: Pull-up/pull-down selection (CS=Control Signal) 000: HighZ (CS=1) - HighZ (CS=0) 001: PullUpVPRE (CS=1) - HighZ (CS=0)	000	PORn RSTn

Range	Field name/description	Reset Value	Reset Event
	010: PullUp 5V_REF (CS=1) - HighZ (CS=0) 011: PullUpVVAR (CS=1) - HighZ (CS=0) 100: PullDown (CS=1) - HighZ (CS=0) 101: PullUpVPRE (CS=1) - PullDown (CS=0) 110: PullUp 5V_REF (CS=1) - PullDown (CS=0) 111: PullUpVVAR (CS=1) - PullDown (CS=0) IO[15:13] PU only to VPRE; VVAR or 5V_REF automatically redirected to VPRE		
[0]	MODE Invert control channel polarity to obtain CONTROL SIGNAL 0: not inverted 1: inverted	0	PORn RSTn

16.7 CURR_SRC_CTRL_[9:12]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	CIS_3	CIS_2	CIS_1	CIS_0	CTR_1	CTR_0	CV_2	CV_1	CV_0	CV_DW_1	CV_DW_0	SEL_2	SEL_1	SEL_0	MODE_INV
	RW				RW		RW (LSF_MD_x = 0), R (LSF_MD_x = 1)			RW		RW (LSF_MD_x = 0), R (LSF_MD_x = 1)			RW

Address: 0b0010_1001 up to 0b0010_1100

Description: Current source control register

Table 59. **CURR_SRC_CTRL_[9:12] register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:11]	CIS[3:0]: Control channel selection 0000: Force to 0 0001: Channel 1 …. CIS == x: Select VRS or CTRL_CFG according to bit AUX_EVENCH or AUX_ODDCH 1111: Channel 15	0000	PORn RSTn
[10:9]	CTR: Comparator threshold 00: Uth1 01: Uth2 10: Uth3 11: Uth Ratiometric	00	PORn RSTn
[8:6]	CV[2:0] Current source value **When LSF_MDx(x=9:12) = ‘1’ . Other combination are not allowed** 100: 1 µA (PU current to VVAR) - 250 µA (PU current to 5V_REF) 101: 1 µA (PU current to VVAR) - 500 µA (PU current to 5V_REF) 110: 20 µA (PU current to VVAR) - 250 µA (PU current to 5V_REF) 111: 20 µA (PU current to VVAR) - 500 µA (PU current to 5V_REF) **When LSF_MDx(x=9:12) = ‘0'** 000: 7.5 µA (PU) - 1uA (PU-VVAR) - 600 µA(PD) 001: 20 µA (PU) - 20 µA (PD) 010: 250 µA (PU) - 100 µA (PD) 011: 500 µA (PU) - 500 µA (PD) 100: 1 mA (PU) - 1 mA (PD) 101: 5 mA (PU) - 5 mA (PD) 110: 10 mA (PU) - 10 mA (PD) 111: 20 mA (PU) - 20 mA (PD)	000	PORn RSTn

Range	Field name/description	Reset Value	Reset Event
[5:4]	CV_DW: Current source value during dewetting phase 00: 5 mA 01: 10 mA 10: 20 mA 11: current source value as from CV[2:0]	11	PORn RSTn
[3:1]	SEL[2:0]: Pull-up/pull-down selection (CS=Control Signal) **When LSF_MDx(x=9:12) = ‘1’** 111: PullUpVVAR (CS=1) - PullUp 5V_REF (CS=0) - **when LSF_MDx(x=9:12) = ‘0’** 000: HighZ (CS=1) - HighZ (CS=0) 001: PullUPVPRE (CS=1) - HighZ (CS=0) 010: PullUp 5V_REF (CS=1) - HighZ (CS=0) 011: PullUpVVAR (CS=1) - HighZ (CS=0) 100: PullDown (CS=1) - HighZ (CS=0) 101: PullUPVPRE (CS=1) - PullDown (CS=0) 110: PullUp 5V_REF (CS=1) - PullDown (CS=0) 111: PullUpVVAR (CS=1) - PullDown (CS=0) IO[15:13] PU only to VPRE; VVAR or 5V_REF automatically redirected to VPRE	000	PORn RSTn
[0]	MODE Invert control channel polarity to obtain CONTROL SIGNAL 0: not inverted 1: inverted	0	PORn RSTn

16.8 CURR_SRC_CTRL_[13:15]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	CIS_3	CIS_2	CIS_1	CIS_0	CTR_1	CTR_0	CV_2	CV_1	CV_0	CV_DW_1	CV_DW_0	SEL_2	SEL_1	SEL_0	MODE
-	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: 0010_1101 up to 0010_1111

Description: Current source control register

Table 60. **CURR_SRC_CTRL_[13:15] register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:11]	CIS[3:0]: Control channel selection (read/write field) 0000: Force to 0 0001: Channel 1 …. CIS == x: Select VRS or CTRL_CFG according to bit AUX_EVENCH or AUX_ODDCH 1111: Channel 15	0000	PORn RSTn
[10:9]	CTR: Comparator threshold 00: Uth1 01: Uth2 10: Uth3 11: Uth Ratiometric	00	PORn RSTn
[8:6]	CV[2:0] Current source value 000: 7.5 µA (PU) - 1uA (PU-VVAR) - 600uA(PD) 001: 20 µA (PU) - 20 µA (PD) 010: 250 µA (PU) - 100 µA (PD) 011: 500 µA (PU) - 500 µA (PD) 100: 1 mA (PU) - 1mA (PD) 101: 5 mA (PU) - 5mA (PD) 110: 1 0mA (PU) - 10mA (PD) 111: 2 0mA (PU) - 20mA (PD)	000	PORn RSTn
[5:4]	CV_DW: Current source value during dewetting phase 00: 5 mA 01: 10 mA 10: 20 mA 11: current source value as from CV[2:0]	11	PORn RSTn
[3:1]	SEL[2:0]: Pull-up/pull-down selection (CS=Control Signal) 000: HighZ (CS=1) - HighZ (CS=0) 001: PullUpVPRE (CS=1) - HighZ (CS=0)	000	PORn RSTn

Range	Field name/description	Reset Value	Reset Event
	010: PullUp 5V_REF (CS=1) - HighZ (CS=0) 011: PullUpVVAR (CS=1) - HighZ (CS=0) 100: PullDown (CS=1) - HighZ (CS=0) 101: PullUpVPRE (CS=1) - PullDown (CS=0) 110: PullUp 5V_REF (CS=1) - PullDown (CS=0) 111: PullUpVVAR (CS=1) - PullDown (CS=0) IO[15:13] PU only to VPRE; VVAR or 5V_REF automatically redirected to VPRE		
[0]	MODE Invert control channel polarity to obtain CONTROL SIGNAL 0: not inverted 1: inverted	0	PORn RSTn

16.9 SWITCH_ROUTE / GTM_AOX_RSENT_CONF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	RESERVED	AUX_EVENCH	AUX_ODDCH	DIG_FIL_4	DIG_FIL_3	DIG_FIL_2	DIG_FIL_1	RAOX_3	RAOX_2	RAOX_1	RAOX_0	RSENT_4	RSENT_3	RSENT_2	RSENT_1
-		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: 0b0011_0000

Description: Current Source Control Register

Table 61. **SWITCH_ROUTE / GTM_AOX_RSENT_CONF register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14]	RESERVED	0	PORn
[13]	AUX_EVENCH Control channel selection for even numbered channels when CIS==x (see register CURR_SRC_CTRL_x) 0: VRS 1: CTRL_CFG	1	PORn RSTn
[12]	AUX_ODDCH Control channel selection for odd numbered channels when CIS==x (see register CURR_SRC_CTRL_x) 0: VRS 1: CTRL_CFG	0	PORn RSTn
[11:8]	DIG_FIL_[4-1] 1 µs digital filter enable 0: not enable 1: enable	0 if RSENT_x=0 1 if RSENT_x=1	PORn
[7:4]	RAOX_[3-0] AOX channel source 0000: AOX to HiZ 0001: Channel 1 …. 1100: Channel 12 1101: Band Gap (internal voltage, 1.24 V Tamb) 1110: internal ADCx reference achieved partitioning 5 V_REF pin, (1.25 V assuming 5V_REF = 5 V) 1111: VSRP	0000	PORn RSTn
[3:0]	RSENT_[4-1] SENT Channel enable xxx1: SENT on channel 1 enabled	0000	PORn RSTn

Range	Field name/description	Reset Value	Reset Event
	xx1x: SENT on channel 2 enabled x1xx: SENT on channel 3 enabled 1xxx: SENT on channel 4 enabled		

16.10 DWT_VOLT_SRC_LSF_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	RESERVED	RESERVED	LSF_MD12	LSF_MD11	LSF_MD10	LSF_MD9	RESERVED	DWT_2	DWT_1	DWT_0	VAR_V_4	VAR_V_3	VAR_V_2	VAR_V_1	VAR_V_0
-			RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW

Address: 0b0011_0001

Description: Dewetting voltage source register

Table 62. **DWT_VOLT_SRC_LSF_CTRL register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:13]	RESERVED	00	PORn
[12:9]	LSF_MDx(x=9:12) CH 9-12 binary lambda mode 0: Binary lambda mode disabled 1: Binary lambda mode enabled	0000	PORn RSTn
[8]	RESERVED	0	PORn
[7:5]	DWT Dewetting timer time configuration 000: 2 ms 001: 16 ms 010: 64 ms 011: 128 ms 100: 256 ms 101: 512 ms 110: 1024 ms 111: 2048 ms	000	PORn RSTn
[4:0]	VVAR_V Channel variable voltage source selection (50 mV steps in limited range 800 mV - 1900 mV) 00000: 800 mV; 00001: 850 mV. 00010: 900 mV 10110: 1900 mV … 11111: 1900 mV	0_0000	PORn RSTn

Every writing access to DWT_VOLT_SRC_LSF_CTRL has impact on IO[12:9] configuration that is automatically reset:

- in case LSF_MD_x=1 default configuration is 250 μA PU VDD5
- in case LSF_MD_x=0 default configuration is HiZ.

16.11 DIG_IN_STAT_LTC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	DIG_IN_LTC_15	DIG_IN_LTC_14	DIG_IN_LTC_13	DIG_IN_LTC_12	DIG_IN_LTC_11	DIG_IN_LTC_10	DIG_IN_LTC_9	DIG_IN_LTC_8	DIG_IN_LTC_7	DIG_IN_LTC_6	DIG_IN_LTC_5	DIG_IN_LTC_4	DIG_IN_LTC_3	DIG_IN_LTC_2	DIG_IN_LTC_1
-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 0b0011_0011

Description: Channel output digital value during last polling

Table 63. **DIG_IN_STAT_LTC register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:0]	DIG_IN_LTC Bit[x]=1 means IOx has been recognized assuming a different value with respect to its value before entering in SLEEP mode when the IC leaves the POLLING phase, regardless whether IOx has been defined as WAKE source or not	0	PORn

16.12 GTM_TO_SENT_ROUTE_1_2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	RESERVED	AN_FIL_2	AN_FIL_1	DIG_BP_2	DIG_BP_1	20kPU_2	20kPU_1	SENT2_GTM_ROUTE_4	SENT2_GTM_ROUTE_3	SENT2_GTM_ROUTE_2	SENT2_GTM_ROUTE_1	SENT1_GTM_ROUTE_4	SENT1_GTM_ROUTE_3	SENT1_GTM_ROUTE_2	SENT1_GTM_ROUTE_1
-		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: 0b0011_0100

Description: GTM to SENT configuration for channel 1 and 2

Table 64. **GTM_TO_SENT_ROUTE_1_2 register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14]	RESERVED	0	PORn
[13:12]	AN_FIL Analog filter selection 0: Slow 1: Fast	0 (RSENT_2=0), 1 (RSENT_2=1); 0 (RSENT_1=0), 1 (RSENT_1=1);	PORn RSTn
[11:10]	DIG_BP Bypass of all digital elaboration 0: Off 1: On	0	PORn RSTn
[9:8]	20kPU Passive 20k pull-up selected 0: Off 1: On	0	PORn RSTn
[7:4]	SENT2_GTM_ROUTE 0000: No channel (HiZ) 0001: Channel 1 …. 1111: Channel 15	0000	PORn RSTn
[3:0]	SENT1_GTM_ROUTE 0000: No channel (HiZ) 0001: Channel 1 …. 1111: Channel 15	0000	PORn RSTn

16.13 GTM_TO_SENT_ROUTE_3_4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	RESERVED	AN_FIL_4	AN_FIL_3	DIG_BP_4	DIG_BP_3	20kPU_4	20kPU_3	SENT4_GTM_ROUTE_4	SENT4_GTM_ROUTE_3	SENT4_GTM_ROUTE_2	SENT4_GTM_ROUTE_1	SENT3_GTM_ROUTE_4	SENT3_GTM_ROUTE_3	SENT3_GTM_ROUTE_2	SENT3_GTM_ROUTE_1
-		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: 0b0011_0101

Description: GTM to SENT configuration for channel 3 and 4

Table 65. **GTM_TO_SENT_ROUTE_3_4 register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14]	RESERVED	000000	PORn
[13:12]	AN_FIL Analog filter selection 0: Slow 1: Fast	0(RSENT_4=0),1(RSENT_4=1) 0(RSENT_3=0),1(RSENT_3=1)	PORn RSTn
[11:10]	DIG_BP Bypass of all digital elaboration 0: Off 1: On	0	PORn RSTn
[9:8]	20kPU Passive 20k pull-up selected 0: Off 1: On	0	PORn RSTn
[7:4]	SENT4_GTM_ROUTE 0000: No channel (HiZ) 0001: Channel 1 …. 1111: Channel 15	1111	PORn RSTn
[3:0]	SENT3_GTM_ROUTE 0000: No channel (HiZ) 0001: Channel 1 …. 1111: Channel 15	0000	PORn RSTn

16.14 ACTIVE_DISCHARGE_LSF_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	RESERVED		ACTIVE_DSCHRG_EN_CH12	ACTIVE_DSCHRG_EN_CH11	ACTIVE_DSCHRG_EN_CH10	ACTIVE_DSCHRG_EN_CH9	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ACTIVE_DSCHRG_TIM_3	ACTIVE_DSCHRG_TIM_2	ACTIVE_DSCHRG_TIM_1	ACTIVE_DSCHRG_TIM_0
-			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: 0b0011_0110

Table 66. ACTIVE_DISCHARGE_LSF_CTRL register bit description

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:13]	Reserved	00	PORn
[12:9]	ACTIVE_DISCHARGE_EN_CHx xxx1: ACTIVE_DISCHARGE enabled on IO9 xx1x: ACTIVE_DISCHARGE enabled on IO10 x1xx: ACTIVE_DISCHARGE enabled on IO11 1xxx: ACTIVE_DISCHARGE enabled on IO12	0000	PORn RSTn
[8:4]	Reserved	0000	PORn
[3:0]	Active discharge time configuration 0000: 0 ms 0001: 1 ms 0010: 2 ms … 1111: 15 ms	0000	PORn RSTn

16.15 WAK_MSK

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	MSK_IN_15	MSK_IN_14	MSK_IN_13	MSK_IN_12	MSK_IN_11	MSK_IN_10	MSK_IN_9	MSK_IN_8	MSK_IN_7	MSK_IN_6	MSK_IN_5	MSK_IN_4	MSK_IN_3	MSK_IN_2	MSK_IN_1
-	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: 0b0100_0000

Description: Wake-up source mask register

Table 67. **WAK_MSK register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:0]	MSK_IN IOx WAKE SOURCES definition 1: IOx defined as WAKE source 0: IOx defined as no WAKE source	0	PORn RSTn

16.16 SLEEP_CONFIG

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	TGT_IN_15	TGT_IN_14	TGT_IN_13	TGT_IN_12	TGT_IN_11	TGT_IN_10	TGT_IN_9	TGT_IN_8	TGT_IN_7	TGT_IN_6	TGT_IN_5	TGT_IN_4	TGT_IN_3	TGT_IN_2	TGT_IN_1
-	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: 0b0100_0001

Description: Wake-up source value before sleep

Table 68. **SLEEP_CONFIG register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:0]	TGT_IN Channel level before entering sleep mode. 1: Channel level high 0: Channel level low	0	PORn RSTn

16.17 WAK_CONFIG

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	RESERVED							PB_1	PB_0	PT_1	PT_0	AC_3	AC_2	AC_1	AC_0
-								RW	RW	RW	RW	RW	RW	RW	RW

Address: 0b0100_0010

Description: Wake-up source register

Table 69. WAK_CONFIG register bit description

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[7:6]	PB Polling Blanking time configuration 00: 160 µs 01: 80 µs 10: 40 µs 11: 16 µs	00	PORn RSTn
[5:4]	PT Polling time configuration 00: 8 ms 01: 16 ms 10: 24 ms 11: 32 ms	01	PORn RSTn
[3:0]	AC Activation code to enter in sleep mode 0101: first frame 1010: second frame 1100: third frame	0000	PORn

16.18 SOFT_RST_CMD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	RESERVED											AC_3	AC_2	AC_1	AC_0
-												RW	RW	RW	RW

Address: 0b0100_0011

Table 70. **SOFT_RST_CMD register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:4]	RESERVED	0	PORn
[3:0]	Activation Code 1001: first frame 0110: second frame 0011: third frame	0000	PORn RSTn

16.19 VRS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	VRS_FAULT_1	VRS_FAULT_0	RESERVED	Lim_Adap_double_edge	DIAG_CLEAR_CMD	MIN_HYST_FORCE	VRS_SEL	VRS_CONF_MODE		VRS_HYST_CONF			VRS_EN_DIAG	VRS_HYST_FB	VRS_FE_FILT_EN
	CR			RW	W	RW									

Address: 0b0101_0001

Description: VRS register

Table 71. **VRS register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:13]	VRS_FAULT VRS diagnostics flags 00: no fault 01: short to ground 10: open load 11: short to battery	00	PORn RSTn
[12]	RESERVED	0	PORn
[11]	Lim_Adap_double_edge Double edge selection 0: disable 1: enable	0	PORn RSTn
[10]	DIAG_CLR_CMD 1: clear diagnostics flags after read out 0: no clear diagnostics flags after read out	0	PORn
[9]	MIN_HYST_FORCE Force minimum hysteresis threshold (limited adaptive mode): 1: Force hysteresis to default value suddenly 0: no hysteresis forcing	0	PORn RSTn
[8]	VRS_SEL Adaptive mode selection 0: Limited adaptive mode 1: Fully adaptive mode	0	PORn RSTn
[7:6]	VRS_CONF_MODE	00	PORn

Range	Field name/description	Reset Value	Reset Event
	VRS configuration 00: Auto filtering disabled, auto hysteresis disabled 01: Auto filtering disabled, auto hysteresis enabled 10: Auto filtering enabled, auto hysteresis disabled 11: Auto filtering enabled, auto hysteresis enabled		RSTn
[5:3]	VRS_HYST_CONF VRS hysteresis threshold selection 000: HI3 (VRS_A) / HI1 (VRS_B) 001: HI1 010: HI2 011: HI3 100: HI4 101: HI5 110: HI3 (VRS_A) / HI1 (VRS_B) 111: Hyst OFF	000	PORn RSTn
[2]	VRS_EN_DIAG VRS diagnostics enable 1: diagnostics enabled 0: normal mode	0	PORn RSTn
[1]	VRS_HYST_FB_MODE VRS hysteresis feedback mode 1: Feedback from filtered VRS 0: Feedback from direct VRS comparator output	0	PORn RSTn
[0]	VRS_FE_FILT_EN VRS falling edge filter enable 0: Falling edge masking enabled 1: Falling edge filter enabled	0	PORn RSTn

16.20 SQNCR_INT_MSK_FLG

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	RESERVED	INT_EU2_CONF_3	INT_EU2_CONF_2	INT_EU2_CONF_1	INT_EU2_CONF_0	INT_EU1_CONF_3	INT_EU1_CONF_2	INT_EU1_CONF_1	INT_EU1_CONF_0	CFG_EU_2	CFG_EU_1	CFG_SC	INT_EU2	INT_EU1	INT_SC
-		W				W				RW			CR		

Address: 0b1000_0000

Description: Sequencer interrupt register

Table 72. **SQNCR_INT_MSK_FLG register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14]	RESERVED	0	PORn
[13:10]	INT_EU2_CONF NEXT_PC which generates interrupt for EU2 (closed loop)	0000	PORn RSTn
[9:6]	INT_EU1_CONF NEXT_PC which generates interrupt for EU1 (closed loop)	0000	PORn RSTn
[5:3]	CFG_EU2; CFG_EU1; CFG_SC Interrupt mask xx1: interrupt of SC masked x1x: interrupt of EU1 masked 1xx: interrupt of EU2 masked	000	PORn RSTn
[2:0]	INT_EU2; INT_EU1; INT_SC End of operation flag xx1: SC completed x1x: EU1 endloop/closed-loop reached 1xx: EU2 endloop/closed-loop reached	000	PORn RSTn

16.21 SC_CONF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	RESERVED						ADC_RUN	ADC_MUX_4	ADC_MUX_3	ADC_MUX_2	ADC_MUX_1	ADC_MUX_0	PUP1_DIV_1	PUP0_DIV_0	R_VOLT_MEAS_SELECT
							RW (set to '1')	RW							

Address: 0b1000_0001

Description: Single conversion module register

Table 73. **SC_CONF register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:9]	RESERVED	0	PORn
[8]	ADC_RUN Single conversion unit 1: Command single conversion unit to run	0	PORn RSTn
[7:3]	ADC_MUX ADC Channel selection Following codes valid for both ADC1 and ADC2: 00000 debug voltage (3V3/3.344 = 0.99 V) 00001: IO1 … 01100: IO12 Following codes valid only for ADC1: 01101: UBSW 01110 VI5V 01111: VIX 10000: IO13 (only UTh2 or Uth_ratio must be selected) 10001: IO14 (only UTh2 or Uth_ratio must be selected) 10010: IO15 (only UTh2 or Uth_ratio must be selected) 10011: BG/2 10100: Tj 10101 – 11111: invalid code	00000	PORn RSTn
[2:1]	PUP_DIV	00	PORn

Range	Field name/description	Reset Value	Reset Event
	Pull-up selection (when ADC Resistance selected), division factor (ADC Voltage selected, except for UBSW, VI5V, VIX, BG) '00: no pullup, full range = 5 V (1.2 5 V for IO[15:13]) [01] pullup RR1, full range = 20 V 10: pullup RR2, full range = 40 V 11: pullup RR3, full range = 1.25 V		RSTn
[0]	R_VOLT_MEAS_SELECT ADC Resistance / Voltage selection 0: Resistance ADC selected (ADC2) 1: Voltage ADC selected (ADC1)	0	PORn RSTn

16.22 ADC_TIMING

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	CT_AD_2	CT_AD_1	CT_AD_0	CT_PU3_3	CT_PU3_2	CT_PU3_1	CT_PU3_0	CT_PU2_3	CT_PU2_2	CT_PU2_1	CT_PU2_0	CT_PU1_3	CT_PU1_2	CT_PU1_1	CT_PU1_0
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: 0b1000_0010

Description: ADC timing register

Table 74. **ADC_TIMING register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:12]	CT_AD ADC Volt settling time configuration in 8 µs steps 000: 0 µs 001: 8 µs ..... 111: 56 µs	000	PORn RSTn
[11:8]	CT_PU3 ADC Resistance settling time configuration in 200 µs steps (Pull-up RR3 selected) 0000: 0 µs 0001: 200 µs ...... 1111: 3000 µs	0000	PORn RSTn
[7:4]	CT_PU2 ADC Resistance settling time configuration in 200 µs steps (Pull-up RR2 selected) 0000: 0 µs 0001: 200 µs ...... 1111: 3000 µs	0000	PORn RSTn
[3:0]	CT_PU1 ADC Resistance settling time configuration in 200 µs steps (Pull-up RR1 selected) 0000: 0 µs 0001: 200 µs ...... 1111: 3000 µs	0000	PORn RSTn

16.23 SC_RESULT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	ADC_14/NEW_RSLT_FLG	ADC_13	ADC_12	ADC_11	ADC_10	ADC_9	ADC_8	ADC_7	ADC_6	ADC_5	ADC_4	ADC_3	ADC_2	ADC_1	ADC_0
-	CR	R (ADC1), CR (ADC2)													

Address: 0b1000_0011

Description: ADC result single conversion module

When resistor measurement selected in SC_CONF:

Table 75. **SC_RESULT register bit description ([14:0] ADC_RESULT)**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:0]	ADC_RESULT= 2048*RPD/RRx in new data is available, 0x0000 otherwise ADC result is RPD/RRx represented with 4 bit integer part(bit[14:11]) and 11 bit fractional part(bit[10:0])	0	PORn RSTn

When voltage measurement selected in SC_CONF:

Table 76. **SC_RESULT register bit description ([14] NEW_RESULT_FLAG)**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14]	NEW_RESULT_FLAG New result flag (clear on read)	0	PORn RSTn
[13:12]	RESERVED	00	PORn RSTn
[11:0]	ADC_RESULT	0000-0000-0000	PORn RSTn

16.24 SQNCR_CMD_[1:15]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	RESERVED								NXT_PC_3	NXT_PC_2	NXT_PC_1	NXT_PC_0	PUP1_DIV_1	PUP0_DIV_0	R_VOLT_MEAS_SELECT
-									RW	RW	RW	RW	RW	RW	RW

Address: 0b1100_0001 up to 0b1100_1111

Description: Sequencer configuration table register channel 1 to 15

Table 77. **SQNCR_CMD_[1:15] register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:7]	RESERVED	0000_0000	PORn
[6:3]	NXT_PC[3:0] Next configuration table address to read 0000: ENDLOOP 0001: point to SQNCR_CMD_1 (IO1) 0010: point to SQNCR_CMD_2 (IO2) …. 1100: point to SQNCR_CMD_12 (IO12) 1101: point to SQNCR_CMD_13 (UBSW) 1110: point to SQNCR_CMD_14 (VI5V) 1111: point to SQNCR_CMD_15 (VIX)	0000	PORn RSTn
[2:1]	PUP_DIV Pull-up selection (when ADC Resistance selected), division factor (ADC Voltage selected, except for UBSW, VI5V, VIX) 00: no pullup, full range = 5 V 01: pullup RR1, full range = 20 V 10: pullup RR2, full range = 40 V 11: pullup RR3, full range = 1.25 V	00	PORn RSTn
Bit 0	R_VOLT_MEAS_SELECT 0: Resistance measurement (ADC2) 1: Voltage measurement (ADC1)	0	PORn RSTn

16.25 SQNCR_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	EU2_SYNC_EN	RESERVED	INIT_PC_EU2_3	INIT_PC_EU2_2	INIT_PC_EU2_1	INIT_PC_EU2_0	EU2_EN	SYNC_CMD_EN	EU1_SYNC_EN	RESERVED	INIT_PC_EU1_3	INIT_PC_EU1_2	INIT_PC_EU1_1	INIT_PC_EU1_0	EU1_EN
-	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: 0b1101_0000

Description: Sequencer control register

Table 78. **SQNCR_CTRL register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14]	EU2_SYNC_EN 1 EU2 started by SYNC toggle 0 EU2 not started by SYNC toggle	0	PORn RSTn
[13]	RESERVED	0	PORn
[12:9]	INIT_PC_EU2 Starting address for EU2 0000 not valid as sequencer start 0001: start pointing to SQCNR_CMD1 ….. 1111: start pointing to SQNCR_CMD15	0000	PORn RSTn
[8]	EU2_EN 1 EU2 started by SPI cmd 0 EU2 not started by SPI cmd	0	PORn RSTn
[7]	SYNC_COPY_CMD_EN 0: SYNC does not trigger result buffer copy operation 1: SYNC triggers result buffer copy operation	1	PORn
[6]	EU1_SYNC_EN 1 EU1 started by SYNC toggle 0 EU1 not started by SYNC toggle	1	PORn RSTn
[5]	RESERVED	0	PORn
[4:1]	INIT_PC_EU1 Starting address for EU1 0000 not valid as sequencer start 0001: start pointing to SQCNR_CMD1 …..	0000	PORn RSTn

Range	Field name/description	Reset Value	Reset Event
	1111: start pointing to SQNCR_CMD15		
[0]	EU1_EN 1 EU1 started by SPI cmd 0 EU1 not started by SPI cmd	0	PORn RSTn

16.26 SQNCR_RSLT_COPY_CMD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	SQNCR_RSLT_COPY_CMD_14	SQNCR_RSLT_COPY_CMD_13	SQNCR_RSLT_COPY_CMD_12	SQNCR_RSLT_COPY_CMD_11	SQNCR_RSLT_COPY_CMD_10	SQNCR_RSLT_COPY_CMD_9	SQNCR_RSLT_COPY_CMD_8	SQNCR_RSLT_COPY_CMD_7	SQNCR_RSLT_COPY_CMD_6	SQNCR_RSLT_COPY_CMD_5	SQNCR_RSLT_COPY_CMD_4	SQNCR_RSLT_COPY_CMD_3	SQNCR_RSLT_COPY_CMD_2	SQNCR_RSLT_COPY_CMD_1	SQNCR_RSLT_COPY_CMD_0
-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 0b1101_1111

Description: Sequencer result register copy CMD 14-0

Table 79. **SQNCR_RSLT_COPY_CMD register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:0]	Read operation on this register triggers the copy of the internal sequencer result buffer into SQNCR_RESULT_x	000000000000000	PORn

16.27 DIG_IN_STAT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	DIG_IN 15/NEW_RSLT_FLG	DIG_IN 14	DIG_IN 13	DIG_IN 12	DIG_IN 11	DIG_IN 10	DIG_IN 9	DIG_IN 8	DIG_IN 7	DIG_IN 6	DIG_IN 5	DIG_IN 4	DIG_IN 3	DIG_IN 2	DIG_IN 1
-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 0b1110_0000

Description: Channel output digital value

Table 80. **DIG_IN_STAT register bit description**

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:0]	bit[x] reports the status of the comparator configured for IOx	000000000000000	PORn

16.28 SQNCR_RESULT_[1:15]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity	ADC_14/NEW_RSLT_FLG	ADC_13	ADC_12	ADC_11	ADC_10	ADC_9	ADC_8	ADC_7	ADC_6	ADC_5	ADC_4	ADC_3	ADC_2	ADC_1	ADC_0
-	CR	R (ADC1), CR (ADC2)													

Address: 1110_0001 up to 1110_1111

Description: Sequencer Result Register [1:15]

When **resistor** measurement selected in SQNCR_CMD_x:

Table 81. SQNCR_RESULT_[1:15] register bit description ([14:0] ADC_RESULT

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14:0]	ADC_RESULT= 2048*RPD/RRx in new data is available, 0x0000 otherwise ADC result is RPD/RRx represented with 4 bit integer part(bit[14:11]) and 11 bit fractional part(bit[10:0])	000000000000000	PORn RSTn

When **voltage** measurement selected in SQNCR_CMD_x:

Table 82. SQNCR_RESULT_[1:15] register bit description ([14] NEW_RESULT_FLAG

Range	Field name/description	Reset Value	Reset Event
[15]	Parity	Default	
[14]	NEW_RESULT_FLAG New result flag (clear on read)	0	PORn RSTn
[13:12]	Reserved	00	PORn RSTn
[11:0]	ADC_RESULT	000000000000	PORn RSTn

17 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

17.1 TQFP48 (7x7x1 mm exp. pad down 5.0x5.0) package information

Figure 43. TQFP48 (7x7x1 mm exp. pad down 5.0x5.0) package outline

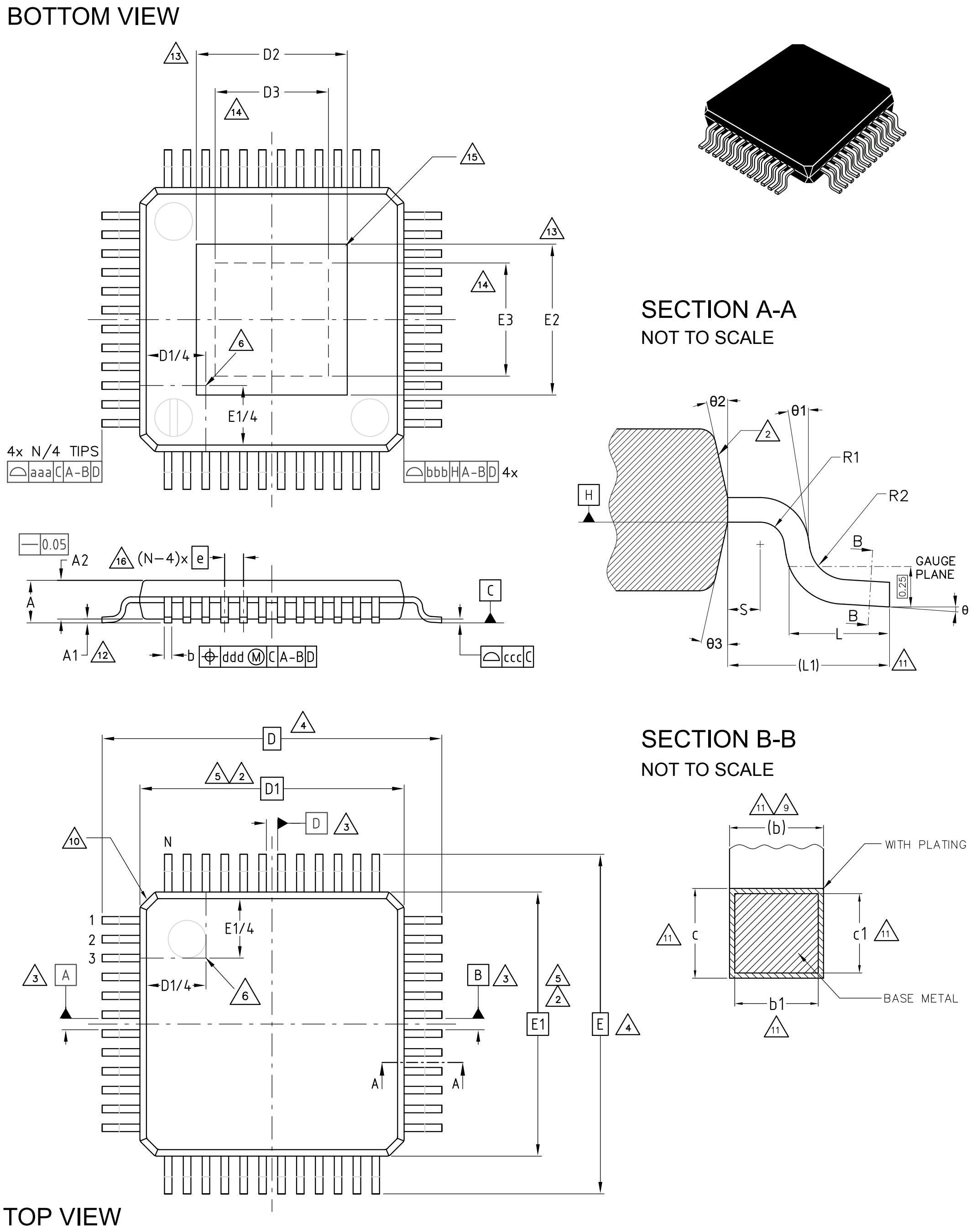


Table 83. **TQFP48 (7x7x1 mm exp. pad down 5.0x5.0) package mechanical data**

Symbol	Dimensions			Note
	Min.	Typ.	Max.	
Θ	0°	3.5°	7°	
Θ1	0°	-	-	
Θ2	10°	12°	14°	
Θ3	10°	12°	14°	
A	-	-	1.20	15
A1	0.05	-	0.15	12
A2	0.95	1.00	1.05	15
b	0.17	0.22	0.27	9, 11
b1	0.17	0.20	0.23	11
c	0.09	-	0.20	11
c1	0.09	-	0.16	11
D	9.00 BSC			4
D1	7.00 BSC			2, 5
D2	-	-	4.47	13
D3	2.50	-	-	14
e	0.50 BSC			
E	9.00 BSC			4
E1	7.00 BSC			2, 5
E2	-	-	4.47	13
E3	2.50	-	-	14
L	0.45	0.60	0.75	
L1	1.00 REF			
N	48			16
R1	0.08	-	-	
R2	0.08	-	0.20	
S	0.20	-	-	
Tolerance of form and position				
aaa	0.20			1, 7, 20
bbb	0.20			
ccc	0.08			
ddd	0.08			

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datum A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.

8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. End user should verify D2 and E2 dimensions according to specific device application.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the number of terminal positions for the specified body size.
17. For Tolerance of Form and Position see Table 83.
18. Critical dimensions:
    18.1 Stand-Off
    18.2 Overall Width
    18.3 Lead Coplanarity
19. ST component cross reference: DM00516738.
20. For Symbols, Recommended Values and Tolerances see table below:

Table 84. Symbols, Recommended Values and Tolerances

SYMBOL	DEFINITION	NOTES
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	-
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly known as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by “b”.

Revision history

Table 85. **Document revision history**

Date	Version	Changes
06-Jul-2018	1	Initial release.
20-Jul-2018	2	Updated *Table 11. Saturation voltages*. Registers *CURR_SRC_CTRL_[1:4]*, *CURR_SRC_CTRL_[5:8]*, *CURR_SRC_CTRL_[9:12]* and *CURR_SRC_CTRL_[13:15]* Range [3:1] added condition (CS=1) to binary value 011.
03-Dec-2018	3	Updated: *Table 14. Pull up current value*; For "ADC1range_1_25" and "ADC1range_40" parameters, corrected pin name in *Table 22. ADC1 parameters*; For "RMEASacc_L (1.5% max.)", "RMEASacc_L (10% max.)" "RMEASsettl time (50 μs max.)" updated condition in *Table 23. ADC2 parameters*.
05-Feb-2019	4	Added *Section 5.5 Temperature ranges and thermal data*.
21-Oct-2019	5	Updated *Table 41. Signal routed on AOX*. Minor text changes.
08-Mar-2021	6	Updated: • *Section 16.3 HW_REV* (address register); • *Section 16.27 DIG_IN_STAT* (bitfield name).
10-May-2022	7	Updated *Section 17.1 TQFP48 (7x7x1 mm exp. pad down 5.0x5.0) package information*.
22-Jun-2022	8	Updated: • *Figure 32. VRS interface block diagram*; • *Figure 33. VRS block diagram - Normal operating mode*; • *Figure 35. VRS_A fully adaptive hysteresis*; • *Figure 38. VRS block diagram - Diagnostic operating mode - Current path*.
04-Aug-2022	9	Updated Table 83. TQFP48 (7x7x1 mm exp. pad down 5.0x5.0) package mechanical data.
08-Sep-2022	10	Document classification changed from Restricted to public.

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