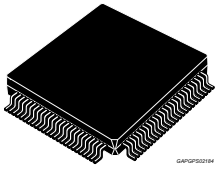
L9679P

Automotive advanced airbag IC for mid/high end applications

Datasheet - production data



TQFP100 exposed pad down (14x14x1.0mm)

Features

- AEC-Q100 qualified
- Boost regulator for energy reserve
  - 1.882 MHz operation, I_{load} = 55 mA max
  - Output voltage user selectable, 23 V/ 33 V ±5%
  - Capacitor value & ESR diagnostics
- Boost regulator for PSI-5 SYNC pulse
  - 1.882 MHz operation,
  - Output voltage, 12 V/14.75 V, user configurable
- Buck regulator for remote sensor
  - 1.882 MHz operation
  - Output voltage, 7.2 V/9 V ±4%, user configurable
- Buck regulator for micro controller unit
  - 1.882 MHz operation
  - Output voltage user selectable, 3.3 V or 5.0 V ±3%
- Integrated energy reserve crossover switch
  - 3 Ω - 912 mA max
  - Switch active output indicator
- Battery voltage monitor & shutdown control with Wake-up control
- System voltage diagnostics with integrated ADC
- Squib deployment drivers
  - 8 channel HSD/LSD
  - 25 V max deployment voltage
  - Various deployment profiles
  - Current monitoring
  - $R_{measure}$, STB, STG & Leakage diagnostics
  - High & low side driver FET tests
- High side safing switch regulator and enable control
- Two channel remote sensor interface
  - PSI-5 satellite sensors
- Three channel GPO, HSD or LSD configurable, with PWM 0-100% control
- Nine channel hall-effect, resistive or switch sensor interface
- User customizable safing logic
- Specific disarm signal for passenger airbag
- Temporal and algorithmic Watchdog timers
- End of life disposal interface
- Temperature sensor
- 32 bit SPI communications
- 5.5 V minimum operating voltage at device battery pin
- Operating temperature, -40 to 95 °C
- Packaging - 100 pin

Table 1. Device summary

Order code	Package	Pacing
L9679P	TQFP100	Tray
L9679PTR		Tape & Reel

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1 Description

The L9679P is an advanced airbag system chip solution targeted for mature airbag market and integrated safety markets. This device is family compatible with the L9678 and L9680 devices. Safety system integration is enabled through higher power supply currents and integrated PSI-5 satellite interface.

High frequency power supply design allows further cost reduction by using smaller and less expensive external components. All switching regulators operate at 1.882 MHz while buck converters have integrated synchronous rectifiers.

Additional attention is given to system integrity and diagnostics. The reserve capacitor is electrically isolated from the boost regulator by a 50 mA nominal fixed current source, controlling in-rush an additional capacitor discharge fixed current source is integrated to diagnose the reserve capacitor value and ESR. The same current sources can be used to discharge the capacitor at shutdown.

Thanks to low quiescent current, the device can be directly connected to battery. In this way, the device start-up and shutdown are controlled through the wake-up input function. The power supply and crossover function are controlled automatically through the internal state machine.

The user can select both ECU logic voltage (V_{CC} at 3.3 V or 5.0 V) and energy reserve output voltage (at either 23 V or 33 V). Deployment voltage is set to a maximum of 25 V for all profiles and can be controlled through external safing switch circuit using the high side safing switch reference enabled through the system SPI interface or the arming logic.

2 Absolute maximum ratings

This part may be irreparably damaged if taken outside the specified absolute maximum ratings. Operation above the absolute maximum ratings may also cause a decrease in reliability.

The operating junction temperature range is -40 °C to +150 °C. The maximum junction temperature must not be exceeded except when in deployment and within the deploy power stages. Deployment is possible starting with a junction temperature of 150 °C. A power dissipation calculation has to be performed for the final application limiting the available functionality to a subset of it in order to respect to the power dissipation capability.

Table 2. Absolute maximum ratings

Pin#	Pin name	Pin function	Min	Max	Unit
1	CS_RS	Remote SPI interface chip select	-0.3	VCC+0.3 ≤ 6.5	V
2	SCLK_RS	Remote SPI interface clock	-0.3	VCC+0.3 ≤ 6.5	V
3	MOSI_RS	Remote SPI interface data in	-0.3	VCC+0.3 ≤ 6.5	V
4	MISO_RS	Remote SPI interface data out	-0.3	VCC+0.3 ≤ 6.5	V
5	RESET	Reset output	-0.3	VCC+0.3 ≤ 6.5	V
6	MISO_G	Global SPI interface data out	-0.3	VCC+0.3 ≤ 6.5	V
7	MOSI_G	Global SPI interface data in	-0.3	VCC+0.3 ≤ 6.5	V
8	SCLK_G	Global SPI interface clock	-0.3	VCC+0.3 ≤ 6.5	V
9	CS_G	Global SPI interface chip select	-0.3	VCC+0.3 ≤ 6.5	V
10	WDT/TM	Watchdog disable	-0.3	20	V
11	SR4	Squib 4 low-side pin	-0.3	35	V
12	SF4	Squib 4 high-side pin	-1.0	40	V
13	SS45	Squib 4 & 5 deployment supply pin	-0.3	40	V
14	SF5	Squib 5 high-side pin	-1.0	40	V
15	SR5	Squib 5 low-side pin	-0.3	35	V
16	SR0	Squib 0 low-side pin	-0.3	35	V
17	SF0	Squib 0 high-side pin	-1.0	40	V
18	SS01	Squib 0 & 1 deployment supply pin	-0.3	40	V
19	SF1	Squib 1 high-side pin	-1.0	40	V
20	SR1	Squib 1 low-side pin	-0.3	35	V
21	NC	Not connected			
22	NC	Not connected			
23	NC	Not connected			
24	NC	Not connected			
25	NC	Not connected			
26	DCS8	DC Sensor interface channel 8	-2	40	V

Table 2. Absolute maximum ratings (continued)

Pin#	Pin name	Pin function	Min	Max	Unit
27	DCS7	DC Sensor interface channel 7	-2	40	V
28	DCS6	DC Sensor interface channel 6	-2	40	V
29	DCS5	DC Sensor interface channel 5	-2	40	V
30	DCS4	DC Sensor interface channel 4	-2	40	V
31	DCS3	DC Sensor interface channel 3	-2	40	V
32	DCS2	DC Sensor interface channel 2	-2	40	V
33	DCS1	DC Sensor interface channel 1	-2	40	V
34	DCS0	DC Sensor interface channel 0	-2	40	V
35	RSU0	PSI-5/WSS ch. 0 remote sensor output	-1	40	V
36	RSU1	PSI-5/WSS ch. 1 remote sensor output	-1	40	V
37	NC	Not connected			
38	NC	Not connected			
39	GPOD0	GPO driver 0 drain output pin	-1	40	V
40	GPOS0	GPO driver 0 source output pin	-1	40	V
41	GPOS1	GPO driver 1 source output pin	-1	40	V
42	GPOD1	GPO driver 1 drain output pin	-1	40	V
43	GPOD2	GPO driver 2 drain output pin	-1	40	V
44	GPOS2	GPO driver 2 source output pin	-1	40	V
45	COVRACT	External Crossover Switch Driver	-0.3	40	V
46	ISOK	ISO9141 bus pin (K-LINE)	-18	40	V
47	NC	Not connected			
48	SATSYNC	Initiate Satellite Sensor Sync Pulse	-0.3	VCC+0.3 ≤ 6.5	V
49	PSINHB	Active Low Passenger Airbag Inhibit Control	-0.3	VCC+0.3 ≤ 6.5	V
50	GNDSUB1	Substrate ground / Squib ground	-0.3	0.3	V
51	NC	Not connected			
52	NC	Not connected			
53	NC	Not connected			
54	NC	Not connected			
55	NC	Not connected			
56	SR3	Squib 3 low-side pin	-0.3	35	V
57	SF3	Squib 3 high-side pin	-1.0	40	V
58	SS23	Squib 2 & 3 deployment supply pin	-0.3	40	V
59	SF2	Squib 2 high-side pin	-1.0	40	V
60	SR2	Squib 2 low-side pin	-0.3	35	V
61	SR7	Squib 7 low-side pin	-0.3	35	V

Table 2. Absolute maximum ratings (continued)

Pin#	Pin name	Pin function	Min	Max	Unit
62	SF7	Squib 7 high-side pin	-1.0	40	V
63	SS67	Squib 6 & 7 deployment supply pin	-0.3	40	V
64	SF6	Squib 6 high-side pin	-1.0	40	V
65	SR6	Squib 6 low-side pin	-0.3	35	V
66	GNDA	Analog ground	-0.3	0.3	V
67	SAF_CS0	SPI interface safing sensor chip select 0	-0.3	VCC+0.3 ≤ 6.5	V
68	SAF_CS1	SPI interface safing sensor chip select 1	-0.3	VCC+0.3 ≤ 6.5	V
69	SAF_CS2	SPI interface safing sensor chip select 2	-0.3	VCC+0.3 ≤ 6.5	V
70	ISOTX	ISO9141 transmit pin	-0.3	VCC+0.3 ≤ 6.5	V
71	WD2_LockOut	WD2 fault output	-0.3	VCC+0.3 ≤ 6.5	V
72	NC	Not connected			
73	ISORX	ISO9141 receiver pin	-0.3	VCC+0.3 ≤ 6.5	V
74	WS1	Wheel speed output Ch1	-0.3	VCC+0.3 ≤ 6.5	V
75	WS0	Wheel speed output Ch0	-0.3	VCC+0.3 ≤ 6.5	V
76	VCCSEL	VCC select	-0.3	40	V
77	ACL	EOL disposal control input	-0.3	40	V
78	WAKEUP	Wake-up control input	-0.3	40	V
79	VBATMON	Battery line voltage monitor	-18(1)	40	V
80	VSF	Safing regulator supply output	-0.3	40	V
81	VIN	Battery connection	-0.3	40	V
82	VER	Reserve voltage	-0.3	40	V
83	ERBOOST	Energy reserve regulator output	-0.3	40	V
84	ERBSTSW	ER Boost switching output	-0.3	40	V
85	BSTGND	Boost regulators ground	-0.3	0.3	V
86	SYNCBSTSW	SYNC Boost switching output	-0.3	40	V
87	SYNCBOOST	SYNC boost output voltage	-0.3	40	V
88	SATBCKSW	SAT Buck switching output	-0.3	40	V
89	SATGND	SAT Buck regulator ground	-0.3	0.3	V
90	SATBUCK	SAT Buck output voltage	-0.3	40	-
91	VCCBCKSW	VCC Buck switch output	-0.3	40	V
92	VCCGND	VCC Buck Ground	-0.3	0.3	V
93	CVDD	Internal 3.3V regulator output	-0.3	4.6	V
94	GNDD	Digital ground	-0.3	0.3	-
95	VCC	VCC Buck voltage	-0.3	6.5	V
96	ARM1	Arming output 1	-0.3	VCC+0.3 ≤ 6.5	V

Table 2. Absolute maximum ratings (continued)

Pin#	Pin name	Pin function	Min	Max	Unit
97	ARM2	Arming output 2	-0.3	VCC+0.3 ≤ 6.5	V
98	NC	Not connected			
99	FENL	LS driver FET control input	-0.3	VCC+0.3 ≤ 6.5	V
100	GNDSUB2	Substrate ground / Squib ground	-0.3	0.3	V
-	Exposed pad down	Substrate ground / Squib ground	-0.3	0.3	V

1. VBATMON negative AMR is -18 V or -20 mA.

3 Operative maximum ratings

Within the operating ratings the part operates as specified and without parameter deviations. Once taken beyond the operative ratings and returned back within, the part will recover with no damage or degradation.

Additional supply voltage and temperature conditions are given separately at the beginning of each specification table.

Table 3. Operative maximum ratings

Pin #	Pin name	Pin function	Min	Max	Unit
1	CS_RS	Remote SPI interface chip select	-0.1	VCC+0.1 ≤ 5.5	V
2	SCLK_RS	Remote SPI interface clock	-0.1	VCC+0.1 ≤ 5.5	V
3	MOSI_RS	Remote SPI interface data in	-0.1	VCC+0.1 ≤ 5.5	V
4	MISO_RS	Remote SPI interface data out	-0.1	VCC+0.1 ≤ 5.5	V
5	RESET	Reset output	-0.1	VCC+0.1 ≤ 5.5	V
6	MISO_G	Global SPI interface data out	-0.1	VCC+0.1 ≤ 5.5	V
7	MOSI_G	Global SPI interface data in	-0.1	VCC+0.1 ≤ 5.5	V
8	SCLK_G	Global SPI interface clock	-0.1	VCC+0.1 ≤ 5.5	V
9	CS_G	Global SPI interface chip select	-0.1	VCC+0.1 ≤ 5.5	V
10	WDT/TM	Watchdog disable	-0.1	15	V
11	SR4	Squib 4 low-side pin	-0.1	SS45	V
12	SF4	Squib 4 high-side pin	-1.0	SS45	V
13	SS45	Squib 4 & 5 deployment supply pin	-0.1	VER	V
14	SF5	Squib 5 high-side pin	-1.0	SS45	V
15	SR5	Squib 5 low-side pin	-0.1	SS45	V
16	SR0	Squib 0 low-side pin	-0.1	SS01	V
17	SF0	Squib 0 high-side pin	-1.0	SS01	V
18	SS01	Squib 0 & 1 deployment supply pin	-0.1	VER	V
19	SF1	Squib 1 high-side pin	-1.0	SS01	V
20	SR1	Squib 1 low-side pin	-0.1	SS01	V
21	NC	Not connected			
22	NC	Not connected			
23	NC	Not connected			
24	NC	Not connected			
25	NC	Not connected			
26	DCS8	DC sensor interface channel 8	-1	18	V
27	DCS7	DC sensor interface channel 7	-1	18	V

Table 3. Operative maximum ratings (continued)

Pin #	Pin name	Pin function	Min	Max	Unit
28	DCS6	DC sensor interface channel 6	-1	18	V
29	DCS5	DC sensor interface channel 5	-1	18	V
30	DCS4	DC sensor interface channel 4	-1	18	V
31	DCS3	DC sensor interface channel 3	-1	18	V
32	DCS2	DC sensor interface channel 2	-1	18	V
33	DCS1	DC sensor interface channel 1	-1	18	V
34	DCS0	DC Sensor interface channel 0	-1	18	V
35	RSU0	PSI-5/WSS ch. 0 remote sensor output	-1	$V_{RSU\_SYNC\_MAX}$	V
36	RSU1	PSI-5/WSS ch. 1 remote sensor output	-1	$V_{RSU\_SYNC\_MAX}$	V
37	NC	Not connected			
38	NC	Not connected			
39	GPOD0	GPO driver 0 drain output pin	-0.1	40	V
40	GPOS0	GPO driver 0 source output pin	-1	40	V
41	GPOS1	GPO driver 1 source output pin	-1	40	V
42	GPOD1	GPO driver 1 drain output pin	-0.1	40	V
43	GPOD2	GPO driver 2 drain output pin	-0.1	40	V
44	GPOS2	GPO driver 2 source output pin	-1	40	V
45	COVRACT	External crossover switch driver	-0.1	40	V
46	ISOK	ISO9141 bus pin (K-LINE)	-0.1	VCC+0.1 ≤ 5.5	V
47	NC	Not connected			
48	SATSYNC	Initiate satellite sensor sync pulse	-0.1	VCC+0.1 ≤ 5.5	V
49	PSINHB	Active low passenger airbag inhibit control	-1	18	V
50	GNDSUB1	Substrate ground / Squib ground	-0.1	0.1	V
51	NC	Not connected			
52	NC	Not connected			
53	NC	Not connected			
54	NC	Not connected			
55	NC	Not connected			
56	SR3	Squib 3 low-side pin	-0.1	SS23	V
57	SF3	Squib 3 high-side pin	-1.0	SS23	V
58	SS23	Squib 2 & 3 deployment supply pin	-0.1	VER	V
59	SF2	Squib 2 high-side pin	-1.0	SS23	V
60	SR2	Squib 2 low-side pin	-0.1	SS23	V
61	SR7	Squib 7 low-side pin	-0.1	SS67	V

Table 3. Operative maximum ratings (continued)

Pin #	Pin name	Pin function	Min	Max	Unit
62	SF7	Squib 7 high-side pin	-1.0	SS67	V
63	SS67	Squib 6 & 7 deployment supply pin	-0.1	VER	V
64	SF6	Squib 6 high-side pin	-1.0	SS67	V
65	SR6	Squib 6 low-side pin	-0.1	SS67	V
66	GNDA	Analog ground	-0.1	0.1	V
67	SAF_CS0	SPI interface safing sensor chip select 0	-0.1	VCC+0.1 <= 5.5	V
68	SAF_CS1	SPI interface safing sensor chip select 1	-0.1	VCC+0.1 <= 5.5	V
69	SAF_CS2	SPI interface safing sensor chip select 2	-0.1	VCC+0.1 <= 5.5	V
70	ISOTX	ISO9141 transmit pin	-0.1	VCC+0.1 <= 5.5	V
71	WD2_LockOut	WD2 Fault Output	-0.1	VCC+0.1 <= 5.5	V
72	NC	Not connected			
73	ISORX	ISO9141 receiver pin	-0.1	VCC+0.1 <= 5.5	V
74	WS1	Wheel Speed Output Ch1	-0.1	VCC+0.1 <= 5.5	V
75	WS0	Wheel Speed Output Ch0	-0.1	VCC+0.1 <= 5.5	V
76	VCCSEL	VCC select	-0.1	35	V
77	ACL	EOL disposal control input	-0.1	35	V
78	WAKEUP	Wake-up control input	-0.1	VIN	V
79	VBATMON	Battery line voltage monitor	-1	18	V
80	VSF	Safing regulator supply output	-0.1	27	V
81	VIN	Battery connection	-0.1	35	V
82	VER	Reserve voltage	-0.1	35	V
83	ERBOOST	Energy reserve regulator output	-0.1	35	V
84	ERBSTSW	ER Boost switching output	-0.1	35	V
85	BSTGND	Boost regulators ground	-0.1	0.1	V
86	SYNCBSTSW	SYNC Boost switching output	-0.1	35	V
87	SYNCBOOST	SYNC boost output voltage	-0.1	35	V
88	SATBCKSW	SAT Buck switching output	-0.1	35	V
89	SATGND	SAT Buck regulator ground	-0.1	0.1	V
90	SATBUCK	SAT Buck output voltage	-0.1	10	-
91	VCCBCKSW	VCC Buck switch Output	-0.1	10	V
92	VCCGND	VCC Buck Ground	-0.1	0.1	V
93	CVDD	Internal 3.3V regulator output	-0.1	3.6	V
94	GNDD	Digital ground	-0.1	0.1	-
95	VCC	VCC Buck Voltage	-0.1	5.5	V

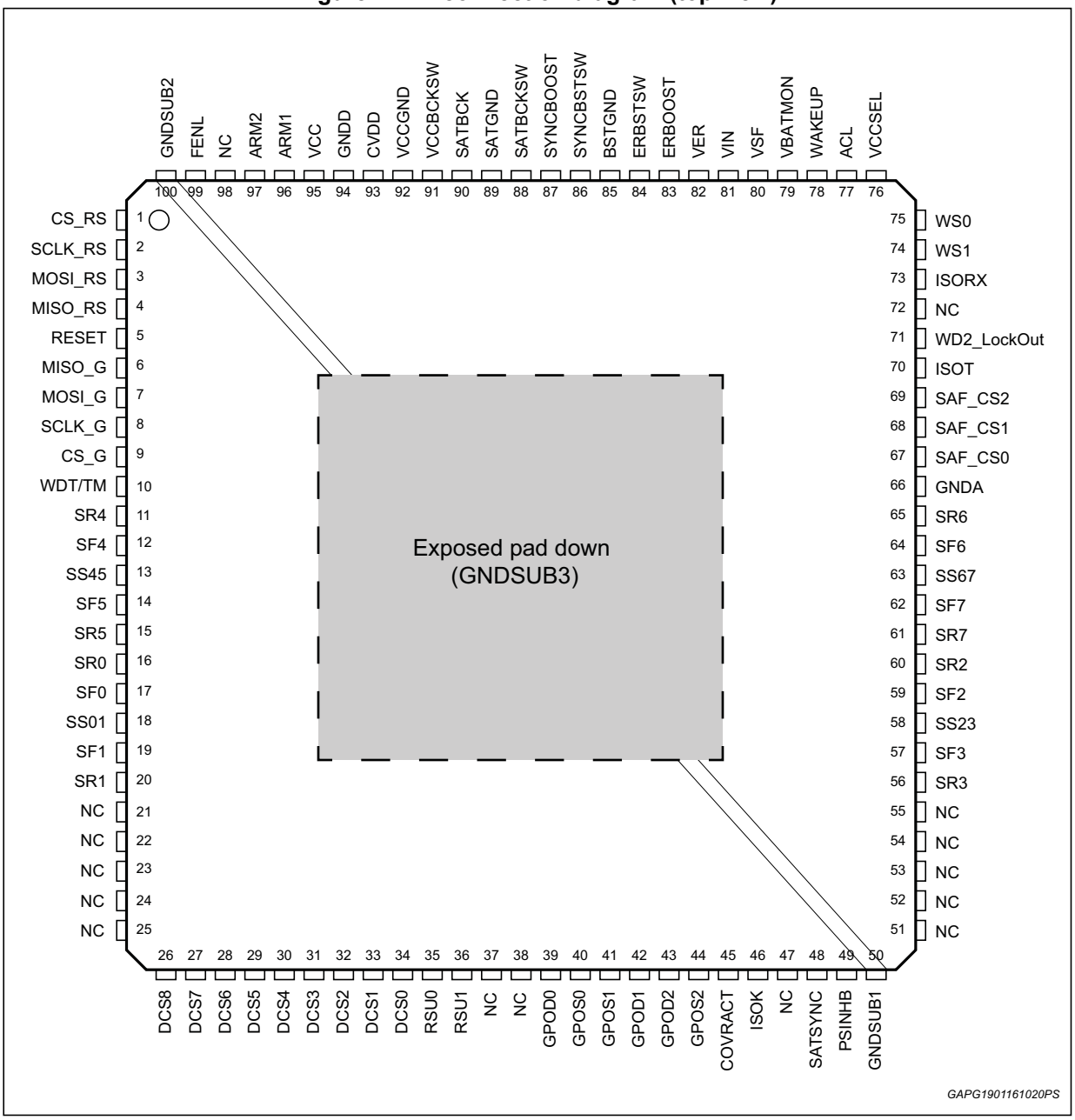
Table 3. Operative maximum ratings (continued)

Pin #	Pin name	Pin function	Min	Max	Unit
96	ARM1	Arming Output 1	-0.1	VCC+0.1 <= 5.5	V
97	ARM2	Arming Output 2	-0.1	VCC+0.1 <= 5.5	V
98	NC	Not connected			
99	FENL	LS Driver FET control input	-0.1	VCC+0.1 <= 5.5	V
100	GNDSUB2	Substrate ground / Squib ground	-0.1	0.1	V
-	Exposed Pad Down	Substrate ground / Squib ground	-0.1	0.1	V

4 Pin out

The L9679P pin out is shown below. The IC is housed in a 100 pin package (14 x 14 x 1.0mm) with a 7.6 x 7.6 mm exposed pad down.

Figure 1. Pin connection diagram (top view)

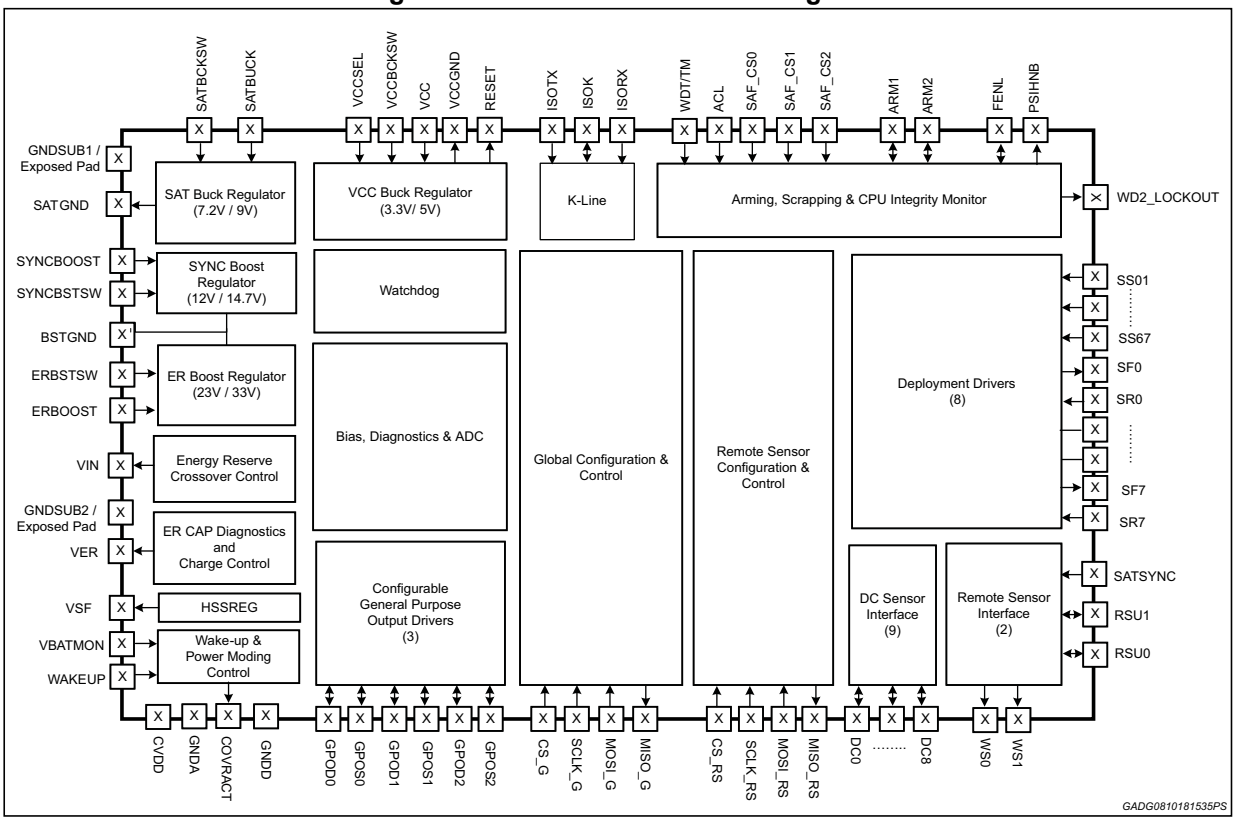


The exposed pad is electrically shorted to the substrate pins GNDSUB1 and GNDSUB2. These three connection nodes are to be kept shorted on the application.

5 Overview and block diagram

The L9679P IC is an application specific standard component air bag system chip. Its main functions include, power management, deployment drivers, remote sensor interfaces (PSI-5 satellite sensors, diagnostics, deployment arming, hall-effect sensor interface, general purpose output drivers, watchdog timer and a dedicated passenger airbag disarm signal. A block diagram for this IC is shown in *Figure 2*.

Figure 2. Device function block diagram



5.1 Power supply

- Integrated 1.882 MHz boost regulator, 33 V ± 5% or 23 V ± 5% nominal output
- Integrated 1.882 MHz boost regulator,12 V/14.75 V nominal output, user selectable via SPI command
- Integrated 1.882 MHz synchronous buck regulator, 7.2 V/9 V ± 4% nominal output, user selectable via SPI command
- Integrated 1.882 MHz synchronous buck regulator, 5 V ± 3% or 3.3 V ± 3% nominal output, user selectable via VCCSEL pin
- Over and under voltage detection and shutdown for all regulators
- Under-voltage lockout to guarantee buck regulator outputs disabled and discharged
- Integrated energy reserve capacitor fixed constant current source (50 mA, nominal) switch for controlled inrush and charge characteristics
- Integrated energy reserve diagnostics, capacitor value and ESR
- Integrated energy reserve crossover switch with current limit and battery input voltage monitoring
- Crossover switch ‘active’ output signal
- Integrated 25 V/20 V SPI selectable linear regulator for high side safing FET gate supply enabled via SPI or arming logic
- Reset output

5.2 Deployment drivers

- 8 high side deployment drivers, 8 low side deployment drivers
- User programmable deployment options
  - 1.20 A or 1.75 A minimum
  - programmable time in 0.1ms increments
- Capability to deploy a squib with a minimum current of 1.2 / 1.75 A and the SFx pin shorted to ground up to 25 V on SSxy
- Independently-controlled high-side and low-side FETs
- Squib resistance measurement
- Firing current monitor feature
- High and low side FET tests
- Open & shorts diagnostics, including between loop drivers
- Independent fire enable logic, SPI and discrete digital input

5.3 Remote sensor interfaces

- Two channel receiver
  - standard PSI-5 v1.3 compatible with sync pulse
- Current limit with short circuit protection diagnostics
- PSI-5 satellite sensor mode
  - Auto-adjusting current trip points for each satellite channel
  - Even parity, 8 or 10 bit messages, 125k or 189kbps
  - Satellite message error detection

5.4 DC sensor interfaces

- Nine integrated switch interfaces with current sense capability
- Compatible with Hall-effect, resistive and switch sensors
- Current limit protected
- System dedicated path to disable the passenger airbag with input from DC sensor interface

5.5 General purpose outputs

- Three configurable high-side or low-side drivers
- ON-OFF mode and PWM 0-100% fine control
- Diagnostics for short circuit protection and open load detection
- Current limit and reverse battery protected

5.6 Arming logic

- User configurable safing algorithms with 12 safing records
- Four digital sensor interfaces through SPI
- Independent user programmable thresholds
- Independent user programmable latch timers
- Two discrete and independent arming logic outputs
- Two discrete and independent internal arming signals
- End-of-life interface

5.7 Other features

- One dedicated 32-bit SPI bus for global configuration and control
- One dedicated 32-bit SPI bus for remote sensor configuration and control
- Integrated watchdog control with 2 independent structures: windowed WD and algorithmic WD
- Temperature sensor
- Independent thermal shutdown protection on the ER boost switch, the SYNC boost switch, the energy reserve crossover switch, the energy reserve charge paths, the remote sensor interfaces and the general purpose outputs
- All diagnostics are digital and are available through SPI communications
- Configurable logic operation, 5 V or 3.3 V

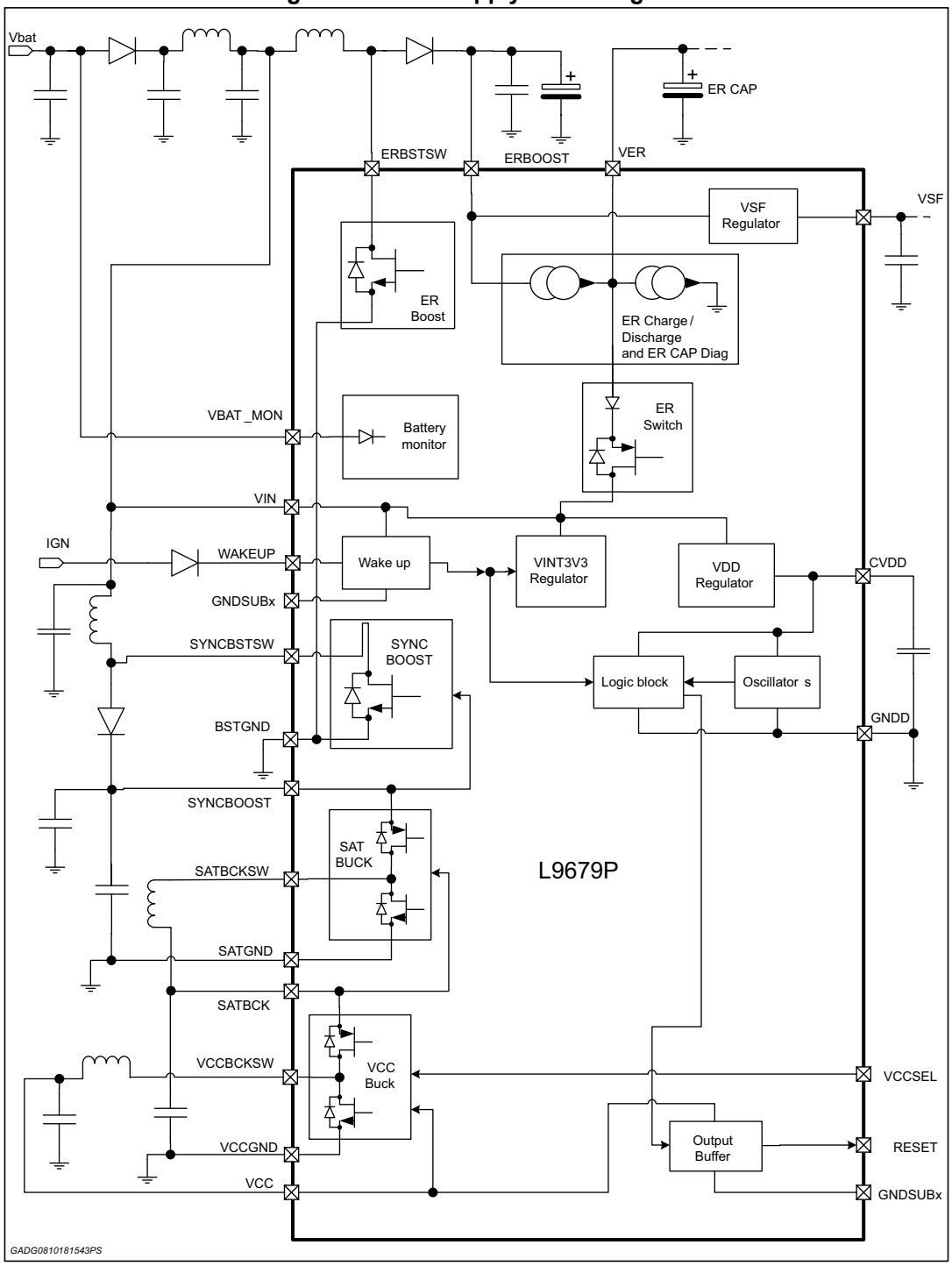
6 Start-up and power control

6.1 Power supply overview

The L9679P IC contains a complete power management system able to provide all necessary voltages for a high feature airbag system or integrated safety system. A general block diagram is shown in *Figure 3*. The power supply block contains the following features:

- Two 3.3 V internal regulators for operating internal logic (CVDD) and analog circuits (VINT3V3). An external CVDD pin is used to provide filtering capacitance to digital section supply rail.
- Energy reserve supply (ERBOOST) achieved through an integrated 1.882 MHz switching boost regulator. The energy reserve capacitor is charged using an internal constant current source controllable through SPI. Besides, a second current source is available to discharge the capacitor. The primary function for the second current source is to diagnose the integrity of the energy reserve capacitor, value and ESR. During system shutdown, the device can enable the discharge current source via SPI command to quickly dissipate the remaining energy stored in the energy reserve capacitor.
- Sync pulse supply (SYNCBOOST) is achieved through an integrated 1.882 MHz switching boost regulator. The SYNCBOOST regulator ensures a minimum voltage is available for operating the satellite sync signal and also provides the input voltage to the remote sensor buck regulator. The sync pulse boost regulator is disabled for battery voltage levels resulting in an output voltage above the set regulation point.
- The integrated current limited ER switch requires no external components. This switch is controlled through the integrated power control state machine and is enabled either once a loss of battery is detected or a shutdown command is received. Under the same conditions also the discrete digital pin COVRACT is activated allowing the control of an external optional cross-over switch.
- Two 1.882MHz synchronous buck regulators for remote sensor supply and VCC. The SATBUCK regulator, remote sensor buck supply, is sourced from the SYNCBOOST regulator and can be selected to be either 7.2 V or 9 V nominal. The VCC regulator is sourced from the SATBUCK regulator and is user selectable through the VCCSEL pin to either 5 V or 3.3 V nominal voltage.
- Battery voltage sense input comparator with hysteresis and wake-up input are the primary control signals for the power supply control state machine.
- Based on own mission profile and ECU total current consumption, the user must evaluate if the activation of fast slope option of each ERBoost, SyncBoost and SatBuck regulator (bit 8/9/10, $3F SW_REGS_CONF SPI register) is needed to increase the overall efficiency.

Figure 3. Power supply block diagram

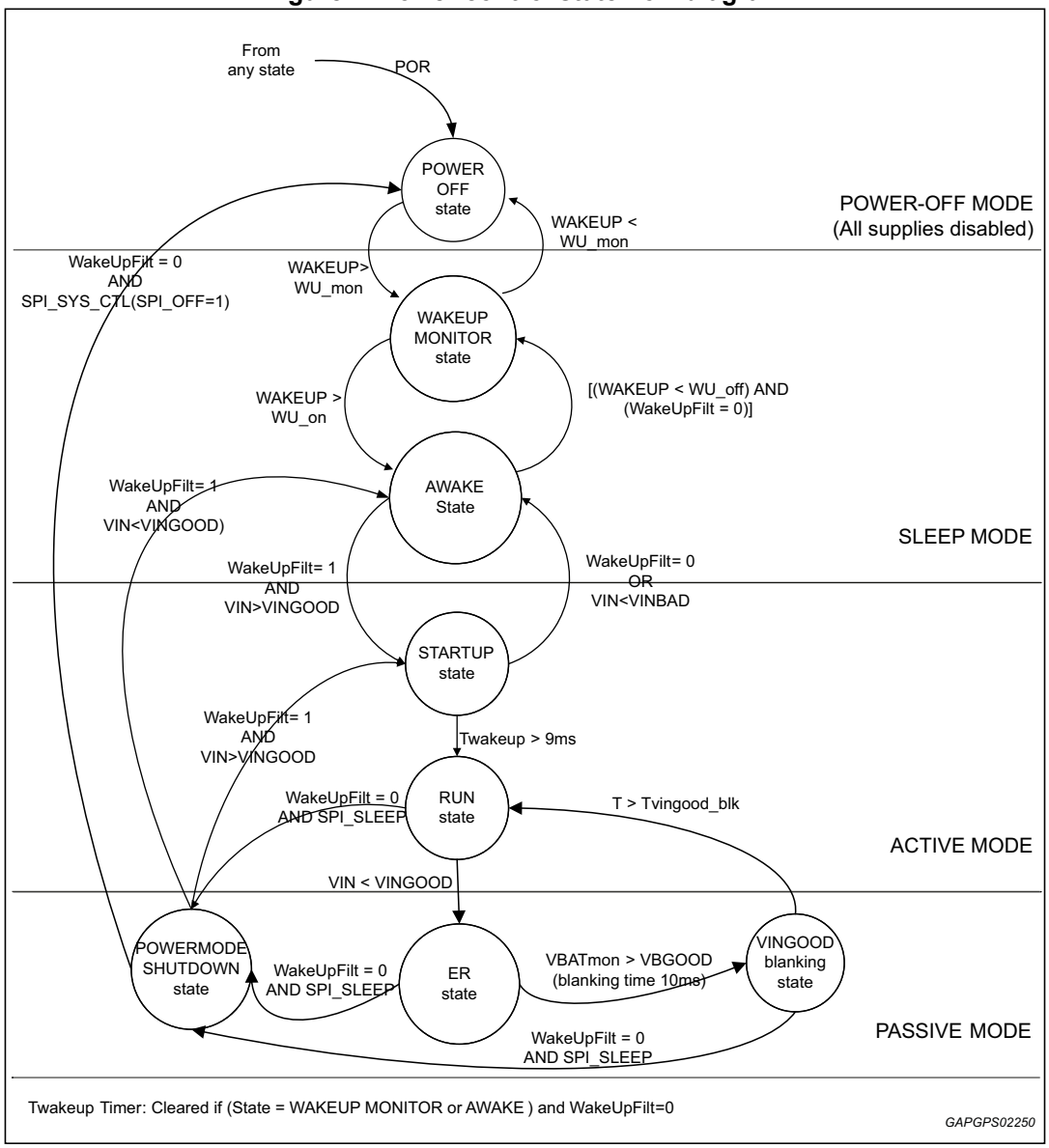


6.2 Power mode control

Start-up and power down of the L9679P are controlled by the WAKEUP pin, VBATMON pin, VIN pin, device status and the SPI interface. There are four main power modes: power-off, sleep, active and passive mode.

Each power mode is described below and represented in the state flow diagram shown in *Figure 4*. The descriptions include references to conditions and sometimes nominal values. The absolute values for each condition are listed in the electrical specifications section.

Figure 4. Power control state flow diagram



6.2.1 POWER OFF mode

During the POWER-OFF Mode all supplies are disabled keeping the system in a quiescent state with very low current draw from battery. As soon as WAKEUP>WU_mon the IC will move to SLEEP Mode.

6.2.2 SLEEP mode

During the Sleep mode the VINT3V3 and CVDD internal regulators are turned on and the IC is ready for full activation of all the other supplies. As soon as VIN voltage is over a minimum threshold, all the other supplies are turned on and the IC enters the ACTIVE mode.

6.2.3 ACTIVE mode

This is the normal operating mode for the system.

All power supplies are enabled and the energy reserve boost converter starts to increase the voltage at ERBOOST. Likewise, the SYNCBOOST boost converter continues to charge and regulate to a nominal 12 V (default level at startup). Once the SYNCBOOST has reached a good value, the SATBUCK regulator starts up. In turn, when SATBUCK has ramped up, VCC regulator is enabled. Once the VCC buck regulator is in regulation, RESET is released allowing the system microcontroller and other components to begin their power-on sequence. Among these, also the ER charge current generator can be enabled by the microcontroller via a dedicated SPI command.

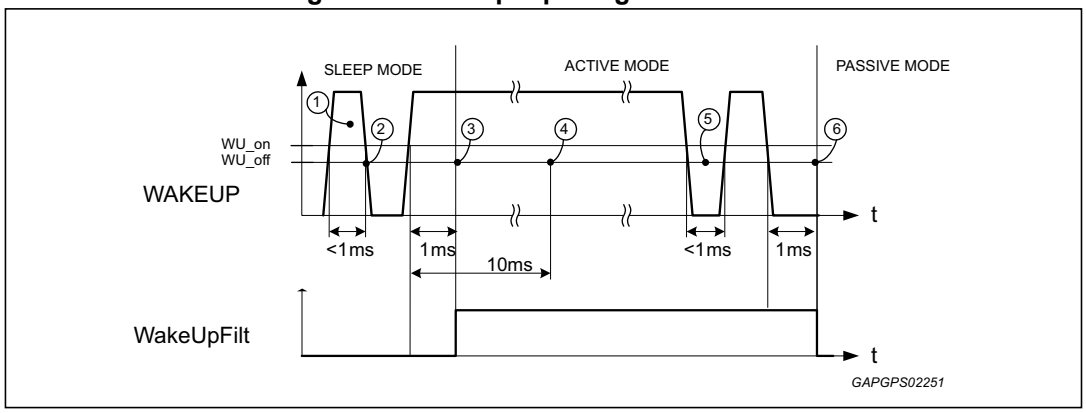
The active mode can be left when either WAKEUP pin or VIN voltage drop down. For the very first 9ms after having entered the active mode, the WAKEUP pin low would immediately cause the IC to switch back to sleep mode. After that time, WAKEUP pin low must be first confirmed by a µC SPI_SLEEP command prior to cause the system to switch to passive mode. Passive mode is also entered in case of VIN voltage low.

6.2.4 PASSIVE mode

In this state, the reserve capacitor charge current and the ERBOOST boost converter are disabled. When in passive mode the device activates both the COVRACT output pin and the integrated ER switch to allow VIN to be connected to the ER capacitor. In this time, VIN is supposed to be increased up to almost VER level and the system operation relies on energy from the ER capacitor. Two scenarios are possible: high or low battery. If VIN < VINGOOD, the device moved from RUN state in ACTIVE mode to the ER state. Here, the ER capacitor is depleted while supplying all the regulators until the POR on internal regulator occurs. The threshold to decide the ER switch activation is based on VIN, because VIN is the supply voltage rail for ERBOOST regulator. If the device has still a good battery level, it entered the POWERMODE SHUTDOWN thanks to a microcontroller command to switch off. In this case, the VER node will be discharged down to approximately VIN level, which then will be supplied out of the battery line. System will continue to run up to a dedicated SPI command to disable the SATBUCK regulator, which will lead the device to enter the POWEROFF state.

The wake-up pin is filtered to suppress undesired state changes resulting from transients or glitches. Typical conditions are shown in the chart below and summarized by state.

Figure 5. Wake-up input signal behaviour



Condition summary:

1. No change of sleep mode state but current consumption may exceed specification for sleep mode.
2. The sleep mode current returns to within specified limits.
3. Power supply exits sleep mode. Switchers start operating if applicable voltages exceed under voltage lockouts. As T_{wakeup} timeout is not elapsed, a low level at WAKEUP instantaneously sends the system back to sleep.
4. Sleep reset is released and the entire system starts operating. An SPI command to enter sleep state would not be executed.
5. No change in system status, an SPI command to turn off switchers would be ignored.
6. No change in system status, but an SPI command to turn off switchers would be accepted and turn the system off.

With the below table, all the functionalities of the device are shown with respect of the power states. When one function is flagged, the related circuitry cannot be activated on that state.

Table 4. Functions disabling by state

Functions	Power MODE							
	Power off	Sleep		Active		Passive		
	Power off	Wakeup monitor	Awake	Startup	Run	Power mode shutdown	ER	VINGOOD blanking
Wakeup detector	X							
Internal regulators	X	X						
ERBOOST regulator	X	X	X			X		
SYNCBOOST regulator	X	X	X					
ER CAP charge current	X	X	X			X	X	X
ER CAP discharge current	X	X	X				X	X
ER switch	X	X	X	X	X			
COVRACT	X	X	X	X	X			X

Table 4. Functions disabling by state (continued)

Functions	Power MODE							
	Power off	Sleep		Active		Passive		
	Power off	Wakeup monitor	Awake	Startup	Run	Power mode shutdown	ER	VINGOOD blanking
SATBUCK regulator	X	X	X					
VCC regulator	X	X	X					
Deployment Drivers	X	X	X					
VSF Safing FET regulator	X	X	X					
Remote Sensor Interfaces	X	X	X					
Watchdog	X	X	X					
Diagnostics	X	X	X					
DC Sensor Interface	X	X	X					
GPO drivers	X	X	X					
Safing Logic	X	X	X					

6.2.5 Power-up and power-down sequences

The behaviour of the IC during normal power-up and power-down is shown in *Figure 6* to *Figure 9*. The following sequences represent just a subset of all possible power-up and power-down scenarios. In *Figure 6* a normal IC power-up controlled by the state of the WAKEUP pin is shown.

Figure 6. Normal power-up sequence

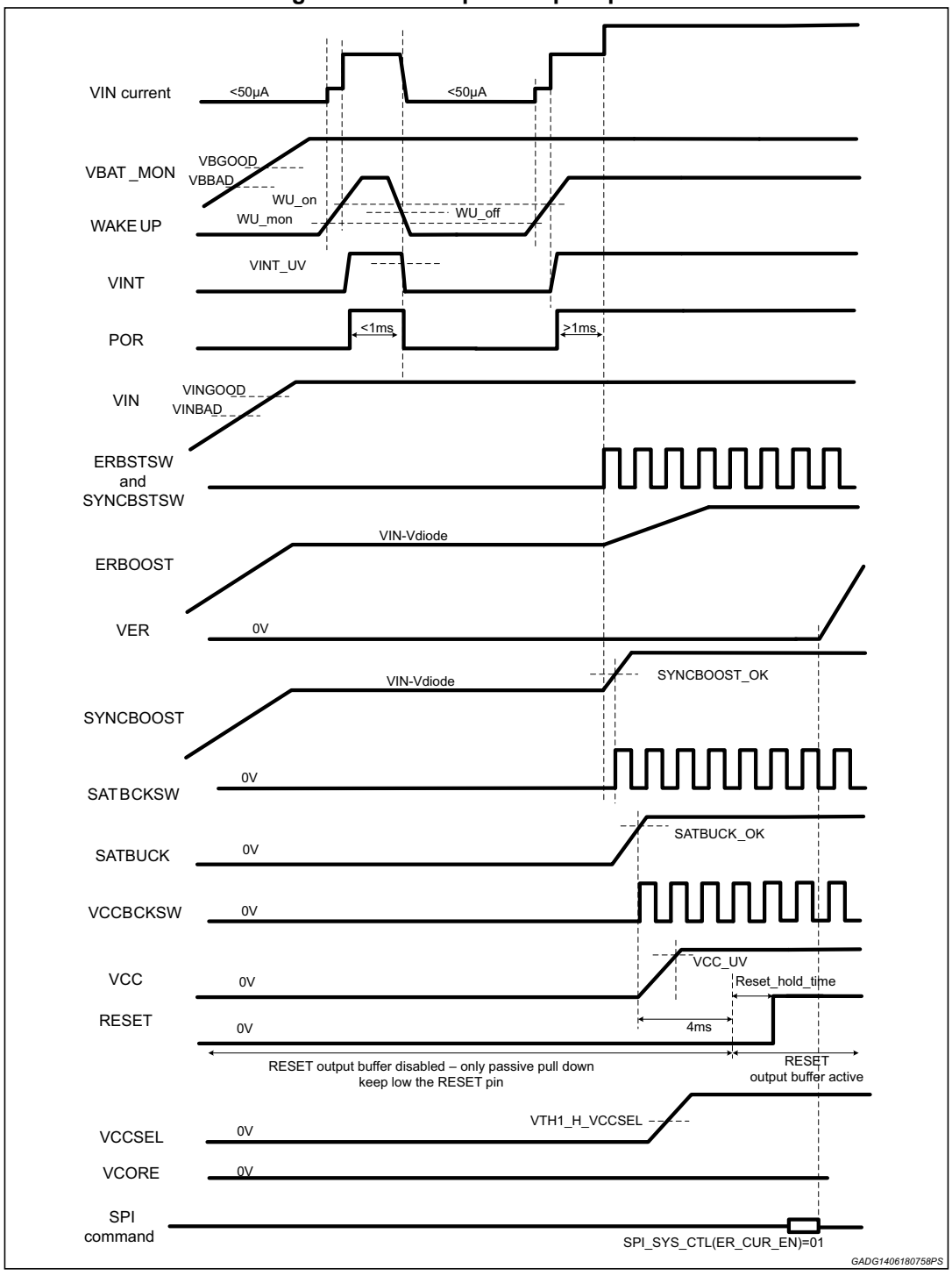


Figure 7. Normal power down sequence through POWERMODE SHUTDOWN state - no ER capactive discharge

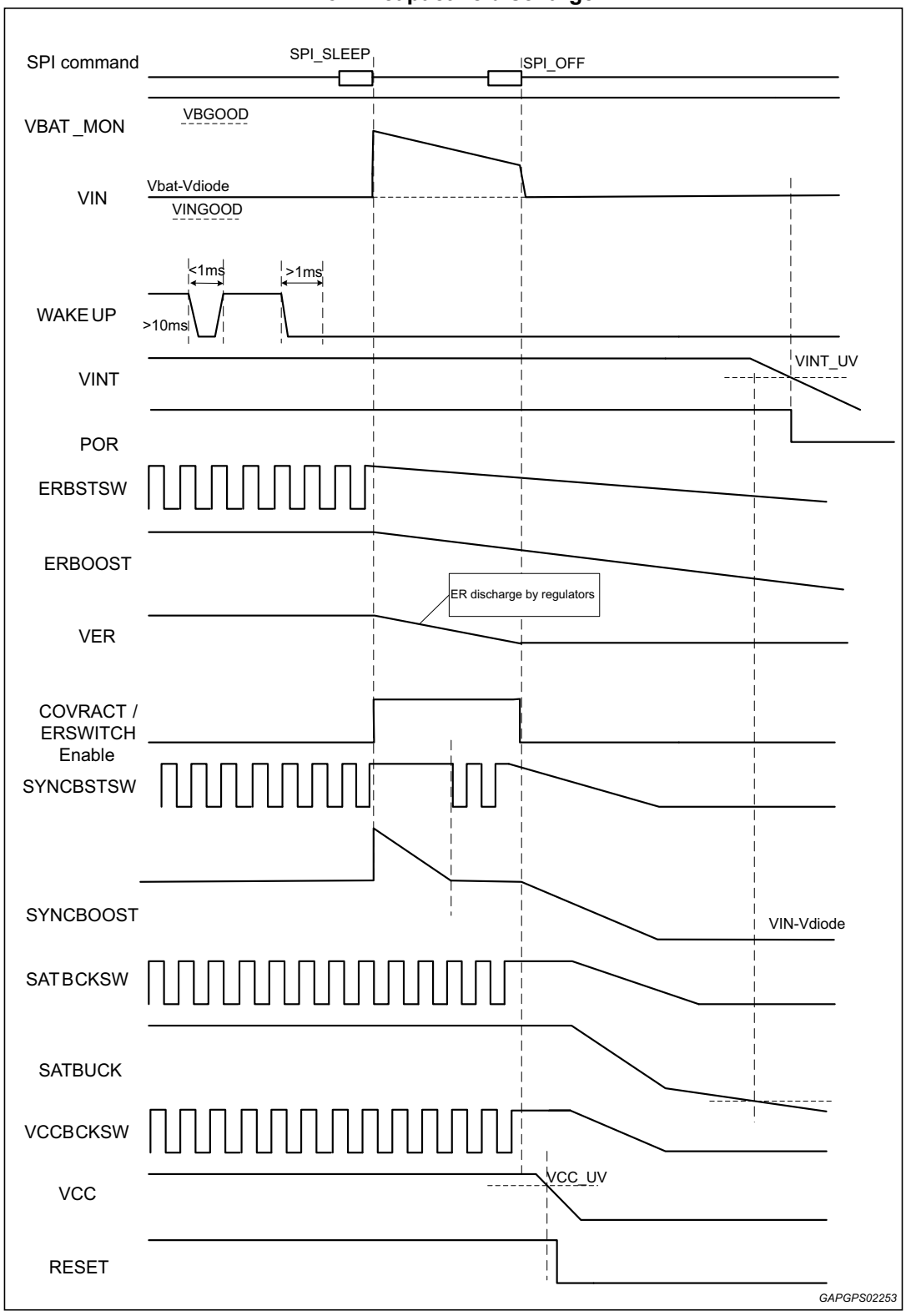


Figure 8. Normal power down sequence through Powermode Shutdown state - ER capactive discharge

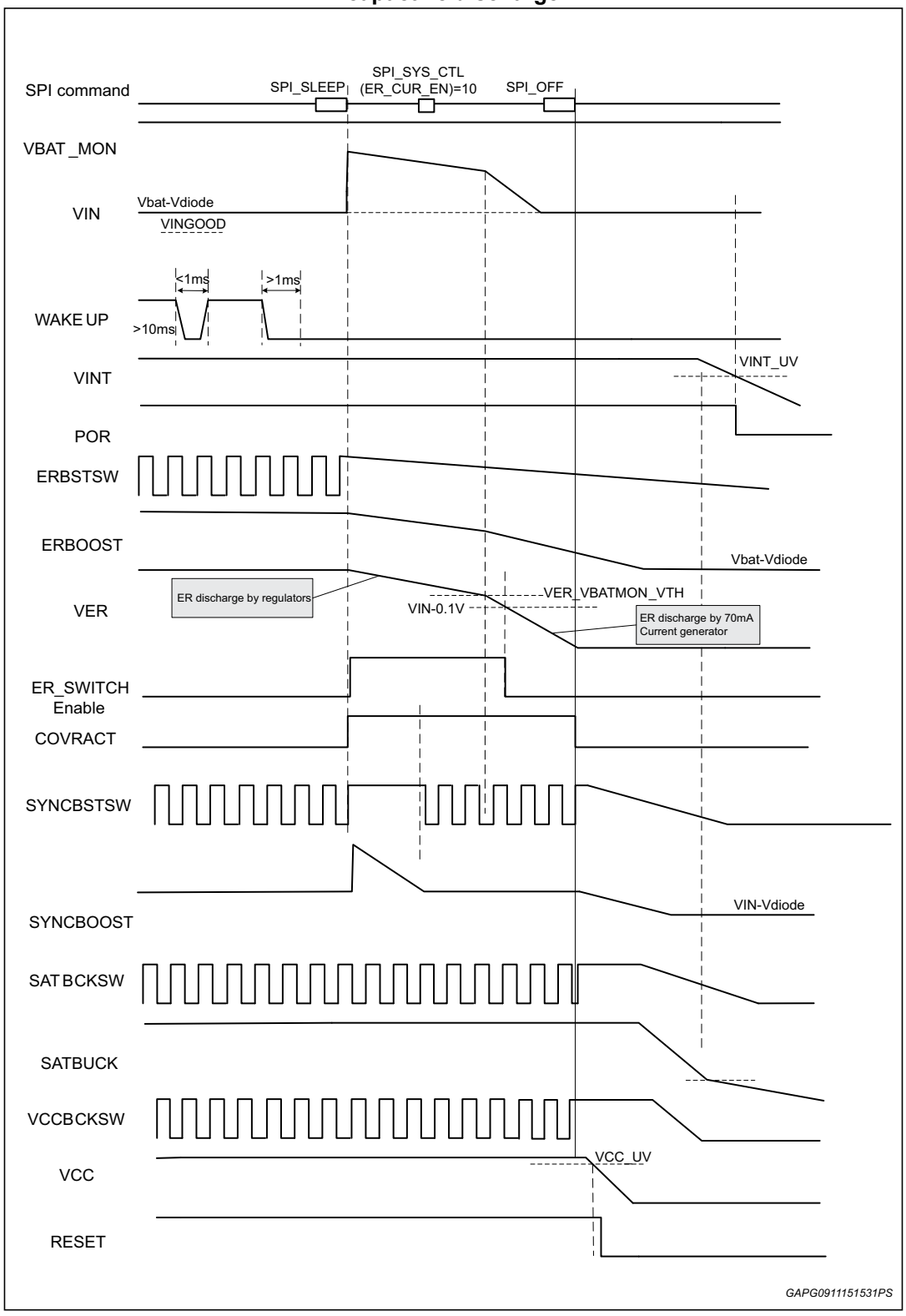
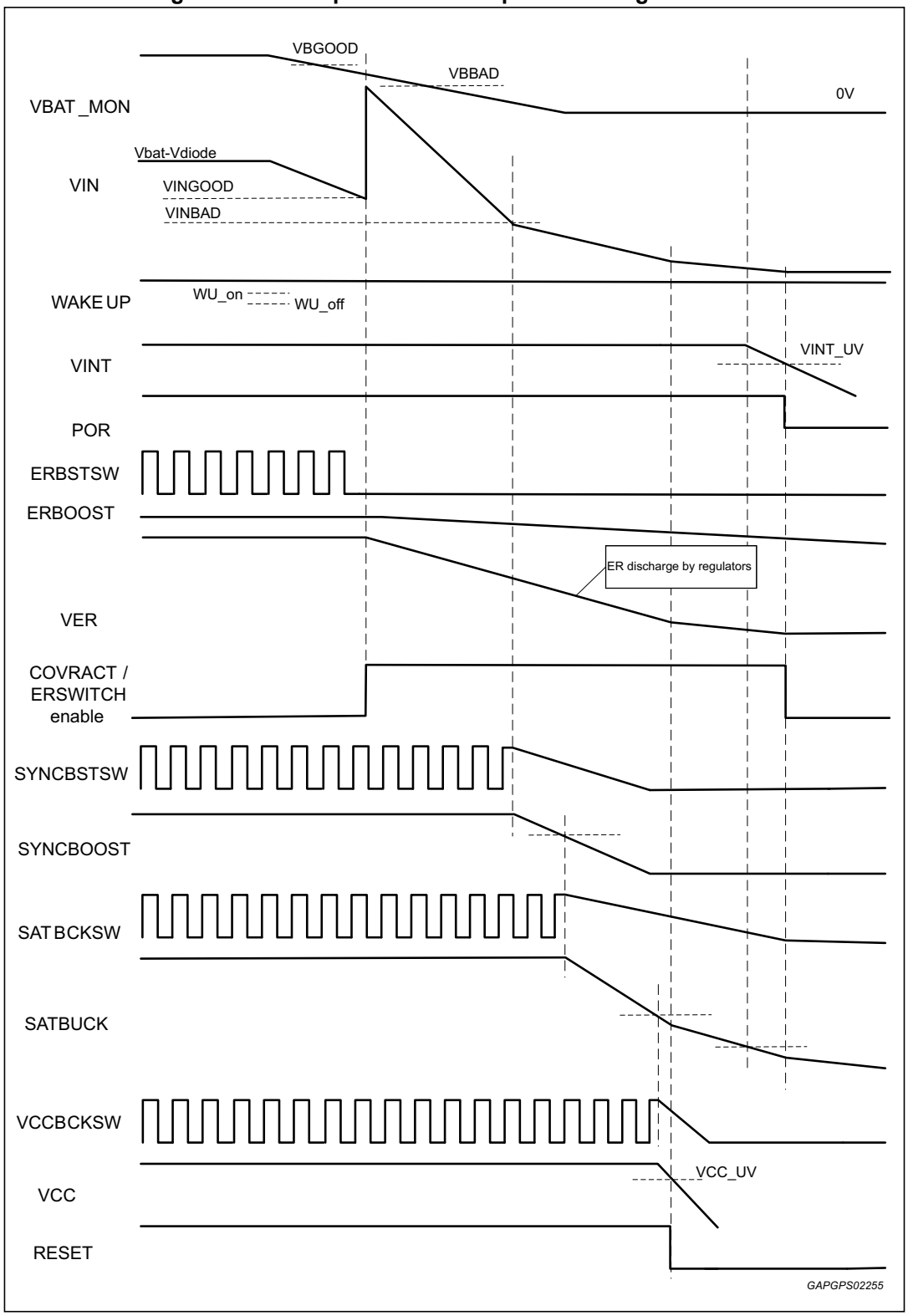


Figure 9. Normal power down sequence through ER state



6.2.6 IC operating states

Different states can be identified while operating the device. These states allow safe and predictable initialization, test, operation and final disposal of the part (scrapping).

As soon as the RESET signal is de-asserted at the beginning of the ACTIVE mode, the microcontroller powers up. At this stage, L9679P is in the Init state: during this state the device must be initialized by the controller. In particular, the watchdog timer window can be programmed during this state.

When the watchdog service begins (upon the first successful watchdog feed), the device switches to Diag state for diagnostics purposes. The remaining configuration of the device is allowed in this state, in particular for safing records and deployment masks. Several tests are also enabled while in this state and all these tests are mutually exclusive to one another. HS and LS switch tests of the squib drivers can only be processed during this Diag state. Also high side safing FET can only be run during this state. When not in Diag state, any commands for squib driver switch tests will be ignored. Other checks are also performed: on the arming outputs to check for non-stuck-at conditions on the pins and on the configured firing time configuration through one of the ARMx pin. The SSM remains in this state until commanded to transition into the Safing state or Scrap state via the dedicated SPI commands.

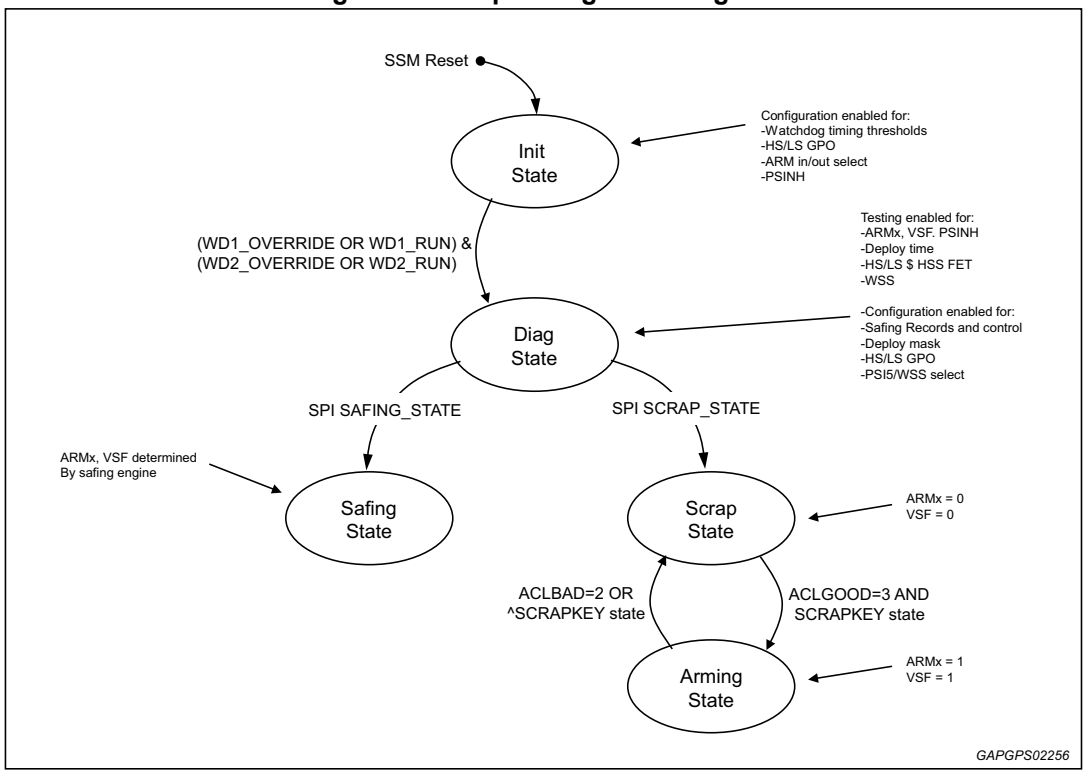
Upon reception of the SAFING_STATE command while in Diag state, the device enters Safing state. This is the primary run-time state for normal operation, and the logic performs the safing function, including monitoring of sensor data and setting of the ARMx signals. The only means of exiting Safing state is by the assertion of the SSM_Reset signal.

The Scrap state is entered upon reception of the SCRAP_STATE command while in Diag state. While in Scrap state, the part allows the main microcontroller to initiate a transition to Arming state, and monitoring of the Remote Sensor SPI interface and the safing logic is disabled. From Scrap state, the device can transition to Arming state only, and the only means of moving back to Init state is through an SSM_Reset.

In order to protect from inadvertent entry into Arming state, and to prevent undesired activation of the safing signals, a handshake mechanism is used to control entry into, and exit from Arming state. This handshake is described further in Section 11.6. While in Arming state, the arming outputs are asserted. Exit from Arming state occurs when the periodic SCRAP_KEY commands cease (timeout), the key value is incorrect, or when SSM_Reset is asserted. Upon exit, the device re-enters Scrap state, except for the case of SSM_Reset, which results in entry into Init state.

The device operating states are shown in *Figure 10*.

Figure 10. IC operating state diagram



6.3 ERBOOST switching regulator

The L9679P IC uses an advanced energy reserve switching regulator operating at 1.882MHz nominal. The higher switching frequency enables the user to select smaller less expensive inductors and moves the operating frequency to permit easier compliance with system emissions.

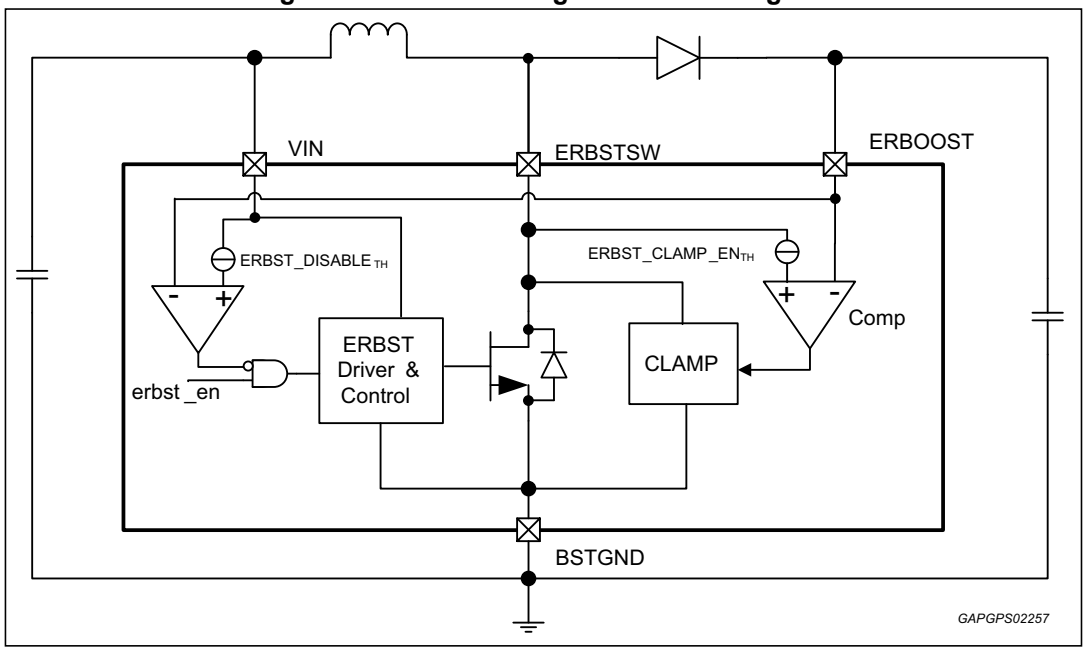
The ERBoost switching regulator uses a classical peak current mode control loop to properly regulate the output voltage and includes an over-voltage protection that immediately switch off the PowerMOS to protect the device. The regulator includes also a soft start circuit which apply a ramp on the over current threshold from the 40% of IOC_ERBST value to the maximum one with 16 steps and within $T_{SOFTST\_OC\_ERCBST}$. The soft start is restarted every time the regulator has a transition from the ER_BST_OFF to the ER_BST_ON state.

The energy reserve boost regulator charges the external system tank capacitor through an integrated fixed current source significantly reducing in-rush currents typical of large energy reserve capacitors. The boost circuit provides energy for the reserve capacitor with assumed run time load of less than 20 mA and to the VSF regulator. Once system shutdown is initiated or a loss of battery condition is diagnosed, the boost regulator is by default disabled so that system power can be taken from the energy reserve capacitor. Alternatively, the ER Boost could be kept on even during the ER State by setting the SYS_CFG(KEEP_ER_BOOST_ON) bit.

The energy reserve boost regulator defaults to 23 V at power-on and can be set to 33 V nominal by the user through an SPI command. The boost converter can also be disabled by the user through an SPI command. Enabling, disabling and setting the boost output voltage

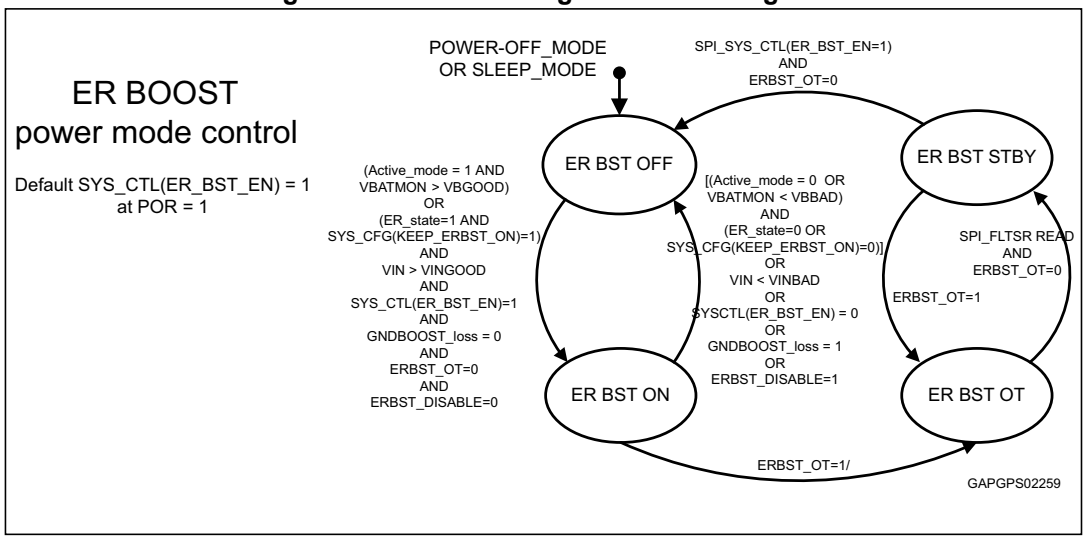
is done through the System Control (SYS_CTL) register. Boost converter diagnostics include over voltage and under voltage and the circuit is fully protected against shorts. Boost fault status is available through the SPI in Fault Status Register (FLTSR). The integrated FET featuring the boost switch is protected against short to battery by means of a thermal shutdown circuit. When thermal fault is detected the FET is switched off and latched in this state until the related fault flag ERBST_OT in the FLTSR register is read. In case of loss of BSTGND ground the FET is not turned on. Loss of ground can be detected also when the FET is off thanks to a pull-up current present on the BSTGND pin. The FET will be automatically reactivated as soon as ground connection is restored. Over-voltage protection from load dump and inductive flyback is provided via an active clamp and an ER_Boost disable circuitry, see *Figure 11*.

Figure 11. ERBOOST regulator block diagram



Normal run time power for the system is provided directly from the battery input, not from the boost. Boost energy is available to the system through the energy reserve crossover switch once battery is lost or a commanded system shutdown is initiated.

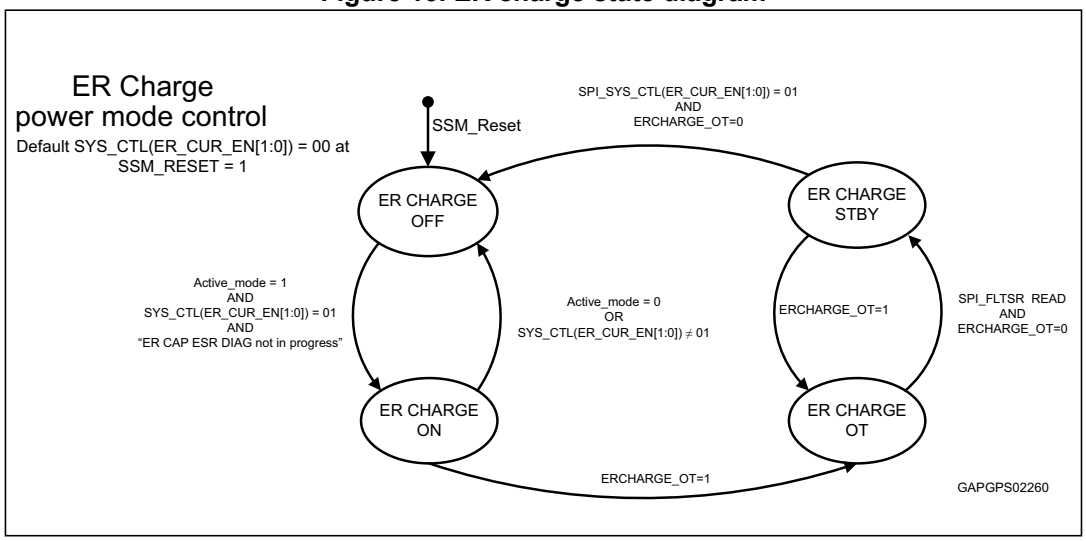
Figure 12. ERBOOST regulator state diagram



6.4 Energy reserve capacitor charging and discharging circuits

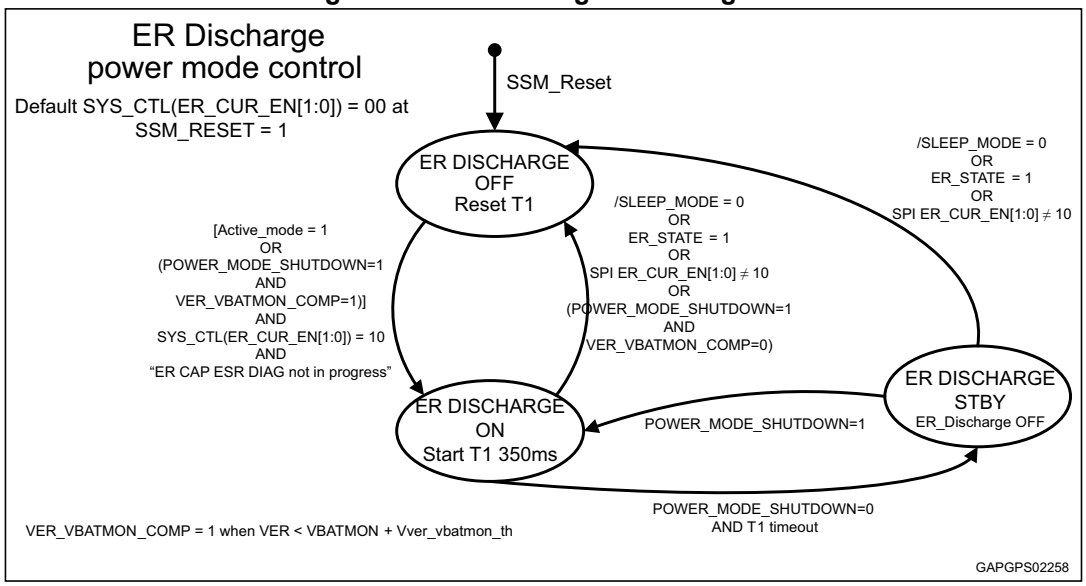
The energy reserve capacitor connected to VER pin can be charged in an efficient way by means of a current generator. Its capability is 50 mA nominal, so that for example a 10 mF capacitor can be charged in approximately 4.8 s to 24 V. The current generator is activated or deactivated by SPI command only while in ACTIVE mode. When not in ACTIVE mode, the generator is always switched off in order to decouple ERBOOST node voltage from VER reserve voltage.

Figure 13. ER charge state diagram



L9679P also offers a safe control to discharge the ER capacitor by means of a fixed current generator. This discharge can be controlled via SPI command while not in SLEEP mode. Furthermore, this discharge circuit is mutually exclusive with the ER charging circuit, to avoid inefficient way of controlling the charge on the VER energy reserve capacitor.

Figure 14. ER discharge state diagram



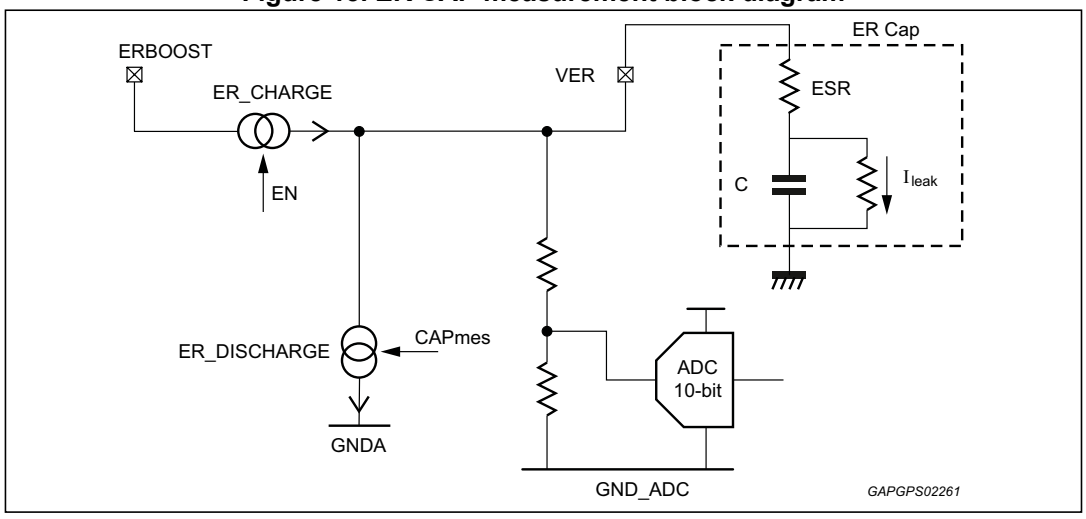
6.5 ER CAP diagnostic

The L9679P IC contains a full integrated solution to check the connection, value and series resistance of energy reserve capacitor independent from ER Cap leakage current and Boost Voltage level.

6.5.1 ER CAP measurement

The IC contains two current generators used to charge and discharge the energy reserve capacitor connected on ER pin. The simplified block diagram is shown in the figure below.

Figure 15. ER CAP measurement block diagram

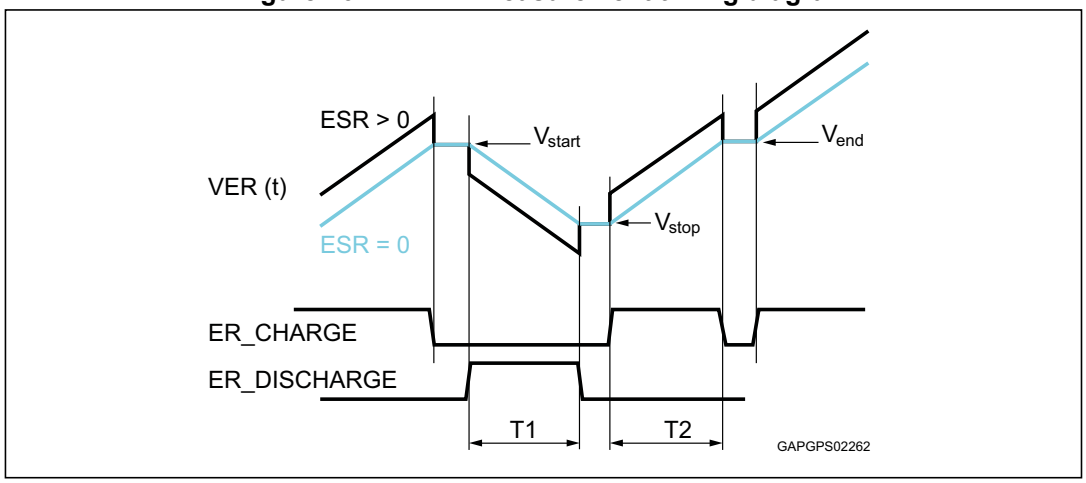


To obtain an accurate ER CAP measurement, the VER voltage conversion must be required when both current generators are off, namely no current flows through ER cap permits to avoid ESR error contribution.

The user can decide the charge and discharge time based on the ER CAP used in application, in order to maximize the differential voltage and then improve the accuracy.

Anyway, a timeout on ER Discharge current has been implemented to prevent thermal issue, so the discharge time cannot be longer than 350 ms.

Figure 16. ER CAP measurement timing diagram



The following formulas can be used to retrieve the ER CAP value from the voltage and timing measurements.

$$\Delta V_1 + \Delta V_2 = \frac{I_1 + I_{LEAK}}{C} T_1 + \frac{I_2 - I_{LEAK}}{C} T_2$$

$$C = \frac{2 \cdot I \cdot T}{V_{start} + V_{end} - 2 \cdot V_{stop}}$$

T_1 = discharge time

T_2 = charge time, same as discharge time

$T_1 = T_2 = T$

$\Delta V_1 = V_{start} - V_{stop}$

$\Delta V_2 = V_{end} - V_{stop}$

I_1 = discharge current

I_2 = charge current, same as discharge current

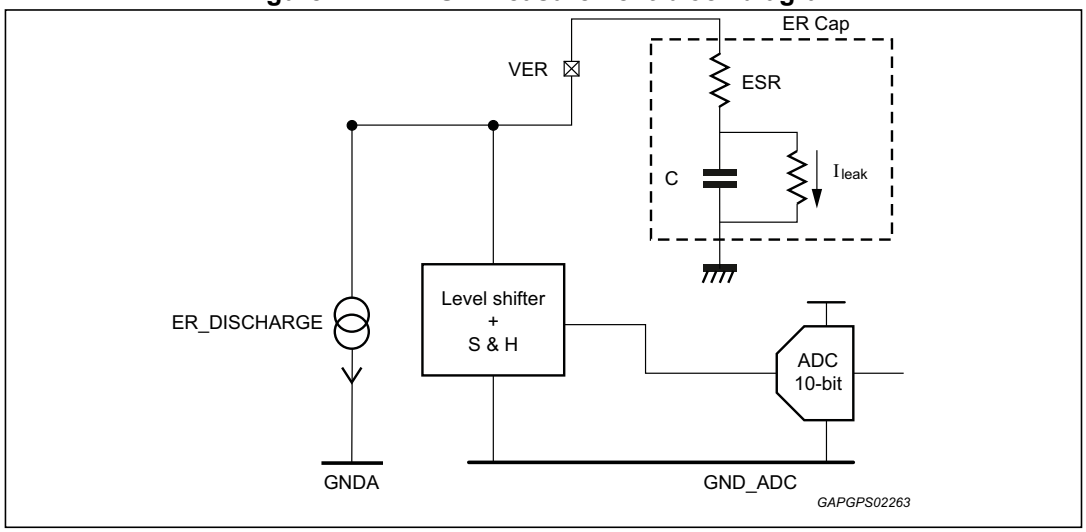
$I_1 = I_2 = I$

I_{LEAK} = leakage current

6.5.2 ER CAP ESR measurement

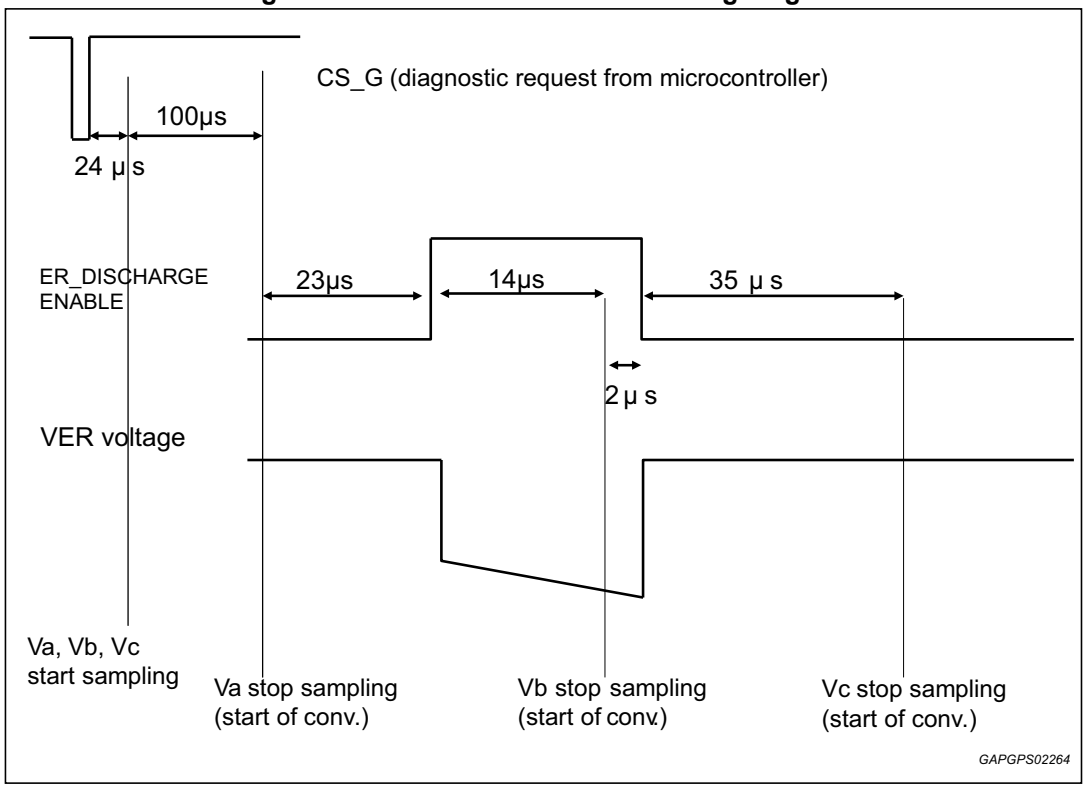
The IC contains the capability to perform a measurement of the equivalent series resistance of energy reserve capacitor. In this case the discharge current is 10 times higher to create a voltage difference proportional to the ER CAP ESR. The voltage measurement and conversion is automatically executed once the user requires the ESR measurement through the LPDIAGREQ register.

Figure 17. ER ESR measurement block diagram



Upon an ESR measurement is requested, the IC executes an internal automatic sequence to take three voltage measurements at the ER node, toggling the ER discharge current source on and off as shown in *Figure 18*. The test lasts for T_{ESR_DIAG}. After this time has elapsed, the results can be retrieved by reading the DIAGCTRL_x registers. The three ER voltage measurements are provided at the same time in DIAGCTRLA, DIAGCTRLB and DIAGCTRLC registers. During the execution of the ESR measurement no other activity on ADC is allowed. The user must ensure no other ADC requests are queued to be executed at the same time of ESR measurement. The ESR diagnostic, once initiated, will continue without interruption even if the device enters in ER State because of a battery loss event.

Figure 18. ER ESR measurement timing diagram



The ER CAP ESR can be calculated according to the following formula:

$$ESR_{ERCAP} = \frac{V_C - V_B}{G_{ER\_ESR} \cdot I_{ER\_DISCHARGE\_HIGH}} + OFF_{ER\_ESR}$$

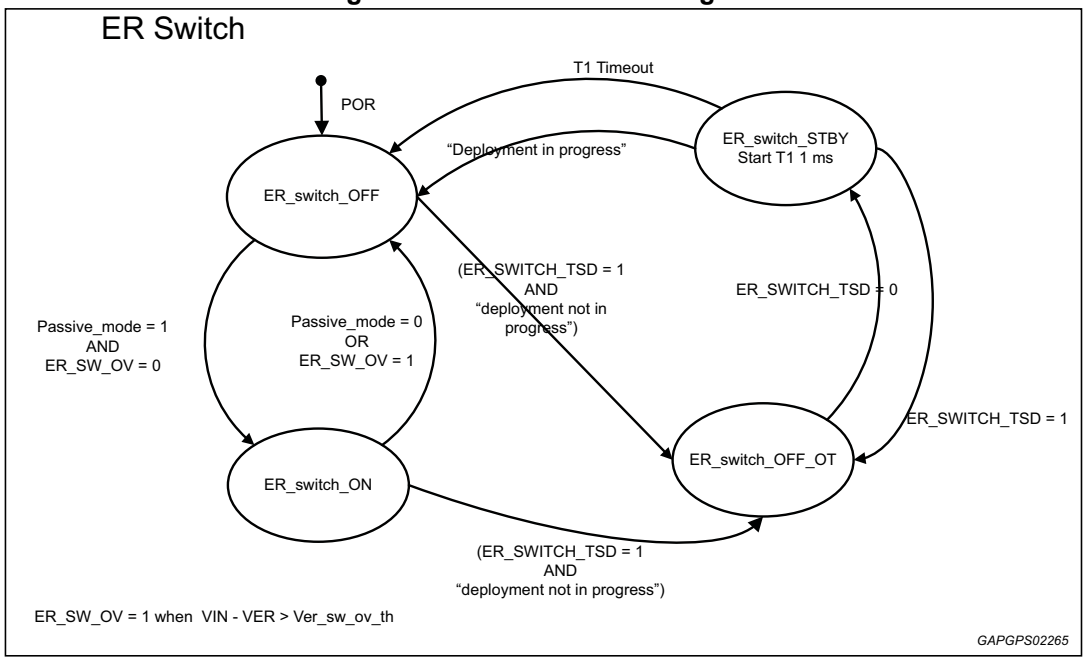
6.6 ER switch and COVRACT pin

L9679P allows the system to run out of the reserve capacitor energy stored on VER node by means of the charging boost regulator. In this way, an extended operation can take place even in case of battery lost. The ER switch implements a connection from the VER pin to the VIN node, supply input for the SYNCBOOST regulator and for internal power supplies.

The ER switch is automatically activated upon entering the PASSIVE mode. Voltage difference between VIN and VER is monitored in order to prevent VER back-feeding when VIN exceeds VER by $V_{ER\_SW\_OV\_TH}$. The ER switch is automatically deactivated upon the above mentioned overvoltage detection.

During PASSIVE mode the discrete digital output pin COVRACT is activated to allow for external optional cross-over switch control (except during VINGOOD blanking state, where the COVRACT is deactivated).

Figure 19. ER switch state diagram



6.7 SYNCBOOST boost regulator

The SYNCBOOST boost regulator also operates at 1.882 MHz allowing the user to select smaller less expensive external components. The regulator provides a 12 V/14.75 V nominal for the sync pulse feature used in PSI-5 bussed satellite sensor configuration. The regulator also provides the power for the SATBUCK regulator.

The SyncBoost switching regulator uses a classical peak current mode control loop to properly regulate the output voltage and includes an over-voltage protection that immediately switch off the PowerMOS to protect the device. The regulator includes also a soft start circuit which apply a ramp on the over current threshold from the 40% of $I_{OC\_SYNCBST}$ value to the maximum one with 16 steps and within $T_{SOFTST\_OC\_SYNCBST}$. The soft start is restarted every time the regulator is enabled, namely there is a transition from the SYNCBOOST_OFF state to the SYNCBOOST_ON state.

In normal operation, the SYNCBOOST regulator operates directly from battery providing a voltage level to operate the sync pulse driver circuit. Should the input voltage be greater than regulation point, the output voltage will track the input voltage less any drops in the external components.

The boost regulator is enabled automatically by the power control state machine, but can be disabled on purpose via SPI command through the SYS_CTL(SYNCBST_EN) bit. The regulation point is fixed at a nominal 12 V at startup. User may increase the output regulation voltage to 14.75 V nominal by setting the SATV bit via a dedicated SPI command, should an extended voltage range be needed.

Boost converter diagnostics include over voltage and under voltage, reported by the S_BST_NOK bit in the POWER_STATE register, and the circuit is fully protected against shorts. The integrated FET featuring the boost switch is protected against short to battery by means of a thermal shutdown circuit. When thermal fault is detected the FET is switched off and latched in this state until the related fault flag ERBST_OT in the FLTSR register is read.

In case of loss of ground the FET is not turned on. Loss of ground can be detected also when the FET is off thanks to a pull-up current present on the BSTGND pin. The FET will be automatically reactivated as soon as ground connection is restored. Over-voltage protection from load dump and inductive flyback is provided via an active clamp and a SYNC_Boost disable circuitry, see *Figure 20*.

Figure 20. SYNCBOOST regulator block diagram

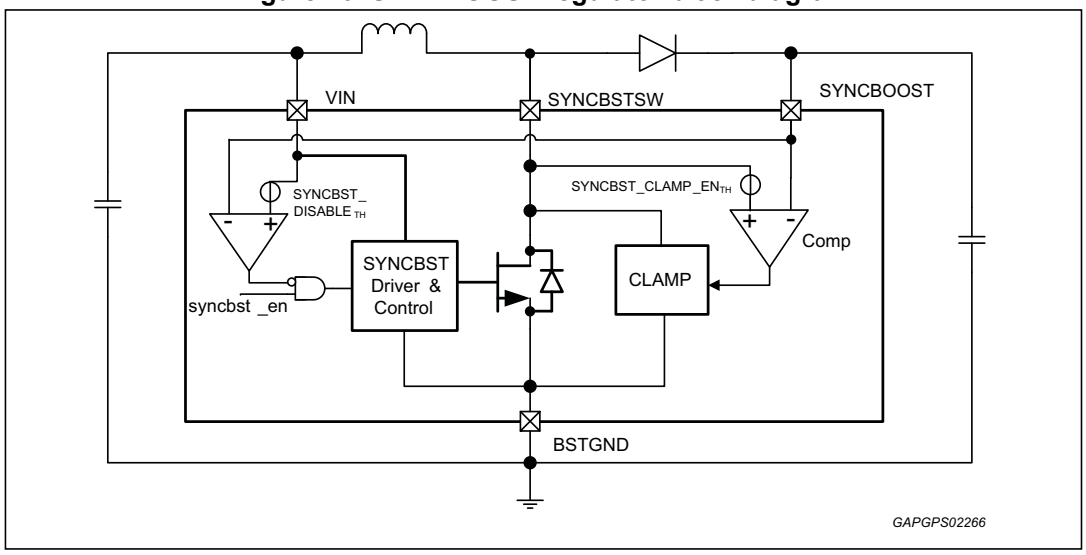
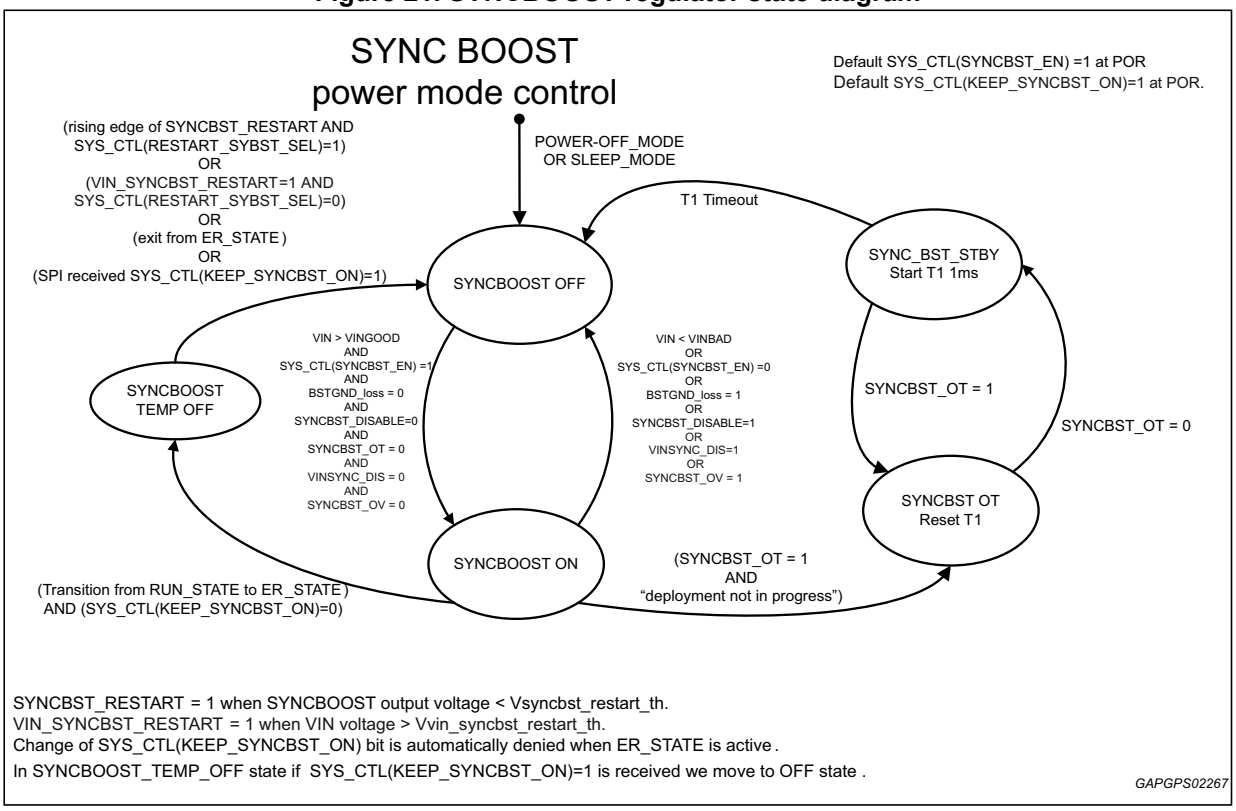


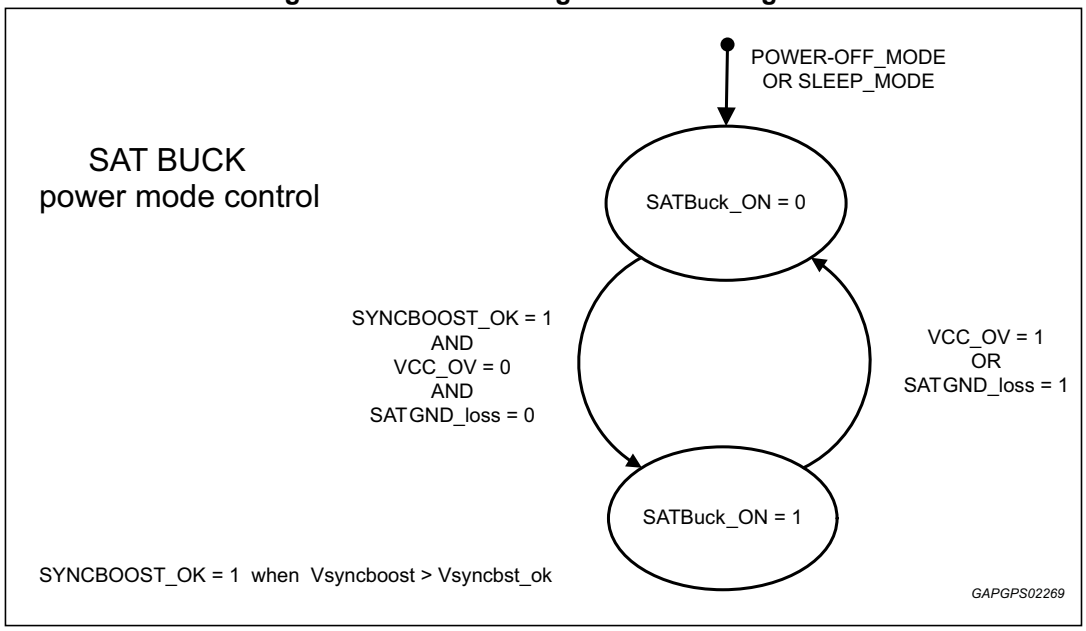
Figure 21. SYNCBOOST regulator state diagram



6.8 SATBUCK regulator

The SATBUCK regulator provides a nominal 7.2 V regulated output voltage at startup for the remote satellite and wheel speed interface circuitry and the VCC buck regulator. The buck regulator is enabled automatically by the power control state machine. This regulator is protected against short circuits. Should the user need a higher voltage range for the remote sensor interface, a specific SPI command allows the output voltage to be increased at 9 V nominal by setting the SAT_V bit. Fault status is available through SPI in the Fault Status Register (FLTSR). The buck converter operates at 1.882 MHz allowing the user to select smaller less expensive external components. Moreover, the synchronous buck regulator integrates the external recirculation diode.

Figure 22. SATBUCK regulator state diagram



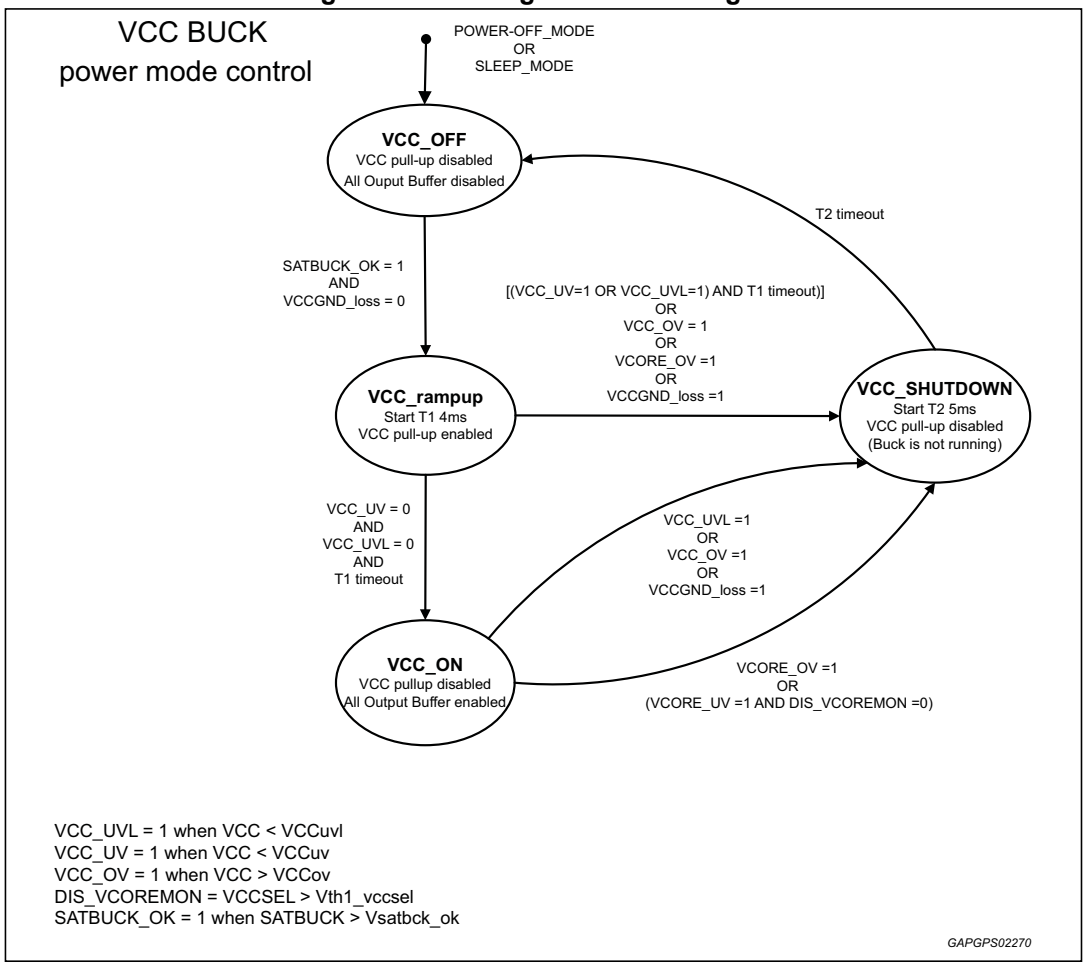
6.9 VCC buck regulator

The VCC buck regulator also operates at 1.882 MHz and is user selectable to either 3.3 V or 5 V nominal output voltage. The user can select the output voltage through the VCCSEL pin. To select 5 V operation, the user must bias VCCSEL to a level higher than $V_{TH2\_H\_VCCSEL}$ for instance SyncBoost. For 3.3 V operation, the VCCSEL pin must be biased to a level lower than $V_{TH2\_L\_VCCSEL}$. An internal weak pull down is connected to VCCSEL to ensure the input remains at ground potential in case of open pin. The internal power control state machine will read the VCCSEL input pin and latch the resulting state upon the SATBUCK voltage reaches the good value (SATBUCK_OK = 1). Upon latching the VCCSEL state, the VCC buck regulator cannot be changed by the user.

The VCC regulator has over and under voltage detections and shutdown capability and it is also protected against short circuits. During start-up an internal pull up current is enabled in order to detect a potential VCC pin open fault trough the over voltage detection. This pull up current is disabled once in VCC_ON or VCC_SHUTDOWN states. During normal operation, VCC_ON state, the VCC pin open fault is quickly detected through the Under Voltage Detection Low to prevent any MCU damage.

An open VCC pin shall lead to an under voltage condition on VCC supply monitor. The SPI related signals (SCLK, MISO, MOSI, CS) or other digital nets shall not power the VCC pin due to back-feeding paths.

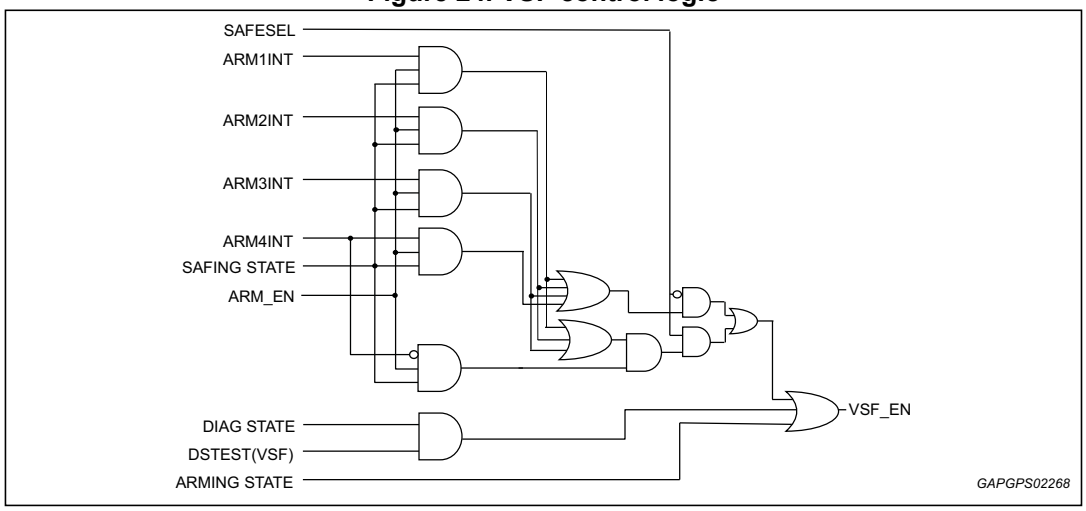
Figure 23. VCC regulator state diagram



6.10 VSF regulator and control

The L9679P provides a low current linear regulator that can be used in the system design to bias the external high side safing switch. The regulator output is 20 V nominal (configurable to 25 V via SPI command). VSF is enabled if any of the ARMxINT signal is asserted, as shown in *Figure 24*. The VSF regulator supply input is ERBOOST.

Figure 24. VSF control logic



VSF voltage can be monitored by the user through the internal ADC. Characteristics for this function are shown in the electrical performance tables.

6.11 Oscillators

The device integrates two trimmed oscillators, both of them with spread spectrum capability selectable via the CLK_CNF register.

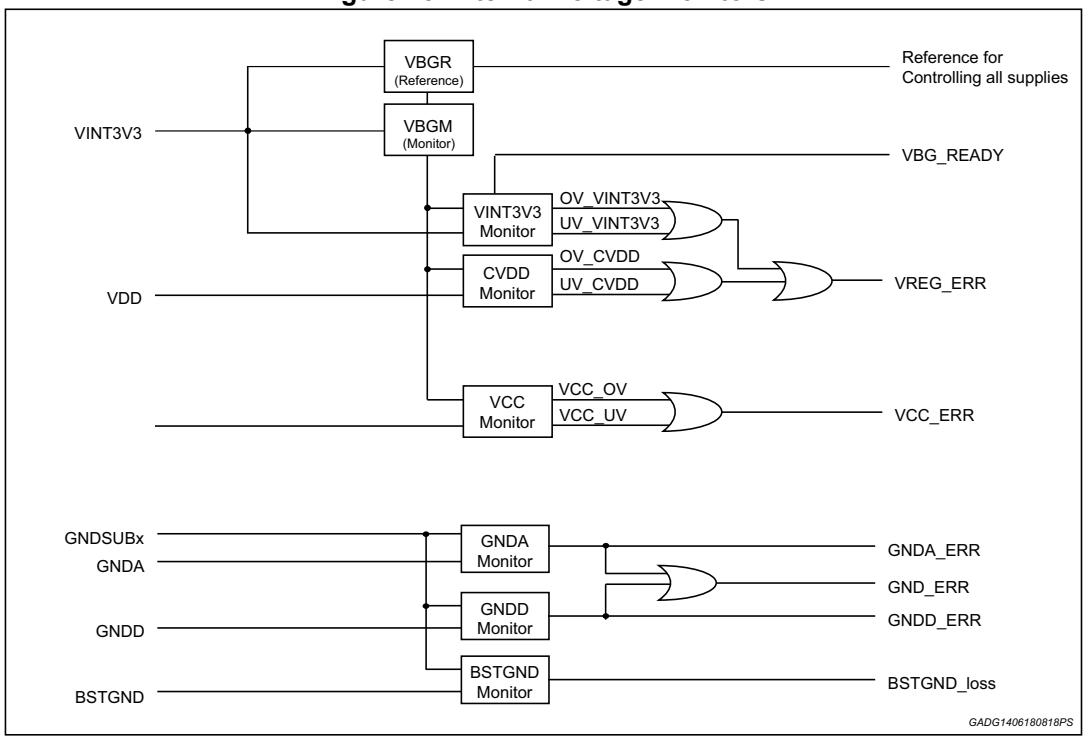
The main oscillator runs at 16 MHz typ and is used to provide clock to the internal synchronous logic. Moreover, this frequency is divided down by factor 8.5 to generate clocks for the switching regulators (1.882 MHz typ).

The auxiliary oscillator runs at 7.5 MHz typ and is used to monitor the main oscillator. In case the main oscillator frequency was lower the $f_{OSC\_LOW\_TH}$ threshold or higher than the $f_{OSC\_HIGH\_TH}$ threshold, the condition is detected by the frequency monitor circuit and then latched into the CLKFRERR flag in the FLTSR register and a POR is issued.

6.12 Reset control

The device provides reset logic to safely control system operation in the event of internal ECU failures. Several internal reset signals are generated depending on the type of failure detected. In *Figure 25* the voltage monitoring diagram is shown.

Figure 25. Internal voltage monitors



An active low pin output (RESET pin) is driven from the L9679P to allow resetting of external devices such as the microcontroller, sensors, and other ICs within the ECU.

Three internal reset signals are generated by the device:

- POR

  Power On Reset - This reset is asserted when a failure is detected in the internal supplies or bandgap circuits. When active, all other resets are asserted.

- WSM_RESET

  Watchdog State Machine Reset - This reset is generated when the POR is active or when a failure is detected in the VCC supply.

- SSM_RESET

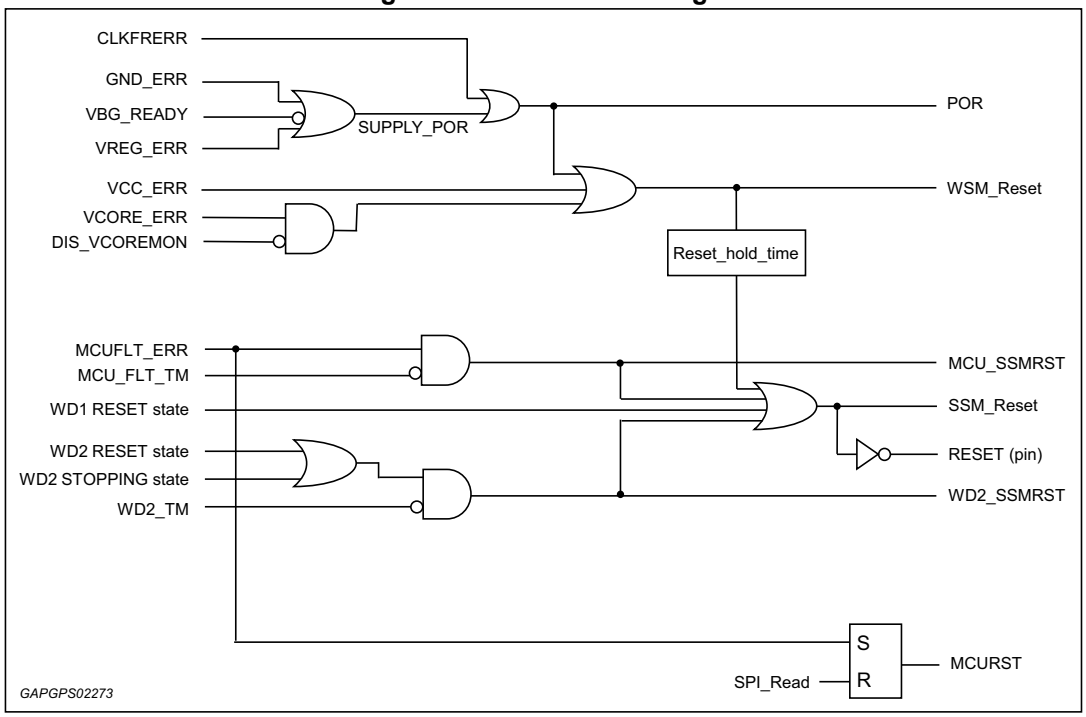
  System State Machine Reset - This reset is asserted when the POR or the WSM_RESET are active, or when a failure is detected in either Watchdog state machine.

The RESET pin is the active-low signal driven on the output pin, and is an inverted form of SSM_RESET.

The cause of the RESET activation is latched and reported into the Fault Status Register FLTSR and cleared upon SPI reading.

The reset logic shall be controlled as shown in the diagram below:

Figure 26. Reset control logic



7 SPI interfaces

The L9679P system solution device has many user selectable features controlled through serial communications by the integrated microcontroller. The device features two SPI interfaces: one global SPI and one Remote Sensor SPI. The global SPI interface provides general configuration, control and status functions for the device, while the Remote Sensor SPI provides dedicated access to Remote Sensor Data and Status Registers.

7.1 SPI protocol

Each SPI interface (Global and Remote Sensor) use their own dedicated set of 4 I/O pins: CS_G, SCLK_G, MOSI_G and MISO_G for Global SPI; CS_RS, SCLK_RS, MOSI_RS and MISO_RS for Remote Sensor SPI. Both the SPI interfaces use the same protocol described here below (the suffix '_X' used in the SPI pin names below is intended to stand for either '_G' or '_RS' depending on the particular SPI interface considered)

The IC SPI interface is composed by an input shift register, an output shift register and four control signals. MOSI_X is the data input to the input shift register. MISO_X is the data output from the output shift register. SCLK_X is the clock input used to shift data into the input shift register or out from the output one while CS_X is the active low chip select input.

All SPI communications are executed in exact 32 bit increments. The general format of the 32 bit transmission for the SPI interface is shown in *Table 5*.

Data sent to the IC (i.e. MOSI_X) consists of a target read register ID (RID), a target write register ID (WID), write data parity (WPAR) and 16 bits of data (WRITE). WRITE data is the data to be written to the target write register indicated by WID. Data returned from the IC (i.e. MISO_X) consists of a global status word (GSW), read data parity (RPAR) and 20 bits of data (READ). READ data will be the contents of the target read register as indicated by the RID bits. The parity bits WPAR and RPAR cover all the 32 bits of the MOSI and MISO frames, respectively. Odd parity type is used.

Table 5. SPI MOSI and MISO frames layout

SPI register R/W																
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SPI_MOSI	GID	RID[6:0]							WID[6:0]							WPAR
SPI_MISO	GSW[10:0]											RPAR	READ[19:16]			
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI_MOSI	WRITE[15:0]															
SPI_MISO	READ[15:0]															

The communications is controlled through CS_X, enabling and disabling communication. When CS_X is at logic high, all SPI communication I/O is tri-stated and no data is accepted. When CS_X is low, data is latched on the rising edge of SCLK_X and data is shifted on the falling edge. The MOSI_X pin receives serial data from the master with MSB first. Likewise for MISO_X, data is read MSB first, LSB last.

The L9679P contains a data validation method through the SCLK_X input to keep transmissions with not exactly 32 bits from being written to the device. The SCLK_X input counts the number of received clocks and should the clock counter exceed or count fewer

than 32 clocks, the received message is discarded and a SPI_FLT bit is flagged in the Global Status Word (GSW). The SPI_FLT bit is also set in case of parity error detected on the MOSI_X frame. Any attempt to access to a register with forbidden access mode (read or write) is not leading to changes to the internal registers but the SPI_FLT bit is not set in this case.

7.2 Global SPI register map

The Global SPI interface consists of several 32-bit registers to allow for configuration, control and status of the IC as well as special manufacturing test modes. The register definition is defined by the read register ID (RID) and the write register ID (WID) as shown in *Table 6*. Global ID bit (GID) is used to extend available register addresses, but it is shared between RID and WID; only RID and WID with the same GID value can be addressed within the same SPI word. The operating states here show in which states the SPI command is processed.

The L9679P checks the validity of the received WID and RID fields in the MOSI_G frame. Should a SPI write command with WID matching a writable register be received in an illegal operating state, the command will be discarded and the ERR_WID bit will be flagged in the next Global Status Word GSW. The ERR_WID flag is not set in case WID is addressing a read/only register. Should a SPI read command be received containing an unused RID address, the command will be discarded and the ERR_RID bit will be flagged in the current GSW.

Table 6. Global SPI register map

GID	RID / WID							Hex	R/W	Name	Description	Operating State(1)				
												Init	Diag	Ssafing	Scrap	Arming
0	0	0	0	0	0	0	0	$00	R	FLTSR	Global fault status register					
0	0	0	0	0	0	0	1	$01	R/W	SYS_CFG	Power supply configuration(2)	X	X	X	X	X
0	0	0	0	0	0	1	0	$02	R/W	SYS_CTL	Register for power management	X	X	X	X	X
0	0	0	0	0	0	1	1	$03	W	SPI_SLEEP	Sleep Mode command	X	X	X	X	X
0	0	0	0	0	1	0	0	$04	R	SYS_STATE	Read register to report in which state the power control state machine is and also in which operating state the device is					
0	0	0	0	0	1	0	1	$05	R	POWER_STATE	Power state register (feedback on regulators' status and voltage thresholds)					
0	0	0	0	0	1	1	0	$06	R/W	DCR_0	Deployment configuration register		X	X	X	X
0	0	0	0	0	1	1	1	$07	R/W	DCR_1			X	X	X	X
0	0	0	0	1	0	0	0	$08	R/W	DCR_2			X	X	X	X
0	0	0	0	1	0	0	1	$09	R/W	DCR_3			X	X	X	X
0	0	0	0	1	0	1	0	$0A	R/W	DCR_4			X	X	X	X
0	0	0	0	1	0	1	1	$0B	R/W	DCR_5			X	X	X	X
0	0	0	0	1	1	0	0	$0C	R/W	DCR_6			X	X	X	X
0	0	0	0	1	1	0	1	$0D	R/W	DCR_7			X	X	X	X
0	0	0	0	1	1	1	0	$0E								
0	0	0	0	1	1	1	1	$0F								
0	0	0	1	0	0	0	0	$10								
0	0	0	1	0	0	0	1	$11								
0	0	0	1	0	0	1	0	$12	R/W	DEPCOM	Deployment command register			X		X
0	0	0	1	0	0	1	1	$13	R	DSR_0	Deployment status register					
0	0	0	1	0	1	0	0	$14	R	DSR_1						
0	0	0	1	0	1	0	1	$15	R	DSR_2						

Table 6. Global SPI register map (continued)

GID	RID / WID								Hex	R/W	Name	Description	Operating State(1)				
													Init	Diag	Ssafing	Scrap	Arming
0	0	0	1	0	1	1	0		$16	R	DSR_3	Deployment status register					
0	0	0	1	0	1	1	1		$17	R	DSR_4						
0	0	0	1	1	0	0	0		$18	R	DSR_5						
0	0	0	1	1	0	0	1		$19	R	DSR_6						
0	0	0	1	1	0	1	0		$1A	R	DSR_7						
0	0	0	1	1	0	1	1		$1B								
0	0	0	1	1	1	0	0		$1C								
0	0	0	1	1	1	0	1		$1D								
0	0	0	1	1	1	1	0		$1E								
0	0	0	1	1	1	1	1		$1F	R	DCMTS01	Deployment current monitor register					
0	0	1	0	0	0	0	0		$20	R	DCMTS23						
0	0	1	0	0	0	0	1		$21	R	DCMTS45						
0	0	1	0	0	0	1	0		$22	R	DCMTS67						
0	0	1	0	0	0	1	1		$23								
0	0	1	0	0	1	0	0		$24								
0	0	1	0	0	1	0	1		$25	R/W	SPIDEPEN	Lock/Unlock command			X		X
0	0	1	0	0	1	1	0		$26	R	LP_GNDLOSS	Loss of ground fault for squib loops					
0	0	1	0	0	1	1	1		$27	R	VERSION_ID	Device version					
0	0	1	0	1	0	0	0		$28	R/W	WD_RETRY_CONF	Watchdog Retry Configuration	X				
0	0	1	0	1	0	0	1		$29	W							
0	0	1	0	1	0	1	0		$2A	R/W	WDTCR	Watchdog first level configuration	X				
0	0	1	0	1	0	1	1		$2B	R/W	WD1T	Watchdog first level key transmission	X	X	X	X	X
0	0	1	0	1	1	0	0		$2C	R	WD_STATE	Watchdog first and second level state					
0	0	1	0	1	1	0	1		$2D	R/W	CLK_CONF	Clock configuration	X	X	X	X	X
0	0	1	0	1	1	1	0		$2E	R	SCRAP_SEED	Scrap Seed command					

Table 6. Global SPI register map (continued)

GID	RID / WID							Hex	R/W	Name	Description	Operating State(1)				
												Init	Diag	Ssafing	Scrap	Arming
0	0	1	0	1	1	1	1	$2F	W	SCRAP_KEY	Scrap Key command				X	X
0	0	1	1	0	0	0	0	$30	W	SCRAP_STATE	Scrap State command		X			
0	0	1	1	0	0	0	1	$31	W	SAFING_STATE	Safing State command		X			
0	0	1	1	0	0	1	0	$32	W	WD2_RECOVER	Watchdog second level recovery command	X	X	X	X	X
0	0	1	1	0	0	1	1	$33	R	WD2_SEED	Watchdog second level seed transmission					
0	0	1	1	0	1	0	0	$34	W	WD2_KEY	Watchdog second level key transmission	X	X	X	X	X
0	0	1	1	0	1	0	1	$35	W	WD_TEST	Watchdog first and second level test	X	X	X	X	X
0	0	1	1	0	1	1	0	$36	R/W	SYSDIAGREQ	Diagnostic command for system safing		X			
0	0	1	1	0	1	1	1	$37	R	LPDIAGSTAT	Diagnostic result register for deployment loops					
0	0	1	1	1	0	0	0	$38	R/W	LPDIAGREQ	Diagnostic configuration command for deployment loops		X	X	X	X
0	0	1	1	1	0	0	1	$39	R/W	SWCTRL	DC sensor diagnostic configuration		X	X	X	X
0	0	1	1	1	0	1	0	$3A	R/W	DIAGCTRL_A	In WID is AtoD converter control register A. In RID is AtoD result A request.		X	X	X	X
0	0	1	1	1	0	1	1	$3B	R/W	DIAGCTRL_B	In WID is AtoD converter control register B. In RID is AtoD result B request.		X	X	X	X
0	0	1	1	1	1	0	0	$3C	R/W	DIAGCTRL_C	In WID is AtoD converter control register C. In RID is AtoD result C request.		X	X	X	X
0	0	1	1	1	1	0	1	$3D	R/W	DIAGCTRL_D	In WID is AtoD converter control register D. In RID is AtoD result D request.		X	X	X	X
0	0	1	1	1	1	1	0	$3E								
0	0	1	1	1	1	1	1	$3F	R/W	SW_REGS_CONF	Configuration register for switching regulators		X	X	X	X
0	1	0	0	0	0	0	0	$40								
0	1	0	0	0	0	0	1	$41								
0	1	0	0	0	0	1	0	$42	R/W	GPOCR	General Purpose Output configuration	X	X			
0	1	0	0	0	0	1	1	$43	R/W	GPOCTRL0	General Purpose Output 0 control register	X	X	X	X	X

Table 6. Global SPI register map (continued)

GID	RID / WID							Hex	R/W	Name	Description	Operating State(1)				
												Init	Diag	Ssafing	Scrap	Arming
0	1	0	0	0	1	0	0	$44	R/W	GPOCTRL1	General Purpose Output 1 control register	X	X	X	X	X
0	1	0	0	0	1	0	1	$45	R/W	GPOCTRL2	General Purpose Output 2 control register	X	X	X	X	X
0	1	0	0	0	1	1	0	$46	R	GPOFLTSR	General Purpose Output fault status register					
0	1	0	0	0	1	1	1	$47								
0	1	0	0	1	0	0	0	$48	R	ISOFLTSR	ISOK Fault Status Register		X			
0	1	0	0	1	0	0	1	$49								
0	1	0	0	1	0	1	0	$4A	R/W	RSCR0	PSI5/WSS configuration register		X			
0	1	0	0	1	0	1	1	$4B	R/W	RSCR1			X			
0	1	0	0	1	1	0	0	$4C								
0	1	0	0	1	1	0	1	$4D								
0	1	0	0	1	1	1	0	$4E	R/W	RSCTRL	Remote sensor control register		X	X	X	X
0	1	0	0	1	1	1	1	$4F								
0	1	0	1	0	0	0	0	$50								
0	1	0	1	0	0	0	1	$51								
0	1	0	1	0	0	1	0	$52								
0	1	0	1	0	0	1	1	$53								
0	1	0	1	0	1	0	0	$54								
0	1	0	1	0	1	0	1	$55								
0	1	0	1	0	1	1	0	$56								
0	1	0	1	0	1	1	1	$57								
0	1	0	1	1	0	0	0	$58								
0	1	0	1	1	0	0	1	$59								
0	1	0	1	1	0	1	0	$5A								
0	1	0	1	1	0	1	1	$5B								
0	1	0	1	1	1	0	0	$5C								

Table 6. Global SPI register map (continued)

GID	RID / WID							Hex	R/W	Name	Description	Operating State(1)				
												Init	Diag	Ssafing	Scrap	Arming
0	1	0	1	1	1	0	1	$5D								
0	1	0	1	1	1	1	0	$5E								
0	1	0	1	1	1	1	1	$5F								
0	1	1	0	0	0	0	0	$60								
0	1	1	0	0	0	0	1	$61								
0	1	1	0	0	0	1	0	$62								
0	1	1	0	0	0	1	1	$63								
0	1	1	0	0	1	0	0	$64								
0	1	1	0	0	1	0	1	$65								
0	1	1	0	0	1	1	0	$66	R/W	SAF_ALGO_CONF	Safing Algorithm configuration register		X			
0	1	1	0	0	1	1	1	$67								
0	1	1	0	1	0	0	0	$68								
0	1	1	0	1	0	0	1	$69								
0	1	1	0	1	0	1	0	$6A	R	ARM_STATE	Status of arming signals					
0	1	1	0	1	0	1	1	$6B								
0	1	1	0	1	1	0	0	$6C								
0	1	1	0	1	1	0	1	$6D								
0	1	1	0	1	1	1	0	$6E	R/W	LOOP_MATRIX_ARM1	Assignment of ARM 1 pin to which LOOPS		X			
0	1	1	0	1	1	1	1	$6F	R/W	LOOP_MATRIX_ARM2	Assignment of ARM 2 pin to which LOOPS		X			
0	1	1	1	0	0	0	0	$70								
0	1	1	1	0	0	0	1	$71								
0	1	1	1	0	0	1	0	$72								
0	1	1	1	0	0	1	1	$73	R	AEPSTS_ARM1	Arming pulse stretch timer value					
0	1	1	1	0	1	0	0	$74	R	AEPSTS_ARM2						
0	1	1	1	0	1	0	1	$75								

Table 6. Global SPI register map (continued)

GID	RID / WID							Hex	R/W	Name	Description	Operating State(1)				
												Init	Diag	Ssafing	Scrap	Arming
0	1	1	1	0	1	1	0	$76								
0	1	1	1	0	1	1	1	$77								
0	1	1	1	1	0	0	0	$78	R/W	PADTHRESH_HI	Passenger Inhibit Thresholds		X			
0	1	1	1	1	0	0	1	$79	R/W	PADTHRESH_LO			X			
0	1	1	1	1	0	1	0	$7A	R/W	LOOP_MATRIX_PSINH	Assignment of PSINH signal to which LOOPS		X			
0	1	1	1	1	0	1	1	$7B								
0	1	1	1	1	1	0	0	$7C								
0	1	1	1	1	1	0	1	$7D								
0	1	1	1	1	1	1	0	$7E								
0	1	1	1	1	1	1	1	$7F	R/W	SAF_ENABLE	Safing record enable		X	X	X	X
1	0	0	0	0	0	0	0	$80	R/W	SAF_REQ_MASK_1	Safing record request mask		X			
1	0	0	0	0	0	0	1	$81	R/W	SAF_REQ_MASK_2			X			
1	0	0	0	0	0	1	0	$82	R/W	SAF_REQ_MASK_3			X			
1	0	0	0	0	0	1	1	$83	R/W	SAF_REQ_MASK_4			X			
1	0	0	0	0	1	0	0	$84	R/W	SAF_REQ_MASK_5			X			
1	0	0	0	0	1	0	1	$85	R/W	SAF_REQ_MASK_6			X			
1	0	0	0	0	1	1	0	$86	R/W	SAF_REQ_MASK_7			X			
1	0	0	0	0	1	1	1	$87	R/W	SAF_REQ_MASK_8			X			
1	0	0	0	1	0	0	0	$88	R/W	SAF_REQ_MASK_9			X			
1	0	0	0	1	0	0	1	$89								
1	0	0	0	1	0	1	0	$8A								
1	0	0	0	1	0	1	1	$8B								
1	0	0	0	1	1	0	0	$8C								
1	0	0	0	1	1	0	1	$8D	R/W	SAF_REQ_MASK_14_pt1			X			

Table 6. Global SPI register map (continued)

GID	RID / WID							Hex	R/W	Name	Description	Operating State(1)				
												Init	Diag	Ssafing	Scrap	Arming
1	0	0	0	1	1	1	0	$8E	R/W	SAF_REQ_MASK_14_pt2			X			
1	0	0	0	1	1	1	1	$8F	R/W	SAF_REQ_MASK_15_pt1			X			
1	0	0	1	0	0	0	0	$90	R/W	SAF_REQ_MASK_15_pt2	Safing record request mask		X			
1	0	0	1	0	0	0	1	$91	R/W	SAF_REQ_MASK_16_pt1			X			
1	0	0	1	0	0	1	0	$92	R/W	SAF_REQ_MASK_16_pt2			X			
1	0	0	1	0	0	1	1	$93	R/W	SAF_REQ_TARGET_1			X			
1	0	0	1	0	1	0	0	$94	R/W	SAF_REQ_TARGET_2			X			
1	0	0	1	0	1	0	1	$95	R/W	SAF_REQ_TARGET_3			X			
1	0	0	1	0	1	1	0	$96	R/W	SAF_REQ_TARGET_4			X			
1	0	0	1	0	1	1	1	$97	R/W	SAF_REQ_TARGET_5			X			
1	0	0	1	1	0	0	0	$98	R/W	SAF_REQ_TARGET_6			X			
1	0	0	1	1	0	0	1	$99	R/W	SAF_REQ_TARGET_7			X			
1	0	0	1	1	0	1	0	$9A	R/W	SAF_REQ_TARGET_8			X			
1	0	0	1	1	0	1	1	$9B	R/W	SAF_REQ_TARGET_9			X			
1	0	0	1	1	1	0	0	$9C			Safing record request target					
1	0	0	1	1	1	0	1	$9D								
1	0	0	1	1	1	1	0	$9E								
1	0	0	1	1	1	1	1	$9F								
1	0	1	0	0	0	0	0	$A0	R/W	SAF_REQ_TARGET_14_pt1			X			
1	0	1	0	0	0	0	1	$A1	R/W	SAF_REQ_TARGET_14_pt2			X			
1	0	1	0	0	0	1	0	$A2	R/W	SAF_REQ_TARGET_15_pt1			X			
1	0	1	0	0	0	1	1	$A3	R/W	SAF_REQ_TARGET_15_pt2			X			
1	0	1	0	0	1	0	0	$A4	R/W	SAF_REQ_TARGET_16_pt1			X			
1	0	1	0	0	1	0	1	$A5	R/W	SAF_REQ_TARGET_16_pt2			X			
1	0	1	0	0	1	1	0	$A6	R/W	SAF_RESP_MASK_1	Safing record response mask		X			

Table 6. Global SPI register map (continued)

GID	RID / WID							Hex	R/W	Name	Description	Operating State(1)				
												Init	Diag	Ssafing	Scrap	Arming
1	0	1	0	0	1	1	1	$A7	R/W	SAF_RESP_MASK_2	Safing record response mask		X			
1	0	1	0	1	0	0	0	$A8	R/W	SAF_RESP_MASK_3			X			
1	0	1	0	1	0	0	1	$A9	R/W	SAF_RESP_MASK_4			X			
1	0	1	0	1	0	1	0	$AA	R/W	SAF_RESP_MASK_5			X			
1	0	1	0	1	0	1	1	$AB	R/W	SAF_RESP_MASK_6			X			
1	0	1	0	1	1	0	0	$AC	R/W	SAF_RESP_MASK_7			X			
1	0	1	0	1	1	0	1	$AD	R/W	SAF_RESP_MASK_8			X			
1	0	1	0	1	1	1	0	$AE	R/W	SAF_RESP_MASK_9			X			
1	0	1	0	1	1	1	1	$AF								
1	0	1	1	0	0	0	0	$B0								
1	0	1	1	0	0	0	1	$B1								
1	0	1	1	0	0	1	0	$B2								
1	0	1	1	0	0	1	1	$B3	R/W	SAF_RESP_MASK_14_pt1			X			
1	0	1	1	0	1	0	0	$B4	R/W	SAF_RESP_MASK_14_pt2			X			
1	0	1	1	0	1	0	1	$B5	R/W	SAF_RESP_MASK_15_pt1			X			
1	0	1	1	0	1	1	0	$B6	R/W	SAF_RESP_MASK_15_pt2			X			
1	0	1	1	0	1	1	1	$B7	R/W	SAF_RESP_MASK_16_pt1			X			
1	0	1	1	1	0	0	0	$B8	R/W	SAF_RESP_MASK_16_pt2			X			
1	0	1	1	1	0	0	1	$B9	R/W	SAF_RESP_TARGET_1	Safing record response target		X			
1	0	1	1	1	0	1	0	$BA	R/W	SAF_RESP_TARGET_2			X			
1	0	1	1	1	0	1	1	$BB	R/W	SAF_RESP_TARGET_3			X			
1	0	1	1	1	1	0	0	$BC	R/W	SAF_RESP_TARGET_4			X			
1	0	1	1	1	1	0	1	$BD	R/W	SAF_RESP_TARGET_5			X			
1	0	1	1	1	1	1	0	$BE	R/W	SAF_RESP_TARGET_6			X			
1	0	1	1	1	1	1	1	$BF	R/W	SAF_RESP_TARGET_7			X			

Table 6. Global SPI register map (continued)

GID	RID / WID							Hex	R/W	Name	Description	Operating State[1]				
												Init	Diag	Ssafing	Scrap	Arming
1	1	0	0	0	0	0	0	$C0	R/W	SAF_RESP_TARGET_8	Safing record response target		X			
1	1	0	0	0	0	0	1	$C1	R/W	SAF_RESP_TARGET_9			X			
1	1	0	0	0	0	1	0	$C2								
1	1	0	0	0	0	1	1	$C3								
1	1	0	0	0	1	0	0	$C4								
1	1	0	0	0	1	0	1	$C5								
1	1	0	0	0	1	1	0	$C6	R/W	SAF_RESP_TARGET_14_pt1			X			
1	1	0	0	0	1	1	1	$C7	R/W	SAF_RESP_TARGET_14_pt2			X			
1	1	0	0	1	0	0	0	$C8	R/W	SAF_RESP_TARGET_15_pt1			X			
1	1	0	0	1	0	0	1	$C9	R/W	SAF_RESP_TARGET_15_pt2			X			
1	1	0	0	1	0	1	0	$CA	R/W	SAF_RESP_TARGET_16_pt1			X			
1	1	0	0	1	0	1	1	$CB	R/W	SAF_RESP_TARGET_16_pt2			X			
1	1	0	0	1	1	0	0	$CC	R/W	SAF_DATA_MASK_1	Safing record data mask		X			
1	1	0	0	1	1	0	1	$CD	R/W	SAF_DATA_MASK_2			X			
1	1	0	0	1	1	1	0	$CE	R/W	SAF_DATA_MASK_3			X			
1	1	0	0	1	1	1	1	$CF	R/W	SAF_DATA_MASK_4			X			
1	1	0	1	0	0	0	0	$D0	R/W	SAF_DATA_MASK_5			X			
1	1	0	1	0	0	0	1	$D1	R/W	SAF_DATA_MASK_6			X			
1	1	0	1	0	0	1	0	$D2	R/W	SAF_DATA_MASK_7			X			
1	1	0	1	0	0	1	1	$D3	R/W	SAF_DATA_MASK_8			X			
1	1	0	1	0	1	0	0	$D4	R/W	SAF_DATA_MASK_9			X			
1	1	0	1	0	1	0	1	$D5								
1	1	0	1	0	1	1	0	$D6								
1	1	0	1	0	1	1	1	$D7								
1	1	0	1	1	0	0	0	$D8								

Table 6. Global SPI register map (continued)

GID	RID / WID							Hex	R/W	Name	Description	Operating State(1)				
												Init	Diag	Ssafing	Scrap	Arming
1	1	0	1	1	0	0	1	$D9	R/W	SAF_DATA_MASK_14_pt1	Safing record data mask		X			
1	1	0	1	1	0	1	0	$DA	R/W	SAF_DATA_MASK_14_pt2			X			
1	1	0	1	1	0	1	1	$DB	R/W	SAF_DATA_MASK_15_pt1			X			
1	1	0	1	1	1	0	0	$DC	R/W	SAF_DATA_MASK_15_pt2			X			
1	1	0	1	1	1	0	1	$DD	R/W	SAF_DATA_MASK_16_pt1			X			
1	1	0	1	1	1	1	0	$DE	R/W	SAF_DATA_MASK_16_pt2			X			
1	1	0	1	1	1	1	1	$DF	R/W	SAF_THRESHOLD_1	Safing record threshold		X			
1	1	1	0	0	0	0	0	$E0	R/W	SAF_THRESHOLD_2			X			
1	1	1	0	0	0	0	1	$E1	R/W	SAF_THRESHOLD_3			X			
1	1	1	0	0	0	1	0	$E2	R/W	SAF_THRESHOLD_4			X			
1	1	1	0	0	0	1	1	$E3	R/W	SAF_THRESHOLD_5			X			
1	1	1	0	0	1	0	0	$E4	R/W	SAF_THRESHOLD_6			X			
1	1	1	0	0	1	0	1	$E5	R/W	SAF_THRESHOLD_7			X			
1	1	1	0	0	1	1	0	$E6	R/W	SAF_THRESHOLD_8			X			
1	1	1	0	0	1	1	1	$E7	R/W	SAF_THRESHOLD_9			X			
1	1	1	0	1	0	0	0	$E8								
1	1	1	0	1	0	0	1	$E9								
1	1	1	0	1	0	1	0	$EA								
1	1	1	0	1	0	1	1	$EB								
1	1	1	0	1	1	0	0	$EC	R/W	SAF_THRESHOLD_14			X			
1	1	1	0	1	1	0	1	$ED	R/W	SAF_THRESHOLD_15			X			
1	1	1	0	1	1	1	0	$EE	R/W	SAF_THRESHOLD_16			X			
1	1	1	0	1	1	1	1	$EF	R/W	SAF_CONTROL_1	Safing record control		X			
1	1	1	1	0	0	0	0	$F0	R/W	SAF_CONTROL_2			X			
1	1	1	1	0	0	0	1	$F1	R/W	SAF_CONTROL_3			X			

Table 6. Global SPI register map (continued)

GID	RID / WID							Hex	R/W	Name	Description	Operating State(1)				
												Init	Diag	Ssafing	Scrap	Arming
1	1	1	1	0	0	1	0	$F2	R/W	SAF_CONTROL_4	Safing record control		X			
1	1	1	1	0	0	1	1	$F3	R/W	SAF_CONTROL_5			X			
1	1	1	1	0	1	0	0	$F4	R/W	SAF_CONTROL_6			X			
1	1	1	1	0	1	0	1	$F5	R/W	SAF_CONTROL_7			X			
1	1	1	1	0	1	1	0	$F6	R/W	SAF_CONTROL_8			X			
1	1	1	1	0	1	1	1	$F7	R/W	SAF_CONTROL_9			X			
1	1	1	1	1	0	0	0	$F8								
1	1	1	1	1	0	0	1	$F9								
1	1	1	1	1	0	1	0	$FA								
1	1	1	1	1	0	1	1	$FB								
1	1	1	1	1	1	0	0	$FC	R/W	SAF_CONTROL_14			X			
1	1	1	1	1	1	0	1	$FD	R/W	SAF_CONTROL_15			X			
1	1	1	1	1	1	1	0	$FE	R/W	SAF_CONTROL_16			X			
1	1	1	1	1	1	1	1	$FF	R	SAF_CC	Safing Record Compare Complete					

1. A check mark indicates in which operating state a WRITE-command is valid.
2. KEEP_ERBOOST_ON, LOW_POWER_MODE, VSF_V and VINGOOD_FILT_SEL bits are writable in all states, the other bits of SYS_CFG are only writable in INIT state.

7.3 Global SPI tables

A summary of all the registers contained within the global SPI map are shown below and are referenced throughout the specification as they apply. The SPI register tables also specify the effect of the internal reset signals assertion on each bit field (the symbol '-' is used to indicate that the register is not affected by the relevant reset signal').

Global SPI global status word

The Global SPI of L9679P contains an 11-bit word that returns global status information. The Global Status Word (GSW) of the Global SPI is the most significant 11 bits of MISO_G data.

Table 7. Global SPI Global Status Word

MISO_G	GSW	Name	POR	WSM	SSM	Description
31	10	SPIFLT	0	0	0	SPI Fault, set if previous SPI frame had wrong parity check or wrong number of bits, cleared upon read 0 No fault 1 Fault
30	9	DEPOK	0	0	0	General Deployment Successful Flag, logical OR of the corresponding CHxDS bits (bit 15) in DSRx Registers 0 All the DSRx-CHDS bits are 0 1 At least one of the DSRx-CHDS bits is 1
29	8	0	0	0	0	Unused
28	7	WDT/TM_S	0	0	0	State of WDT/TM pin 0 WDT/TM=0 1 WDT/TM=1
27	6	ERSTATE	0	0	0	Set when Powermode state machine is in ER state 0 Powermode state machine is not in ER state 1 Powermode state machine is in ER state
26	5	POWERFLT	0	0	0	Fault present in Power State Register, logical OR between bits from 18 to 9 of POWER_STATE Register 0 All the bits from 18 to 9 in the POWER_STATE Registers are 0s 1 At least one of the bits from 18 to 9 in the POWER_STATE Registers is 1
25	4	FLT	1	1	1	Fault present in Fault Status Register (FLTSR), logical OR between all bits of FLTSR 0 All the bits in the Fault Status Register (FLTSR) are 0s 1 At least one of the bits in the Fault Status Register (FLTSR) is 1
24	3	CONVRDY2	0	0	0	ADC Conversion of request C or D has been completed so new results are available 0 No new data available 1 New data available

Table 7. Global SPI Global Status Word (continued)

MISO_G	GSW	Name	POR	WSM	SSM	Description
23	2	CONVRDY1	0	0	0	ADC Conversion of request A or B has been completed so new results are available 0 No new data available 1 New data available
22	1	ERR_WID	0	0	0	Write address of previous SPI frame is not permitted in current operating phase 0 No Error 1 Error
21	0	ERR_RID	0	0	0	Read address received in the actual SPI frame is unused so data in the response is don't care 0 No Error 1 Error

Global SPI read/write register

7.3.1 Fault status register (FLTSR)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	ERCHARGE_OT	0	ERBST_OT	CLKFRERR	WD2 retry cnt				OTPCRC_ERR	WD2_LO	WD2_TM	WD2_WDR	WD1_LO	WD1_TM	WD1_WDR	0	WSMRST	SSMRST	0	POR

ID: 00

Type: R

Read: 0000

Write: -

	POR	WSM	SSM	
ERCHARGE_OT	0	-	-	ER charge over temperature bit Set when over-temp condition detected, cleared on SPI read or POR=1 0 No Fault 1 Fault
ERBST_OT	0	-	-	ER Boost over-temperature bit Set when over-temp condition detected, cleared on SPI read or POR=1 0 No Fault 1 Fault
CLKFRERR	0	-	-	Internal oscillator cross-check error bit Set when osc. error detected, cleared on SPI read or SUPPLY_POR=1 0 No Fault 1 Fault
WD2_retry_cnt[3:0]	$0	$0	$0	Value of WD2 retry counter
OTPCRC_ERR	0	-	-	OTP CRC error bit Set when OTP error detected (tested at release of POR), cleared by POR=1 0 No Fault 1 Fault
WD2_LO	1	0	-	WD2 lockout - reflects WD2 lockout state 0 WD2 Lockout inactive 1 WD2 Lockout active
WD2_TM	0	0	0	WD2 test mode - reflects WD2TM signal state

0 WD2TM=0
1 WD2TM=1

WD2_WDR	0	0	-	WD2 reset latch - set when WD2RESET or STOPPING states are entered, cleared upon read 0 WD2RST signal = 0 1 WD2RST signal = 1
WD1_LO	1	1	-	WD1 lockout - reflects WD1 lockout state Set and cleared per Watchdog Timer Flow Diagram 0 WD1 Lockout inactive 1 WD1 Lockout active
WD1_TM	0	0	0	WD1 test mode - reflects WD1TM signal state Set and cleared per Watchdog Timer Flow Diagram 0 WD1TM=0 1 WD1TM=1
WD1_WDR	0	0	-	WD1 reset latch Set and cleared per Watchdog Timer Flow Diagram 0 WD1_WDR signal = 0 1 WD1_WDR signal = 1
WSMRST	1	1	-	Watchdog state machine reset Set when WSM reset goes to '1', cleared upon SPI read 0 WSM reset has not occurred 1 WSM reset has occurred
SSMRST	1	1	1	Safing state machine reset Set when SSM reset goes to '1', cleared upon SPI read 0 SSM reset has not occurred 1 SSM Reset has occurred
POR	1	-	-	Power on Reset Set when POR goes to '1', cleared upon SPI read 0 POR reset has not occurred 1 POR Reset has occurred

7.3.2 System configuration register (SYS_CFG)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				EN_AUTO_SWITCH_OFF	X	LOW_POWER_MODE	KEEP_ERBST_ON	PSINHSEL	HI_LEV_DIAG_TIME	RSU_SYNCPULSE_SHIFT_CONF	SQMEAS		VMEAS		DCS_PAD_V	SAFESEL	VSF_V	VINGOOD_FILT_SEL	WD1_TO_DIS
MISO	0	0	0	0	EN_AUTO_SWITCH_OFF	0	LOW_POWER_MODE	KEEP_ERBST_ON	PSINHSEL	HI_LEV_DIAG_TIME	RSU_SYNCPULSE_SHIFT_CONF	SQMEAS		VMEAS		DCS_PAD_V	SAFESEL	VSF_V	VINGOOD_FILT_SEL	WD1_TO_DIS

ID: 01

Type: R/W

Read: 0100

Write: 0002

	POR	WSM	SSM	
EN_AUTO_SWITCH_OFF	0	0	0	Enable auto switch off ISRC current source and DCS regulator after measurement completion 0 Auto switch off disabled 1 Auto switch off enabled
LOW_POWER_MODE	0	-	-	Selection of over current detection for SYNCBOOST, SATBUCK and VCCBUCK 0 High current level 1 Low current level
KEEP_ERBST_ON	1	1	1	ER Boost behaviour during ER state 0 ER Boost is disabled 1 ER Boost stay enabled
PSINHSEL	1	1	1	PSINH engine mode select Updated by SSM_RESET or SPI write

				0 Internal 1 External
HI_LEV_DIAG_TIME	0	0	0	Selection of duration of high level squib diagnostics 0 Short time (see high level diag diagram) 1 Long time (see high level diag diagram)
RSU_SYNCPULSE_ SHIFT_CONF	0	0	0	Selection of sync pulses shift duration 0 Long time 1 Short time
SQMEAS	00	00	00	Sample number in DC sensor, squib measurement and temperature conversions Updated by SSM_RESET or SPI write 00 8 samples 01 16 samples 10 4 samples 11 2 sample
VMEAS	00	00	00	Sample number in any other voltage measurement conversions Updated by SSM_RESET or SPI write 00 4 samples 01 16 samples 10 8 samples 11 1 sample
DCS_PAD_V	0	0	0	Passenger inhibit measurement mode 0 Current 1 Voltage
SAFESEL	1	1	1	Safing engine mode select Updated by SSM_RESET or SPI write 0 Internal safing engine 1 external safing engine

VSF_V	0	0	0	VSF voltage select Updated by SSM_RESET or SPI write 0 20V 1 25V
VINGOOD_FILT_SEL	0	-	-	Selector of filter time for VINGOOD going low (time is fixed to 3.5 µs for VINGOOD going high) 0 1 µs 1 3.5 µs
WD1_TO_DIS	0	0	-	Disable of initial 500 ms timeout function of WD1 state machine Updated by WSM_RESET or SPI write 0 timeout function is enabled 1 timeout function is disabled

7.3.3 System control register (SYS_CTL)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				RESTART_SYBST_SEL	PD&VRCM_SEL	KEEP_SYNCBST_ON	VIN_TH_SEL	VBATMON_TH_SEL		ER_BST_V	ER_CUR_EN		ER_BST_EN	SYNCBST_EN	SPI_OFF	x	ERSWITCH_LIM_SEL	SYBST_V	SAT_V
MISO	0	0	0	0	RESTART_SYBST_SEL	PD&VRCM_SEL	KEEP_SYNCBST_ON	VIN_TH_SEL	VBATMON_TH_SEL		ER_BST_V	ER_CUR_EN		ER_BST_EN	VSUP_EN	SPI_OFF	0	ERSWITCH_LIM_SEL	SYBST_V	SAT_V

ID: 02

Type: R/W

Read: 0200

Write: 0004

	POR	WSM	SSM	
RESTART_SYBST_SEL	0	-	-	Selection of comparator used to restart sync boost in erstate (don't care in case SYS_CTL(KEEP_SYNCBST_ON) bit is high) 0 VIN comparator is used; syncboost is switched off entering erstate and switched on once VIN goes above VIN_fastslope threshold. 1 SYNCBST comparator is used; syncboost is switched off entering erstate and switched on when SYNCBST voltage falls down VSYNCBST_RESTART_TH threshold (this condition requires that SYNCBST voltage has been pulled up above the same threshold previously).
PD&VRCM_SEL	0	0	0	Squib pull down current level and VRCM leakage to GND threshold selection 0 1 mA pull down current and 450 µA VRCM leakage to GND threshold 1 5 mA pull down current and 2 mA VRCM leakage to GND threshold
KEEP_SYNCBST_ON	1	-	-	SYNC Boost behaviour during ER state 0 SYNC Boost is disabled entering in ER state 1 SYNC Boost stay enabled in ER state. If boost is OFF in ER state and this command is received during that state the boost is switched on.
VIN_TH_SEL	0	0	0	VIN comparators threshold selector 0 VINGOOD= VINgood0 1 VINGOOD= VINgood1

VBATMON_TH_SEL	00	00	00	VBATMON comparators threshold selector 00 VBGOOD= VBgood0 01 VBGOOD= VBgood1 10 VBGOOD= VBgood2 11 VBGOOD= VBgood0
ER_BST_V	0	0	0	ER Boost voltage select Updated by SSM_RESET or SPI write 0 set 23 V boost 1 set 33 V boost
ER_CUR_EN	00	00	00	ER charge / discharge control 00 Current sources off 01 ER charge enabled 10 ER discharge enabled 11 Current sources off
ER_BST_EN	1	1	1	Boost enable Updated by SSM_RESET or SPI write 0 ER_BOOST OFF request 1 ER_BOOST ON request
SYNCBST_EN	1	1	1	Syncboost enable Updated by SSM_RESET or SPI write 0 SYNC_BOOST OFF request 1 SYNC_BOOST ON request
SPI_OFF	0	0	0	Go to POWER OFF state from POWERMODE SHUTDOWN state Updated by SSM_RESET or SPI write while in POWERMODE SHUTDOWN state 0 no effect 1 transition to POWER OFF state
ERSWITCH_LIM_SEL	0	-	-	ERswitch current limitation select Updated by POR or SPI write 0 Low current limit 1 High current limit is no more available
SYBST_V	0	0	0	Sync Boost voltage select Updated by SSM_RESET or SPI write 0 Low - syncboost = 12 V 1 High - syncboost = 14.75 V

SAT_V	0	0	0	SatBuck and Satellite Interface voltage select Updated by SSM_RESET or SPI write 0 Low - satbuck=7.2V 1 High - satbuck=9V

7.3.4 SPI Sleep command register (SPI_SLEEP)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				$3C95															
MISO	0	0	0	0	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID: 03

Type: W

Read: -

Write: 0006

	POR	WSM	SSM	
SLEEP_MODE	N/A	N/A	N/A	Non-latched command that allows transition into POWERMODE_SHUTDOWN state according to the Power Control State Flow Diagram

7.3.5 System state register (SYS_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	OPER_CTL_STATE			0	0	0	0	0	POWER_CTL_STATE		

ID: 04

Type: R

Read: 0400

Write: -

	POR	WSM	SSM	
OPER_CTL_STATE[2:0]	000	000	000	Reports Operating Control State Updated per Power Up Phases diagram 000 = INIT 001 = DIAG 010 = SAFING 011 = SCRAP 100 = ARMING 101 unused 110 unused 111 unused
POWER_CTL_STATE[2:0]	000	-	-	Reports Power Control State Updated per Power Control State Flow Diagram 000 = AWAKE 001 = STARTUP 010 = RUN 011 = ER 100 = POWER MODE SHUTDOWN 101 unused 110 unused 111 unused

7.3.6 Power state register (POWER_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	WAKEUP	VBBAD	NOT_VBGOOD	VINBAD	NOT_VINGOOD	S_BST_NOK	SATBUCK_NOK	ER_BST_NOK	VCC_UV	VCC_OV	0	ER_BST_ON	ER_CHRG_ON	ER_LCDIS_ON	ER_HCDIS_ON	ER_SW_ON	S_BST_ACT	SATBUCK_ACT	VCC_ACT	VSF_ACT

ID: 05

Type: R

Read: 0500

Write: -

	POR	WSM	SSM	
WAKEUP	-	-	-	WAKEUP pin status Set and cleared based on voltage 0 WAKEUP pin < WU_off 1 WAKEUP pin > WU_on
VBBAD	-	-	-	VBATMON bad pin status Set and cleared based on voltage 1 VBATMON < VBBAD 0 VBATMON > VBBAD
NOT_VBGOOD	-	-	-	VBATMON good pin status Set and cleared based on voltage 1 VBATMON < VBGOOD 0 VBATMON > VBGOOD
VINBAD	-	-	-	VIN bad pin status Set and cleared based on voltage 0 VIN > VINBAD 1 VIN < VINBAD
NOT_VINGOOD	-	-	-	VIN good pin status Set and cleared based on voltage 0 VIN > VINGOOD 1 VIN < VINGOOD
S_BST_NOK	-	-	-	SYNCBOOST bad pin status

				Set based on voltage, cleared on SPI read 1 V_SYNCBOOST < SYNCBOOST_OK 0 V_SYNCBOOST > SYNCBOOST_OK
SATBUCK_NOK	-	-	-	SATBUCK bad pin status Set based on voltage, cleared on SPI read 1 V_SATBUCK < SATBUCK_OK 0 V_SATBUCK > SATBUCK_OK
ER_BST_NOK	-	-	-	ERBOOST pin status Set and cleared based on voltage 1 V_ERBOOST < ERBOOST_OK 0 V_ERBOOST > ERBOOST_OK
VCC_UV	-	-	-	VCC_UV status Set based on voltage, cleared on SPI read 0 VCC > VCC_UV 1 VCC < VCC_UV
VCC_OV	-	-	-	VCC_OV status Set based on voltage, cleared on SPI read 0 VCC < VCC_OV 1 VCC > VCC_OV
ER_BST_ON	0	-	-	ERBOOST_ON state Updated according to ER_BOOST Control Behavior diagram 0 RBOOST_OFF or ERBOOST_OT state or ER_BST_STBY state (boost not running) 1 ERBOOST_ON state (boost running)
ER_CHRG_ON	0	0	0	ERCHARGE_ON state Updated according to ER_CHARGE Power Mode Control diagram 0 ERCHARGE_ON = 0 1 ERCHARGE_ON = 1
ER_LCDIS_ON	0	-	-	ER Low Current Discharge State Updated according to ER Low current discharge state diagram 0 ER_LCDIS_OFF 1 ER_LCDIS_ON

ER_HCDIS_ON	0	-	-	ER High Current Discharge State Updated according to ER High Current discharge state diagram 0 ER_HCDIS_OFF 1 ER_HCDIS_ON
ER_SW_ON	0	-	-	ER_SWITCH State Updated according to ER Switch state diagram 0 ER_SWITCH_OFF 1 ER_SWITCH_ON
S_BST_ACT	0	-	-	SYNCBOOST Active state Updated according to SYNCBOOST Power Mode Control state diagram 0 SYNCBOOST supply in SYNCBOOST_OFF state 1 SYNCBOOST supply in SYNCBOOST_ON state
SATBUCK_ACT	0	0	0	SATBUCK Active state Updated according to SATBUCK Power Mode Control state diagram 0 SATBUCK supply in SATBUCK_OFF state 1 SATBUCK supply in SATBUCK_ON state
VCC_ACT	0	-	-	Buck Active state Updated according to VCC Power Mode Control state diagram 0 VCC supply in VCC_OFF or VCC_SHUTDOWN states 1 VCC supply in VCC_RAMPUP or VCC_ON states
VSF_ACT	0	0	0	VSF Active state Updated according to VSF Control Logic diagram 0 VSF_EN = 0 1 VSF_EN = 1

7.3.7 Deployment configuration registers (DCR_x)

Deployment Configuration Channel 0 (DCR_0)
Deployment Configuration Channel 2 (DCR_2)
Deployment Configuration Channel 4 (DCR_4)
Deployment Configuration Channel 6 (DCR_6)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	Deploy_Time						Dep_Current		Dep_expire_time		X	PD_CURR_CSR
MISO	0	0	0	0	0	0	0	0	Deploy_Time						Dep_Current		Dep_expire_time		0	PD_CURR_CSR

ID: 06 (DCR_0)
08 (DCR_2)
0A (DCR_4)
0C (DCR_6)

Type: R/W

Read: 0600 (DCR_0)
0800 (DCR_2)
0A00 (DCR_4)
0C00 (DCR_6)

Write: 000C (DCR_0)
0010 (DCR_2)
0014 (DCR_4)
0018 (DCR_6)

	POR	WSM	SSM	
Deploy_Time[5:0]	0000 00	0000 00	0000 00	Default deployment time = 0 µs (no deployment, 8 us pulse output on ARM1 pin during PULSE TEST) Deployment time: actual deployment time (ms) = Deploy_Time*0.064ms (0.064ms/count up to 4.032ms max)
Dep_Current[1:0]	00	00	00	Deployment Current limit select Updated by SSM_RESET or SPI write while in DIAG state 00 Unused (no deploy) 01 1.75 A min 10 1.2 A min 11 Unused (no deploy)
Dep_expire_time[1:0]	00	00	00	Deploy command expiration timer select

Updated by SSM_RESET or SPI write while in DIAG state

00 500 ms
01 250 ms
10 125 ms
11 0 ms

PD_CURR_CSR 0 0 0 Pull down current control for Common SR connection
Updated by SSM_RESET or SPI write

0 PD Current OFF only for channel selected for diagnostic measurement, ON for all other channel

1 PD Current OFF for both channels of the channel pair selected for diagnostic measurement, ON for all other channel

Deployment Configuration Channel 1 (DCR_1)
Deployment Configuration Channel 3 (DCR_3)
Deployment Configuration Channel 5 (DCR_5)
Deployment Configuration Channel 7 (DCR_7)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	Deploy_Time						Dep_Current		Dep_expire_time		X	X
MISO	0	0	0	0	0	0	0	0	Deploy_Time						Dep_Current		Dep_expire_time		0	0

ID: 07 (DCR_1)
09 (DCR_3)
0B (DCR_5)
0D (DCR_7)

Type: R/W

Read: 0700 (DCR_1)
0900 (DCR_3)
0B00 (DCR_5)
0D00 (DCR_7)

Write: 000E (DCR_1)
0012 (DCR_3)
0016 (DCR_5)
001A (DCR_7)

	POR	WSM	SSM	
Deploy_Time[5:0]	0000 00	0000 00	0000 00	Default deployment time = 0 µs (no deployment, 8 us pulse output on ARM1 pin during PULSE TEST) Deployment time: actual deployment time (ms) = Deploy_Time*0.064 ms (0.064 ms/count up to 4.032 ms max)
Dep_Current[1:0]	00	00	00	Deployment Current limit select Updated by SSM_RESET or SPI write while in DIAG state 00 Unused (no deploy) 01 1.75A min 10 1.2A min 11 Unused (no deploy)
Dep_expire_time[1:0]	00	00	00	Deploy command expiration timer select Updated by SSM_RESET or SPI write while in DIAG state 00 500 ms 01 250 ms 10 125 ms 11 0 ms

7.3.8 Deployment command (DEPCOM)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	CHBDEPREQ	CHADEPREQ	CH9DEPREQ	CH8DEPREQ	CH7DEPREQ	CH6DEPREQ	CH5DEPREQ	CH4DEPREQ	CH3DEPREQ	CH2DEPREQ	CH1DEPREQ	CH0DEPREQ
MISO	0	0	0	0	0	0	0	0	CHBDEP	CHADEP	CH9DEP	CH8DEP	CH7DEP	CH6DEP	CH5DEP	CH4DEP	CH3DEP	CH2DEP	CH1DEP	CH0DEP

ID: 12

Type: R/W

Read: 1200

Write: 0024

	POR	WSM	SSM	
CHxDEPREQ	N/A	N/A	N/A	Channel x Deploy Request - non-latched channel-specific deploy request 0 No change to deployment control for channel x 1 Clear and start Expiration timer if in ARMING or SAFING state and in DEPLOY_ENABLED state
CHxDEP	0	0	0	Channel x deployment expiration timer enable Set when SPI_DEPCOM(CHxDEPREQ=1) AND in ARMING or SAFING state AND in DEP_ENABLED state Cleared on SSM_RESET OR when in DEP_DISABLED state OR when Deploy Expiration Timer x reaches timeout threshold 1 Expiration timer enabled - Deploy command still valid 0 Expiration Timer disabled - Deploy command no more valid

7.3.9 Deployment status registers (DSR_x)

Deployment Status Channel 0 (DSR_0)
Deployment Status Channel 1 (DSR_1)
Deployment Status Channel 2 (DSR_2)
Deployment Status Channel 3 (DSR_3)
Deployment Status Channel 5 (DSR_5)
Deployment Status Channel 6 (DSR_6)
Deployment Status Channel 7 (DSR_7)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	CHxDS	CHxSTAT	0	DCRxERR							DEP_CHx_ExpTimer					

ID: 13 (DSR_0)
14 (DSR_1)
15 (DSR_2)
16 (DSR_3)
17 (DSR_4)
18 (DSR_5)
19 (DSR_6)
1A (DSR_7)

Type: R

Read: 1300 (DSR_0)
1400 (DSR_1)
1500 (DSR_2)
1600 (DSR_3)
1700 (DSR_4)
1800 (DSR_5)
1900 (DSR_6)
1A00 (DSR_7)

Write: -

	POR	WSM	SSM	
CHxDS	0	0	0	Channel x deployment successful Updated according to Deployment Driver Control Logic (set when deployment terminates on ch x due to deploy timer timeout, cleared on SSM_RESET OR when deployment starts on ch x) 0 Deployment not successful 1 Deployment successful
CHxSTAT	0	0	0	Channel x deployment status Updated according to Deployment Driver Control Logic (set when deployment starts on ch x, cleared on SSM_RESET OR when deployment terminates due to deploy timer timeout, LS Over current OR GND Loss)

				0 Deployment not in progress 1 Deployment in progress
DCRxERR	0	0	0	Deployment configuration register error 0 Deploy configuration change accepted and stored in memory 1 Deploy configuration change rejected because deploy is in progress (or DEP_EXPIRE_TIME changed when in DEP_ENABLED state)
DEP_CHx_ExpTimer[5:0]	000000	000000	000000	Channel x Deployment Expiration Timer value 8 ms/count Updated according to Deployment Driver Control Logic (Cleared on SSM_RESET OR when Exp Timer times out OR when SPI_DEPREQx is received while in DEP_ENABLED state AND in ARMING or SAFING states)

7.3.10 Deployment current monitor registers (DCMTSxy)

Deployment Current Monitor Status Channel 0,1 (DDCMTS01)
Deployment Current Monitor Status Channel 2,3 (DDCMTS23)
Deployment Current Monitor Status Channel 4,5 (DDCMTS45)
Deployment Current Monitor Status Channel 6,7 (DDCMTS67)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	Current_Mon_Timer_y[7:0]								Current_Mon_Timer_x[7:0]							

ID: 1F (DDCMTS01)
20 (DDCMTS23)
21 (DDCMTS45)
22 (DDCMTS67)

Type: R

Read: 1F00 (DDCMTS01)
2000 (DDCMTS23)
2100 (DDCMTS45)
2202 (DDCMTS67)

Write: -

	POR	WSM	SSM	
Current_Mon_Timer_y[7:0]	$00	$00	$00	Channel y current monitor timer value corresponding to SPI command DCMTSxy. Set to default (cleared) on SSM_RESET or when a new deployment starts on channel y. Increments each 16 µs while deployment current exceeds monitor threshold on channel y
Current_Mon_Timer_x[7:0]	$00	$00	$00	Channel x current monitor timer value corresponding to SPI command DCMTSxy. Set to default (cleared) on SSM_RESET or when a new deployment starts on channel x. Increments each 16 µs while deployment current exceeds monitor threshold on channel y

7.3.11 Deploy enable register (SPIDEPEN)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				DEPEN_WR[15:0]															
MISO	0	0	0	0	DEPEN_STATE[15:0]															

ID: 25

Type: R/W

Read: 2500

Write: 004A

	POR	WSM	SSM	
DEPEN_WR[15:0]	N/A	N/A	N/A	Non-latched encoded value for LOCK / UNLOCK command $0FF0 LOCK - enter DEP_DISABLED state $F00F UNLOCK - enter DEP_ENABLED state.
DEPEN_STATE[15:0]	$0FF0	$0FF0	$0FF0	Deploy Enabled State Updated according to Global SPI Deployment Enable State Diagram $0FF0 In DEP_DISABLED state $F00F In DEP_ENABLED state

7.3.12 Deployment ground loss register (LP_GNDLOSS)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	GNDLOSSB	GNDLOSSA	GNDLOSS9	GNDLOSS8	GNDLOSS7	GNDLOSS6	GNDLOSS5	GNDLOSS4	GNDLOSS3	GNDLOSS2	GNDLOSS1	GNDLOSS0

ID: 26

Type: R

Read: 2600

Write: -

	POR	WSM	SSM	
GNDLOSSx	0	0	0	Loop x Squib Ground loss Cleared upon SSM_RESET or SPI read. Set when GND loss is detected during deployment or loop diag's (HS sw test, LS sw test, squib resistance) 0 Loss of ground not detected 1 Loss of ground detected

7.3.13 Device version register (VERSION_ID)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	DEVICE ID			0	0	VERSN					

ID: 27

Type: R

Read: 2700

Write: -

	POR	WSM	SSM	
DEVICE ID	-	-	-	Identification of the device Static value - never updated 001 Low end 010 Medium end 011 High end
VERSN	-	-	-	Identification of the silicon version Static value - never updated 000000 AA version 000001 AB version 001000 BA version 001001 BB version 010000 CA version

7.3.14 Watchdog retry configuration register (WD_RETRY_CONF)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-						WD2_ERR_TH			WD2_RETRY_TH			X	X	X	X	X	WD1_RETRY_TH		
MISO	0	0	0	0	0	0	WD2_ERR_TH			WD2_RETRY_TH			0	0	0	0	0	WD1_RETRY_TH		

ID: 28

Type: R/W

Read: 2800

Write: 0050

	POR	WSM	SSM	
WD2_ERR_TH	4	4	-	WD2 error counter threshold (number of W2 reset permitted before going to WD2_STOP state)
WD2_RETRY_TH	4	4	-	WD2 retry counter threshold (number of W2 errors permitted before asserting WD2_Lockout and increment WD2_ERRcnt)
WD1_RETRY_TH	7	7	-	WD1 retry counter threshold (number of WD errors permitted before latching WD1_LOCKOUT=1)

7.3.15 Watchdog timer configuration register (WDTCR)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	WD1_MODE	WDTMIN[6:0]							WDTDELTA[6:0]						
MISO	0	0	0	0	0	WD1_MODE	WDTMIN[6:0]							WDTDELTA[6:0]						

ID: 2A

Type: R/W

Read: 2A00

Write: 0054

	POR	WSM	SSM	
WD1_MODE	0	0	-	WD1_MODE Updated by WSM RESET or SPI write while in WD1 INIT state 0 Fast WD1 mode - nominal 8 µs timer resolution (2 ms max value) 1 Slow WD1 mode - nominal 64 µs timer resolution (16.3 ms max value)

WDTMIN[6:0]	$32	$32	-	WD1 window minimum value - resolution according to WD1_MODE bit ($32 = 400 µs in WD1 fast mode) Updated by WSM RESET or SPI write while in WD1 INT state.
WDTDELTA[6:0]	$19	$19	-	WD1 window delta value - WDTMAX = WDTMIN + WDTDELTA - resolution according to WD1_MODE bit ($19 = 200 µs in WD1 fast mode) Updated by WSM RESET or SPI write while in WD1 INT state.

7.3.16 WD1 timer control register (WD1T)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	WD1CTL[1:0]	
MISO	0	0	0	0	WD1_TIMER								0	0	0	0	0	0	WD1CTL[1:0]	

ID: 2B

Type: RW

Read: 2B00

Write: 0056

	POR	WSM	SSM	
WD1CTL[1:0]	00	00	00	WD1 Control command Updated by SSM_RESET or SPI write 00 NOP 01 Code ‘A’ 10 Code ‘B’ 11 NOP 1 Slow WD1 mode - nominal 64µs timer resolution (16.3ms max value)
WD1_TIMER	$00	$00	$00	WD1 window timer value -Cleared by SSM_RESET or by WD1 refresh, incremented every 8 µs or 64 µs while in WD1_RUN or WD1_TEST states

7.3.17 WD state register (WDSTATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	WD1_ERR_CNT[3:0]				WD_STATE[2:0]			WD2_ERR_CNT[3:0]				WD2_STATE[2:0]			

ID: 2C

Type: R

Read: 2C00

Write: -

	POR	WSM	SSM	
WD1_ERR_CNT[3:0]	0000	0000	-	Watchdog 1 error counter Updated according to Watchdog State Diagram
WD1_STATE[2:0]	000	000	-	Watchdog state Updated according to Watchdog State Diagram 000 INITIAL 001 RUN 010 TEST 011 RESET 100 OVERRIDE
WD2_ERR_CNT[3:0]	0000	0000	-	Watchdog 2 error counter Updated according to Watchdog State Diagram
WD2_STATE[3:0]	0000	0000	-	Watchdog state Updated according to Watchdog State Diagram 0000 INITIAL 0001 OVERRIDE 0010 INITSEED 0011 RUN 0100 TEST 0101 QUAL 0110 LOCK 0111 STOPPING 1000 STOP 1001 RESET

7.3.18 Clock configuration register (CLK_CONF)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	VCCBCK_F_SEL[1:0]		SATBCK_F_SEL[1:0]		SYBST_F_SEL[1:0]		AUX_SS_DIS	MAIN_SS_DIS	ERBST_F_SEL[1:0]	
MISO	0	0	0	0	0	0	0	0	0	0	VCCBCK_F_SEL		SATBCK_F_SEL		SYBST_F_SEL		AUX_SS_DIS	MAIN_SS_DIS	ERBST_F_SEL	

ID: 2D

Type: R/W

Read: 2D00

Write: 005A

	POR	WSM	SSM	
VCCBCK_F_SEL[1:0]	00	-	-	VCCBuck switching frequency select Updated by POR or SPI write 00 1.88 MHz 01 2.13 MHz 10 2.00 MHz 11 2.00 MHz
SATBCK_F_SEL[1:0]	00	-	-	SatBuck switching frequency select Updated by POR or SPI write 00 1.88 MHz 01 2.13 MHz 10 2.00 MHz 11 2.00 MHz
SYBST_F_SEL[1:0]	00	-	-	Sync Boost switching frequency select Updated by POR or SPI write 00 1.88 MHz 01 2.13 MHz 10 2.00 MHz 11 2.00 MHz
AUX_SS_DIS	1	-	-	Auxiliary oscillator Spread Spectrum disable Updated by POR or SPI write 0 Spread Spectrum enabled 1 Spread Spectrum disabled

MAIN_SS_DIS	0	-	-	Main oscillator Spread Spectrum disable Updated by POR or SPI write 0 Spread Spectrum enabled 1 Spread Spectrum disabled
ERBST_F_SEL[1:0]	00	-	-	ER Boost switching frequency select Updated by POR or SPI write 00 1.88 MHz 01 2.13 MHz 10 2.00 MHz 11 2.00 MHz

7.3.19 Scrap seed read command register (SCRAP_SEED)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	0	0	0	SEED[7:0]							

ID: 2E

Type: R

Read: -

Write: 2E00

	POR	WSM	SSM	
	N/A	N/A	N/A	
SEED[7:0]	$00	$00	$00	Random scrap seed value - generated from a free-running 8-bit counter

7.3.20 Scrap key write command register (SCRAP_KEY)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	KEY[7:0]							
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID: 2F

Type: W

Read: -

Write: 005E

	POR	WSM	SSM	
	N/A	N/A	N/A	
KEY[7:0]	$00	$00	$00	KEY value submitted to the SCRAP state machine (correct value is derived from the seed value using a simple logical inversion on the even-numbered bits (0, 2, 4, 6))

7.3.21 Scrap state entry command register (SCRAP_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				$3535															
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID: 30

Type: W

Read: -

Write: 0060

POR	WSM	SSM	
N/A	N/A	N/A	
			Non-latched Scrap State entry command
			Enter Scrap state from DIAG state

7.3.22 Safing state entry command register (SAFING_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				$ACAC															
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID: 31

Type: W

Read: -

Write: 0062

POR	WSM	SSM	
N/A	N/A	N/A	Non-latched Safing State entry command Enter safing state from DIAG state and clear arming pulse stretch counter (if received in DIAG or SAFING state)

7.3.23 WD2 recover write command register (WD2_RECOVER)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	**$AA**							
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID: 32

Type: W

Read: -

Write: 0064

POR	WSM	SSM	
N/A	N/A	N/A	Non-latched command to clear WD2_retry counter during WD2 LOCK state

7.3.24 WD2 seed read command register (WD2_SEED)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	WD2_PREV_KEY[7:0]								WD2_SEED[7:0]							

ID: 33

Type: R

Read: -

Write: 3300

	POR	WSM	SSM	
WD2_PREV_KEY[7:0]	$0D	$0D	$0D	Previous WD2 key value - stored key from previous comparison
WD2_SEED[7:0]	$F0	$F0	$F0	Random WD2 seed value - generated from a free-running 8-bit counter

7.3.25 WD2 key write command register (WD2_KEY)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	KEY[7:0]							
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID: 34

Type: W

Read: -

Write: 0068

	POR	WSM	SSM	
KEY[7:0]	$00	$00	$00	KEY value submitted to the WD2 state machine (correct value is derived from WD2_KEY = WD2_SEED ‡ WD2_PREV_KEY + $01 where ‡ denotes a bit-wise XOR operation)

7.3.26 WD test command register (WD_TEST)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				WD1_TEST = $3C								WD2_TEST = $3C							
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID: 35

Type: W

Read: -

Write: 006A

POR	WSM	SSM	
N/A	N/A	N/A	Non-latched WD1 and WD2 Test Commands WD1_TEST and WD2_TEST SPI command as described in Watchdog State Diagram

7.3.27 System diagnostic register (SYSDIAGREQ)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	DSTEST[3:0]			
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTEST[3:0]			

ID: 36

Type: R/W

Read: 3600

Write: 006C

	POR	WSM	SSM	
DSTEST[3:0]	0000	0000	0000	Diagnostic State Test selection

Updated by SSM_RESET or SPI write while in DIAG state

0000 = all outputs inactive
0001 = ARM 1 pin active
0010 = ARM 2 pin active
0011 = ARM 3 pin active
0100 = ARM 4 pin active
0101 = PSINHB pin inactive (high)
0110 = VSF regulator active
0111 = HS squib driver FET active
1000 = LS squib driver FET active
1001 = Output deployment timing pulses on ARM1 (separated by 8 ms)
1010 = HS squib driver FET active to test full path (FET switched off by the comparator used in the deployment current timer monitor)
1011 - 1111 = all outputs inactive

7.3.28 Diagnostic result register for deployment loops (LPDIAGSTAT)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	DIAG_LEVEL	TIP	0	FP	FETON	HS_DRV_OK	HSR_HI	HSR_LO	RES_MEAS_CHSEL/HIGH_LEV_DIAG_SELECTED				SBL	STG	STB	SQP	LEAK_CHSEL			

ID: 37

Type: R

Read: 3700

Write: -

	POR	WSM	SSM	
DIAG_LEVEL	0	0	0	Diagnostic mode selector Not present for low level diagnostic Updated by SSM_RESET or SPI write to LPDIAGREQ 0 low level mode 1 high level mode
TIP	0	0	0	High level diagnostic test is running Updated by SSM_RESET or Loops diagnostic state machine 0 High level diagnostic test is not running 1 High level diagnostic test is running
FP	0	0	0	Fault present before requested diagnostic Updated by SSM_RESET or Loops diagnostic state machine 0 Fault not present before requested diagnostic 1 Fault present before requested diagnostic
FETON	0	0	0	FET activation during diagnostic Updated by SSM_RESET or Loops diagnostic state machine or when HS or LS FET is activated during DIAG state

0 FET is off during diagnostic

1 FET is on during diagnostic

HS_DRV_OK 0 0 0 FET Test Status

Updated by SSM_RESET or Loops diagnostic state machine or when driver full path test is run test is run

0 HS squib driver full path test did not complete successfully

1 HS squib driver full path test complete successfully

HSR_HI 0 0 0 HSR Diagnostic - HIGH Range

Updated by SSM_RESET or Loops diagnostic state machine or when squib resistance test is run

0 HSR measurement < HSR HIGH value

1 HSR measurement > HSR HIGH value

HSR_LO 0 0 0 HSR Diagnostic - Low Range

Updated by SSM_RESET or Loops diagnostic state machine or when squib resistance test is run

1 HSR measurement< HSR LOW value

0 HSR measurement > HSR LOW value

RES_MEAS_CHSEL[3:0] 0000 0000 0000 Channel selected for resistance measurement HIGH_LEV_DIAG_SELECTED[3:0]

Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib resistance channel selected

0000 = Ch 0	0000 No diagnostic selected
0001 = Ch 1	0001 VRCM CHECK
0010 = Ch 2	0010 Leakage CHECK
0011 = Ch 3	0011 Short Between Loops CHECK
0100 = Ch 4	0100 ER cap ESR measure
0101 = Ch 5	0101Squib resistance range CHECK
0110 = Ch 6	0110 Squib resistance measurement
0111 = Ch 7	0111 FET test
0100 - 1111 None Selected	

SBL 0 0 0 Short between loop state

Updated by SSM_RESET or Loops diagnostic state machine

0 Short between squib loops is not present

1 Short between squib loops is present

STG 0 0 0 Short to Ground Test Status

				Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib leakage diagnostic 0 STG not detected 1 STG detected
STB	0	0	0	Short to Battery Test Status Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib leakage diagnostic 0 STB not detected 1 STB detected
SQP	0	0	0	Squib PIN where leakage test has been performed Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib leakage diagnostic 0 SRx 1 SFx
LEAK_CHSEL[3:0]	0000	0000	0000	Channel selected for leakage measurement Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib leakage diagnostic 0000 = Ch 0 0001 = Ch 1 0010 = Ch 2 0011 = Ch 3 0100 = Ch 4 0101 = Ch 5 0110 = Ch 6 0111 = Ch 7 1100 - 1111 None Selected

7.3.29 Loops diagnostic configuration command register for low level diagnostic (LPDIAGREQ)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				DIAG_LEVEL	ISRC_CURR_SEL	PD_CURR	ISRC [1:0]		ISINK	VRCM[1:0]		RES_MEAS_CHSEL[3:0]				LEAK_CHSEL[3:0]			
MISO	0	0	0	0	DIAG_LEVEL	ISRC_CURR_SEL	PD_CURR	ISRC [1:0]		ISINK	VRCM[1:0]		RES_MEAS_CHSEL[3:0]				LEAK_CHSEL[3:0]			

ID: 38

Type: R/W

Read: 3800

Write: 0070

	POR	WSM	SSM	
DIAG_LEVEL	0	0	0	Diagnostic mode selector Updated by SSM_RESET or SPI write 0 low level mode 1 N/A - see description below
ISRC_CURR_SEL	0	0	0	Selection of ISRC current value 0 40 mA 1 8 mA
PD_CURR	0	0	0	Pull down current control Updated by SSM_RESET or SPI write 0 Request OFF only for channels connected to VRCM or ISINK or ISRC, ON for all other channels 1 Request OFF for all channels
ISRC [1:0]	00	00	00	High side current source for channel selected in RES_MEAS_CHSEL[3:0] Updated by SSM_RESET or SPI write 00 = OFF

01 = ON 40 mA/ 8 mA current for channel selected in RES_MEAS_CHSEL, OFF on all other channels

10 = ON bypass current for channel selected in RES_MEAS_CHSEL, OFF ON all other channels

11 = ON ISRC 40mA or 8mA current for channel selected in RES_MEAS_CHSEL and connect the SRM Differential Amplifier to the other squib channel of the selected channel pair

ISINK	0	0	0	Low Side current sink control (max 50 mA) Updated by SSM_RESET or SPI write 0 All channels OFF 1 ON for channel selected by RES_MEAS_CHSEL[3:0], OFF on all other channels
VRCM[1:0]	00	00	00	Voltage Regulator Current Monitor control Updated by SSM_RESET or SPI write 00 VRCM not connected 01 VRCM connected to SFx of channel selected by LEAK_CHSEL[3:0] 10 VRCM connected to SRx of channel selected by LEAK_CHSEL[3:0] and pull down current of the same channel disabled 11 VRCM connected to SRx of channel selected by LEAK_CHSEL[3:0] and pull down current of the same channel enabled (ISINK and ISRC must be switched off)
RES_MEAS_CHSEL[3:0]	0000	0000	0000	Squib Resistance Measurement Channel select - selects the channel and muxes for the resistance test, and the channel for HS driver test (full path fet test) activation Updated by SSM_RESET or SPI write 0000 Channel 0 0001 Channel 1 0010 Channel 2 0011 Channel 3 0100 Channel 4 0101 Channel 5 0110 Channel 6 0111 Channel 7 0100 - 1111 None Selected
LEAK_CHSEL[3:0]	0000	0000	0000	Squib Leakage Measurement Channel select - selects the channel and muxes for the leakage test, and the channel for HS/LS FET test activation. Updated by SSM_RESET or SPI write 0000 Channel 0

0001 Channel 1

0010 Channel 2

0011 Channel 3

0100 Channel 4

0101 Channel 5

0110 Channel 6

0111 Channel 7

0100 - 1111 None Selected

7.3.30 Loops diagnostic configuration command register for high level diagnostic (LPDIAGREQ)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				DIAG_LEVEL	X	X	X	X	X	X	X	HIGH_LEVEL_DIAG_SEL			SQP	LOOP_DIAG_CHSEL[3:0]			
MISO	0	0	0	0	DIAG_LEVEL	0	0	0	0	0	0	0	HIGH_LEVEL_DIAG_SEL			SQP	LOOP_DIAG_CHSEL[3:0]			

ID: 38

Type: R/W

Read: 3800

Write: 0070

	POR	WSM	SSM	
DIAG_LEVEL	0	0	0	Diagnostic mode selector 0 0 N/A - see description above 1 1 high level mode
HIGH_LEVEL_DIAG_SEL	000	000	000	Selection of high level squib diagnostic Updated by SSM_RESET or SPI write 000 No diagnostic selected 001 VRCM CHECK 010 Leakage CHECK 011 Short Between Loops CHECK 100 ER cap ESR measure 101 Squib resistance range CHECK 110 Squib resistance measurement 111 FET test
SQP	0	0	0	Squib pin select for all leakage diagnostic Updated by SSM_RESET or SPI write

0 SRx

1 SFx

LOOP_DIAG_CHSEL[3:0] 0000 0000 0000 Channel select - selects the channel and muxes for all squib diagnostic.

Updated by SSM_RESET or SPI write

0000 Channel 0
0001 Channel 1
0010 Channel 2
0011 Channel 3
0100 Channel 4
0101 Channel 5
0110 Channel 6
0111 Channel 7
1100 - 1111 None Selected

7.3.31 DC sensor diagnostic configuration command register (SWCTRL)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	PSINHPOL	DCS_PDCURR	SWOEN	X	X	CHID[3:0]			
MISO	0	0	0	0	0	0	0	0	0	0	0	PSINHPOL	DCS_PDCURR	SWOEN	0	0	CHID[3:0]			

ID: 39

Type: R/W

Read: 3900

Write: 0072

	POR	WSM	SSM	
PSINHPOL	0	0	0	Selector of in range/ out of range for passenger inhibit function 0 if result is inside thresholds the counter is initialized to start value 1 if result is outside thresholds the counter is initialized to start value
DCS_PDCURR	0	0	0	Disable of all pull down current for DC sensor Updated by SSM_RESET or SPI write 0 OFF for channel under voltage or current measurement, ON for all other channels 1 OFF for all channels

SWOEN	0	0	0	Switch Output Enable Updated by SSM_RESET or SPI write 0 OFF 1 ON
CHID[3:0]	0000	0000	0000	Channel ID - selects DC sensor channel for output activation Updated by SSM_RESET or SPI write 0000 Channel 0 0001 Channel 1 0010 Channel 2 0011 Channel 3 0100 Channel 4 0101 Channel 5 0110 Channel 6 0111 Channel 7 1000 Channel 8 0100 - 1111 None Selected

7.3.32 ADC request and data registers (DIAGCTRL_x)

ADC A control command (DIAGCTRL_A)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	ADCREQ_A[6:0]						
MISO	NEWDATA_A	0	0	ADCREQ_A[6:0]							ADCRES_A[9:0]									

ID: 3A

Type: RW

Read: 3A00

Write: 0074

ADC B control command (DIAGCTRL_B)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	ADCREQ_B[6:0]						
MISO	NEWDATA_B	0	0	ADCREQ_B[6:0]							ADCRES_B[9:0]									

ID: 3B

Type: R/W

Read: 3B00

Write: 0076

ADC C control command (DIAGCTRL_C)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	ADCREQ_C[6:0]						
MISO	NEWDATA_C	0	0	ADCREQ_C[6:0]							ADCRES_C[9:0]									

ID: 3C

Type: R/W

Read: 3C00

Write: 0078

ADC D control command (DIAGCTRL_D)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	ADCREQ_D[6:0]						
MISO	NEWDATA_D	0	0	ADCREQ_D[6:0]							ADCRES_D[9:0]									

ID: 3D

Type: R/W

Read: 3D00

Write: 007A

	POR	WSM	SSM	
NEWDATA_x	0	0	0	New data available from convertion Updated by SSM_RESET or ADC state machine 0 cleared on read 1 convertion finished
ADCREQ_x[6:0]	$00	$00	$00	ADC Request select command Updated by SSM_RESET or SPI write to DIAGCTRL_x Measurement $00 Unused $01 Ground Ref $02 Full scale Ref $03 DCSx voltage $04 DCSx current $05 DCSx resistance $06 Squib x resistance $07 Internal BG reference voltage (BGR) $08 Internal BG monitor voltage (BGM) $09 Vcore $0A Temperature $0B DCS 0 voltage $0C DCS 1 voltage $0D DCS 2 voltage $0E DCS 3 voltage $0F DCS 4 voltage $10 DCS 5 voltage $11 DCS 6 voltage $12 DCS 7 voltage $13 DCS 8 voltage

$14 Vb voltage of ER ESR measure (valid only for ADCREQ_x field of MISO response when ESR measure results are available)
$15 Va voltage of ER ESR measure (valid only for ADCREQ_x field of MISO response when ESR measure results are available)
$16 Vc voltage of ER ESR measure (valid only for ADCREQ_x field of MISO response when ESR measure results are available)
$20 VBATMON pin voltage
$21 VIN pin voltage
$22 Internal analog supply voltage (VINT)
$23 Internal digital supply voltage (VDD)
$24 ERBOOST pin voltage
$25 SYNCBOOST pin voltage
$26 VER pin voltage
$27 SATBUCK voltage
$28 VCC voltage
$29 WAKEUP pin voltage
$2A VSF pin voltage
$2B WDTDIS pin voltage
$2C GPOD0 pin voltage
$2D GPOS0 pin voltage
$2E GPOD1 pin voltage
$2F GPOS1 pin voltage
$30 GPOD2 pin voltage
$31 GPOS2 pin voltage
$32 RSU0 pin Voltage
$33 RSU1 pin Voltage
$34 RSU2 pin Voltage
$35 RSU3 pin Voltage
$36 SS0 pin voltage
$37 SS1 pin voltage
$38 SS2 pin voltage
$39 SS3 pin voltage
$3A SS4 pin voltage
$3B SS5 pin voltage
$3C SS6 pin voltage
$3D SS7 pin voltage
$3E SS8 pin voltage
$3F SS9 pin voltage
$40 SSA pin voltage
$41 SSB pin voltage
$46 SF0
$47 SF1
$48 SF2
$49 SF3
$4A SF4
$4B SF5
$4C SF6
$4D SF7

ADCRES_x[9:0]	$000	$000	$000	10-bit ADC result value corresponding to ADCREQ_x request Updated by SSM_RESET or ADC state machine

7.3.33 Configuration register for switching regulators (SW_REGS_CONF)

	19	18	17	16	15	14	13	12	11	10	9	8	7 6	5 4	3 2	1 0
MOSI	-				LOW_ERBST_ILIM_ERON	EN_VCC_GNDLOSS_DET	EN_SAT_GNDLOSS_DET	SATBCK_LS_ON_DELAY	VCCBCK_LS_ON_DELAY	SATBCK_FORCE_F_SLOPE	SYBST_FORCE_F_SLOPE	ERBST_FORCE_F_SLOPE	VCCBCK_PH_SEL[1:0]	SATBCK_PH_SEL[1:0]	SYBST_PH_SEL[1:0]	ERBST_PH_SEL[1:0]
MISO	0	0	0	0	LOW_ERBST_ILIM_ERON	EN_VCC_GNDLOSS_DET	EN_SAT_GNDLOSS_DET	SATBCK_LS_ON_DELAY	VCCBCK_LS_ON_DELAY	SATBCK_FORCE_F_SLOPE	SYBST_FORCE_F_SLOPE	ERBST_FORCE_F_SLOPE	VCCBCK_PH_SEL	SATBCK_PH_SEL	SYBST_PH_SEL	ERBST_PH_SEL

ID: 3F

Type: R/W

Read: 3F00

Write: 007E

	POR	WSM	SSM	
LOW_ERBST_ILIM_ERON	0	-	-	ERBoost current limitation behavior selection Updated by POR or SPI write 0 ERBoost current limitation is NOT reduced if ER Switch is activated 1 ERBoost current limitation is reduced if ER Switch is activated
EN_VCC_GNDLOSS_DET	0	-	-	New VCC ground loss detection enable Updated by POR or SPI write 0 run time ground loss detection disabled 1 run time ground loss detection enabled
EN_SAT_GNDLOSS_DET	0	-	-	New SAT ground loss detection enable Updated by POR or SPI write 0 run time ground loss detection disabled 1 run time ground loss detection enabled
SATBCK_LS_ON_DELAY	0	-	-	SATBuck low side activation delay Updated by POR or SPI write

0 No delay is applied

1 Delay is applied

VCCBCK_LS_ON_DELAY	0	-	-	VCCBuck low side activation delay Updated by POR or SPI write 0 No delay is applied 1 Delay is applied
SATBCK_FORCE_F_SLOPE	0	-	-	SatBuck fast slope selection Updated by POR or SPI write 0 Fast slope activation depends on VIN voltage 1 Fast slope is forced ON
SYBST_FORCE_F_SLOPE	0	-	-	SyncBoost fast slope selection Updated by POR or SPI write 0 Fast slope activation depends on VIN voltage 1 Fast slope is forced ON
ERBST_FORCE_F_SLOPE	0	-	-	ER Boost fast slope selection Updated by POR or SPI write 0 Fast slope activation depends on VIN voltage 1 Fast slope is forced ON
VCCBCK_PH_SEL[1:0]	11	-	-	VCCBuck phase shifting selection (if switching frequency is different respect to another regulator, the phase shift between them is not guaranteed) Updated by POR or SPI write 00 0 ns switching ON shift respect to t0 01 125 ns switching ON shift respect to t0 10 250 ns switching ON shift respect to t0 11 375 ns switching ON shift respect to t0
SATBCK_PH_SEL[1:0]	10	-	-	SatBuck phase shifting selection (if switching frequency is different respect to another regulator, the phase shift between them is not guaranteed) Updated by POR or SPI write 00 0 ns switching ON shift respect to t0 01 125 ns switching ON shift respect to t0 10 250 ns switching ON shift respect to t0 11 375 ns switching ON shift respect to t0
SYBST_PH_SEL[1:0]	01	-	-	SyncBoost phase shifting selection (if switching frequency is different respect to another regulator, the phase shift between them is not guaranteed) Updated by POR or SPI write 00 0 ns switching ON shift respect to t0

01 125 ns switching ON shift respect to t0

10 250 ns switching ON shift respect to t0

11 375 ns switching ON shift respect to t0

ERBST_PH_SEL[1:0] 00 - - ER Boost phase shifting selection (if switching frequency is different respect to another regulator, the phase shift between them is not guaranteed) Updated by POR or SPI write

00 0 ns switching ON shift respect to t0

01 125 ns switching ON shift respect to t0

10 250 ns switching ON shift respect to t0

11 375 ns switching ON shift respect to t0

7.3.34 Global configuration register for GPO driver function (GPOCR)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	GPO2LS	GPO1LS	GPO0LS
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GPO2LS	GPO1LS	GPO0LS

ID: 42

Type: R/W

Read: 4200

Write: 0084

	POR	WSM	SSM	
GPOxLS	0	0	0	GPO driver configuration bit

Updated by SSM_RESET or SPI write

0 High-side Driver configuration for GPOx (ER_BOOST_OK is required to enable GPO as HS)

1 Low-side Driver configuration for GPOx (ER_BOOST_OK is not required to enable GPO as LS)

7.3.35 GPOx control register (GPOCTRLx)

Channel 0 (GPOCTRL0)
Channel 1 (GPOCTRL1)
Channel 2 (GPOCTRL2)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	GPOxPWM[5:0]					
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GPOxPWM[5:0]					

ID: 43 (GPOCTRL0)
44 (GPOCTRL1)
45 (GPOCTRL2)

Type: RW

Read: 4300 (GPOCTRL0)
4400 (GPOCTRL1)
4500 (GPOCTRL2)

Write: 0086 (GPOCTRL0)
0088 (GPOCTRL1)
008A (GPOCTRL2)

	POR	WSM	SSM	
GPOxPWM	000000	000000	000000	6 bit value for PWM% with scaling of 1.6% per count Updated by SSM_RESET or SPI write

7.3.36 GPO fault status register (GPOFLTSR)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	GPO2DISABLE	GPO1DISABLE	GPO0DISABLE	0	GPOS_NOT_CONF	GPO2TEMP	GPO2LIM	GPO2ONOPN	GPO2OFFOPN	GPO2SHORT	GPO1TEMP	GPO1LIM	GPO1ONOPN	GPO1OFFOPN	GPO1SHORT	GPO0TEMP	GPO0LIM	GPO0ONOPN	GPO0OFFOPN	GPO0SHORT

ID: 46

Type: R

Read: 4600

Write: -

	POR	WSM	SSM	
GPO2DISABLE	1	1	1	GPO 2 disable state 0 GPO enable to work 1 GPO disabled due to thermal fault or configuration not received or ERBOOST not OK (only HS mode)
GPO1DISABLE	1	1	1	GPO 1 disable state 0 GPO enable to work 1 GPO disabled due to thermal fault or configuration not received or ERBOOST not OK (only HS mode)
GPO0DISABLE	1	1	1	GPO 0 disable state 0 GPO enable to work 1 GPO disabled due to thermal fault or configuration not received or ERBOOST not OK (only HS mode)
GPOS_NOT_CONF	1	1	1	GPOs configuration status 0 GPOs configured (activation is permitted) 1 GPOs not yet configured (activation is denied)
GPO2TEMP	0	0	0	GPO 2Thermal Fault Cleared as reported in GPO-Over Temp diagram, set by detection circuit 0 Fault not detected 1 Fault detected

GPO2LIM	0	0	0	GPO 2 Current Limit Flag Cleared by SSM_RESET or SPI read, set by detection circuit while ON 0 Fault not detected 1 Fault detected
GPO2ONOPN	0	0	0	GPO 2 Open Detection Cleared by SSM_RESET or SPI read, set by detection circuit while ON 0 Fault not detected 1 Fault detected
GPO2OFFOPN	0	0	0	GPO 2 Open detection in OFF condition Cleared by SSM_RESET or SPI read, set by detection circuit while OFF 0 Fault not detected 1 Fault detected
GPO2SHORT	0	0	0	GPO 2 Short Detection in OFF condition (short to battery in HS mode, short to ground in LS mode) Cleared by SSM_RESET or SPI read, set by detection circuit while OFF 0 Fault not detected 1 Fault detected
GPO1TEMP	0	0	0	GPO 1 Thermal Fault Cleared as reported in GPO-Over Temp diagram, set by detection circuit 0 Fault not detected 1 Fault detected
GPO1LIM	0	0	0	GPO 1 Current Limit Flag Cleared by SSM_RESET or SPI read, set by detection circuit while ON 0 Fault not detected 1 Fault detected
GPO1ONOPN	0	0	0	GPO 1 Open Detection Cleared by SSM_RESET or SPI read, set by detection circuit while ON 0 Fault not detected 1 Fault detected
GPO1OFFOPN	0	0	0	GPO 1 Open detection in OFF condition Cleared by SSM_RESET or SPI read, set by detection circuit while OFF 0 Fault not detected 1 Fault detected

GPO1SHORT	0	0	0	GPO 1 Short Detection in OFF condition (short to battery in HS mode, short to ground in LS mode) Cleared by SSM_RESET or SPI read, set by detection circuit while OFF 0 Fault not detected 1 Fault detected
GPO0TEMP	0	0	0	GPO 0 Thermal Fault Cleared as reported in GPO-Over Temp diagram, set by detection circuit 0 Fault not detected 1 Fault detected
GPO0LIM	0	0	0	GPO 0 Current Limit Flag Cleared by SSM_RESET or SPI read, set by detection circuit while ON 0 Fault not detected 1 Fault detected
GPO0ONOPN	0	0	0 OK	GPO 0 Open Detection Cleared by SSM_RESET or SPI read, set by detection circuit while ON 0 Fault not detected 1 Fault detected
GPO0OFFOPN	0	0	0	GPO 0 Open detection in OFF condition Cleared by SSM_RESET or SPI read, set by detection circuit while OFF 0 Fault not detected 1 Fault detected
GPO0SHORT	0	0	0	GPO 0 Short Detection in OFF condition (short to battery in HS mode, short to ground in LS mode) Cleared by SSM_RESET or SPI read, set by detection circuit while OFF 0 Fault not detected 1 Fault detected

7.3.37 ISOK fault status register (ISOFLTSR)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ISOTEMP	ISOLIM

ID: 47

Type: R

Read: 4700

Write: -

	POR	WSM	SSM	
ISOTEMP	0	0	0	ISO Temp fault Cleared by SSM_RESET or SPI read, set by detection circuit 0 Fault not detected 1 Fault detected
ISOLIM	0	0	0	ISO current limit flag Cleared by SSM_RESET or SPI read, set by detection circuit while ON (ISOK) = 0) 0 Fault not detected 1 Fault detected

7.3.38 Wheel speed sensor test request register (WSS_TEST)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	WSSSEL [6:0]							X	WSSTP
MISO	0	0	0	0	0	0	0	0	0	0	0	WSSSEL [6:0]							X	WSSTP

ID: 48

Type: RW

Read: 4800

Write: 0090

	POR	WSM	SSM	
WSSSEL [6:0]	000000	000000	000000	Wheel Speed Sensor Selection - code below uniquely selects one of the four WSx outputs to place a static output level on 1011001 WSS Test Mode for WS1 Output 1010110 WSS Test Mode for WS0 Output all other WSS Test Mode disabled
WSSTP	0	0	0	WSx Output Test Value 1 Output for selected WSx set 'high' 0 Output for selected WSx set 'low'

7.3.39 PSI5 configuration register for channel x (RSCRx)

PSI5 configuration register for channel 0 (RSCR0)
PSI5 configuration register for channel 1 (RSCR1)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				REDUCED_RANGE	BLOCK_CURR_IN_MSG	PERIOD_MEAS_DISABLE	FIX_THRESH	TSxDIS	BLKTxSEL	WSFILT[3:0]				RSPTEN	AVG/SSDIS	STS[3:0]			
MISO	0	0	0	0	REDUCED_RANGE	BLOCK_CURR_IN_MSG	PERIOD_MEAS_DISABLE	FIX_THRESH	TSxDIS	BLKTxSEL	WSFILT[3:0]				RSPTEN	AVG/SSDIS	STS[3:0]			

ID: 4A (RSCR0)
4B (RSCR1)

Type: R/W

Read: 4A00 (RSCR0)
4B00 (RSCR1)

Write: 0094 (RSCR0)
0096 (RSCR1)

PSI5 configured channel

	POR	WSM	SSM	
REDUCED_RANGE	0	0	0	Tracking speed of base and delta current 0 Fast tracking of Ibase if rx_sat_pre_filt is low; Slow tracking otherwise. Fast tracking of Idelta if rx_sat_pre_filt is high; Blocked otherwise. 1 Fast tracking of Ibase if current is less than (Ibase+(Idelta/4)); Slow tracking otherwise. Fast tracking of Idelta if current is higher than (top current -(Idelta/4)); Slow otherwise.
BLOCK_CURR_IN_MSG	0	0	0	Tracking enable of base and delta current during message transmission 0 Ibase tracking is enabled during blanking and after start bits recognition. Idelta tracking is disabled during blanking and enabled after start bits recognition.

1 Ibase tracking is enabled during blanking and disabled after start bits recognition.
Idelta tracking is disabled during blanking and enabled after start bits recognition

PERIOD_MEAS_DISABLE 0 0 0 Disabling of start bits period measure to decode following bits

0 Period is measured

1 Period is not measured (default is used)

FIX_THRESH 0 0 0 PSI5 selection of fixed or auto adaptive thresholds

0 auto adaptive threshold

1 fixed threshold (threshold is latched when this bit is set to high, we recommend to set this bit before enabling of the interface)

TSxDIS 0 0 0 Time Slot Control Disable

0 Slot control enabled

1 Slot control disabled

BLKTxSEL 0 0 0 Blanking Time Selection

0 Blanking time = 5ms

1 Blanking time = 10ms

WSFILT[3:0] 0010 0010 0010 Wheel speed filter time selection

189k: 125k:

(16+x)*Tosc (24+x)*Tosc Tosc=1/16MHz

RSPTEN 0 0 0 Pass Through mode Enable

0 Off

1 On

AVG/SSDIS 0 0 0 Current average enable during message transmission

0 Off (base and delta work as configured with bits #12, 14, 15)

1 On: base is freezed during data message and during blanking time and delta is averaged during message (fcut of the filter=2500 Hz) while is freezed during blanking time.

STS[3:0]	0000	0000	0000	Sensor Type Selection 0000 Synchronous PSI5, parity, 8-bit, 125k (P8P-500/3L) 0001 Synchronous PSI5, parity, 8-bit, 189k (P8P-500/3H) 0010 Synchronous PSI5, parity, 10-bit, 125k (P10P-500/3L) 0011 Synchronous PSI5, parity, 10-bit, 189k (P10P-500/3H) 0100 Synchronous PSI5, parity, 8-bit, 125k (P8P-500/3L) 0101 Synchronous PSI5, parity, 8-bit, 189k (P8P-500/4H) 0110 Synchronous PSI5, parity, 10-bit, 125k (P10P-500/3L) 0111 Synchronous PSI5, parity, 10-bit, 189k (P10P-500/4H) 1000 NA 1001 NA 1010 NA 1011 NA 1100 unused (default automatically selected) 1101 unused (default automatically selected) 1110 unused (default automatically selected) 1111 unused (default automatically selected)

7.3.40 Remote sensor control register (RSCTRL)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	CH3EN	SYNC3EN	CH2EN	SYNC2EN	CH1EN	SYNC1EN	CH0EN	SYNC0EN
MISO	0	0	0	0	0	0	0	0	0	0	0	0	CH3EN	SYNC3EN	CH2EN	SYNC2EN	CH1EN	SYNC1EN	CH0EN	SYNC0EN

ID: 4E

Type: R/W

Read: 4E00

Write: 009C

	POR	WSM	SSM	
CHxEN	0	0	0	Channel x Output enable Updated by SSM_RESET or SPI write 0 Off 1 On
SYNCxEN	0	0	0	Channel x Sync Pulse Enable 0 Off 1 On

7.3.41 Safing algorithm configuration register (SAF_ALGO_CONF)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				NO_DATA	X	ARMN_TH				ARMP_TH				SUB_VAL			ADD_VAL		
MISO	0	0	0	0	NO_DATA	0	ARMN_TH				ARMP_TH				SUB_VAL			ADD_VAL		

ID: 66

Type: R/W

Read: 6600

Write: 00CC

	POR	WSM	SSM	
NO_DATA	0	0	0	Event counter no data select Updated by SSM_RESET or SPI write while in DIAG state 0 Event counter reset to 0 if CC=0 or (ABS value of response > limit determined by LIM_SELx) and LIM_ENx=1 when SPI read of SAF_CC bit is performed (end of sample cycle) 1 Event counter decremented by SUB_VAL if CC=0 or (ABS value of response > limit determined by LIM_SELx) and LIM_ENx=1 when SPI read of SAF_CC bit is performed (end of sample cycle)
ARMN_TH	0011	0011	0011	Negative event counter threshold to assert arming Updated by SSM_RESET or SPI write while in DIAG state 0000 Negative event counter disabled
ARMP_TH	0011	0011	0011	Positive event counter threshold to assert arming Updated by SSM_RESET or SPI write while in DIAG state 0000 Positive event counter disabled
SUB_VAL	011	011	011	Decremental step size of the event counter Updated by SSM_RESET or SPI write while in DIAG state
ADD_VAL	001	001	001	Incremental step size of the event counter Updated by SSM_RESET or SPI write while in DIAG state

7.3.42 Arming signals register (ARM_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	0	PSINHINT	PSINH_EXP_TIME	ACL_PIN_STATE	ACL_VALID	0	0	ARMINT2	ARMINT_1	FENL	0

ID: 6A

Type: R

Read: 6A00

Write: -

	POR	WSM	SSM	
ARMINT_x	-	-	-	State of armint signals Updated per Safing Engine output logic diagram in case of internal safing engine otherwise is the echo of ARMx pins
ACL_VALID	0	0	0	Valid ACL detection 0 Cleared when ACL_BAD=2 1 Set when ACL_GOOD=3
ACL_PIN_STATE	-	-	-	Echo of ACL pin
PSINH_EXP_TIME	0	0	0	State of PSINH expiration timer 0 If timer is 0 1 If timer is counting
PSINHINT	-	-	-	State of PSINHINT signal Updated per PSINH output logic diagram in case of internal engine otherwise is the echo of PSINH pin inverted
FNL	-	-	-	State of external arming control signal (used to arm low side of deployment loops only in case of external arming) Updated based on pin state

7.3.43 ARMx assignment registers to specific Loops (LOOP_MATRIX_ARMx)

Assignment of ARM1 to specific loops (LOOP_MATRIX_ARM1)
Assignment of ARM2 to specific loops (LOOP_MATRIX_ARM2)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	ARMx_L7	ARMx_L6	ARMx_L5	ARMx_L4	ARMx_L3	ARMx_L2	ARMx_L1	ARMx_L0
MISO	0	0	0	0	0	0	0	0	0	0	0	0	ARMx_L7	ARMx_L6	ARMx_L5	ARMx_L4	ARMx_L3	ARMx_L2	ARMx_L1	ARMx_L0

ID: 6E (LOOP_MATRIX_ARM1)
6F (LOOP_MATRIX_ARM2)

Type: R/W

Read: 6E00 (LOOP_MATRIX_ARM1)
6F00 (LOOP_MATRIX_ARM2)

Write: 00DC (LOOP_MATRIX_ARM1)
00DE (LOOP_MATRIX_ARM2)

	POR	WSM	SSM	
ARMx_Ly	0	0	0	Configures ARMx for Loop_y Updated by SSM_RESET or SPI write while in DIAG state 0 ARMx signal is not associated with Loopy 1 ARMx signal is associated with Loopy

7.3.44 ARMx enable pulse stretch timer status (AEPSTS_ARMx)

ARM1 enable pulse stretch timer status (AEPSTS_ARM1)
ARM2 enable pulse stretch timer status (AEPSTS_ARM2)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	0	Timer Count[9:0]									

ID: 73 (AEPSTS_ARM1)
74 (AEPSTS_ARM2)

Type: R

Read: 7300 (AEPSTS_ARM1)
7400 (AEPSTS_ARM2)

Write: -

	POR	WSM	SSM	
Timer Count	$000	$000	$000	10-bit ARMing Enable Pulse Stretcher timer value
				Cleared by SSM_RESET
				Loaded with initial value based on ARMx bit and DWELL[1:0] of SAF_CONTROL_y while safing is met for record y provided current value is < DWELL[1:0] value
				Decremented every 2ms while > 0
				Contains remaining pulse stretcher timer value

7.3.45 Passenger inhibit upper threshold for DC sensor 0 (PADTHRESH_HI)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	PADTHRESH_HI									
MISO	0	0	0	0	0	0	0	0	0	0	PADTHRESH_HI									

ID: 78

Type: R/W

Read: 7800

Write: 00F0

	POR	WSM	SSM	
PADTHRESH_HI	$000	$000	$000	Upper threshold - measurements above this upper value will assert the PSINH signal and deactivate loops identified in the PSINH mask

7.3.46 Passenger inhibit lower threshold for DC sensor 0 (PADTHRESH_LO)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	PADTHRESH_LO									
MISO	0	0	0	0	0	0	0	0	0	0	PADTHRESH_LO									

ID: 79

Type: R/W

Read: 7900

Write: 00F2

	POR	WSM	SSM	
PADTHRESH_LO	$3FF	$3FF	$3FF	Lower threshold - measurements below this lower value will assert the PSINH signal and deactivate loops identified in the PSINH mask

7.3.47 Assignment of PSINH signal to specific Loop(s) (LOOP_MATRIX_PSINH)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	PSINH_L7	PSINH_L6	PSINH_L5	PSINH_L4	PSINH_L3	PSINH_L2	PSINH_L1	PSINH_L0
MISO	0	0	0	0	0	0	0	0	0	0	0	0	PSINH_L7	PSINH_L6	PSINH_L5	PSINH_L4	PSINH_L3	PSINH_L2	PSINH_L1	PSINH_L0

ID: 7A

Type: R/W

Read: 7A00

Write: 00F4

	POR	WSM	SSM	
PSINH_Ly	0	0	0	Configures PSINH for Loop_y 0 PSINH signal is not associated with Loopy 1 PSINH signal is associated with Loopy

7.3.48 Safing records enable register (SAF_ENABLE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				EN_SAF16	EN_SAF15	EN_SAF14	X	X	X	X	EN_SAF9	EN_SAF8	EN_SAF7	EN_SAF6	EN_SAF5	EN_SAF4	EN_SAF3	EN_SAF2	EN_SAF1
MISO	0	0	0	0	EN_SAF16	EN_SAF15	EN_SAF14	0	0	0	0	EN_SAF9	EN_SAF8	EN_SAF7	EN_SAF6	EN_SAF5	EN_SAF4	EN_SAF3	EN_SAF2	EN_SAF1

ID: 7F

Type: R/W

Read: 7F00

Write: 00FE

	POR	WSM	SSM	
EN_SAFx	0	0	0	Safing Record enable Updated by SSM_RESET or SPI write 0 Disable 1 Enable

7.3.49 Safing records request mask registers (SAF_REQ_MASK_x)

Safing record request mask for record 1 (SAF_REQ_MASK_1)
Safing record request mask for record 2 (SAF_REQ_MASK_2)
Safing record request mask for record 3 (SAF_REQ_MASK_3)
Safing record request mask for record 4 (SAF_REQ_MASK_4)
Safing record request mask for record 5 (SAF_REQ_MASK_5)
Safing record request mask for record 6 (SAF_REQ_MASK_6)
Safing record request mask for record 7 (SAF_REQ_MASK_7)
Safing record request mask for record 8 (SAF_REQ_MASK_8)
Safing record request mask for record 9 (SAF_REQ_MASK_9)
Safing record request mask for record 14_pt1 (SAF_REQ_MASK_14)_pt1
Safing record request mask for record 14_pt2 (SAF_REQ_MASK_14)_pt2
Safing record request mask for record 15_pt1 (SAF_REQ_MASK_15)_pt1
Safing record request mask for record 15_pt2 (SAF_REQ_MASK_15)_pt2
Safing record request mask for record 16_pt1 (SAF_REQ_MASK_16)_pt1
Safing record request mask for record 16_pt2 (SAF_REQ_MASK_16)_pt2

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				SAF_REQ_MASKx[15:0]															
MISO	0	0	0	0	SAF_REQ_MASKx[15:0]															

ID: 80 (SAF_REQ_MASK_1)
81 (SAF_REQ_MASK_2)
82 (SAF_REQ_MASK_3)
83 (SAF_REQ_MASK_4)
84 (SAF_REQ_MASK_5)
85 (SAF_REQ_MASK_6)
86 (SAF_REQ_MASK_7)
87 (SAF_REQ_MASK_8)
88 (SAF_REQ_MASK_9)
8D (SAF_REQ_MASK_14_pt1
8E (SAF_REQ_MASK_14_pt2)
8F (SAF_REQ_MASK_15_pt1)
90 (SAF_REQ_MASK_15_pt2)
91 (SAF_REQ_MASK_16_pt1)
92 (SAF_REQ_MASK_16_pt2)

Type: R/W

Read: 8000 (SAF_REQ_MASK_1)
8100 (SAF_REQ_MASK_2)
8200 (SAF_REQ_MASK_3)
8300 (SAF_REQ_MASK_4)
8400 (SAF_REQ_MASK_5)
8500 (SAF_REQ_MASK_6)
8600 (SAF_REQ_MASK_7)
8700 (SAF_REQ_MASK_8)
8800 (SAF_REQ_MASK_9)
8D00 (SAF_REQ_MASK_14_pt1
8E00 (SAF_REQ_MASK_14_pt2)

8F00 (SAF_REQ_MASK_15_pt1)
9000 (SAF_REQ_MASK_15_pt2)
9100 (SAF_REQ_MASK_16_pt1)
9200 (SAF_REQ_MASK_16_pt2)

Write:

8000 (SAF_REQ_MASK_1)
8002 (SAF_REQ_MASK_2)
8004 (SAF_REQ_MASK_3)
8006 (SAF_REQ_MASK_4)
8008 (SAF_REQ_MASK_5)
800A (SAF_REQ_MASK_6)
800C (SAF_REQ_MASK_7)
800E (SAF_REQ_MASK_8)
8010 (SAF_REQ_MASK_9)
801A (SAF_REQ_MASK_14_pt1
801C (SAF_REQ_MASK_14_pt2)
801E (SAF_REQ_MASK_15_pt1)
8020 (SAF_REQ_MASK_15_pt2)
8022 (SAF_REQ_MASK_16_pt1)
8424 (SAF_REQ_MASK_16_pt2)

	POR	WSM	SSM	
SAF_REQ_MASKx[15:0]	$0000	$0000	$0000	Safing Request Mask for safing record x - 16-bit request mask that is bit-wise ANDed with MOSI data from SPI monitor Updated by SSM_RESET or SPI write while in DIAG state

7.3.50 Safing records request target registers (SAF_REQ_TARGET_x)

Safing record request mask for record 1 (SAF_REQ_TARGET_1)
Safing record request mask for record 2 (SAF_REQ_TARGET_2)
Safing record request mask for record 3 (SAF_REQ_TARGET_3)
Safing record request mask for record 4 (SAF_REQ_TARGET_4)
Safing record request mask for record 5 (SAF_REQ_TARGET_5)
Safing record request mask for record 6 (SAF_REQ_TARGET_6)
Safing record request mask for record 7 (SAF_REQ_TARGET_7)
Safing record request mask for record 8 (SAF_REQ_TARGET_8)
Safing record request mask for record 9 (SAF_REQ_TARGET_9)
Safing record request mask for record 14_pt1 (SAF_REQ_TARGET_14)_pt1
Safing record request mask for record 14_pt2 (SAF_REQ_TARGET_14)_pt2
Safing record request mask for record 15_pt1 (SAF_REQ_TARGET_15)_pt1
Safing record request mask for record 15_pt2 (SAF_REQ_TARGET_15)_pt2
Safing record request mask for record 16_pt1 (SAF_REQ_TARGET_16)_pt1
Safing record request mask for record 16_pt2 (SAF_REQ_TARGET_16)_pt2

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				SAF_REQ_TARGET[15:0]															
MISO	0	0	0	0	SAF_REQ_TARGET[15:0]															

ID:
93 (SAF_REQ_TARGET_1)
94 (SAF_REQ_TARGET_2)
95 (SAF_REQ_TARGET_3)
96 (SAF_REQ_TARGET_4)
97 (SAF_REQ_TARGET_5)
98 (SAF_REQ_TARGET_6)
99 (SAF_REQ_TARGET_7)
9A (SAF_REQ_TARGET_8)
9B (SAF_REQ_TARGET_9)
A0 (SAF_REQ_TARGET_14_pt1
A1 (SAF_REQ_TARGET_14_pt2)
A2 (SAF_REQ_TARGET_15_pt1)
A3 (SAF_REQ_TARGET_15_pt2)
A4 (SAF_REQ_TARGET_16_pt1)
A5 (SAF_REQ_TARGET_16_pt2)

Type: R/W

Read:
9300 (SAF_REQ_TARGET_1)
9400 (SAF_REQ_TARGET_2)
9500 (SAF_REQ_TARGET_3)
9600 (SAF_REQ_TARGET_4)
9700 (SAF_REQ_TARGET_5)
9800 (SAF_REQ_TARGET_6)
9900 (SAF_REQ_TARGET_7)
9A00 (SAF_REQ_TARGET_8)
9B00 (SAF_REQ_TARGET_9)
A000 (SAF_REQ_TARGET_14_pt1
A100 (SAF_REQ_TARGET_14_pt2)

A200 (SAF_REQ_TARGET_15_pt1)
A300 (SAF_REQ_TARGET_15_pt2)
A400 (SAF_REQ_TARGET_16_pt1)
A500 (SAF_REQ_TARGET_16_pt2)

Write: 8026 (SAF_REQ_TARGET_1)
8028 (SAF_REQ_TARGET_2)
802A (SAF_REQ_TARGET_3)
802C (SAF_REQ_TARGET_4)
802E (SAF_REQ_TARGET_5)
8030 (SAF_REQ_TARGET_6)
8032 (SAF_REQ_TARGET_7)
8034 (SAF_REQ_TARGET_8)
8036 (SAF_REQ_TARGET_9)
8040 (SAF_REQ_TARGET_14_pt1
8042 (SAF_REQ_TARGET_14_pt2)
8044 (SAF_REQ_TARGET_15_pt1)
8246 (SAF_REQ_TARGET_15_pt2)
8048 (SAF_REQ_TARGET_16_pt1)
804A (SAF_REQ_TARGET_16_pt2)

	POR	WSM	SSM	
SAF_REQ_TARGET[15:0	$0000	$0000	$0000	Safing Request target for safing record x - 16-bit request target that is compared to the bit-wise AND result of the SAF_REQ_MASKx and MOSI data from SPI monitor Updated by SSM_RESET or SPI write while in DIAG state

7.3.51 Safing records response mask registers (SAF_RESP_MASK_x)

Safing record response mask for record 1 (SAF_RESP_MASK_1)
Safing record response mask for record 2 (SAF_RESP_MASK_2)
Safing record response mask for record 3 (SAF_RESP_MASK_3)
Safing record response mask for record 4 (SAF_RESP_MASK_4)
Safing record response mask for record 5 (SAF_RESP_MASK_5)
Safing record response mask for record 6 (SAF_RESP_MASK_6)
Safing record response mask for record 7 (SAF_RESP_MASK_7)
Safing record response mask for record 8 (SAF_RESP_MASK_8)
Safing record response mask for record 9 (SAF_RESP_MASK_9)
Safing record response mask for record 14_pt1 (SAF_RESP_MASK_14_pt1)
Safing record response mask for record 14_pt2 (SAF_RESP_MASK_14_pt2)
Safing record response mask for record 15_pt1 (SAF_RESP_MASK_15_pt1)
Safing record response mask for record 15_pt2 (SAF_RESP_MASK_14_pt2)
Safing record response mask for record 16_pt1 (SAF_RESP_MASK_16_pt1)
Safing record response mask for record 16_pt2 (SAF_RESP_MASK_16_pt2)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				SAF_RESP_MASKx[15:0]															
MISO	0	0	0	0	SAF_RESP_MASKx[15:0]															

ID:
A6 (SAF_RESP_MASK_1)
A7 (SAF_RESP_MASK_2)
A8 (SAF_RESP_MASK_3)
A9 (SAF_RESP_MASK_4)
AA (SAF_RESP_MASK_5)
AB (SAF_RESP_MASK_6)
AC (SAF_RESP_MASK_7)
AD (SAF_RESP_MASK_8)
AE (SAF_RESP_MASK_9)
B3 (SAF_RESP_MASK_14_pt1)
B4 (SAF_RESP_MASK_14_pt2)
B5 (SAF_RESP_MASK_15_pt1)
B6 (SAF_RESP_MASK_15_pt2)
B7 (SAF_RESP_MASK_16_pt1
B8 (SAF_RESP_MASK_16_pt2

Type: R/W

Read:

Read:
A600 (SAF_RESP_MASK_1)
A700 (SAF_RESP_MASK_2)
A800 (SAF_RESP_MASK_3)
A900 (SAF_RESP_MASK_4)
AA00 (SAF_RESP_MASK_5)
AB00 (SAF_RESP_MASK_6)
AC00 (SAF_RESP_MASK_7)
AD00 (SAF_RESP_MASK_8)
AE00 (SAF_RESP_MASK_9)

B300 (SAF_RESP_MASK_14_pt1)
B400 (SAF_RESP_MASK_14_pt2)
B500 (SAF_RESP_MASK_15_pt1)
B600 (SAF_RESP_MASK_15_pt2)
B700 (SAF_RESP_MASK_16_pt1
B801 (SAF_RESP_MASK_16_pt1

Write:

804C (SAF_RESP_MASK_1)
804E (SAF_RESP_MASK_2)
8050 (SAF_RESP_MASK_3)
8052 (SAF_RESP_MASK_4)
8054 (SAF_RESP_MASK_5)
8056 (SAF_RESP_MASK_6)
8058 (SAF_RESP_MASK_7)
805A (SAF_RESP_MASK_8)
805C (SAF_RESP_MASK_9)
8066 (SAF_RESP_MASK_14_pt1)
8068 (SAF_RESP_MASK_14_pt2)
806A (SAF_RESP_MASK_15_pt1)
806C (SAF_RESP_MASK_15_pt2)
806E (SAF_RESP_MASK_16_pt1
8070 (SAF_RESP_MASK_16_pt2

	POR	WSM	SSM	
SAF_RESP_MASKx[15:0]	0000	0000	0000	Safing Response Mask for safing record x - 16-bit response mask that is bit-wise ANDed with MISO data from SPI monitor Updated by SSM_RESET or SPI write while in DIAG state

7.3.52 Safing records response mask registers (SAF_RESP_TARGET_x)

Safing record response target for record 1 (SAF_RESP_TARGET_1)
Safing record response target for record 2 (SAF_RESP_TARGET_2)
Safing record response target for record 3 (SAF_RESP_TARGET_3)
Safing record response target for record 4 (SAF_RESP_TARGET_4)
Safing record response target for record 5 (SAF_RESP_TARGET_5)
Safing record response target for record 6 (SAF_RESP_TARGET_6)
Safing record response target for record 7 (SAF_RESP_TARGET_7)
Safing record response target for record 8 (SAF_RESP_TARGET_8)
Safing record response target for record 9 (SAF_RESP_TARGET_9)
Safing record response target for record 14_pt1 (SAF_RESP_TARGET_14)_pt1
Safing record response target for record 14_pt2 (SAF_RESP_TARGET_14)_pt2
Safing record response target for record 15_pt1 (SAF_RESP_TARGET_15)_pt1
Safing record response target for record 15_pt2 (SAF_RESP_TARGET_15)_pt2
Safing record response target for record 16_pt1 (SAF_RESP_TARGET_16)_pt1
Safing record response target for record 16_pt2 (SAF_RESP_TARGET_16)_pt2

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				SAF_RESP_TARGETx[15:0]															
MISO	0	0	0	0	SAF_RESP_TARGETx[15:0]															

ID:
B9 (SAF_RESP_TARGET_1)
BA (SAF_RESP_TARGET_2
BB (SAF_RESP_TARGET_3
BC (SAF_RESP_TARGET_4
BD (SAF_RESP_TARGET_5
BE (SAF_RESP_TARGET_6
BF (SAF_RESP_TARGET_7
C0 (SAF_RESP_TARGET_8
C1 (SAF_RESP_TARGET_9
C6 (SAF_RESP_TARGET_14_pt1
C7 (SAF_RESP_TARGET_14_pt2
C8 (SAF_RESP_TARGET_15_pt1
C9 (SAF_RESP_TARGET_15_pt2
CA (SAF_RESP_TARGET_16_pt1
CB (SAF_RESP_TARGET_16_pt2

Type: R/W

Read:
B900 (SAF_RESP_TARGET_1)
BA00 (SAF_RESP_TARGET_2
BB00 (SAF_RESP_TARGET_3
BC00 (SAF_RESP_TARGET_4
BD00 (SAF_RESP_TARGET_5
BE00 (SAF_RESP_TARGET_6
BF00 (SAF_RESP_TARGET_7
C000 (SAF_RESP_TARGET_8
C100 (SAF_RESP_TARGET_9
C600 (SAF_RESP_TARGET_14_pt1
C700 (SAF_RESP_TARGET_14_pt2

C800 (SAF_RESP_TARGET_15_pt1
C900 (SAF_RESP_TARGET_15_pt2
CA00 (SAF_RESP_TARGET_16_pt1
CB00 (SAF_RESP_TARGET_16_pt2)

Write: 8072 (SAF_RESP_TARGET_1)
8074 (SAF_RESP_TARGET_2
8076 (SAF_RESP_TARGET_3
8078 (SAF_RESP_TARGET_4
807A (SAF_RESP_TARGET_5
807C (SAF_RESP_TARGET_6
807E (SAF_RESP_TARGET_7
8080 (SAF_RESP_TARGET_8
8082 (SAF_RESP_TARGET_9
808C (SAF_RESP_TARGET_14_pt1
808E (SAF_RESP_TARGET_14_pt2
8090 (SAF_RESP_TARGET_15_pt1
8092 (SAF_RESP_TARGET_15_pt2
8094 (SAF_RESP_TARGET_16_pt1
CB00 (SAF_RESP_TARGET_16_pt2)

	POR	WSM	SSM	
SAF_RESP_TARGETx[15:0]	0000	0000	0000	Safing Response target for safing record x - 16-bit response target that is compared to the bit-wise AND result of the SAF_RESP_MASKx and MISO data from SPI monitor Updated by SSM_RESET or SPI write while in DIAG state

7.3.53 Safing records data mask registers (SAF_DATA_MASK_x)

Safing record data mask for record 1 (SAF_DATA_MASK_1)
Safing record data mask for record 2 (SAF_DATA_MASK_2)
Safing record data mask for record 3 (SAF_DATA_MASK_3)
Safing record data mask for record 4 (SAF_DATA_MASK_4)
Safing record data mask for record 5 (SAF_DATA_MASK_5)
Safing record data mask for record 6 (SAF_DATA_MASK_6)
Safing record data mask for record 7 (SAF_DATA_MASK_7)
Safing record data mask for record 8 (SAF_DATA_MASK_8)
Safing record data mask for record 9 (SAF_DATA_MASK_9)
Safing record data mask for record 14 (SAF_DATA_MASK_14_pt1)
Safing record data mask for record 14 (SAF_DATA_MASK_14_pt2)
Safing record data mask for record 15 (SAF_DATA_MASK_15_pt1)
Safing record data mask for record 15 (SAF_DATA_MASK_15_pt2)
Safing record data mask for record 16 (SAF_DATA_MASK_16_pt1)
Safing record data mask for record 16 (SAF_DATA_MASK_16_pt2)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				SAF_DATA_MASKx[15:0]															
MISO	0	0	0	0	SAF_DATA_MASKx[15:0]															

ID: CC (SAF_DATA_MASK_1)
CD (SAF_DATA_MASK_2)
CE (SAF_DATA_MASK_3)
CF (SAF_DATA_MASK_4)
D0 (SAF_DATA_MASK_5)
D1 (SAF_DATA_MASK_6)
D2 (SAF_DATA_MASK_7)
D3 (SAF_DATA_MASK_8)
D4 (SAF_DATA_MASK_9)
D9 (SAF_DATA_MASK_14_pt1)
DA (SAF_DATA_MASK_14_pt2)
DB (SAF_DATA_MASK_15_pt1)
DC (SAF_DATA_MASK_15_pt2)
DD (SAF_DATA_MASK_16_pt1)
DE (SAF_DATA_MASK_16_pt2)

Type: R/W

Read: CC00 (SAF_DATA_MASK_1)
CD00 (SAF_DATA_MASK_2)
CE00 (SAF_DATA_MASK_3)
CF00 (SAF_DATA_MASK_4)
D000 (SAF_DATA_MASK_5)
D100 (SAF_DATA_MASK_6)
D200 (SAF_DATA_MASK_7)
D300 (SAF_DATA_MASK_8)
D400 (SAF_DATA_MASK_9
D900 (SAF_DATA_MASK_14_pt1)
DA00 (SAF_DATA_MASK_14_pt2)

DB00 (SAF_DATA_MASK_15_pt1)
DC00 (SAF_DATA_MASK_15_pt2)
DD00 (SAF_DATA_MASK_16_pt1)
DE00 (SAF_DATA_MASK_16_pt2)

Write: 8099 (SAF_DATA_MASK_1)
809A (SAF_DATA_MASK_2)
809C (SAF_DATA_MASK_3)
809E (SAF_DATA_MASK_4)
80A0 (SAF_DATA_MASK_5)
80A2 (SAF_DATA_MASK_6)
80A4 (SAF_DATA_MASK_7)
80A6 (SAF_DATA_MASK_8)
80A8 (SAF_DATA_MASK_9)
80B2 (SAF_DATA_MASK_14_pt1)
80B4 (SAF_DATA_MASK_14_pt2)
80B6 (SAF_DATA_MASK_15_pt1)
80B8 (SAF_DATA_MASK_15_pt2)
80BA (SAF_DATA_MASK_16_pt1)
80BC (SAF_DATA_MASK_16_pt2)

	POR	WSM	SSM	
SAF_DATA_MASKx[15:0]	0000	0000	0000	Safing Data Mask for safing record x - 16-bit data mask that is bit-wise ANDed with MISO data from SPI monitor Updated by SSM_RESET or SPI write while in DIAG state

7.3.54 Safing record threshold registers (SAF_THRESHOLD_x)

Safing record threshold for record 1 (SAF_THRESHOLD_1)
Safing record threshold for record 2 (SAF_THRESHOLD_2)
Safing record threshold for record 3 (SAF_THRESHOLD_3)
Safing record threshold for record 4 (SAF_THRESHOLD_4)
Safing record threshold for record 5 (SAF_THRESHOLD_5)
Safing record threshold for record 6 (SAF_THRESHOLD_6)
Safing record threshold for record 7 (SAF_THRESHOLD_7)
Safing record threshold for record 8 (SAF_THRESHOLD_8)
Safing record threshold for record 9 (SAF_THRESHOLD_9)
Safing record threshold for record 14 (SAF_THRESHOLD_14)
Safing record threshold for record 15 (SAF_THRESHOLD_15)
Safing record threshold for record 16 (SAF_THRESHOLD_16)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				SAF_THRESHOLDx[15:0]															
MISO	0	0	0	0	SAF_THRESHOLDx[15:0]															

ID:
DF (SAF_THRESHOLD_1)
E0 (SAF_THRESHOLD_2)
E1 (SAF_THRESHOLD_3)
E2 (SAF_THRESHOLD_4)
E3 (SAF_THRESHOLD_5)
E4 (SAF_THRESHOLD_6)
E5 (SAF_THRESHOLD_7)
E6 (SAF_THRESHOLD_8)
E7 (SAF_THRESHOLD_9)
EC (SAF_THRESHOLD_14)
ED (SAF_THRESHOLD_15)
EE (SAF_THRESHOLD_16)

Type: R/W

Read:
DF00 (SAF_THRESHOLD_1)
E000 (SAF_THRESHOLD_2)
E100 (SAF_THRESHOLD_3)
E200 (SAF_THRESHOLD_4)
E300 (SAF_THRESHOLD_5)
E400 (SAF_THRESHOLD_6)
E500 (SAF_THRESHOLD_7)
E600 (SAF_THRESHOLD_8)
E700 (SAF_THRESHOLD_9)
EC00 (SAF_THRESHOLD_14)
ED00 (SAF_THRESHOLD_15)
EE00 (SAF_THRESHOLD_16)

Write:
80BE (SAF_THRESHOLD_1)
80C0 (SAF_THRESHOLD_2)
80C2 (SAF_THRESHOLD_3)

80C4 (SAF_THRESHOLD_4)
80C6 (SAF_THRESHOLD_5)
80C8 (SAF_THRESHOLD_6)
80CA (SAF_THRESHOLD_7)
80CC (SAF_THRESHOLD_8)
80CE (SAF_THRESHOLD_9)
80D8 (SAF_THRESHOLD_14)
80DA (SAF_THRESHOLD_15)
80DB (SAF_THRESHOLD_16)

	POR	WSM	SSM	
SAF_THRESHOLD_x	$FFFF	$FFFF	$FFFF	Safing threshold for safing record x - 16-bit threshold used for safing data comparison Updated by SSM_RESET or SPI write while in DIAG state

7.3.55 Safing control x registers (SAF_CONTROL_x)

Safing control registers for record 1 (SAF_CONTROL_1)
Safing control registers for record 2 (SAF_CONTROL_2)
Safing control registers for record 3 (SAF_CONTROL_3)
Safing control registers for record 4 (SAF_CONTROL_4)
Safing control registers for record 5 (SAF_CONTROL_5)
Safing control registers for record 6 (SAF_CONTROL_6)
Safing control registers for record 7 (SAF_CONTROL_7)
Safing control registers for record 8 (SAF_CONTROL_8)
Safing control registers for record 9 (SAF_CONTROL_9)
Safing control registers for record 14 (SAF_CONTROL_14)
Safing control registers for record 15 (SAF_CONTROL_15)
Safing control registers for record 16 (SAF_CONTROL_16)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				ARMSELx		SPIFLDSELx	LIM SELx	LIM Enx	COMBx	DWELLx[1:0]		X	X	ARM2x	ARM1x	CSx[2:0]			IFx
MISO	0	0	0	0	ARMSELx		SPIFLDSELx	LIM SELx	LIM Enx	COMBx	DWELLx[1:0]		0	0	ARM2x	ARM1x	CSx[2:0]			IFx

ID:
EF (SAF_CONTROL_1)
F0 (SAF_CONTROL_2)
F1 (SAF_CONTROL_3)
F2 (SAF_CONTROL_4)
F3 (SAF_CONTROL_5)
F4 (SAF_CONTROL_6)
F5 (SAF_CONTROL_7
F6 (SAF_CONTROL_8)
F7 (SAF_CONTROL_9)
FC (SAF_CONTROL_14)
FD (SAF_CONTROL_15)
FE (SAF_CONTROL_16)

Type: R/W

Read:
EF00 (SAF_CONTROL_1)
F000 (SAF_CONTROL_2)
F100 (SAF_CONTROL_3)
F200 (SAF_CONTROL_4)
F300 (SAF_CONTROL_5)
F400 (SAF_CONTROL_6)
F500 (SAF_CONTROL_7
F600 (SAF_CONTROL_8)
F700 (SAF_CONTROL_9)
FC00 (SAF_CONTROL_14)

FD00 (SAF_CONTROL_15)
FE00 (SAF_CONTROL_16)

Write: 80DE (SAF_CONTROL_1)
80E0 (SAF_CONTROL_2)
80E2 (SAF_CONTROL_3)
80E4 (SAF_CONTROL_4)
80E6 (SAF_CONTROL_5)
80E8 (SAF_CONTROL_6)
80EA (SAF_CONTROL_7
80EC (SAF_CONTROL_8)
80EE (SAF_CONTROL_9)
80F8 (SAF_CONTROL_14)
80FA (SAF_CONTROL_15)
80FC (SAF_CONTROL_16)

	POR	WSM	SSM	
ARMSELx	00	00	00	ARMINT select for safing record x - correlates A Updated by SSM_RESET or SPI write while in DIAG state 00 ARMP OR ARMN 01 ARMP 10 ARMN 11 ARMP OR ARMN
SPIFLDSELx	0	0	0	SPI field select for safing record x - determines which 16-bit field in long SPI messages (>31 bit) to use for response on MISO of SPI monitor. In case of messages less than 32 bits this bit is don't care. Updated by SSM_RESET or SPI write while in DIAG state. 0 First 16 bits of SPI MISO frame used for Response Mask and Data Mask bit-wise AND 1 Last 16 bits of SPI MISO frame used for Response Mask and Data Mask bit-wise AND
LIM SELx	0	0	0	Data range limit select for safing record x - When enabled, determines the range limit used for incoming sensor data Updated by SSM_RESET or SPI write while in DIAG state 0 8-bit data range limit - incoming |data| >120d is not recognized as valid data 1 10-bit data range limit - incoming |data| > 480d is not recognized as valid data
LIM Enx	0	0	0	Data range limit enable for safing record x Updated by SSM_RESET or SPI write while in DIAG state 0 Data range limit disabled 1 Data range limit enabled
COMBx	0	0	0	Combine function enable for safing record x Updated by SSM_RESET or SPI write while in DIAG state

				0 Combine function disabled 1 Combine function enabled For record pairs = x,x+1, the comparison for record x uses |data(x) + data(x+1)| and the comparison for record x+1 uses |data(x) - data(x+1)| Combine function is not available for 32 bits safing records (x=1,3,5,7,9,11 for high-end; x=1,3,5,7 for mid-end);
DWELLx[1:0]	00	00	00	Safing dwell extension time select for safing record x Updated by SSM_RESET or SPI write while in DIAG state 00 2048 ms 01 256 ms 10 32 ms 11 0 ms
ARM2x	0	0	0	ARM2INT select for safing record x - correlates safing result to ARM2INT Updated by SSM_RESET or SPI write while in DIAG state 0 Safing record x not assigned to ARM2INT 1 Safing record x assigned to ARM2INT
ARM1x	0	0	0	ARM1INT select for safing record x - correlates safing result to ARM1INT Updated by SSM_RESET or SPI write while in DIAG state 0 Safing record x not assigned to ARM1INT 1 Safing record x assigned to ARM1INT
CSx[2:0]	000	000	000	SPI Monitor CS select for safing record x Updated by SSM_RESET or SPI write while in DIAG state 000 None selected for record x 001 SAF_CS0 selected for record x 010 SAF_CS1 selected for record x 011 SAF_CS2 selected for record x 100 None selected for record x 101 CS_RS selected for record x 110 None selected for record x 111 None selected for record x
IFx	0	0	0	SPI format select for safing record x - selects response protocol for SPI monitor. Updated by SSM_RESET or SPI write while in DIAG state 0 Out of frame response for record x 1 In Frame response for record x

7.3.56 Safing record compare complete register (SAF_CC)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	CC_16	CC_15	CC_14	0	0	0	0	CC_9	CC_8	CC_7	CC_6	CC_5	CC_4	CC_3	CC_2	CC_1

ID: FF

Type: R

Read: FF00

Write: -

	POR	WSM	SSM	
CC_xx	0	0	0	Indicates compare complete status of each of the 16 safing records, and defines the end of the sample cycle for safing Cleared by SSM_RESET or upon SPI read, set by safing engine when request, response mask and target registers match the incoming SPI frame 0 Compare not completed for record x 1 Compare completed for record x

7.4 Remote sensor SPI register map

The Remote Sensor SPI interface consists of twelve 32-bit read registers (one for each logical channel) to allow for access to decoded sensor data and fault registers. The registers are addressed by the read register ID and the Global ID bit.

The L9679P checks the validity of the received RID field in the MOSI_RS frame. Should a SPI read command be received containing an unused RID address, the command will be discarded and the ERR_RID bit will be flagged in the current GSW.

Table 8. Remote sensor SPI register map

GID	RID / WID							Hex	R/W	Name	Description	Operating State				
												Init	Diag	Safing	Scrap	Arming
0	1	0	1	0	0	0	0	$50	R	RSDR0	Remote sensor data/status registers (PSI-5 or WSS)					
0	1	0	1	0	0	0	1	$51	R	RSDR1						
0	1	0	1	0	0	1	0	$52								
0	1	0	1	0	0	1	1	$53								
0	1	0	1	0	1	0	0	$54	R	RSDR4						
0	1	0	1	0	1	0	1	$55	R	RSDR5						
0	1	0	1	0	1	1	0	$56								
0	1	0	1	0	1	1	1	$57								
0	1	0	1	1	0	0	0	$58	R	RSDR8						
0	1	0	1	1	0	0	1	$59	R	RSDR9						
0	1	0	1	1	0	1	0	$5A								
0	1	0	1	1	0	1	1	$5B								
0	1	0	1	1	1	0	0	$5C	R	RSTHR0_L	Remote sensor (PSI-5 or WSS)					
0	1	0	1	1	1	0	1	$5D	R	RSTHR1_L						
0	1	0	1	1	1	1	0	$5E	R	RSTHR2_L						
0	1	0	1	1	1	1	1	$5F	R	RSTHR3_L						
0	1	1	0	0	0	0	0	$60								
0	1	1	0	0	0	0	1	$61								
0	1	1	0	0	0	1	0	$62								
0	1	1	0	0	0	1	1	$63								
0	1	1	0	1	0	1	0	$6A	R	ARM_STATE	Arming signals status register					
1	1	1	1	1	1	1	1	$FF	R	SAF_CC	Safing record compare complete register					

7.5 Remote sensor SPI tables

A summary of all the registers contained within the remote sensor SPI map are shown below and are referenced throughout the specification as they apply. The SPI register tables also specify the effect of the internal reset signals assertion on each bit field (the symbol '-'is used to indicate that the register is not affected by the relevant reset signal').

7.5.1 Remote sensor SPI global status word

The Remote Sensor SPI of L9679P contains an 11-bit word that returns global status information. The Global Status Word (GSW) of the Remote Sensor SPI is the most significant 11 bits of MISO_RS data.

Table 9. GSW - Remote sensor SPI global status word

MISO_RS	GSW	Name	POR	WSM	SSM	Description
31	10	SPIFLT	0	0	0	SPI Fault, set if previous SPI frame had wrong parity check or wrong number of bits, cleared upon read '
						0 No fault
						1 Fault
30	9	0	0	0	0	Unused
29	8	RSFLT	0	0	0	Remote Sensor Interface Fault Present, logical OR of the corresponding FLTBIT bits (bit 15) for all faults but NODATA
						0 All the RSDRx-FLTBIT bits are 0
						1 At least one of the RSDRx-FLTBIT bits is 1 and the associated fault code is different from NODATA
28	7	0	0	0	0	Unused
27	6	0	0	0	0	Unused
26	5	0	0	0	0	Unused
25	4	0	0	0	0	Unused
24	3	0	0	0	0	Unused
23	2	0	0	0	0	Unused
22	1	0	0	0	0	Unused
21	0	ERR_RID	0	0	0	Read address received in the actual SPI frame is unused so data in the response is don't care
						0 No Error
						1 Error

7.6 Remote sensor SPI read/write registers

7.6.1 Remote sensor data/fault registers (RSDRx @FLT = 0)

Note: The value in Bit15 (FLT) will re-define the use of the other bits, hence the tables below are divided into two groups (Section 7.6.1 and Section 7.6.2).

Remote Sensor 0 Data and Fault Flag Register ch 0, slot 1 (RSDR0)
Remote Sensor 1 Data and Fault Flag Register ch 1, slot 1 (RSDR1)
Remote Sensor 4 Data and Fault Flag Register ch 0, slot 2 (RSDR4)
Remote Sensor 5 Data and Fault Flag Register ch 1, slot 2 (RSDR5)
Remote Sensor 8 Data and Fault Flag Register ch 0, slot 3 (RSDR8)
Remote Sensor 9 Data and Fault Flag Register ch 1, slot 3 (RSDR9)

Bit 15 = 0 NO FAULT Condition

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI_RS					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO_RS (PSI5)	CRC			0	**FLT=0**	On/Off	LCID [3:0]				DATA [9:0]									

ID: 50 (RSDR0)
51 (RSDR1)
54 (RSDR4)
55 (RSDR5)
58 (RSDR8)
59 (RSDR9)

Type: R

Read: 5000 (RSDR0)
5100 (RSDR1)
5400 (RSDR4)
5500 (RSDR5)
5800 (RSDR8)
5900 (RSDR9)

Write: -

	POR	WSM	SSM	
CRC[2:0]	-	-	-	CRC based on bits [16:0] Updated based on bits [16:0]
FLT	1	1	1	Fault Status - Depending on Fault Status, the DATA bits are defined differently Cleared when all of the following bits are '0': STG, STB, CURRENT_HI, OPENDET, RSTEMP, INVALID, SLOT_ERROR, NODATA

				Set when any of the following bits are '1': STG, STB, CURRENT_HI, OPENDET, RSTEMP, INVALID, SLOT_ERROR, NODATA 0 No fault 1 Fault
On/Off	0	0	0	Channel On/Off Status Cleared by SSM_RESET or when channel is commanded OFF via SPI RSCTRL or when the STG bit is set or the RSTEMP bit is set Set when channel is commanded ON by SPI RSCTRL 0 Off 1 On
LCID[3:0]	-	-	-	Logical Channel ID Updated based on SPI read request 0000 RSU0 SLOT1 0001 RSU0 SLOT2 0010 RSU0 SLOT3 0100 RSU1 SLOT1 0101 RSU1 SLOT2 0110 RSU1 SLOT3
DATA[9:0]	$000	$000	$000	10-bit data from Manchester decoder Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL updated when a valid PSI5 frame is received

7.6.2 Remote sensor data/fault registers (RSDRx @ FLT=1)

Bit 15 = 1 FAULTED condition

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOS_RSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO_RS (PSI5)	CRC			X	**FLT=1**	On/Off	LCID [3:0]				STG	STB	CURRENT_HI	OPENDET	RSTEMP	INVALID	NODATA	SLOT_ERROR	X	X

	POR	WSM	SSM	
CRC[2:0]	-	-	-	CRC based on bits [16:0] Updated based on bits [16:0]
FLT	1	1	1	Fault Status Cleared when all of the following bits are '0': STG, STB, CURRENT_HI, OPENDET, RSTEMP, NODATA, INVALID, SLOT ERROR, PULSE OVERFLOW ERROR Set when any of the following bits are '1': STG, STB, CURRENT_HI, OPENDET, RSTEMP, NODATA, INVALID, SLOT ERROR, PULSE OVERFLOW ERROR 0 No fault 1 Fault
On/Off	0	0	0	Channel On/Off Status Cleared by SSM_RESET or when channel is commanded OFF via SPI RSCTRL or when the STG bit is set or the RSTEMP bit is set Set when channel is commanded ON by SPI RSCTRL 0 Off 1 On
LCID[0:3]	0000	0000	0000	Logical Channel ID Updated based on SPI read request 0000 RSU0 SLOT1 0001 RSU0 SLOT2 0010 RSU0 SLOT3 0100 RSU1 SLOT1 0101 RSU1 SLOT2 0110 RSU1 SLOT3
STG	0	0	0	Short to Ground (in current limit condition) Cleared by SSM_RESET or when channel is commanded OFF via SPI RSCTRL

0 No fault
1 Fault

STB	0	0	0	Short to Battery Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL Not cleared by channel OFF caused by STG or RSTEMP Set when channel voltage exceeds VSUP for a time greater than T_{STBTH} 0 No fault 1 Fault
CURRENT_HI	0	0	0	Current High Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL Set when channel current exceeds ILKGG for a time determined by an up/down counter 0 No fault 1 Fault
OPENDET	0	0	0	Open Sensor Detected Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL Set when channel current exceeds ILKGB for a time determined by an up/down counter 0 No fault 1 Fault
RSTEMP	0	0	0	Over temperature detected Cleared by SSM_RESET or when channel is commanded OFF via SPI RSCTRL Set when over-temp condition is detected 0 No fault 1 Fault
INVALID	0	0	0	Invalid Data Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL or if one of the following is set: STG, STB, CURRENT_HI, OPEN_DET, RSTEMP, SLOT ERROR (PSI5) or if a new valid data is received. Set in PSI5 configuration when two valid start bits are received and a Manchester error (# of bits, bit timing) or parity error is detected 0 No fault 1 Fault
NODATA	1	1	1	No Data in buffer

				Cleared when a valid PSI5/WSS frame is received or if one of the following is set: STG, STB, CURRENT_HI, OPEN_DET, RSTEMP, SLOT ERROR, PULSE OVERFLOW ERROR, INVALID Set upon SPI read of RSDRx and none of the following bits are set: STG, STB, CURRENT_HI, OPEN_DET, RSTEMP, SLOT ERROR, PULSE OVERFLOW ERROR, INVALID 0 No fault 1 Fault
SLOT ERROR	0	0	0	Slot error fault (valid only for PSI5 sensors) Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL or if one of the following is set: STG, STB, CURRENT_HI, OPEN_DET, RSTEMP or if a new valid data is received Set in case of slot control enabled and frame not completely inside slot or more than one frame inside the slot 0 No fault 1 Fault

7.6.3 Remote sensor x current registers y (RSTHRx_y)

Remote sensor 0, base current and delta to calculate 1st top current (RSTHR0_L)
Remote sensor 1, base current and delta to calculate 1st top current (RSTHR1_L

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI_RS	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO_RS	DELTA 1ST TOP [9:0]										BASE CURRENT [9:0]									

ID: 5C (RSTHR0_L)
5D (RSTHR1_L)

Type: R

Read: 5C00 (RSTHR0_L)
5D00 (RSTHR1_L)

Write: -

	POR	WSM	SSM	
BASE CURRENT [9:0]	$A1	$A1	$A1	Base current measured by internal converter (93.75 µA ±9% each LSB).
DELTA 1ST TOP [9:0]	$103	$103	$103	Delta measured by internal converter respect to base current (93.75 µA ±9% each LSB) to get top current. Low threshold = base current+(DELTA_1ST_TOP/2) in case of PSI5 without current averaged algorithm (bit 4 of RSRCx register equal to 0). Low threshold = base current+(DELTA_1ST_TOP) in case of PSI5 with current averaged algorithm (bit 4 of RSRCx register equal to 1).

7.6.4 Arming signals status register (ARM_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI/ MOSI_RS	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MOSI/ MOSI_RS	0	0	0	0	0	0	0	0	0	0	PSINHINT	PSINH_EXP_TIME	ACL_PIN_STATE	ACL_VALID	0	0	ARMINT_2	ARMINT_1	FENL	0

ID: 6A

Type: R

Read: 6A00

Write: -

	POR	WSM	SSM	
ARMINT_x	-	-	-	State of ARMINT signals Updated per Safing Engine output logic diagram in case of internal safing engine otherwise is the echo of ARMx pins
ACL_VALID	0	0	0	Valid ACL detection 0 Cleared when ACL_BAD=2 1 Set when ACL_GOOD=3
ACL_PIN_STATE	-	-	-	Echo of ACL pin
PSINH_EXP_TIME	0	0	0	State of PSINH expiration timer 0 If timer is 0 1 If timer is counting
PSINHINT	-	-	-	State of PSINHINT signal Updated per PSINH output logic diagram in case of internal engine otherwise is the echo of PSINH pin inverted
FENL	-	-	-	State of external arming control signal (used to arm low side of deployment loops only in case of external arming) Updated based on pin state

7.6.5 Safing record compare complete register (SAF_CC)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI/ MOSI_RS	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO/ MISO_RS	0	0	0	0	CC_16	CC_15	CC_14	0	0	0	0	CC_9	CC_8	CC_7	CC_6	CC_5	CC_4	CC_3	CC_2	CC_1

ID: FF

Type: R

Read: FF00

Write: -

	POR	WSM	SSM	
CC_xx	0	0	0	Indicates compare complete status of each of the 16 safing records, and defines the end of the sample cycle for safing Cleared by SSM_RESET or upon SPI read, set by safing engine when request, response mask and target registers match the incoming SPI frame 0 Compare not completed for record x 1 Compare completed for record x

8 Deployment drivers

The squib deployment block consists of 8 independent high side drivers and 8 independent low side drivers. Squib deployment logic requires a deploy command received through SPI communications and either an arming condition processed by safing logic or a proper ARMx input pin assessment, depending on whether the internal safing engine is used or not. Both conditions must exist in order for the deployment to occur. Once a deployment is initiated, it can only be terminated by an SSM_RESET event.

L9679P allows all 8 squib loops to be deployed at the very same time or in other possible timing sequence. Deployment drivers are capable of granting a successful deployment also in case of short to ground on low-side circuit (SRx pins). Firing voltage capability across high side circuit is maximum 25 V. High side and low side drivers account for a maximum series total resistance of 2 Ω. Each loop is granted for a minimum number of deployments of 50, under all normal operating conditions and with a deployment repetition time higher than 10s. Both the High and the Low side FET drivers are equipped with passive gate turn-off circuitries to guarantee the FETs are kept in off state also when the device is unpowered or during power-up/down transients.

8.1 Control logic

A block diagram representing the deployment driver logic is shown below. Deployment driver logic features include:

- Deploy command logic
- Deployment current selection
- Deployment current monitoring and deploy success feedback
- Diagnostic control and feedback

Figure 27. Deployment driver control blocks

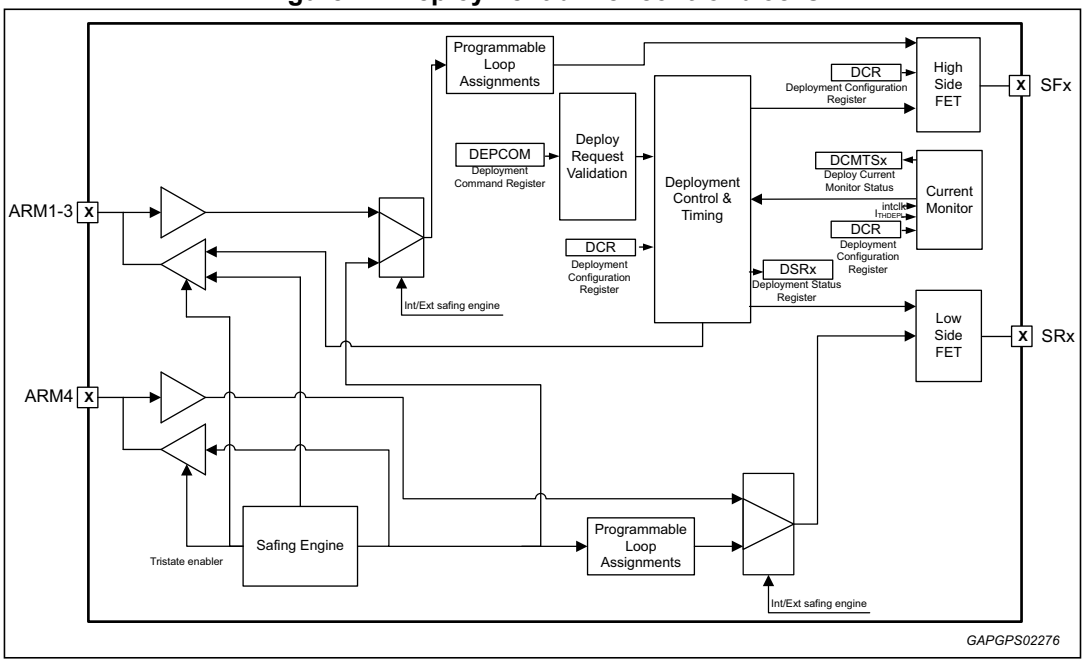


Figure 28. Deployment driver control logic - Enable signal

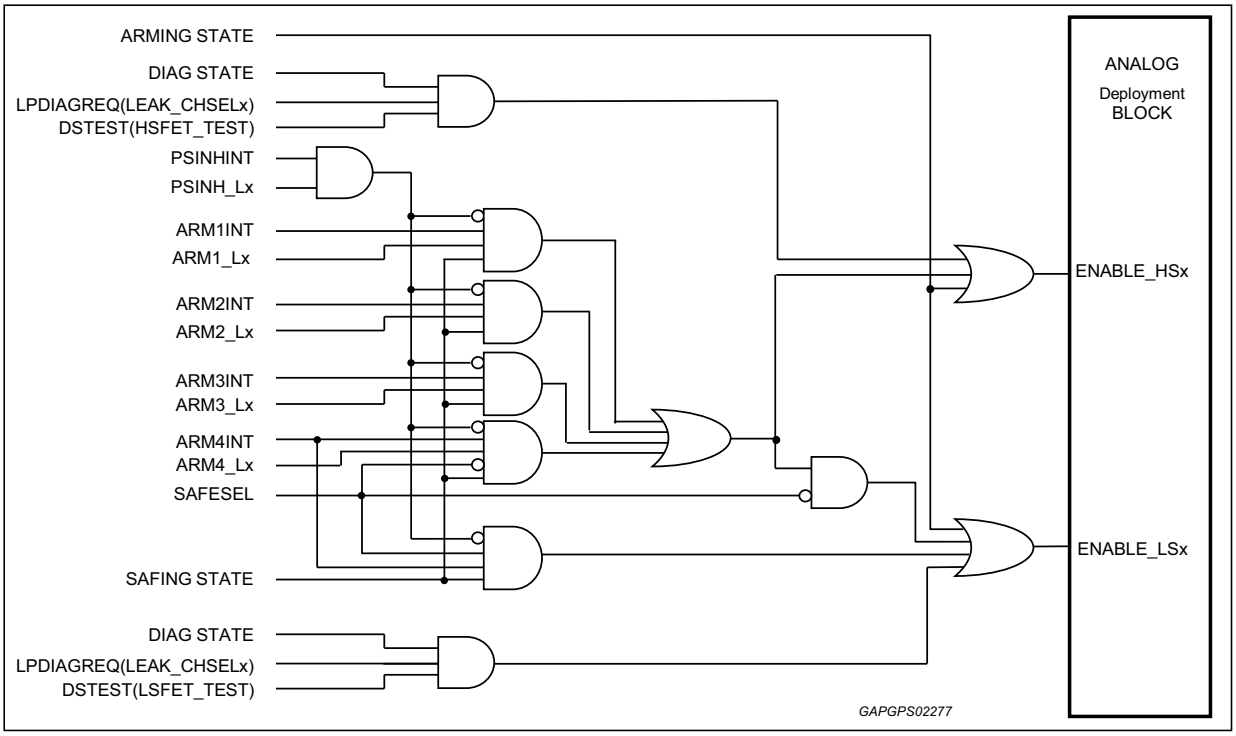
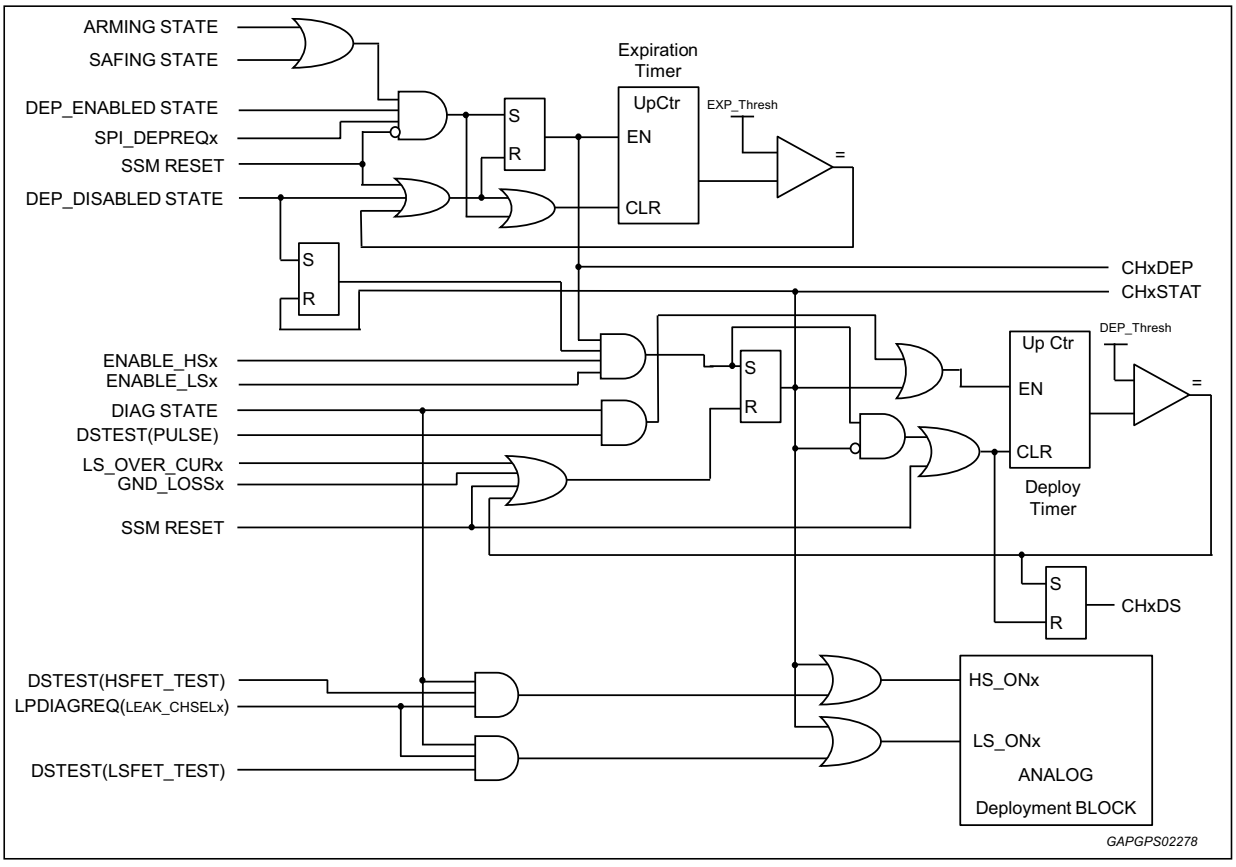
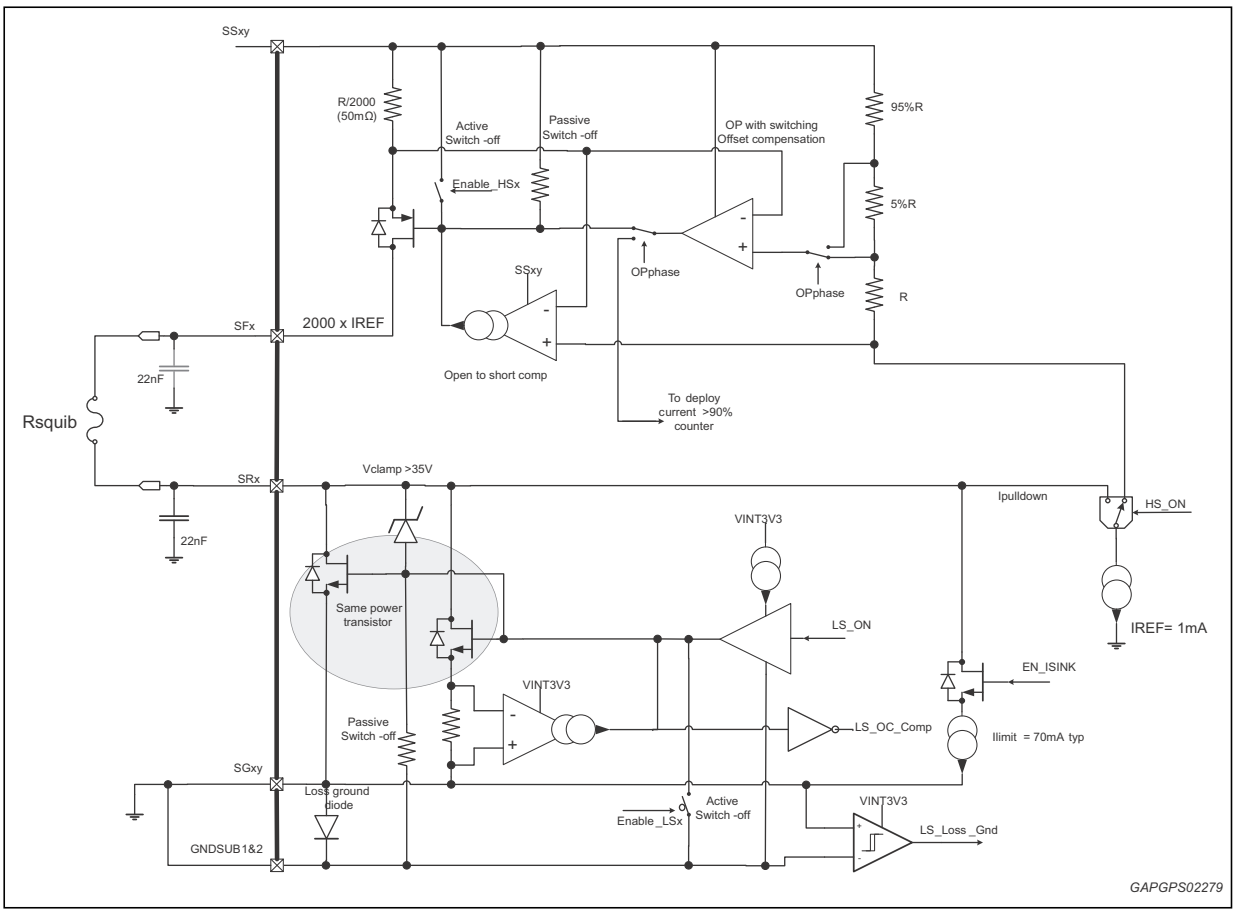


Figure 29. Deployment driver control logic - Turn-on signals



The high level block diagram for the deployment drivers is shown below:

Figure 30. Deployment driver block



8.1.1 Deployment current selection

Deployment current is programmed for each channels using the Deploy Configuration Register (DCRx) shown in *Section 7.3.7*.

The deploy time selection allows the device to deploy for a time up to 4.032 ms. Careful considerations should be done in order to avoid damage on the squib driver section for excessive thermal heat. In order to prevent device damage, it is suggested to avoid excessive voltage drop between SSxy and SFxy. In case the 1.75 A deployment current level is selected, the voltage drop across the pins should be limited to maximum 17 V for deployment times longer than 0.7 ms and up to 2 ms and 15 V up to 3.2 ms. In case 1.2 A is selected, the voltage drop should be limited to maximum 22 V for deployment times longer than 2 ms and up to 3.2 ms.

8.1.2 Deploy command expiration timer

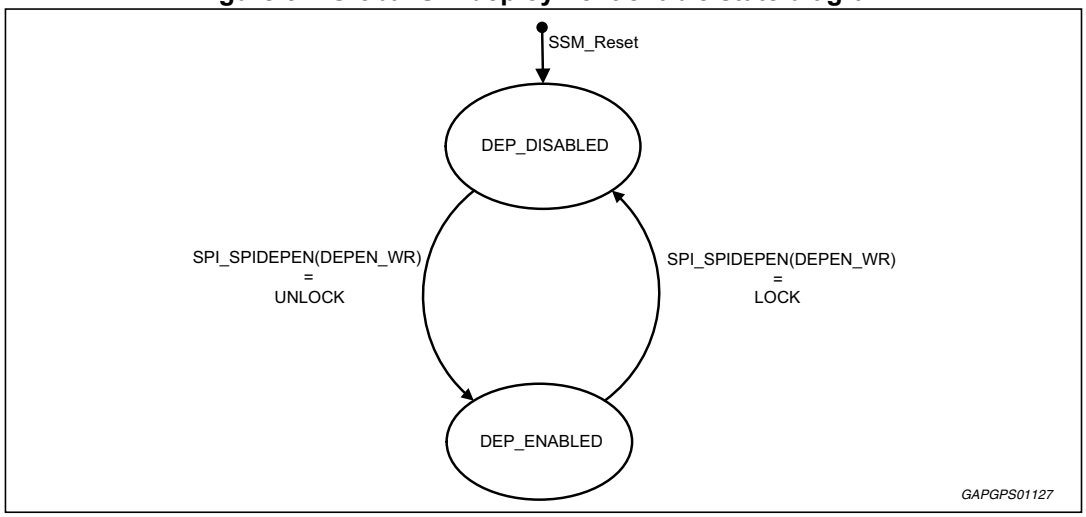
Deploy commands are received for all channels using SPI communications. Once a deploy command is received, it will remain valid for a specified time period selected in the *Deployment configuration registers (DCR_x)*. The deploy status and deploy expiration timer can be read through the *Deployment status registers (DSR_x)*. The deploy expiration timer is selectable via 2 bits and the maximum programmable time is 500 ms nominal.

8.1.3 Deployment control flow

Deployment control logic requires the following conditions to be true to successfully operate a deployment:

- POR = 0
- SSM to be either in Safing State or Arming State
- a valid arming condition processed by safing logic or ARMx signals to be set (depending on selection of internal or external safing engine)
- channel-specific deploy command request bits to be set via SPI in the Deploy command Register (DEPCOM)
- a global deployment state has to be active, as described in the following figure.

Figure 31. Global SPI deployment enable state diagram



In case a multiple deployment request would be needed, i.e. deploying the same channel in sequence, a toggle on DEP_DISABLED has to be performed and a new DEPCOM command on the same channel has to be sent.

The SPI DEPCOM command is ignored if the device is in the DEP_DISABLED state and the deploy command is not set. While in DEP_ENABLED state, the following functionalities that could be active are forced to their reset state:

- All squib and DC sensor diagnostic current or voltage sources
- All squib, DC sensor and ADC diagnostic MUX settings, state machine, etc.

The SPI_LOCK and SPI_UNLOCK signals are available in the SPIDEPEN command:

High-side and Low-side enablers (ARMx) are assigned to the desired channels by means of the programmable loop matrix. Deploy commands in the Deploy Command Register (DEPCOM) are channel specific.

Deployment requires a valid arming condition from safing logic or ARMx signals to be set any time before, during or after the specific sequence of deploy commands is received. It is feasible for a deploy command to be received without a valid arming condition from safing logic or the ARMx being set. In this case, the deploy command will be terminated according to the *Deploy command expiration timer*. Likewise, a valid arming condition signal can be set without receiving a Deploy Command. In this case, the enabling signals will remain

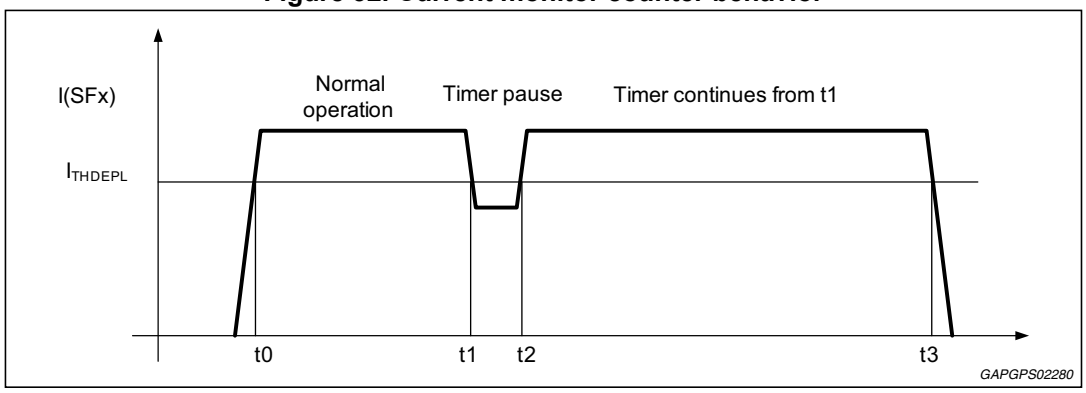
active according to the Arming Enable Pulse Stretch Timer or the ARMx enabling state. The Arming Enable Pulse Stretch Timers is available in the AEPSTS register.

8.1.4 Deployment current monitoring

A current comparator is used to indicate when the output current from the HSD, SFx, exceeds the deployment current threshold, I_{THDEPL}. The timer signal remains active and increments while the current meets the programmed deploy current as set in the Deploy Configuration Register. The deploy current counter value is stored in the Deploy Current Monitor Timer Register XY (DCMTSxy). There is a unique timer register for each channel.

If the deploy current falls below the specified current threshold momentarily and recovers, the deploy current counter will pause during the drop-out and continue once the current exceeds the threshold. The deploy current counter will not be reset by the presence or absence of current in the deployment channel.

Figure 32. Current monitor counter behavior



The deploy current counter is reset to $0000 as soon as a toggle on DEP_DISABLED is performed and a new DEPCOM command on the same channel is received.

8.1.5 Deployment success

Deploy success flag is set when the deploy timer elapses. This bit (CHxDS) is contained in the Deploy Status Register. Within the Global Status Word register (GSW), a single bit (DEPOK) is also set once any of the 12 deployment channels sets a deploy success flag.

8.2 Energy reserve - deployment voltage

One deployment voltage source pin is used for adjacent channels (e.g. SS23 for channels 2 and 3). These pins are directly connected to the high side drivers for each channel.

8.3 Deployment ground return

L9679P is hosted in a particular frame allowing squib driver ground feedback to be connected to an internal ground ring. This ring is electrically connected to the package exposed pad and to the GNDSUB1 and GNDSUB2 pins. Connection to these two pins is made by means of a strong metal layer, therefore this connection is sufficient for all deployments occurring simultaneously, even in case of only one out of the three possible connections being available.

8.4 Deployment driver protections

8.4.1 Delayed low-side deactivation

To control voltage spikes at the squib pins during drivers deactivation at the end of a deployment, the low side driver is switched off after $t_{depl\_ls\text{-}dly}$ delay time with respect to the high side deactivation.

8.4.2 Low-side voltage clamp

The Low side driver is protected against overvoltage at the SRx pins by means of a clamping structure as shown in *Figure 30*. When the Low side driver is turned off, voltage transients at the SRx pin may be caused by squib inductance. In this case a low side FET drain to gate clamp will reactivate the low side FET allowing for residual inductance current recirculation, thus preventing potential low side FET damage by overvoltage.

8.4.3 Short to battery

The Low side driver is equipped with current limitation and overcurrent protection circuitry. In case of short to battery at the squib pins, the short circuit current is limited by the Low side driver to I_{LIMSRx}. If this condition lasts for longer than t_{LIM} deglitch filter time then the low and high-side drivers will be switched off and latched in this state until a new deployment is commanded after SPI_DEPEN is re-triggered.

8.4.4 Short to ground

The squib driver is designed to stand a short to ground at the squib pins during deployment. In particular, the current flowing through the short circuit is limited by the high side driver (deployment current) and the high-side FET is sized to handle the related energy.

In case the short to ground during deployment occurs after an open circuit, a protection against damage is also available. The high side current regulator would have normally reacted to the open circuit by increasing the Vgs of the high side FET. Thanks to a dedicated fast comparator detecting the open condition, the driver is able to discharge the FET gate quickly in order to reduce current overshoot and prevent potential driver damage when the short to ground occurs.

8.4.5 Intermittent open squib

A dedicated protection is also available in case of intermittent open load during deployment. In this case, if load is restored after an open circuit, due to slow reaction of the high-side current regulation loop, the current through the squib is limited only to I_{LIMSRx} by the low side driver. If this condition lasts for longer than t_{LIMOS} then the high side is turned off for $t_{HSOFFOS}$ and then reactivated. By this feature, intermittent open squib and short to battery faults may be distinguished and handled properly by the drivers.

8.5 Diagnostics

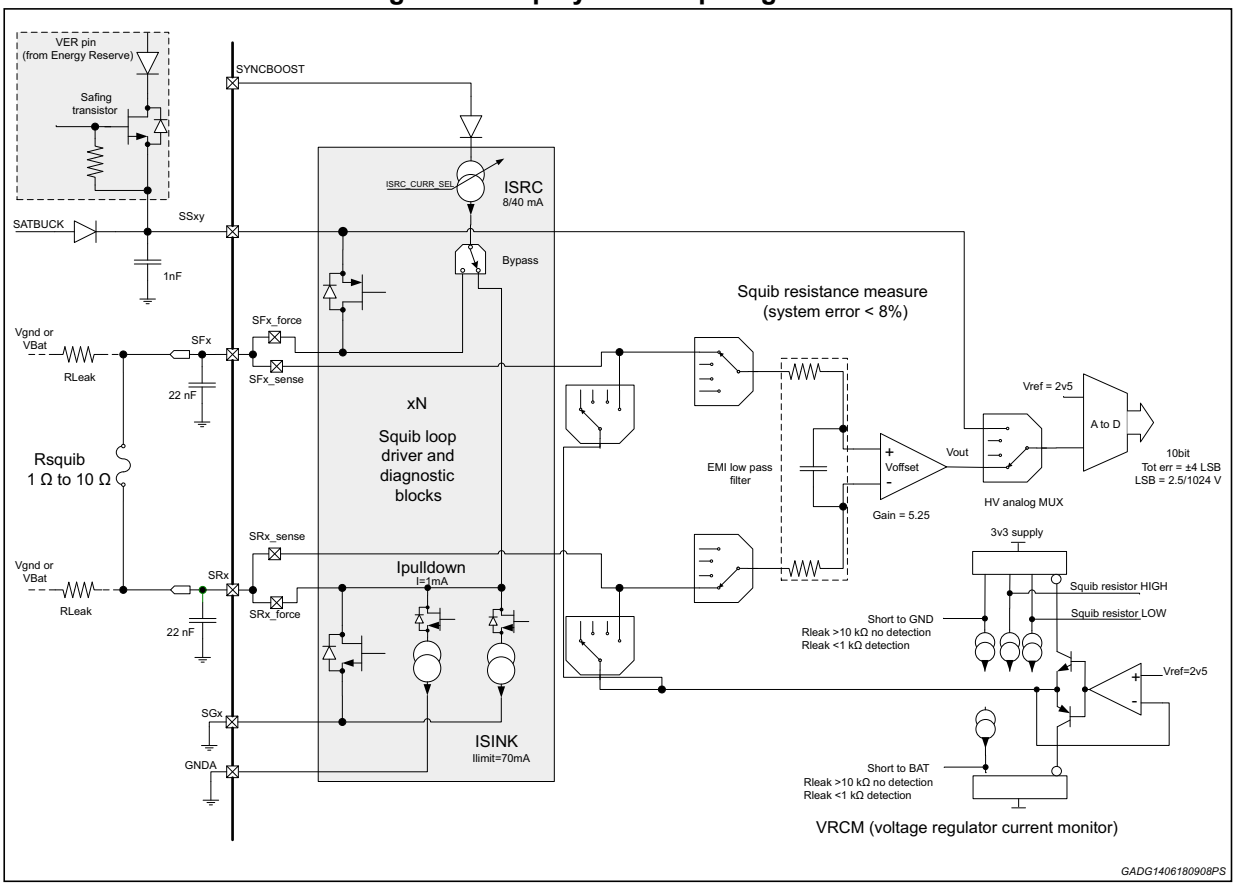
The L9679P provides the following diagnostic feedback for all deployment channels:

- High voltage leakage test for oxide isolation check on SFx and SRx
- Leakage to battery and ground on both SFx and SRx pins with or without a squib
- Short between loops diagnostics
- Squib resistance measurement with leakage cancellation and selectable range (10/50 Ω)
- High squib resistance with range from 500 Ω to 2000 Ω
- SSxy, SFx and VER voltage status
- High and Low side FET diagnostics
- High side driver diagnostics
- Loss of ground return diagnostics
- High Side Safing FET diagnostics

The above diagnostic results are processed through a 10 bit Analog to digital algorithmic converter. These tests can be addressed in two different ways, with a high level approach or a low-level one. The main difference between the two approaches is that with the low level approach the user is allowed to precisely control the diagnostic circuitry, also deciding the proper timings involved in the different tests. On the other hand, the high level approach is an automatic way of getting diagnostic results for which an internal state machine is taking care of instructions and timings.

The following is block diagram of the Squib Diagnostics.

Figure 33. Deployment loop diagnostics



The leakage diagnostic includes short to battery, short to ground and shorts between loops. The test is applied to each SFx and SRx pin so shorts can be detected regardless of the resistance between the squib pins.

8.5.1 Low level diagnostic approach

In this approach, each of the test steps described in the sections below requires user intervention by issuing the proper SPI command.

High voltage leakage test for oxide isolation check

This test is mandatory to address possible leakages that could not be experienced at low voltages on SFx or SRx pins. The I_{source} current generator (ISRC) is enabled on the chosen SFx pin. To confirm that the SFx pin has then reached a suitable voltage level, a dedicated ADC measurement on the SFx pin can be requested. Once this test is performed, a leakage test on SFx and SRx pins can be issued to double check possible leakages.

Leakage to battery/ground diagnostics

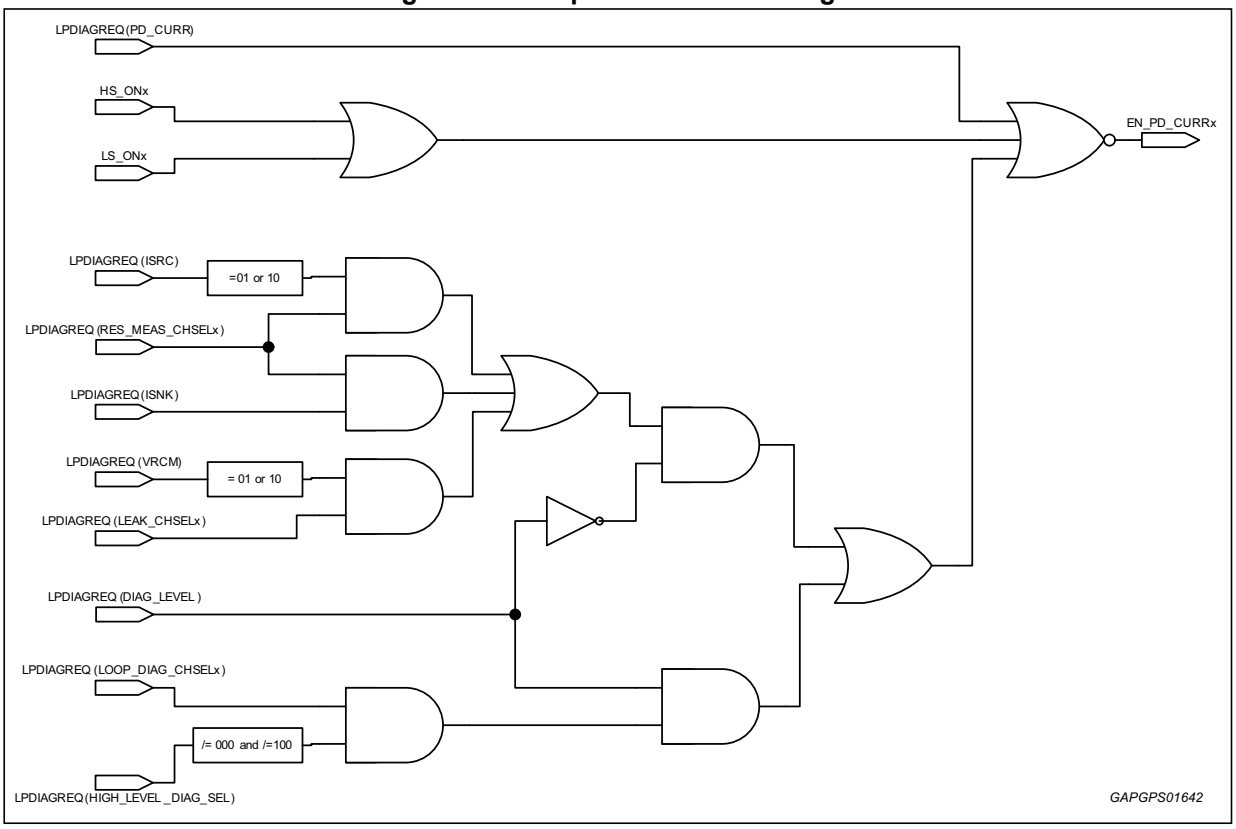
Prior to the real test, the Voltage Regulator Current Monitor block (VRCM) has to be tested and validated. The validation of VRCM goes into verifying both the short to battery and short to ground flags.

The I_{source} current generator (ISRC) is first connected to SFx pin to raise its voltage to SYNCBOOST. Then, the Voltage Regulator Current Monitor block (VRCM) is enabled and

connected to the selected SFx pin. The I_{sink} current limited switch (ISNK) is turned off, as well as the pull-down current generator. If the VRCM block works properly, the short to battery flag would be asserted.

Then, the I_{sink} current limited switch (ISNK) is connected to SRx pin, the Voltage Regulator Current Monitor block (VRCM) is enabled and connected to the selected SRx pin. The I_{source} current generator (ISRC) is turned off, as well as the pull-down current generator. If the VRCM block works properly, the short to ground flag would be asserted.

Figure 34. SRx pull-down enable logic



Once the VRCM block is validated, the real leakage tests can be performed. ISRC and ISNK currents have to be kept switched off. The VRCM shall be connected to the desired pin (either SFx or SRx pins); by doing this, also the pull-down current on the selected SRx pin is automatically deactivated). During the test, if no leakage is present the voltage on the selected SFx or SRx pin will be forced by the VRCM to the VREF level and no current is detected or sourced by the VRCM. If there is leakage to ground or battery, the VRCM will sink or source current trying to maintain VREF. Two current comparators, ISTB and ISTG, will detect the abnormal current flow and the relative flags will be given in the LPDIAGSTAT. These flags are not latched and report the real time status of the relevant comparators in case of low-level leakage diagnostic test. Voltage conversion is not required to have these flags updated. In LPDIAGSTAT register are also reported the channel and the pin (SFx or SRx) under test, respectively with LEAK_CHSEL and SQP bit fields.

The pull-down currents on the other SRx pins are still active. Therefore, the leakage test that would show a leakage to ground may be depending on a real leakage on the pin under test or on a short between loops.

Short between loops diagnostics

In case the previous test has reported a leakage to ground fault, the short between loops diagnostics shall be run. The same procedure is followed as described for normal leakage tests except the fact that in this case all the pull-down current generators have to be deactivated (not only the one for the pin under test), by means of the PD_CURR bit in the Diagnostic Request Register (LPDIAGREQ). If a leakage or ground fault is not present, then the channel under test has a short to another squib loop.

Table 10. Short between loops diagnostics decoding

Fault condition on squib channel	Channel leakage diagnostics with PD_CURR on (for other channels than the one under test	Channel leakage diagnostics with PD_CURR off (for all channels)
No shorts	No fault	No fault
Short to battery	STB fault	STB fault
Short to ground	STG fault	STG fault
Short between loops	STG fault	No fault

The condition of two open channels, i.e. without squib resistance connecting SFx to SRx, that have a short between loops on SFx cannot be detected. If only one of the two shorted SFx pins is open, the fault will be indicated on the open channel.

Squib resistance measurement

During a resistance measurement, a two-step process is performed. At the first step, both ISRC current generator and ISNK current limited switch are enabled and connected to the selected SFx and SRx channel, through ISRC, ISRC_CURR_SEL, ISNK and RES_MEAS_CHSEL bit fields in the Loop Diagnostic Request Register (LPDIAGREQ). The ISRC current can be configured to either 40 mA or 8 mA nominal value through the ISRC_CURR_SEL bit in the LPDIAGREQ register providing the user with two different measurement range options. A differential voltage is created between the SFx and SRx pin based on the ISRC current and squib resistance between the pins. The SPI interface will provide the first resistance measurement voltage (Vdiff1) based on the amplifying factor of the differential amplifier and a 10 bit internal ADC conversion. The second measurement step (bypass measurement) is performed redirecting ISRC to the selected SRx pin, while keeping ISNK on; this way, the differential amplifier and following ADC will output the offset measurement through SPI (Vdiff2). Microcontroller is then allowed to calculate the mathematical difference between first and second measurements to obtain the real squib resistance value.

$$V_{diff1} = G_{RSQ} \times \left[I_{SRC\_*} \times \left(\frac{R_{LKG\_SF} \times R_{SQ}}{R_{LKG\_SF} + R_{SQ}} \right) + \frac{R_{SQ}}{R_{LKG\_SF} + R_{SQ}} (V_{LKG\_SF} - V_{SRx\_RM}) \right] +$$

$$+ G_{RSQ} \times V_{off\_RSQ}$$

$$V_{diff2} = \frac{G_{RSQ} \times R_{SQ}}{R_{LKG\_SF} + R_{SQ}} \times (V_{LKG\_SF} - V_{SRx\_RM}) + G_{RSQ} \times V_{off\_RSQ}$$

$$R_{SQ} = \frac{V_{diff1} - V_{diff2}}{G_{RSQ} \times I_{SRC\_*}} \text{ (assuming } R_{LKG\_SF} >> R_{SQ})$$

The simplification in the calculation method reported above can result in some amount of error that is already incorporated in the overall tolerance of the squib resistance measurement reported in the electrical parameters table.

Values of each measurement step can be required addressing the proper ADCREQx code in *Section 7.3.32: ADC request and data registers (DIAGCTRL_x)*.

This calculation is tolerant to leakages and, thanks to a dedicated EMI low-pass filter, also to high frequency noises on squib lines. Moreover, L9679P features a slew rate control on the ISRC current generator to mitigate emissions.

High squib resistance diagnostics

With this test, the device is able to understand if the squib resistance value is below 200 Ω, between 500 Ω and 2000 Ω or beyond 5000 Ω. During a high squib resistance diagnostics, VRCM and ISNK are enabled and connected respectively to SFx and SRx on the selected channel. VREF voltage level will be output on SFx. Current flowing on SFx will be measured and compared to I_{SRlow} and I_{SRhigh} thresholds to identify if the resistance is above or below RSRlow or RSRhigh levels. The results are reported in the LPDIAGSTAT register. The relative flags (HSR_HI and HSR_LO) are not latched and reflect the current status of the comparators.

High and low side FET diagnostics

This couple of tests can only be run during the diagnostic mode of the power-up sequence *Figure 10*. Tests are performed individually for HS driver or LS driver, with two dedicated commands. Prior to either the HS or LS FET diagnostics being run, the VRCM has to be first enabled. Within the command to enable the VRCM, also the channel onto which the FET test will be run has to be selected with the LEAK_CHSEL bit field. Running the leakage diagnostics with the appropriate delay time prior to either the HS or LS FET diagnostics will precondition the squib pin to the appropriate voltage level. When the FET diagnostic command is issued with the Diagnostic Register SPI command (SYSDIAGREQ), the VRCM flags will be cleared, the VRCM deglitch filter time is switched from the leakage diagnostic deglitch filter time (TFLT_LKG) to the FET test deglitch filter time (TFLT_LKGB_FT) for both HS and LS and the output of the VRCM deglitch filter is now allowed to disable the appropriate HS or LS squib driver during FET test.

The device monitors the current through the VRCM. If the FET is working properly, this current will exceed $I_{HS\_FET\_TH}$ or $I_{LS\_FET\_TH}$ current threshold, respectively for HS or LS FET test for the deglitch filter time of TFLT_LKGB_FT, and the driver under test is turned off immediately and automatically.

If there is a substantial leakage fault to Vbat or GND present during the FET test, leading this leakage current to exceed the IHS_FET_TH or ILS_FET_TH current threshold, for the deglitch filter time of TFLT_LKGB_FT, then the driver under test is turned off immediately and automatically, and the corresponding VRCM flag, STG or STB, is set.

If the current does not exceed the current threshold, the test will be terminated and the driver is anyway turned off within $T_{FETTIMEOUT}$.

Table 11. HS FET TEST

VRCM Flags		Result
STG	STB	
0	0	FET test fail
0	1	FET test pass OR Leakage to Vbat
1	0	FET test disabled due to Leakage to Gd
1	1	State not possible

Table 12. LS FET TEST

VRCM Flags		Result
STG	STB	
0	0	FET test fail
0	1	FET test disabled due to Leakage to Vbat
1	0	FET test pass OR Leakage to GND
1	1	State not possible

During $T_{FETTIMEOUT}$ period, the bit stating that the FET is enabled will be set (FETON=1) and will be cleared as soon as the FET is switched back off.

For all conditions the current on SFx/SRx pins will not exceed the VRCM current limitation value ($I_{LIM\_VRCM\_SINK}$ or $I_{LIM\_VRCM\_SRC}$). There may be higher currents on the squib lines due to the presence of filter capacitors. During these FET tests, energy available to the squib is limited to less than E_{FET_TEST}. For high side FET diagnostics, if no faults were indicated in the preceding leakage diagnostics then a normal result would be [STB=1, STG=0]. If the returned result for the high side FET test is not as the previous then either the FET is not functional, a short to ground occurred during the test, or there is a missing SSxy connection for that channel.

For low side FET diagnostics if no faults were indicated in the preceding leakage diagnostics then a normal result would be [STB=0, STG=1]. If the returned result for the low side FET test is not as the previous then either the FET is not functional or a short to battery occurred during the test. In case of ground loss the low-side FET diagnostic would not indicate a FET fault.

The VRCM flags will be given in the LPDIAGSTAT register. The status of the VRCM flags after FET test is latched and can be cleared upon either LPDIAGREQ or SYSDIAGREQ SPI commands.

Finally, after FET test is completed, the VRCM deglitch filter time is switched from the FET test deglitch filter time (TFLT_LKGB_FT) to the leakage diagnostic test deglitch filter time

(TFLT_LKG) for both HS and LS and the output of the VRCM deglitch filter is now not allowed to disable the appropriate HS or LS squib driver anymore.

High side driver diagnostics

This test is intended to verify the proper functionality of the HS FET driver, but also the external squib connection and other internal circuitries.

First, the ISNK current has to be activated via the LPDIAGREQ register; the channel onto which the ISNK current is activated has to be selected with the RES_MEAS_CHSEL bit field. Then, the HS FET related to the loop channel as indicated in the RES_MEAS_CHSEL bit field is activated with the dedicated DSTEST code for the HS squib driver test in the Diagnostic Register SPI command (SYSDIAGREQ). In such condition, the HS driver will control the FET current to a level $I_{LIM\_HS\_FET}$ much lower than the usual deployment current. The HS_DRV_OK flag will be set accordingly to the test result in the LPDIAGSTAT register, as soon as the deployment current monitoring comparator will detect that the current through the HS FET exceeds the diagnostic current threshold, 90%*$I_{LIM\_HS\_FET}$.

Loss of ground return diagnostics

This diagnostics is available during a squib measurement or a high side driver diagnostics. This test is based on the voltage drop across the ground return, if the voltage drop exceeds SG_{xy_OPEN}, ground connection is considered as lost. Should the ground connection on the squib driver circuit be missing, the bit related to the channel under test by the two above diagnostics will be activated in the LP_GNDLOSS register. The flag is latched after a proper filter time T_{FLT_SGOPEN} and cleared upon read.

High side safing FET diagnostics

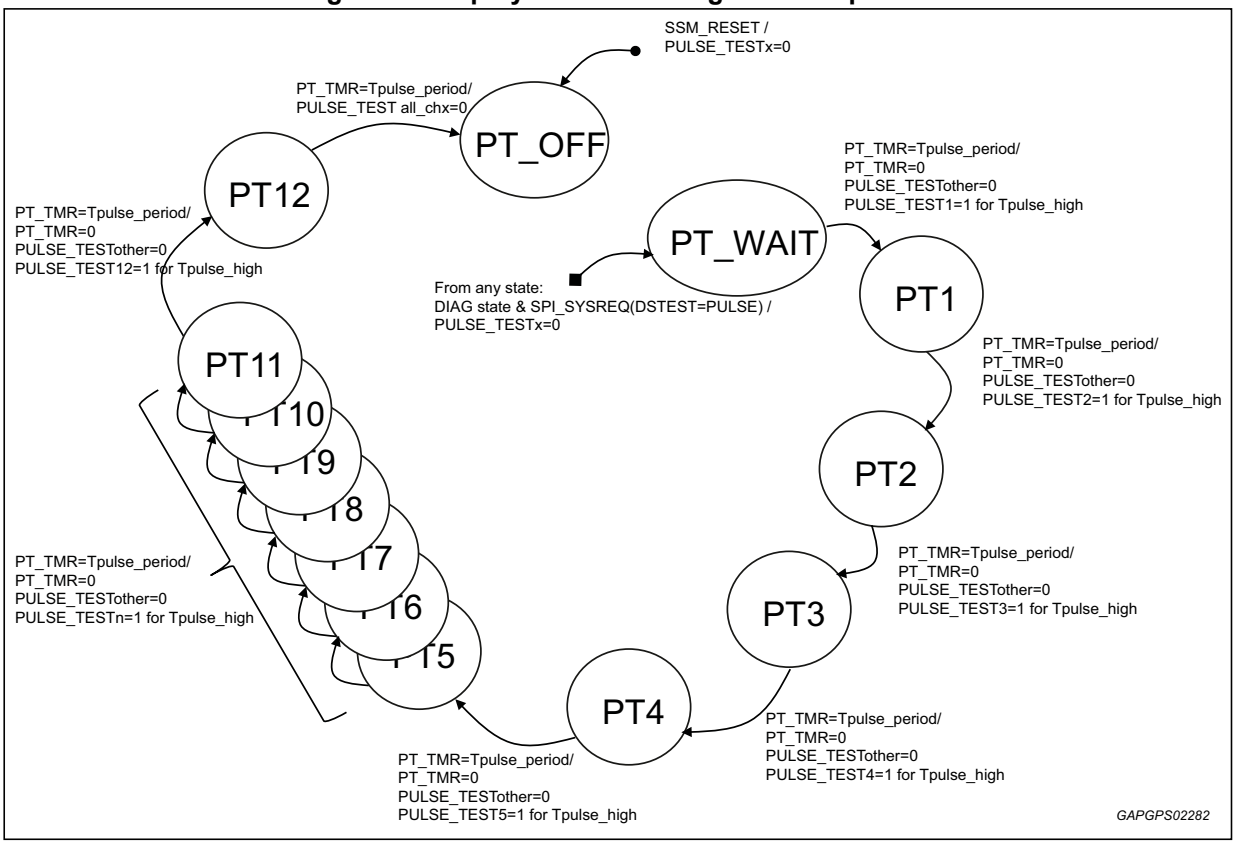
This test has to be issued during the Diag state of the power-up sequence (*Figure 10*). Safing FET has to be switched on with the proper code in DSTEST bit field of the SYSDIAGREQ. Therefore, when the command is received, the device will activate VSF regulator to supply the external safing FET controller. The user can measure the voltage levels of both the VSF regulator and the SSxy nodes. If the safing FET is properly switched on, the voltage on SSxy will be regulated.

The measurement request is done via Diagnostic Control command (DIAGCTRLx), while results will be reported through ADCRESx bit fields.

Deployment Timer diagnostic

This test allows verifying the correct functionality and duration of the timers used to control the deployment times. This test can be executed only when the IC is in the Diag state by setting the appropriate code in the DSTEST field of the SYSDIAGREQ register. When the test is launched, the IC sequentially triggers the activation of the deployment timers of the various channels (each of them separated by 8ms idle time) and outputs the relevant waveform to the ARM1 output discrete pin. See the sequence detail in *Figure 35*. The µC can therefore test the deployment times by measuring the duration of the high pulses sent by the IC on the ARM1 pin. The deployment time configuration used during this test is the latest one programmed in the DCRx registers. In case the test is run on a channel with no DCRx deployment time previously configured, a default 8 µs high pulse is output on ARM for the relevant channel.

Figure 35. Deployment timer diagnostic sequence



Squib diagnostic with common SRx connected loops

In case of two SRx pins are intentionally connected together, the PD_CURR_CSR bit of the Deployment Configuration register (DCR_x, where x = 0, 2, 4, 6, 8, A) must be used to indicate which loop pairs have the common SRx connection. The purpose of this additional bit is to control the pull-down current on each channel to be consistent with or without the Common SRx connected loops. When the DCR_x(PD_CURR_CSR) bit is set for one loop pair and the Deployment diagnostic is run on that loop pair, the pull-down current is disabled on both channels of the loop pair selected.

For the squib channel pair with common SRx connection, to understand if the two SFx pins are shorted together, the squib resistance measurement must be required with the following setting: LPDIAGREQ[12:11]=11. In this way the ISRC current generator is enabled on the channel selected by RES_MEAS_CHSEL[3:0] bits while the Differential Operational Amplifier is connected on the other channel of the squib channel pair. If the short between the two SFx pin is not present then the Squib resistance measurement results will be close to 0, otherwise it will be half the real squib resistance.

Loop diagnostics control and results registers

Diagnostic tests and channels for each test are controlled through the Loop Diagnostic Request Register (LPDIAGREQ), diagnostic results are stored in the Loop Diagnostic Status Register (LPDIAGSTAT).

8.5.2 High level diagnostic approach

In this approach, the test steps described in the sections below are coded into a dedicated state machine that helps reducing the user intervention to a minimum.

The high-level diagnostic commands are contained in the LPDIAGREQ, LOOP_DIAG_SEL, and LOOP_DIAG_CHSEL registers. The high-level diagnostic response is available in the LPDIAGSTAT register.

The concept is depicted in the following figures.

Figure 36. High level loop diagnostic flow1

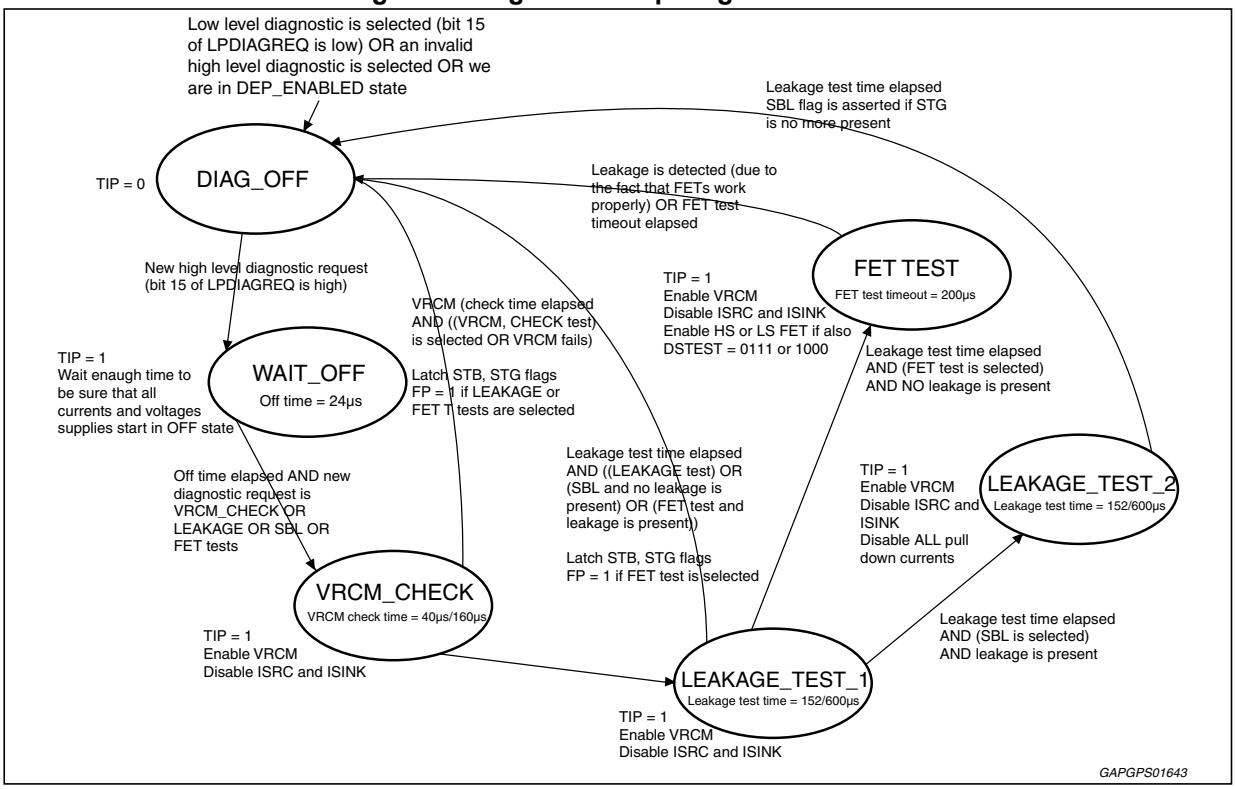
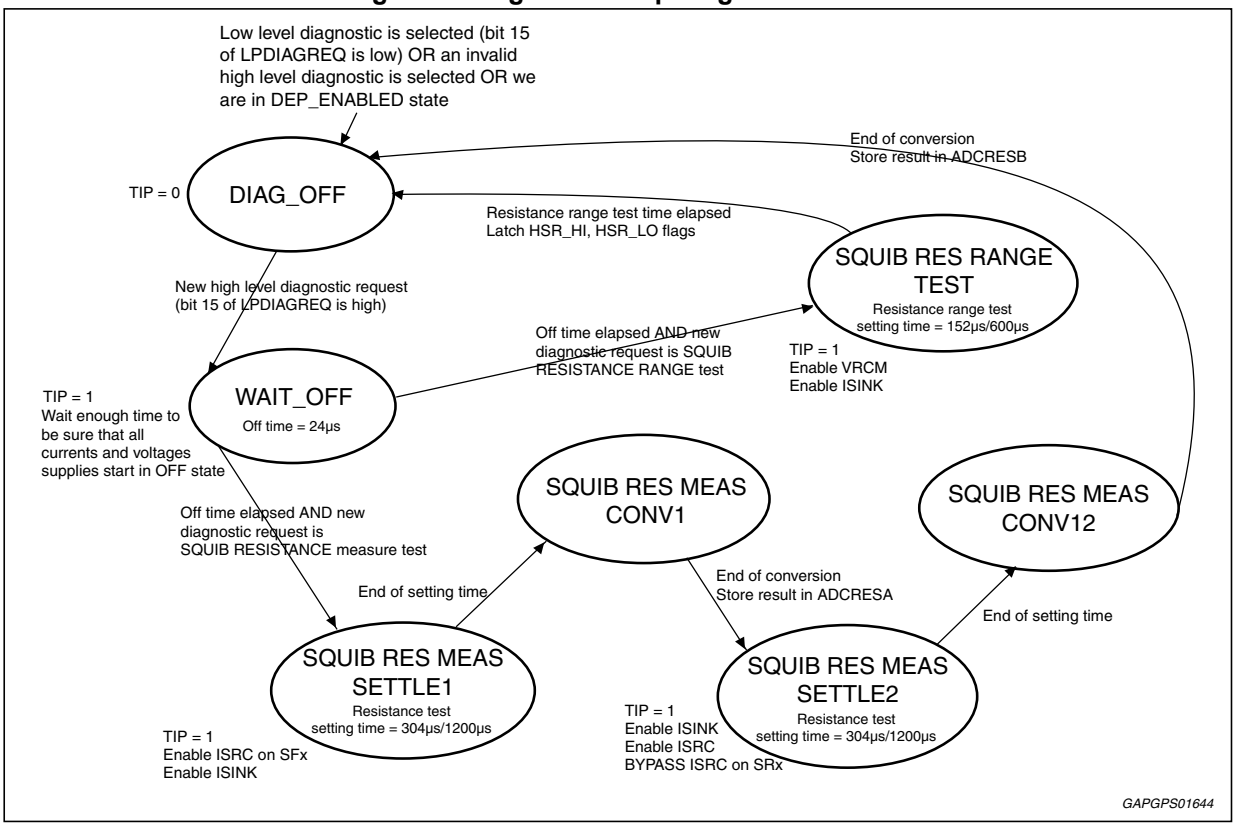


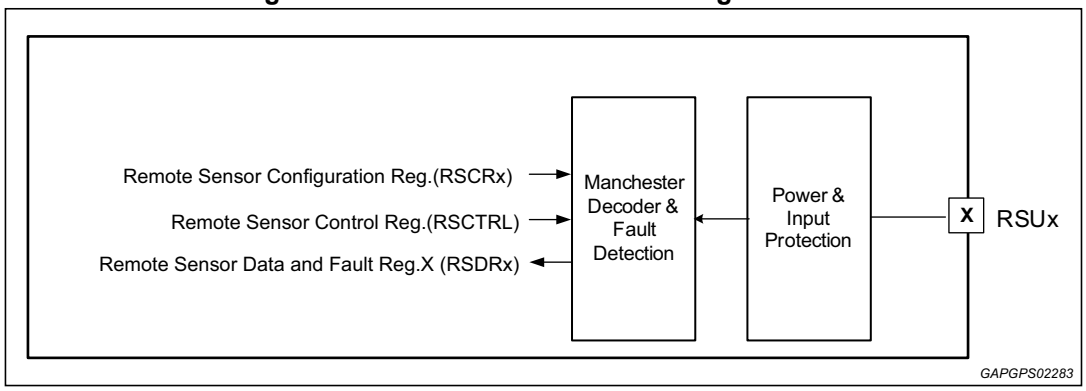
Figure 37. High level loop diagnostic flow2



9 Remote sensor interface

The L9679P contains 2 remote sensor interfaces, capable of supporting PSI-5 protocol (synchronous mode, increased voltage, extended range) . A simplified block diagram of the interface is shown below. The interface supply is given on the SATBUCK pin (refer to *Figure 3: Power supply block diagram*). The circuitry consists of a power interface that mirrors current flowing in the external sensor and transmits this current information to the decoder, which produces a digital value for each remote sensor channel. The voltage at the RSUx pins can be limited by the power interface in case of SATBUCK supply overvoltage to protect the external sensors. Decoded data are then output through the Remote Sensor Data Registers (RSDRx). Received signals can be processed to the corresponding discrete logic output pin WS0-WS1. The power interface also contains error detection circuitry. When a fault is detected, the error code is stored in a global SPI data buffer in the Remote Sensor Data Registers (RSDRx).

Figure 38. Remote sensor interface logic blocks



Remote sensor configuration can be addressed via the Remote Sensor Configuration Registers (RSCRx). In particular, TSxDIS bit allows overriding the time slot control for PSI5 I/F and BLKTxSEL allows selection between 5 ms and 10ms for the blanking time applied to the current limitation fault detection each time a channel is activated.

The Remote Sensor Control Register (RSCTRL) allows for interface channels to be switched on and off and for Sync Pulse control via SPI.

The remote sensor interface reports both data information and fault information in the Remote Sensor Data Register (RSDRx). The device accommodates for a total of 6 data registers. Independent data registers are defined for each remote sensor interface.

If the device detects an error on the sensor interface, the MSB in RSDRx (FLTBIT) will be set to '1' and the following bits will be used to report the detected errors. Otherwise, the register will contain only data information. Detailed information on data and fault reporting are explained in the following sections.

When a fault condition is detected, the RSFLT bit of the global status word (GSW) is set to 1. Faults other than Short to Ground and Over-temperature will only clear after read, not by the disabling of channel.

Data are cleared upon reading the RSDRx register.

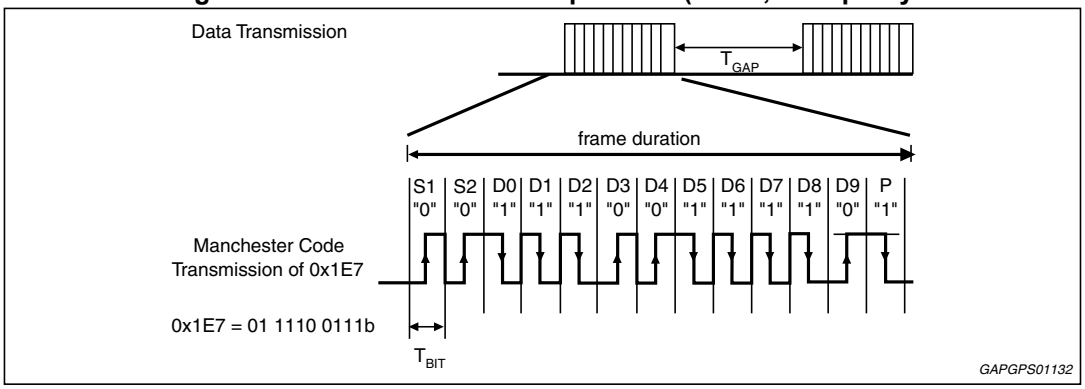
9.1 PSI5 mode

All channels are compliant to the PSI-5 v1.3 specification as described below:

- Two-wire current interface
- Manchester coded digital data transmission
- High data transmission speeds of 125 kbps and 189 kbps
- Variable data word length (8 & 10 bit only)
- 1-bit parity
- Synchronous operating mode with 3 time slots

An example of the data format for one possible PSI-5 protocol configuration is shown below. Data size and the error checking may vary, but the presence of 2 sync start bits (referenced below as sync bits) and 2 T_{Gap} time is consistent regardless.

Figure 39. PSI-5 remote sensor protocol (10-bit, 1-bit parity



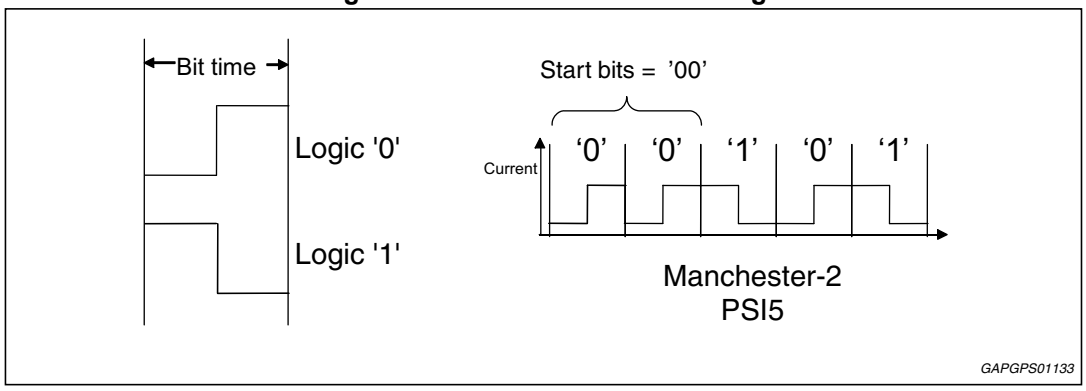
9.1.1 Functional description

The Remote Sensor Interface block provides a hardware connection between the microcontroller and up to twelve remote sensors (maximum three per channel). Each channel is independent on the others, and is not influenced by possible fault conditions occurring on other channels, such as short circuits to ground or to vehicle battery. Each channel is supplied by a current limited DC voltage derived from SATBUCK, and monitors the current sunk from its supply in order to extract encoded data. The remote sensor modulates the current draw to transmit Manchester-encoded data back to the receiver. The current level detection threshold for all channels is internally computed by the IC in order to adapt the signal level to the sensors quiescent current.

All channels can be enabled or disabled independently via SPI commands. The operational status of all channels can also be read via SPI command. All channels support individual selective sync-pulse control to allow communication back to the remote sensor via sync-pulse voltage modulation as described in the PSI5 v1.3 specification.

The message bits are encoded using a Manchester format, in which logic values are determined by a current transition in the middle of the bit time. When configured for PIS5 sensors each interface supports Manchester 2 encoding as shown in *Figure 40*.

Figure 40. Manchester bit encoding

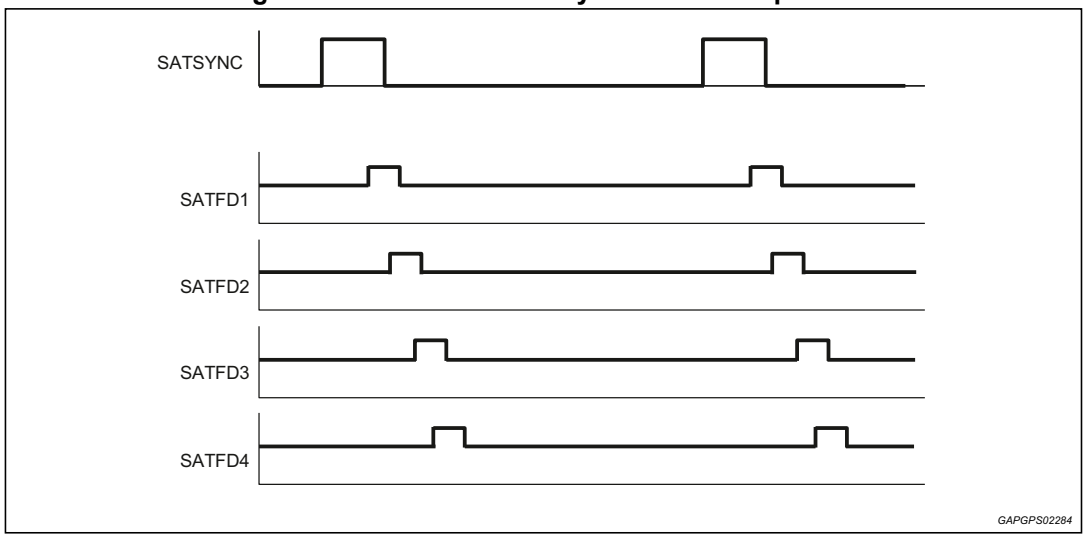


The sensor input filter time, deglitch filter, (delay until a threshold crossing is detected) can be configured in 15 steps. Filters can be selected individually for each channel, through the Remote Sensor Configuration Register, WSFILT bits

The received message data are stored in input data registers that are read out by the microcontroller via the SPI interface. For PSI5, three data registers per channel are used to store remote sensor messages received during timeslots 1, 2, and 3 respectively. Each register is updated after a certain delay ($T_{WRITE\_EN\_DELAY}$) from the end of relative sensor message. All the bits inside the register itself are simultaneously updated upon reception of the remote sensor message to prevent partial frame data from being sampled via the SPI interface. After the data for a given channel is read via the SPI interface, subsequent requests for data from this channel will result in an error response.

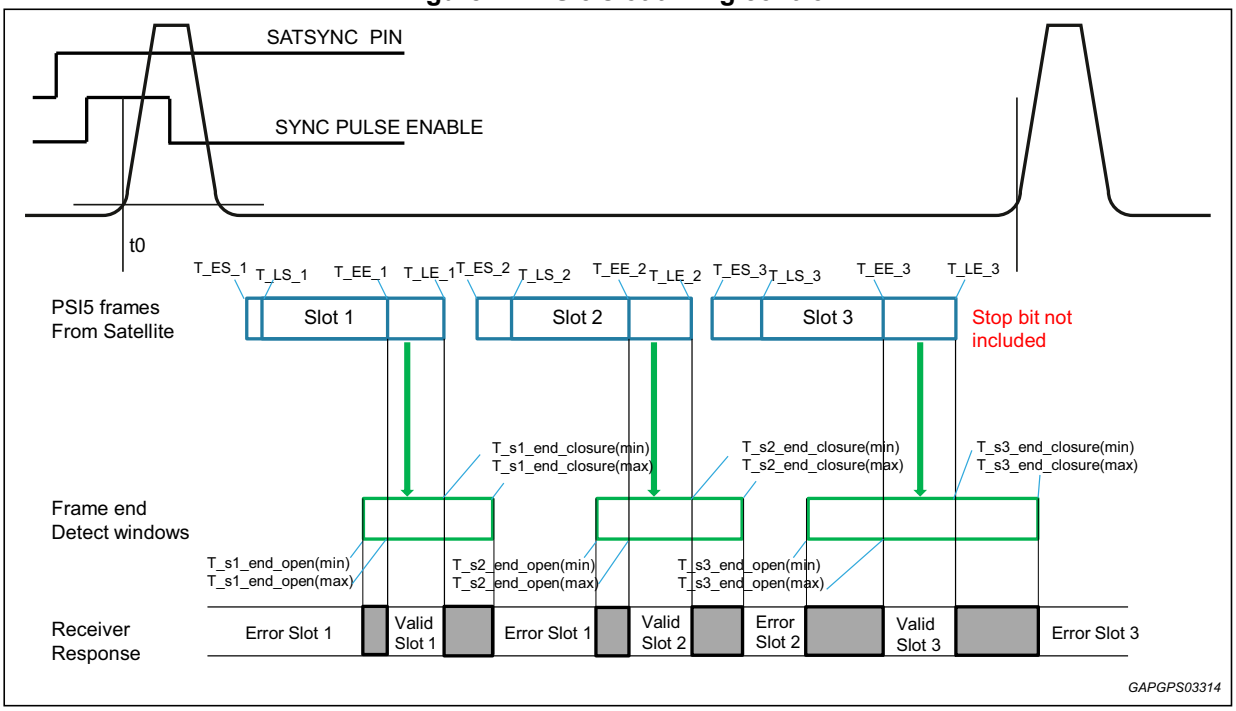
To allow for sampling synchronization of remote sensor data with the software in the microcontroller, the Remote sensor Interface block includes sync-pulse circuitry to signal initiation of sampling in the remote sensor. The sync-pulse is output to the remote sensors in the form of an increased voltage level on the RSUx pins when sampling is to be conducted. The higher voltage level required for the sync-pulse is sourced from the SYNCBOOST boost regulator. Pulse shaping is used to limit the slew rate of the pulses to reduce EMI. Feedback protection is provided to prevent fault conditions on one channel from affecting the others during sync-pulse generation. The microcontroller schedules the activation of the sync pulses to the four channels by providing a periodic signal to the SATSYNC pin. When a rising edge is detected on SATSYNC pin, the Remote sensor Interface block outputs sync pulses on channels RSU0-RSU1 in sequence to reduce the average current inrush to the remote sensors as shown in *Figure 41*. The voltage source in the Remote Sensor Interface block can source and sink current and is used to discharge the bus capacitance at the end of the sync pulse. The pull down device used to sink current is current limited.

Figure 41. Remote sensor synchronization pulses



L9679P supports three time slots in a sync period with associated RSDRx registers. The messages received within one sync period are routed to the corresponding RSDRx register associated to each time slot. A time slot control is performed to check if the incoming messages fall within the valid time slots reported in *Table 62* and sketched in *Figure 42* If the end of the received message occurs after the end of the checked outside a valid time slot, a SLOT_ERROR fault will be detected and stored in the related RSDRx register. Slot error assignment is described in *Figure 42*. For instance, if the end of second message falls before expected valid time window the error slot 1 is asserted and then also the data received with the first message is lost. If two messages end within the same slot, the second message will be assigned to that slot, regardless its validity. The time slot control can be disabled by setting the TSxDIS bit in the RSCRx register.

Figure 42. PSI5 slot timing control



The remote sensor interface is also able to detect faults occurring on the sensor interface. The Remote Sensor Data Register (RSDRx) will report multiple fault flags.

When the number of bits decoded is incorrect (either too many or too few), a bit error is indicated. When any bit error is detected (bit time, too many bits, too few bits), the decoder will revert to the minimum bit time of the selected range and the message is discarded.

Error bit INVALID is an OR-ed combination of the following errors:

- Start bit error outside of selected operating range
- Data length error or stop bit error
- Parity Error of received Remote sensor Message
- Bit time error (a data bit edge is not received inside the expected time window)

All fault bit related to channel error are loaded in the 3 time slot register and the fault has the priority, so the fault overwrite valid data.

9.1.2 Sensor data integrity: LCID and CRC

Each RSDRx data register contains a Logical Channel ID which is a 4/2-bit field for remote sensors used to link the received data to the corresponding logical channel number. Each RSDRx register contains also a CRC bit field computed on the data packet for data integrity check. To satisfy functional safety requirements LCID, DATA and CRC bit fields propagate through the same data path as a single item to the SPI output.

The polynomial calculation implemented for PSI5 data is described as in PSI5 specification g(x)=1+x+x^3 with initialization value equal to ‘111’.

Below are the equations to calculate the CRC in combinatorial way.

CRC[2] = CRCext[0]+D[0]+D[1]+D[3]+D[6]+D[7]+D[8]+D[10]+D[13]+D[14]+D[15]

CRC[1] = CRCext[2]+D[0]+D[1]+D[2]+D[4]+D[7]+D[8]+D[9]+D[11]+D[14]+D[15]+D[16]

CRC[0] = CRCext[1]+CRCext[0]+D[0]+D[2]+D[5]+D[6]+D[7]+D[9]+D[12]+D[13]+D[14]+D[16]

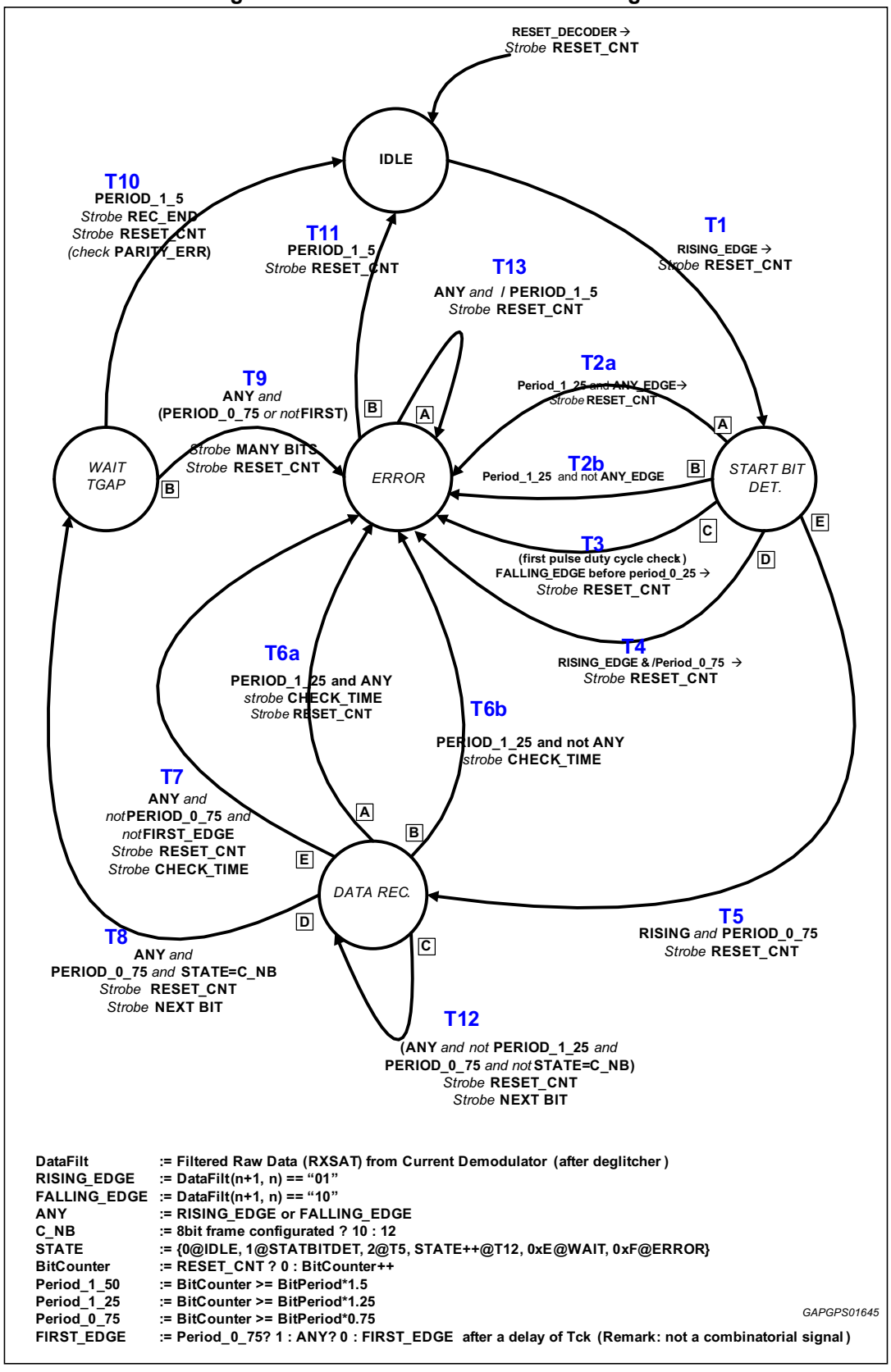
Where D[16:0]= RSDR[16:0] and CRCext[n] are the starting seed values (all '1').

9.1.3 Detailed description

Manchester decoding

The Manchester decoder will support remote sensor communication as per PSI specification rev 1.3 for the modes configurable via the STS bits in the RSCRx registers. The Manchester Decoder checks the duty-cycle and period of the start bits to determine their validity, depending on the configuration of the PERIOD_MEAS_DISABLE bit in the RSCRx registers. The expected time windows for the mid bit transitions of each subsequent bit within the received frame are determined by means of the internal oscillator time base. Glitches shorter than 25% of the minimum bit time duration are rejected.

Figure 43. Manchester decoder state diagram



DataFilt := Filtered Raw Data (RXSAT) from Current Demodulator (after deglitcher)
RISING_EDGE := DataFilt(n+1, n) == "01"
FALLING_EDGE := DataFilt(n+1, n) == "10"
ANY := RISING_EDGE or FALLING_EDGE
C_NB := 8bit frame configurated ? 10 : 12
STATE := {0@IDLE, 1@STATBITDET, 2@T5, STATE++@T12, 0xE@WAIT, 0xF@ERROR}
BitCounter := RESET_CNT ? 0 : BitCounter++
Period_1_50 := BitCounter >= BitPeriod*1.5
Period_1_25 := BitCounter >= BitPeriod*1.25
Period_0_75 := BitCounter >= BitPeriod*0.75
FIRST_EDGE := Period_0_75? 1 : ANY? 0 : FIRST_EDGE after a delay of Tck (Remark: not a combinatorial signal)

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A Manchester Decoder Error occurs if one or more of the following are true:

- Two valid start bits are detected, and at least one of the expected 13 mid-bit transitions are not detected
- Two valid start bits are detected, and more than 13 mid-bit transitions are detected
- When the number of bits decoded is incorrect (either too many or too few), a bit error is indicated. When any bit error is detected (bit time, too many bits, too few bits), the decoder will revert to the minimum bit time of the selected range and the message is discarded.

The Manchester decoder re-initializes at the start of each timeslot, such that remote sensor frames violating timeslot boundaries will result in the setting of a Manchester Error. All errors are readable through the Sensor Fault Status Register and the RSFLT bit in the Global Status Word Register.

When a valid message is correctly decoded, the 10/8 data bits are stored into the appropriate RSDRx register together with the related LCID. The RSDRx register contains the 10/8 bits data as they are received from the sensor (no data range check/mask is done at this stage). The 8-bit data word is right-justified inside the 10-bit data field in the RSDRx registers.

Current sensor w/ auto-adjust trip current

The current sensor is responsible for translating the current drawn by the sensor into a digital state. Each remote sensor channel has a dedicated current sensor.

The current flowing through the RSU power stage is internally downscaled by a factor 100, sent to a 10 bits A/D converter and digitally processed to extract both the sensor quiescent and delta currents.

The delta current threshold for signal detection can either be fixed or auto-adjusted to the actual calculated sensor delta current, depending on the FIX_THRESH bit setting in the RSCRx registers.

The current trip point is dynamically determined by adding the delta current threshold (fixed/auto-adjusted) to the quiescent current (auto-adjusted). The RSU current is compared against the current trip point to determine the current demodulator digital output. A logic '1' represents the sensor current above the current trip point. The current demodulator output is fed into the Manchester decoder and optionally to the WSx discrete output pins, depending on the configuration of the RSPTEN bit in the RSCRx registers.

Thanks to the quiescent and delta current tracking features the receiver is capable to automatically adapt to different nominal sensor currents and/or to be tolerant to sensor current drifts over lifetime.

Both the sensor quiescent and delta current tracking algorithms can be configured by setting appropriately the REDUCED_RANGE, BLOCK_CURR_IN_MSG and AVG/SSDIS bits in the RSCRx registers.

9.2 Test mode

In order test the input structures of the connected microcontroller, the L9679P features a wheel speed test mode that allows test patterns to be applied on the four wheel speed outputs WS0-WS1. The test mode can be entered via SPI and the test patterns can also be controlled via SPI commands. Test patterns can be composed only of static high or low signals, which can be selected via SPI. For failsafe reasons only one channel at a time can be switched into test mode.

9.3 Remote sensor interface fault protection

9.3.1 Short to ground, current limit

Each output is short circuit protected by an independent current limit. Should the output current level reach or exceed the ILIMTH for a time period greater than TILIMTH or the remote sensor interface the output stage is disabled. An internal up-down counter will count in 25 µs increment up to TILIMTH. The filter time is chosen in order to avoid false current limit detection for in-rush current that may happen at interface switch-on. When the output is turned off due to current limit, the appropriate fault code STG is set in the Remote Sensor Data Register (RSDR). The fault timer latch is cleared when the sensor channel is first disabled and then re-enabled through the Remote Sensor Control Register (RSCTRL). This fault condition does not interfere neither with the normal operation of the IC, nor with the operation of the other channels. When a sensor fault is detected, the RSFLT bit of the GSW is set indicating a fault occurred and can be decoded by addressing the RSDR register.

In order to fulfill the blanking time requirement at channel activation as per PSI-5 specification, a dedicated masking time is applied to the current limitation fault detection each time a channel is activated.

9.3.2 Short to battery

All outputs are independently protected against a short to battery condition. Short to battery protection disconnects the channel from its supply rail to guarantee that no adverse condition occurs within the IC. The short-to-battery detection circuit has input offset voltage (10mV, minimum) to prevent disconnecting of the output under an open circuit condition. A short to battery is detected when the output RSUx pin voltage increases above SATBUCK or SYNCBOOST (depending on operation) supply pin voltage for a T_{STBTH} time. An internal up-counter will count in 1.5 µs increment up to T_{STBTH}. The counter will be cleared if the short condition is not present for at least 1.5 µs. The channel in short to battery is not shut down by this condition. Other channels are not affected in case of short of one output pin. As in the case previously described, the STB fault code can be read from RSDR bits and any fault will set the RSFLT bit of the global status word register (GSW). The STB bit is cleared upon read or upon channel disabled via SPI RSCTRL register.

9.3.3 Cross link

The device provides also the capability of a cross link check between outputs, in order to reveal conditions where two output channels are in short. This functionality is allowed by enabling one output channel, while asking for voltage measurement on any of the other ones.

9.3.4 Leakage to battery, sensor open

The sensor interface offers also open sensor detection. The auto-adjusting counter for remote sensor current sensing will drop to 0 in case the current flowing through RSUx pin is lower than 2.5 mA typ. The OPENDET fault flag is asserted when the fault condition lasts for longer than TRSUOP_FILT deglitch filter time. This fault flag can be read from RSDR bits and any fault will set the RSFLT bit of the global status word register (GSW). The channel in this condition is not shutdown. This fault bit is cleared upon read or upon channel disabled via SPI RSCTRL register.

9.3.5 Leakage to ground

The sensor interface offers as well the detection of a leakage to ground condition, which will possibly raise the sensor current higher than 42 mA/12 mA typ in PSI5/WSS modes respectively. The CURRENT_HI fault flag is asserted when the fault condition lasts for longer than T_{RSUCH_FILT} deglitch filter time. This fault flag can be read from RSDR bits and any fault will set the RSFLT bit of the global status word register (GSW). The channel in this condition is not shutdown. This fault bit is cleared upon read or upon channel disabled via SPI RSCTRL register.

9.3.6 Thermal shutdown

Each output is protected by an independent over-temperature detection circuit should the remote sensor interface thermal protection be triggered the output stage is disabled and a corresponding thermal fault is latched and reported through the RSTEMP flag in the Remote Sensor Data Register (RSDRx). The thermal fault flag is cleared when the sensor channel is first disabled and then re-enabled through the Remote Sensor Configuration Register (RSCRx).

10 Watchdog timers

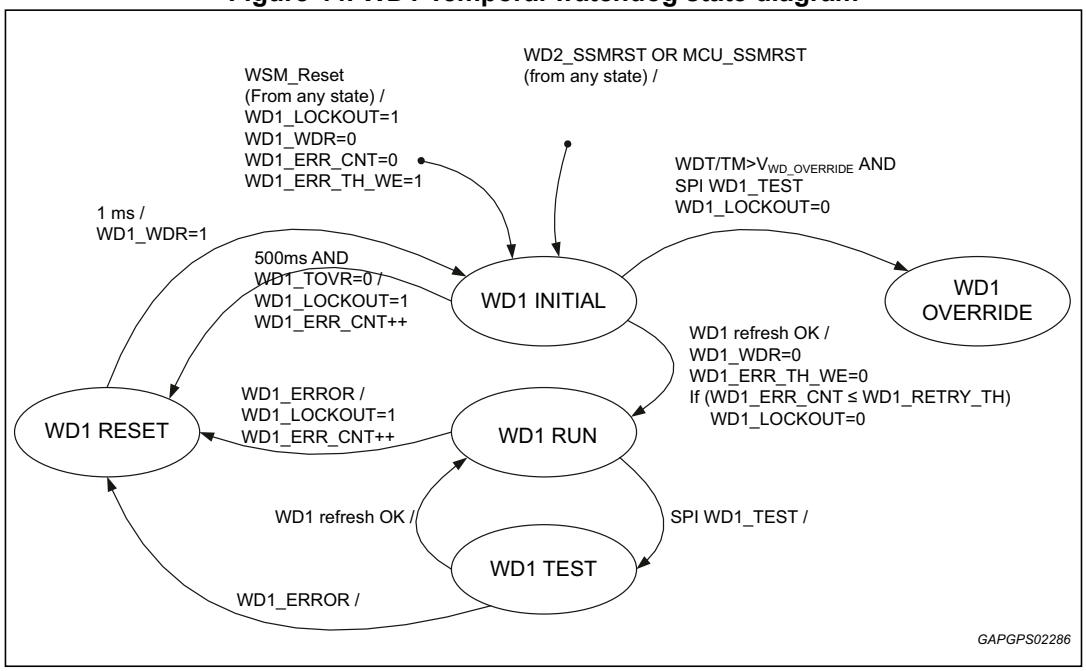
This device offers a 2-level watchdog control approach. The first control level is given by means of a temporal watchdog (WD1). The WD1 window times are SPI programmable and a couple of specific codes have to be written within this window in order to serve the WD1 control. The second control level is featured by an algorithmic seed/key watchdog (WD2). Unlike the temporal watchdog, the algorithmic watchdog service must be maintained before a timeout occurs, i.e. there is no restriction on refreshing the watchdog too early. Both WD1 and WD2 watchdog functionalities can be tested trough the WD_TEST SPI command.

10.1 Temporal watchdog (WD1)

The temporal watchdog ensures the system software is operating correctly by requiring periodic service from the microcontroller at a programmable rate. This service (watchdog refresh) must occur within a time window, and if serviced too early or too late will enter an error state reported via the FLTSR register (WD1_WDR bit).

The overall WD1 functionality is described in the state diagram reported in *Figure 44*.

Figure 44. WD1 Temporal watchdog state diagram



Following the description of the WD1 states and signals (most of them reported in related SPI registers)

Table 13. Watchdog timer status description

State/Signal	Description
WD1 INITIAL	Default state entered from startup. While in this state, no watchdog service is required, and the IC may stay in this state indefinitely. For system safety, all arming signals are disabled during this state to prevent deployment.
WD1 RUN	Normal run time state where WD1 service is required.
WD1 TEST	A special state used to test the watchdog function. Normally, this state will only be checked once per power cycle by the software, but there is no inherent restriction in the watchdog logic preventing periodic testing. This state allows testing of the watchdog without setting WD1_LOCKOUT=1, which can only be cleared via WSM reset. Deployment is inhibited when the WD state machine is in this state.
WD1 RESET	State entered when a WD1_ERROR occurs. This is a timed-duration state that is automatically exited after 1ms.
WD1 OVERRIDE	A special state used to disable watchdog functionality for development purposes. Other logic within the IC can use this state to emulate the WD1 RUN state without the need to service WD1.
WSM_RESET	Signal used to reset the WD1 state machine to the WD1 INITIAL state and all signals to their inactive values
WD1_refresh OK	Signal that is asserted only if the watchdog is refreshed ('A' - 'B' or 'B' - 'A' seq.) within the WD1 time window
WD1_ERROR	Signal that is asserted if the watchdog refresh fails to occur during the WD1 time window.
WD1_WDR	Watchdog Reset – latched signal that is activated whenever a watchdog error is qualified. For WD1, this occurs when WD1 service is required, but not received. This signal is SPI-readable.
WD1_TM	Test Mode – a signal that indicates that WD1 is being tested. This signal is SPI-readable.
WD1_LOCKOUT	A latched signal activated if an unexpected WD1 error occurs. This signal is permanently latched when set (until WSM_RESET). When set, all arming signals are disabled, preventing deployment. This signal is SPI-readable.
SPI_WD1_TEST	SPI command used to enter WD1 TEST state from WD1 RUN state, or to enter WD1 OVERRIDE state from INITIAL state if WDT/TM pin voltage is greater than the threshold. This command has no effect in other states.

10.1.1 Watchdog timer configuration

The watchdog timer can be configured on two different frequency modes:

- Fast watchdog with maximum range of 2ms and a resolution of 8 µs;
- Slow watchdog with maximum range of 16.3ms and a resolution of 64 µs.

The watchdog window times are SPI programmable. The configuration of watchdog timer frequency and window times can be done by setting the Watchdog Timer Configuration Register (WDTCR) with the appropriate values. However, this configuration is accepted only when the device is in the Init operating state, as shown in *Figure 10*. As soon as the device enters in Diag state, the watchdog control is enabled and the watchdog configuration is fixed and cannot be changed anymore.

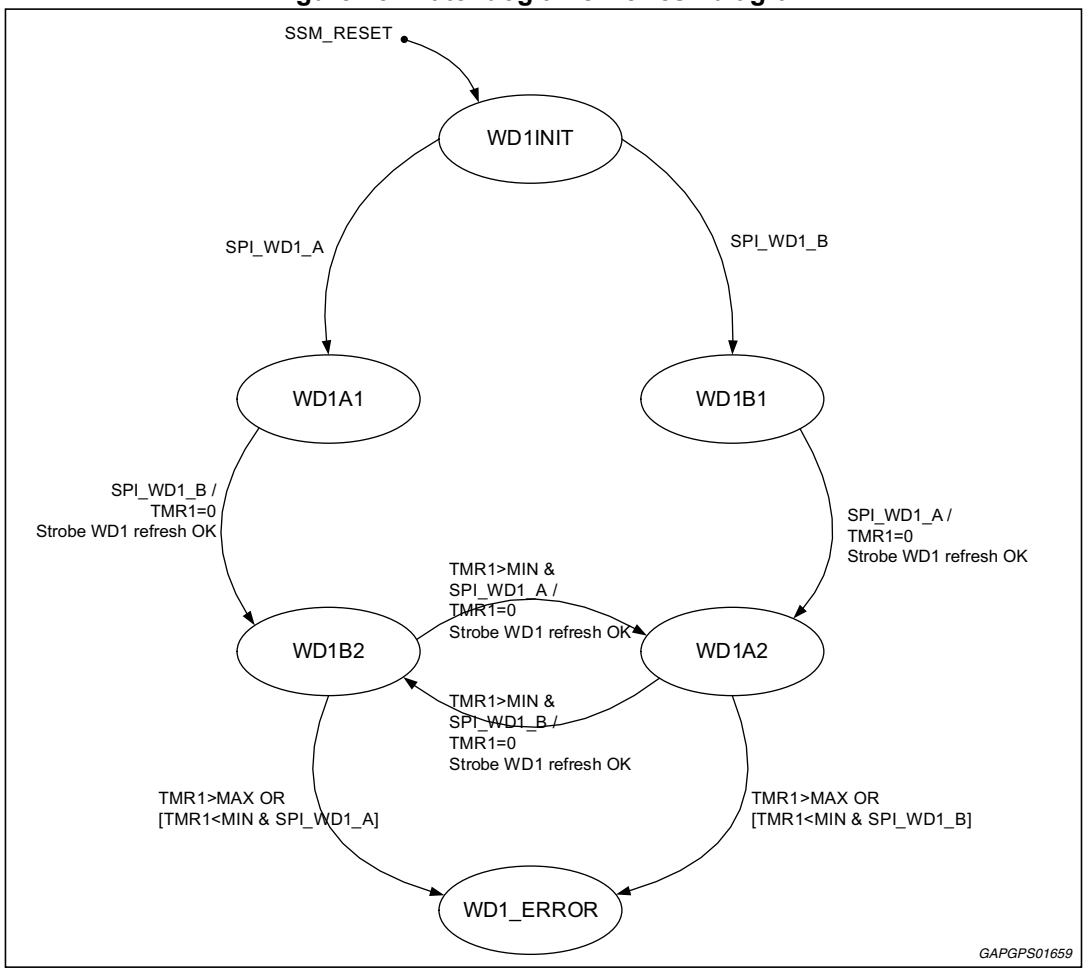
10.1.2 Watchdog timer operation

While in the WD1_INITIAL state, watchdog service must begin or a SPI command with WD1_TO_DIS=1 must be received within the first 500 ms. If the WD1 Timeout Disable bit is set, the device can stay in the WD1_INITIAL state indefinitely without watchdog service.

To refresh WD1, the logic must receive a Watchdog Timer Register (WD1T) SPI command containing the expected key value within the WD1 time window (WDTMIN+WDTDELTA). If it is received too early, too late the WD1_ERROR signal will be asserted. The WD1_ERROR will not be asserted in case a SPI command containing the Watchdog Timer Register (WD1T) with an incorrect key value is received at any time relative to the window. This allows the system software to repeatedly transmit the key value until it needs to change to the correct key value. Upon reception of the correct key within the window, the logic will reset the watchdog timer to create a new window.

The timer is cleared upon writing code 'A' and code 'B' (either in 'A' - 'B' or 'B' - 'A' sequences) to the WD1CTL [1:0] bits, in the WD1T register. The watchdog timer value can be read via the WD1T register.

Figure 45. Watchdog timer refresh diagram

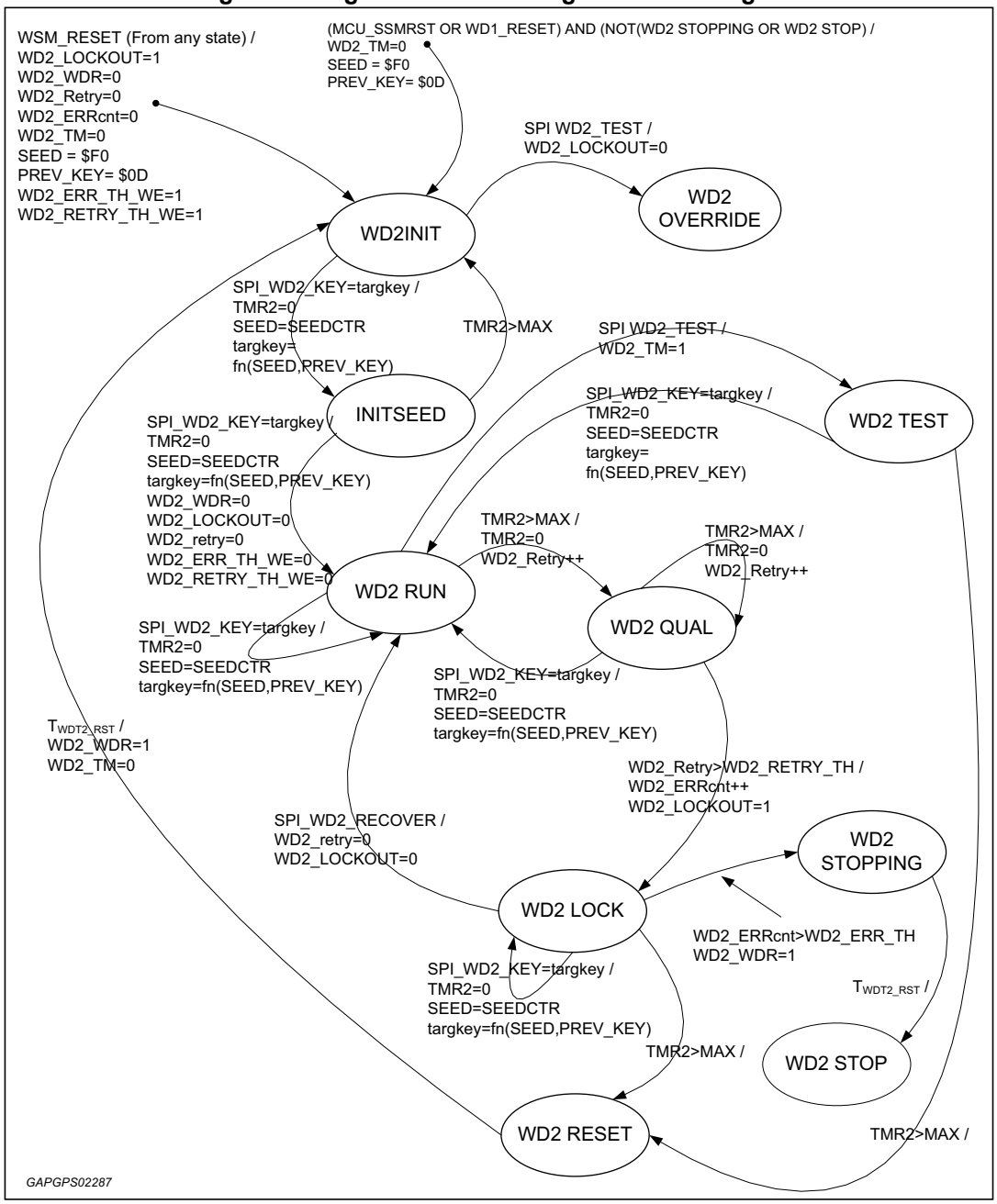


10.2 Algorithmic watchdog (WD2)

The algorithmic watchdog (WD2) is intended to protect higher software layers, and as such requires servicing at a much slower rate and allows for software jitter as compared with WD1. Additionally, WD2 is not implemented as a window watchdog, but is a maximum-time watchdog, where refresh is accepted at any time before the timer expires.

The overall WD2 functionality is described in the following state diagram:

Figure 46. Algorithmic watchdog timer flow diagram



Following the description of the WD2 states and signals (most of them available through SPI registers)

Table 14. WD2 states and signals

State / Signal	Description
WD2 INIT	Default state entered from startup or after a SSM reset (if not in WD2 STOP state).
WD2 OVERRIDE	Special state used to disable WD2 watchdog functionality.
WD2 INITSEED	State entered when the correct default key is received in INIT state. Here the timer starts to count waiting for the real first key.
WD2 RUN	Normal run-time state where WD2 service is required.
WD2 TEST	A special state used to test the watchdog function. Normally, this state will only be checked once per power cycle by the software, but there is no inherent restriction in the watchdog logic preventing periodic testing. This state allows testing of the watchdog without affecting WD2 error (no reset is generated, WD2_LOCKOUT stay low). Only WD2_WDR latch could be set to 1, in this way µC is able to verify the functionality of the watchdog.
WD2 QUAL	A state used to qualify a number of WD2_ERROR occurrences before action is taken. The intent is to use this state to permit a retry strategy to account for software jitter.
WD2 LOCK	A state entered after the allowed retries have been exhausted. This is where action is taken due to WD2 service failure.
WD2 STOPPING	This is a timed-duration state that is automatically exited after 1ms
WD2 STOP	A state used to prevent continual recovery of WD2 errors using the WD2_KEY key mechanism to restart watchdog service.
WD2 RESET	State entered when a WD2_ERROR occurs after having been qualified in the WD2_QUAL state (when all retries are exhausted), or when testing the WD2. This is a timed-duration state that is automatically exited after 1ms.
WSM_RESET	Watchdog State Machine reset – used to force a transition to the WD2 INIT state and reset all signals to their inactive states
WD2_RETRY	Counter that tracks the number of retry attempts. It is incremented each time the logic detects a WD2 error while qualifying the error.
WD2_WDR	Watchdog Reset – latched signal that is activated whenever a watchdog error is qualified. For WD2, this occurs when WD2 service not received after all retry attempts have previously failed. This signal is SPI-readable.
WD2_TM	Test Mode – a signal that indicates that WD2 is being tested. This signal is SPI-readable.
WD2_LOCKOUT	A latched signal that is activated on startup, or whenever a WD2 error is fully qualified (all retry attempts have failed). Recovery is still possible after this is set going into WD2 RUN state. This signal drives the WD2_LOCKOUT output pin. This signal is SPI-readable.
SPI_WD2_TEST	SPI command used to enter WD2_TEST state or to enter WD2 OVERRIDE state from INIT.
TMR2	Timer to count the maximum time limit to receive the correct key
SPI_WD2_RECOVER	SPI command used to clear retry counter
WD2_ERR_CNT	Counter that tracks the number of WD2 error occurred

To refresh WD2, the logic must receive a WD2_KEY command containing the expected key value before the WD2 timer expires. If it is received too late the refresh criteria have not been met. The WD2 error is asserted if the refresh does not occur before the end of the timeout. The WD2 error is not asserted if it receives continuously a WD2_KEY command with the correct key. This allows the system software to repeatedly transmit the correct key value at any rate faster than the required timeout.

Upon reception of the correct key, the logic will generate a new seed value, then calculate a new key using the new seed and reset the watchdog timer to create a new timeout.

When in WD2 INITSEED state, the three steps above are executed anyway. The seed is latched from a free-running counter that starts when WSM is released. The WD2_KEY command is used for transmission of the watchdog key, while WD2_SEED command is used to read the new seed and the previous key.

The SEED is generated by latching the value from a free-running counter. The free-running seed counter runs at a rate of f_{WD2_SEED} as specified in *Table 29*. The key value and seed value are 8-bits in length. The key shall be calculated as follows: (KEY = SEED ‡ PrevKEY + $01) where ‡ denotes a bit-wise XOR operation

10.3 Watchdog reset assertion timer

Upon either a WD1 or a WD2 watchdog reset, the watchdog logic will momentarily assert the RESET pin for time duration T_{WDT1_RST} / T_{WDT2_RST}. When the RESET pin has been asserted through the watchdog reset assertion timer, stored faults are maintained and can be read by the microcontroller via SPI following the RESET period.

10.4 Watchdog timer disable input (WDT/TM)

This input pin has a passive pull-down and is used to disable the watchdog timer. The state of this pin can be read by SPI through the WDT/TM_S bit in the GSW register. When WDT/TM pin is asserted, the watchdog timer is disabled, the timer is reset to its starting value and no faults are generated.

The WDT/TM input pin must not be biased HIGH (WDT/TM > V_{WDTDIS_TH}) prior to POR in order to have a proper start-up.

11 DC sensor interface

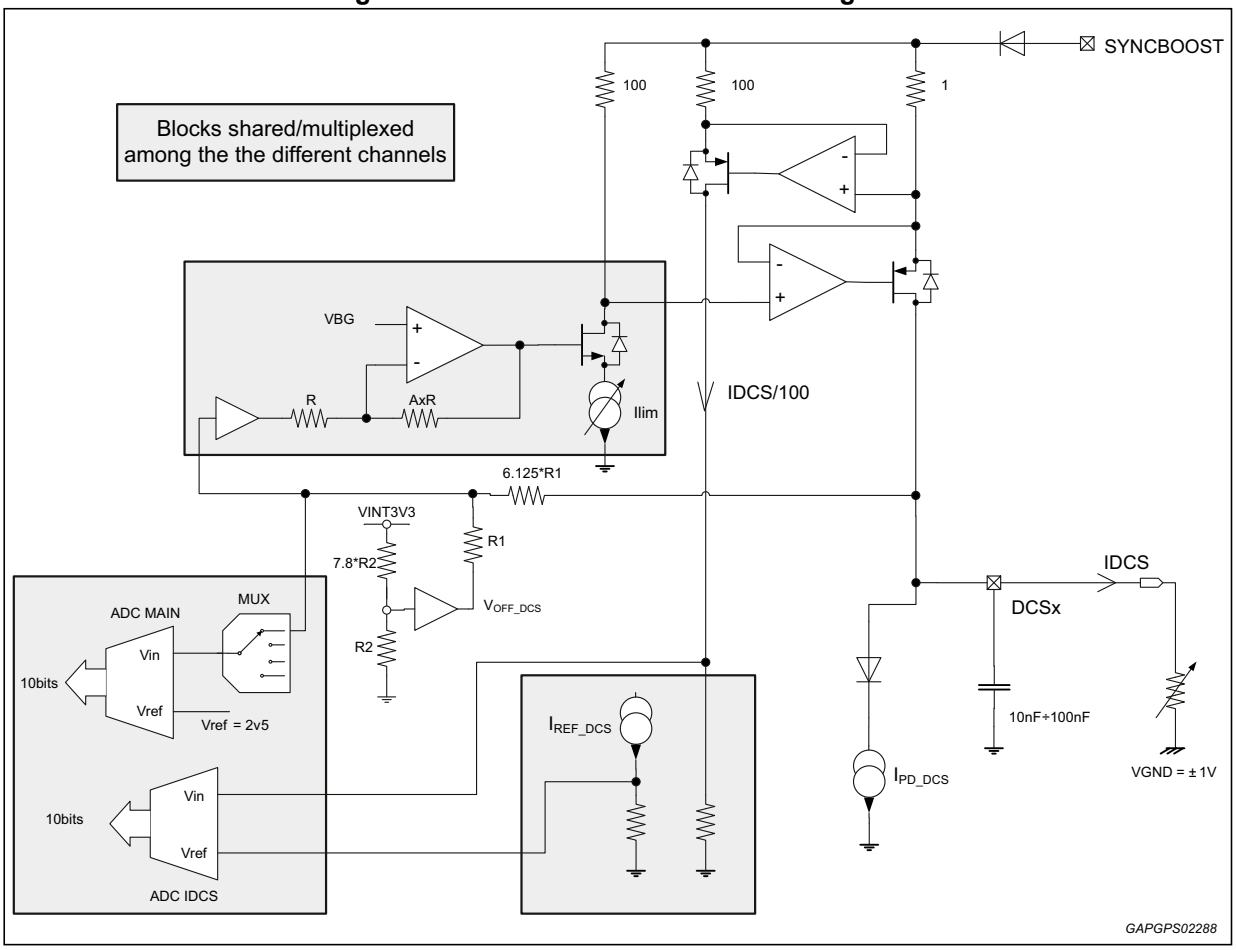
L9679P implements a circuitry able to interface with a variety of positioning sensors. The sensors that can be connected to the device are Hall-effect, resistive or simple switches.

Range of measurements is:

- Resistive sensor: 65 Ω to 3 kΩ
- Hall-effect sensor: 1 mA to 2 0 mA.

Within the above ranges, accuracy of ±15% is granted. A reduced accuracy is given in the range 1 mA to 2 mA. Hall sensor and switch interface block diagram is shown below.

Figure 47. DC sensor interface block diagram



The global SPI contains several bits to control and configure the interface. The SWOEN bit is used to enable the output voltage on DCSx pins. The channel to be activated can be chosen by accordingly setting CHID bits. The interface activation is started and switched off upon user SPI command. Alternatively it could be configured via the SYS_CFG(EN_AUTO_SWITCH_OFF) bit to automatically switch off as soon as the measurement is complete, in case of current or resistance measurements; this would help preventing thermal conditions. The interface would not auto-switched off in case of voltage measurement, instead.

The voltage and current for the selected channel are made available to the main ADC by selecting the proper channel and enabling the measurement process by dedicated DIAGCTRLx commands.

The device offers the capability to actively keep all the DCSx lines discharged by means of a weak pull down. The pull down is active by default on all channels and it is deactivated in either of the following cases:

1. when the voltage source is active on the relevant channel
2. when a voltage measurement is requested on the relevant channel
3. if SPI bit SWCTRL(DCS_PD_CURR) is set (global pull-down disable for all channels)

In case of Hall-effect sensors, a single current measurement is processed. The current load needed for regulating the pin is internally reflected to a reference resistance, whose voltage drop is then measured through the internal ADC converter.

When resistive or switch sensors are used, a more complex measurement is performed. In a first step the current information as above described is provided. Then, also the information on the voltage level achieved on the output pin is provided via ADC. By processing these two values, the micro-controller can understand the resistive value. The DCSx voltage is internally rescaled by a voltage divider into the ADC converter voltage range as shown in Figure 48. Additionally a positive voltage offset is internally applied to the scaled voltage in order to allow voltage measurement capability for DCSx down to -1V.

In order to get accurate resistive information even in case of an external ground voltage shift on the sensor of up to +/-1V, the voltage measurement step actually needs two DCSx voltage measurements. A first voltage measurement has to be done with selection of 6.25V on the output channel and a second one with the regulator switched off. The difference between the two measurements will cancel out the offsets (both external ground shift and internal offset).

The DCSx current and voltage can be retrieved from ADC readings according to the following formulas and related parameters specified in the Electrical Characteristics section.

$$I_{DCSx} = 100 \cdot \frac{I_{REF\_DCS}}{2^{ADC_{RES}}} \cdot DIAGCTRLn(ADCRESn) \quad @DIAGCTRL(ADCREQn = \$04$$

$$V_{DCSx} = RATIO_{VDCSx} \cdot \left(\frac{ADC_{REF\_hi}}{2^{ADC_{RES}}} \cdot DIAGCTRLn(ADCRESn) - V_{OFF\_DCSx} \right) -$$

$$- V_{OFF\_DCSx} \cdot (RATIO_{VDCSx} - 1) \; @DIAGCTRLn(ADCREQn) = \$03$$

The DCSx sensor resistance can be calculated according to the following formula:

$$R_{sensor_x} = \frac{\Delta V_{DCSx}}{I_{DCSx}} = \frac{V_{DCSx}@(SWCTRL(SWOEN)=1 - V_{DCSx}@(SWCTRL(SWOEN)=0}{I_{DCSx}}$$

@SWCTRL(CHID) = x

The device provides also the capability of a cross link check between outputs, in order to reveal conditions where two output channels are in short. This functionality is allowed by enabling one output channel, while asking for voltage measurement on any of the other ones.

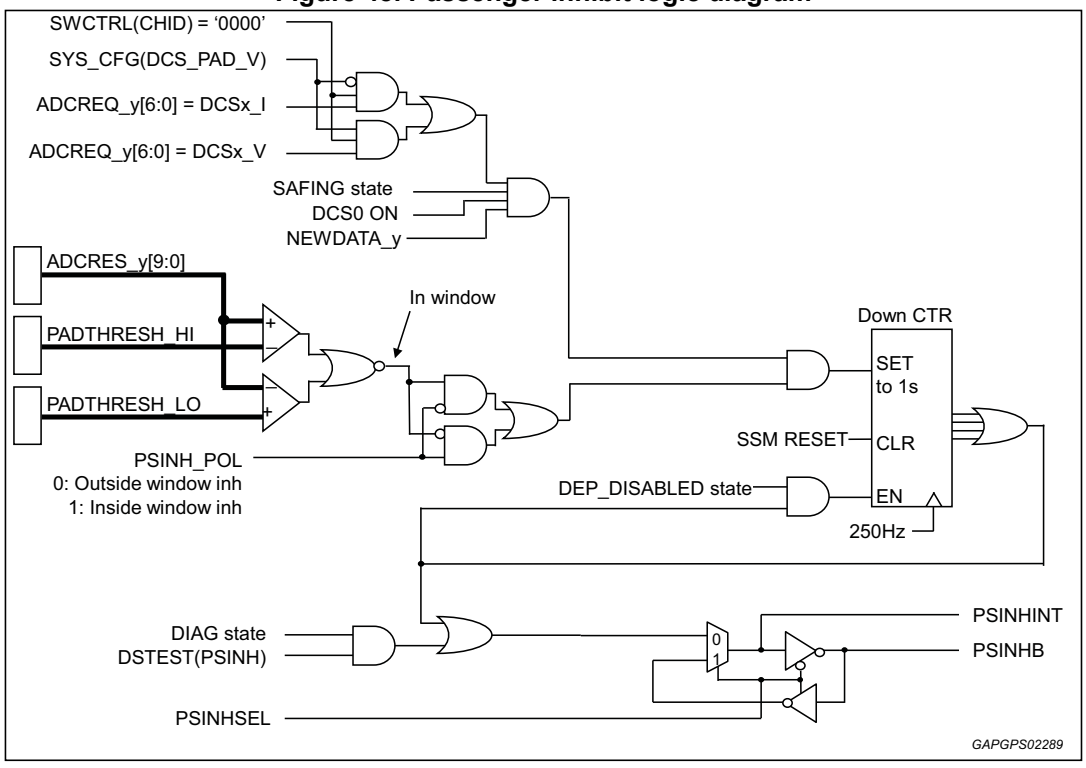
Each output is protected against

- Overload conditions by current limit
- Ground offset between the ECU and the loads of up to ±1 V.
- Loss of ECU battery
- Loss of ground
- Unpowered shorts to battery
- Shorts to ground

11.1 Passenger inhibit interface

L9679P provides a feature to deactivate passenger restraint devices based on a preprogrammed mask. It generates a signal (PSINHINT) based on microcontroller-initiated measurements performed on DC Sensor channel 0. The PSINHINT signal is bitwise AND-ed with the LOOP_MATRIX_PSINH mask register, allowing selective deactivation of squib loops independent of microcontroller control. This signal is also inverted and output on the PSINHB pin of the IC to activate externally controlled squib loops.

Figure 48. Passenger inhibit logic diagram



An upper and lower threshold is preprogrammed via SPI by writing the desired 10-bits values into the PADTHRESH_HI and PADTHRESH_LO registers during the Diag state. These thresholds define the measurement window where the passenger restraints are active. Any measurement outside this window will result in the assertion of the PSINHINT signal (as described below), thereby deactivating the squib loops identified in the PSINH mask. The PSINH mask is also preprogrammed during the Diag state.

Another control (DCS_PAD_V bit in SYS_CFG register) is preprogrammed to select either a voltage measurement or a current measurement on DCS0 for this purpose.

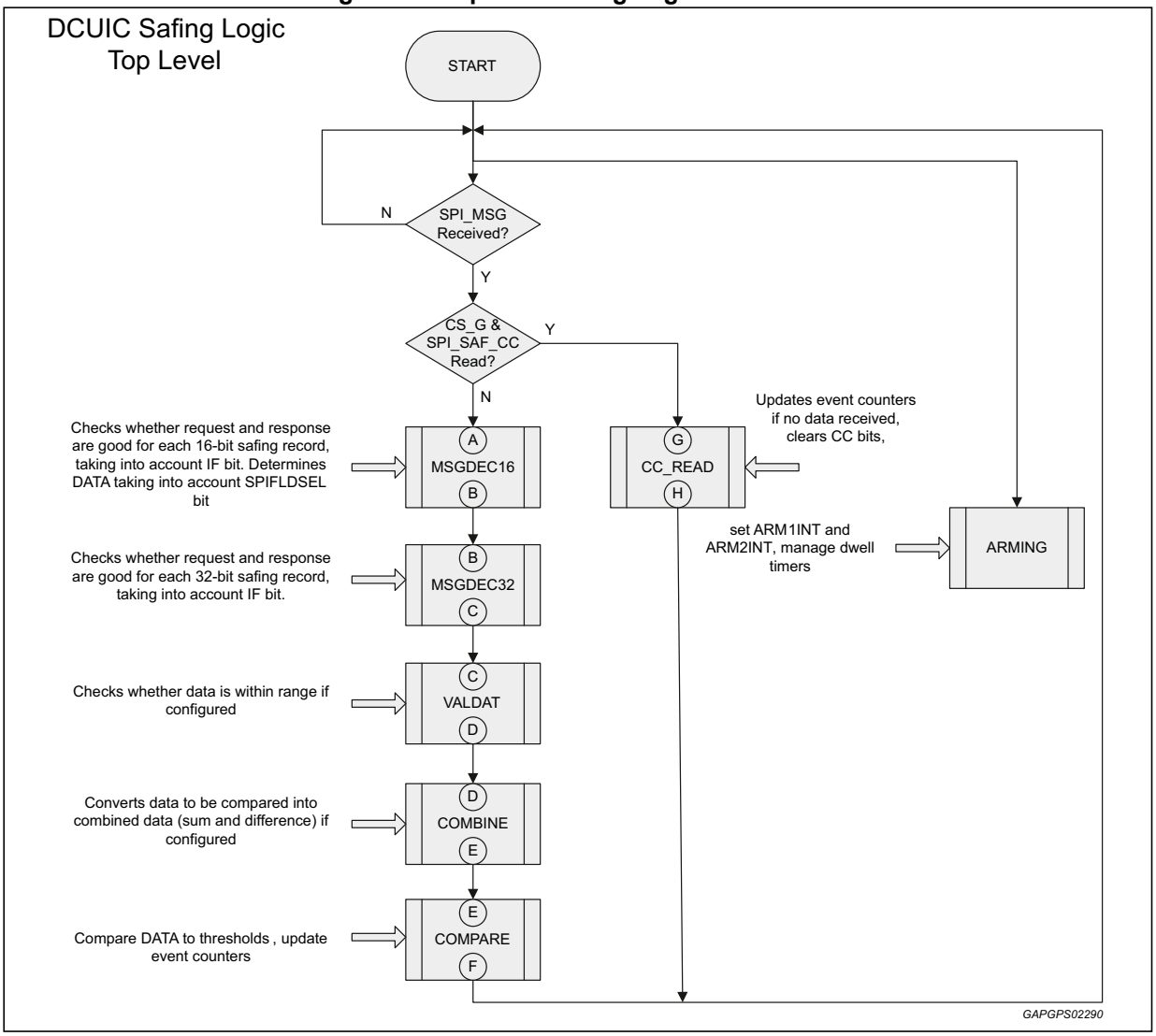
The automated control of the PSINHINT signal occurs when the microcontroller runs diagnostic testing of the DCS0 interface. A 1 second timer is included to ensure the diagnostic test is run periodically. When the timer expires (down-counts to 0), the PSINHINT signal is asserted. When the measurement of the DCS0 voltage or DCS current (as selected by the DCS_PAD_V bit) is taken, and the value falls within the preprogrammed window, the timer will be reloaded. If the measurement is outside the window, the timer will not be reloaded, and it will continue to count down until it expires, resulting in activation of PSINHINT. For testing purposes, the PSINHINT can be controlled directly via SPI while in DIAG state using the Diag State Test Selection (DSTEST) register.

12 Safing logic

12.1 Safing logic overview

The integrated safing logic uses data from on-board and remote locations by decoding the various SPI communications between the interfaces and the main microcontroller. The safing logic has several programmable features enabling its ability to decode SPI transmissions and can process data from up to 16 sensors. The operating mode involves simple symmetrical data threshold comparisons, with the use of symmetrical or asymmetrical counters. A high level diagram is shown in the figure below. Please note that this top-level diagram is simplified, and references more detailed flowcharts to show a) message decoding, b) valid data limits, c) effects of the 'combine' function, d) comparison to thresholds and arming, and e) the setting of the 'compare complete bit. Two independent arming outputs, ARM1INT and ARM2INT, are also mapped internally to any of the integrated squib drivers.

Figure 49. Top level safing engine flow chart



12.2 SPI sensor data decoding

Sensor data is regularly communicated with the main microcontroller through multiple SPI messages. The L9679P monitors SPI traffic on MISO_RS bus. Since not all communications between sensors and the microcontroller contain data, it is important for the decoder to properly sort the communications and extract only the targeted data. The solution involves defining specific masking functions, contained within independent safing records, programmed by the user. The following figures detail the SPI message decoding methodology and the ensuing comparisons of valid sensor data to the programmed thresholds.

Figure 50. Safing engine – 32-bit message decoding flow chart

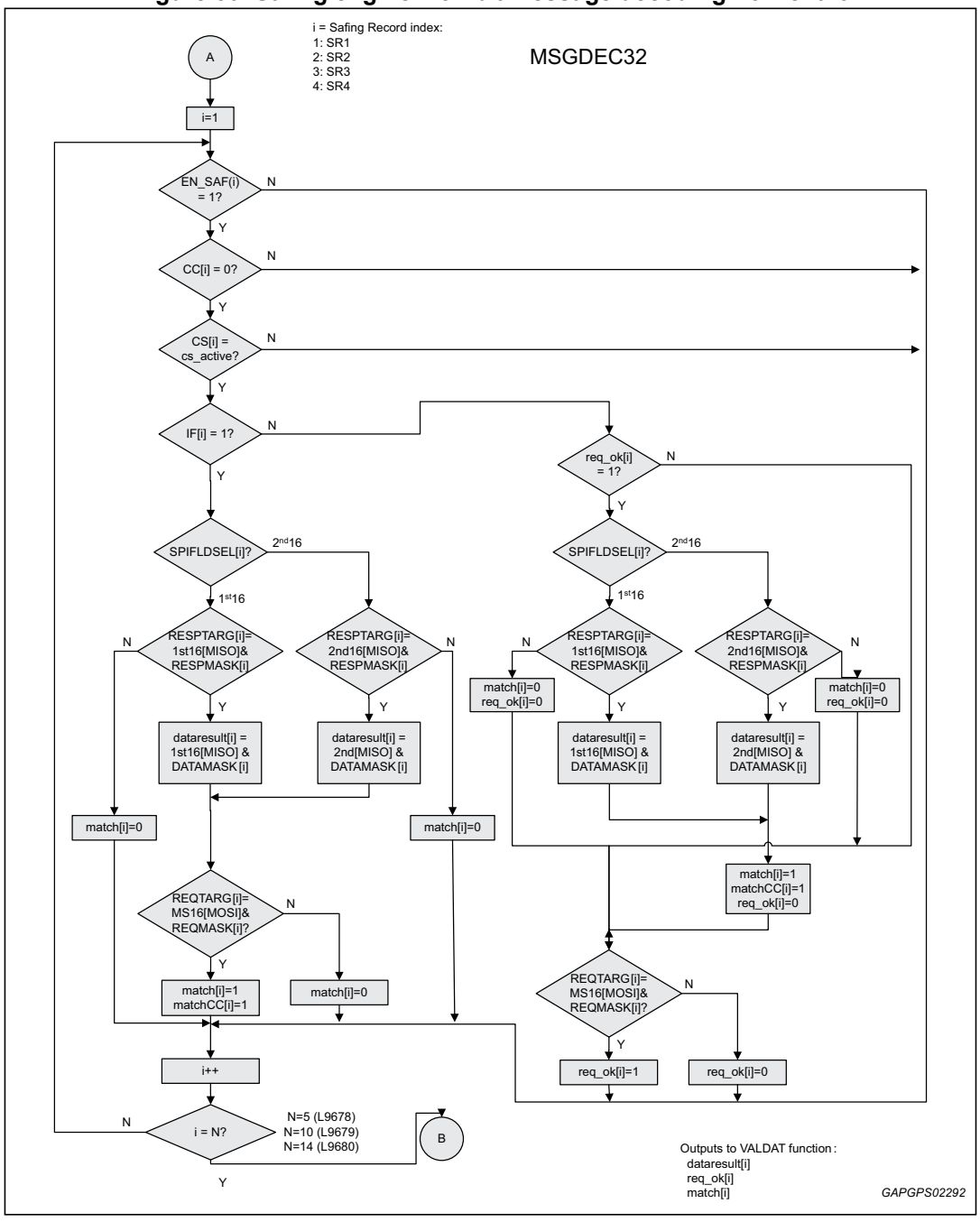


Figure 51. Safing engine – 16-bit Message decoding flow chart

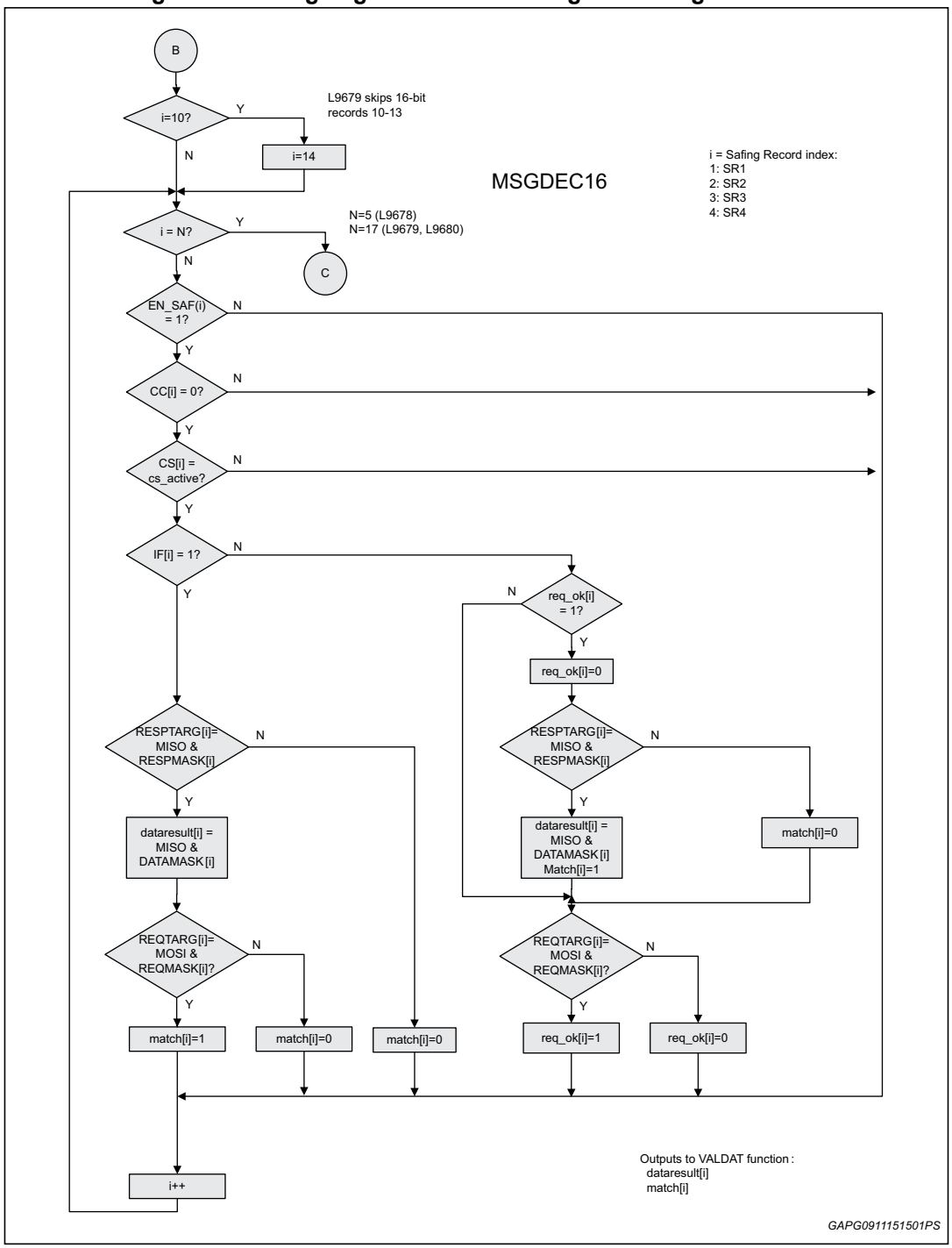


Figure 52. Safing engine - Validate data flow chart

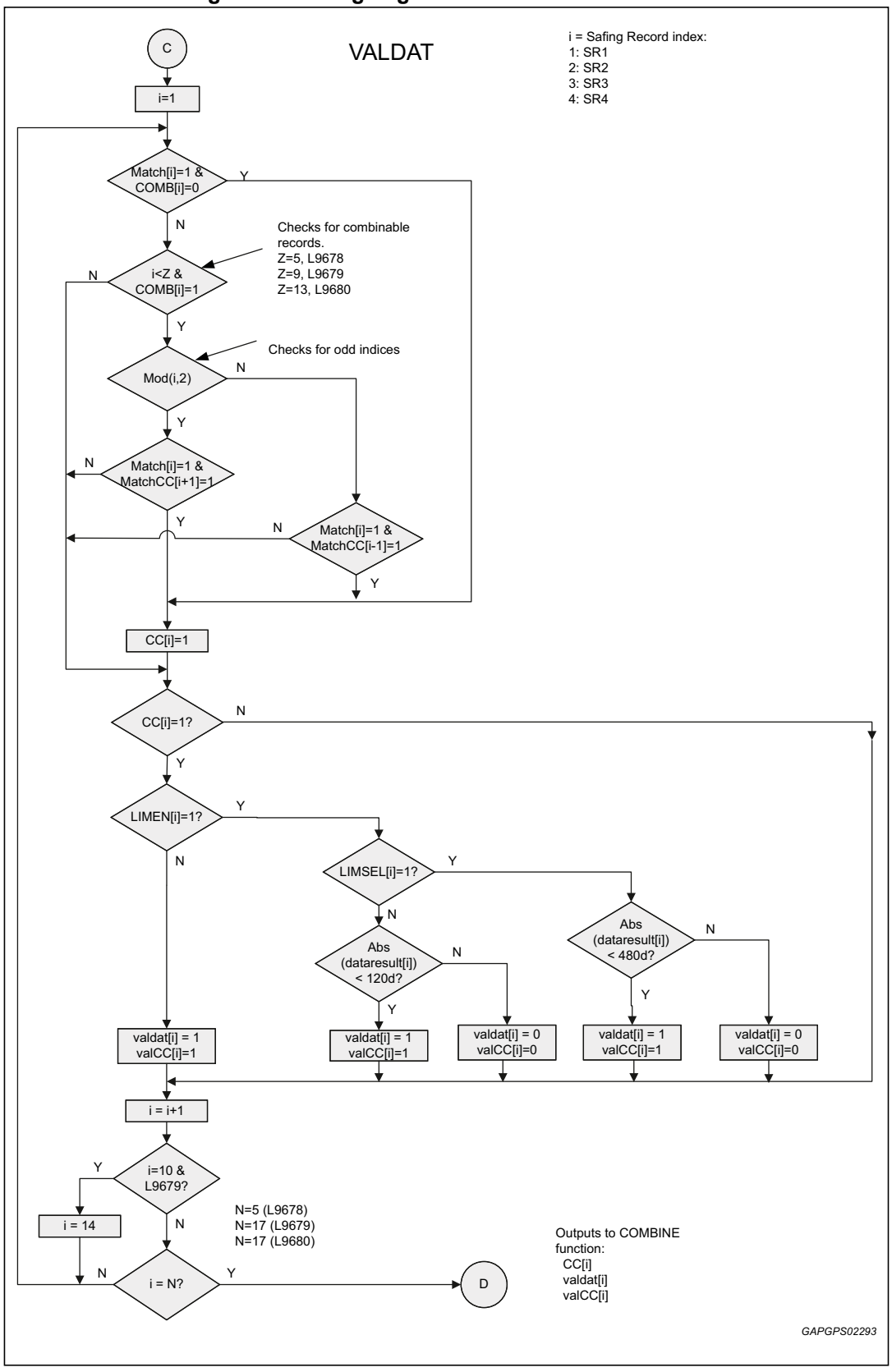


Figure 53. Safing engine - Combine function flow chart

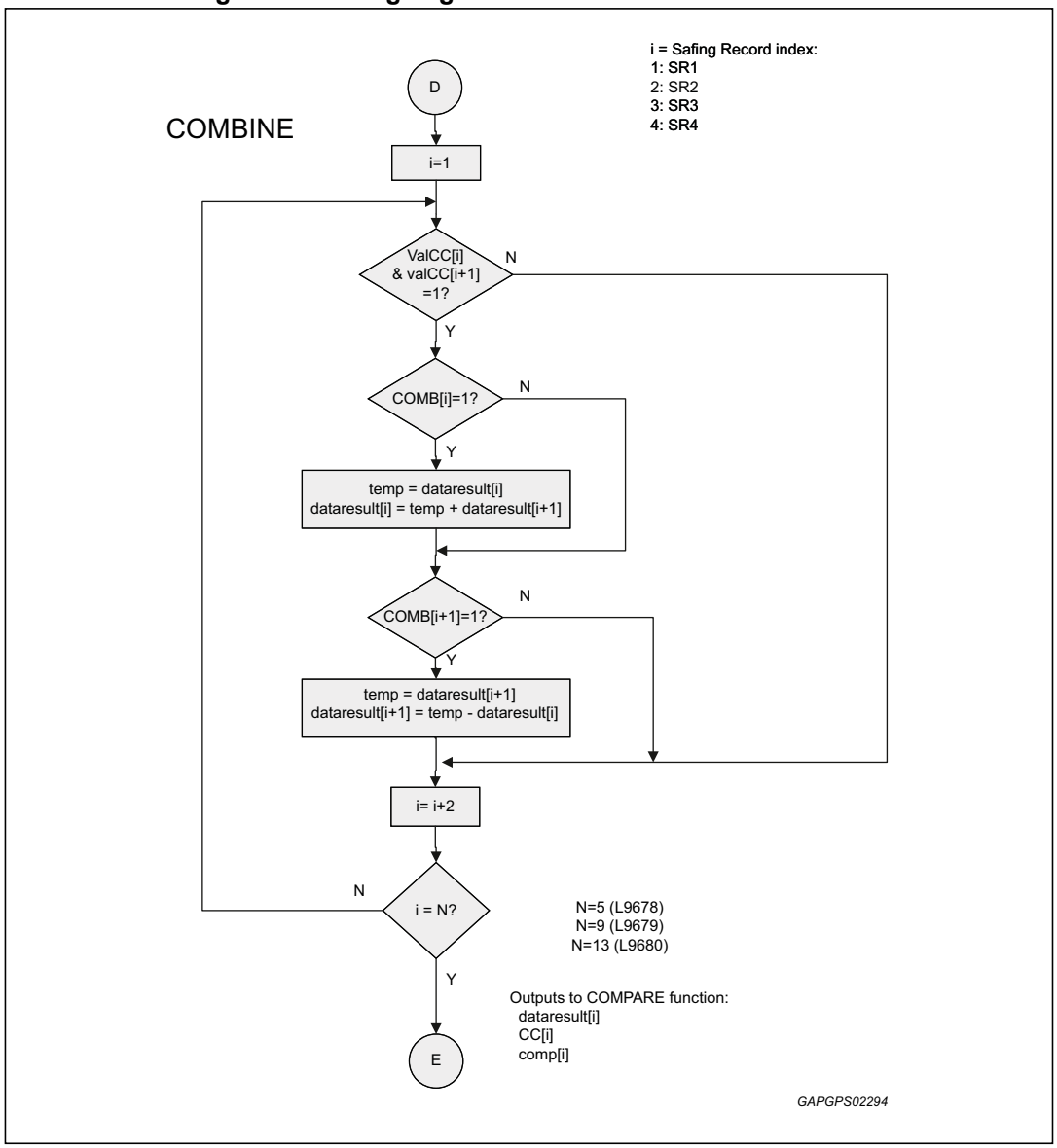


Figure 54. Safing engine threshold comparison

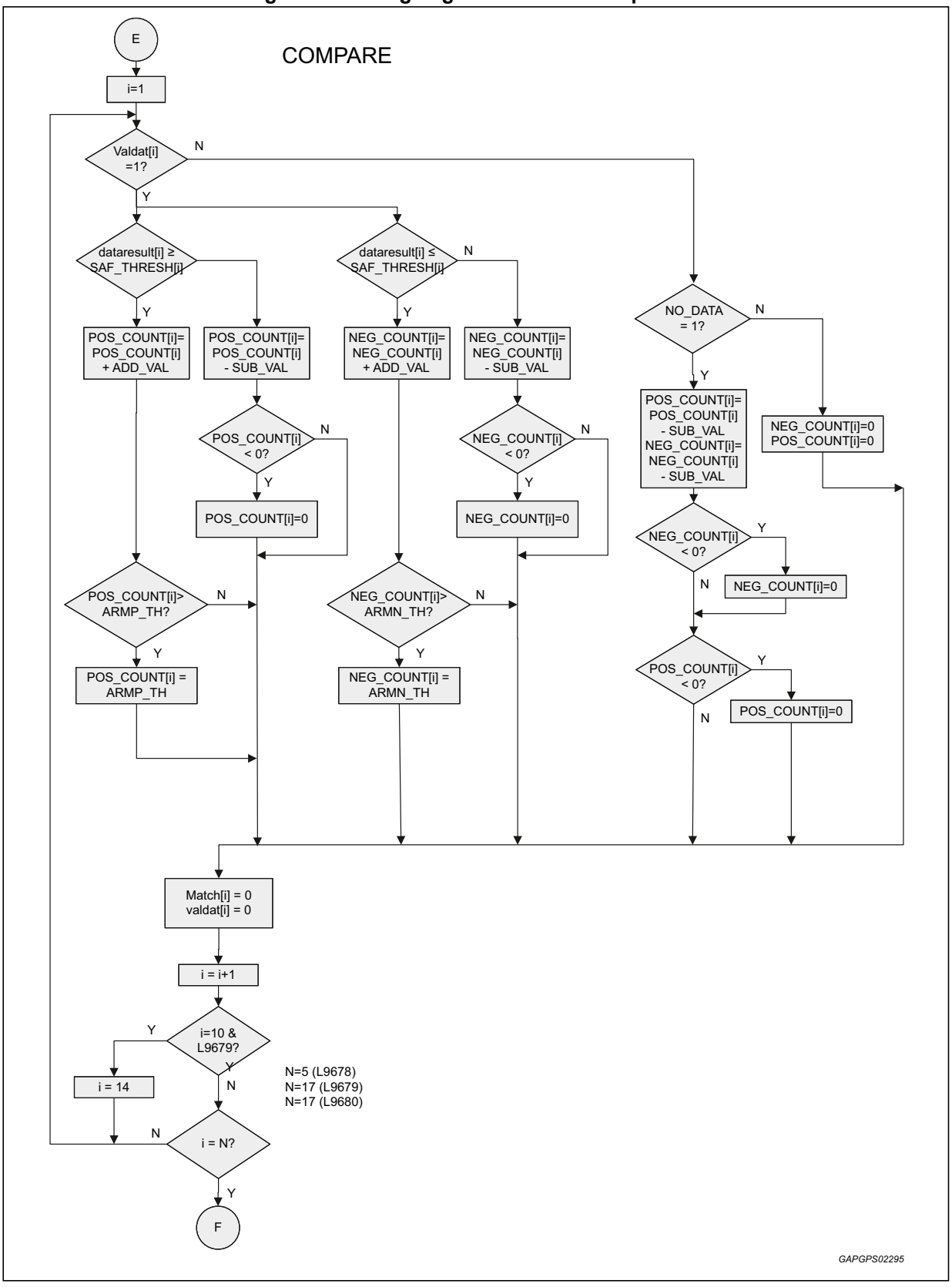
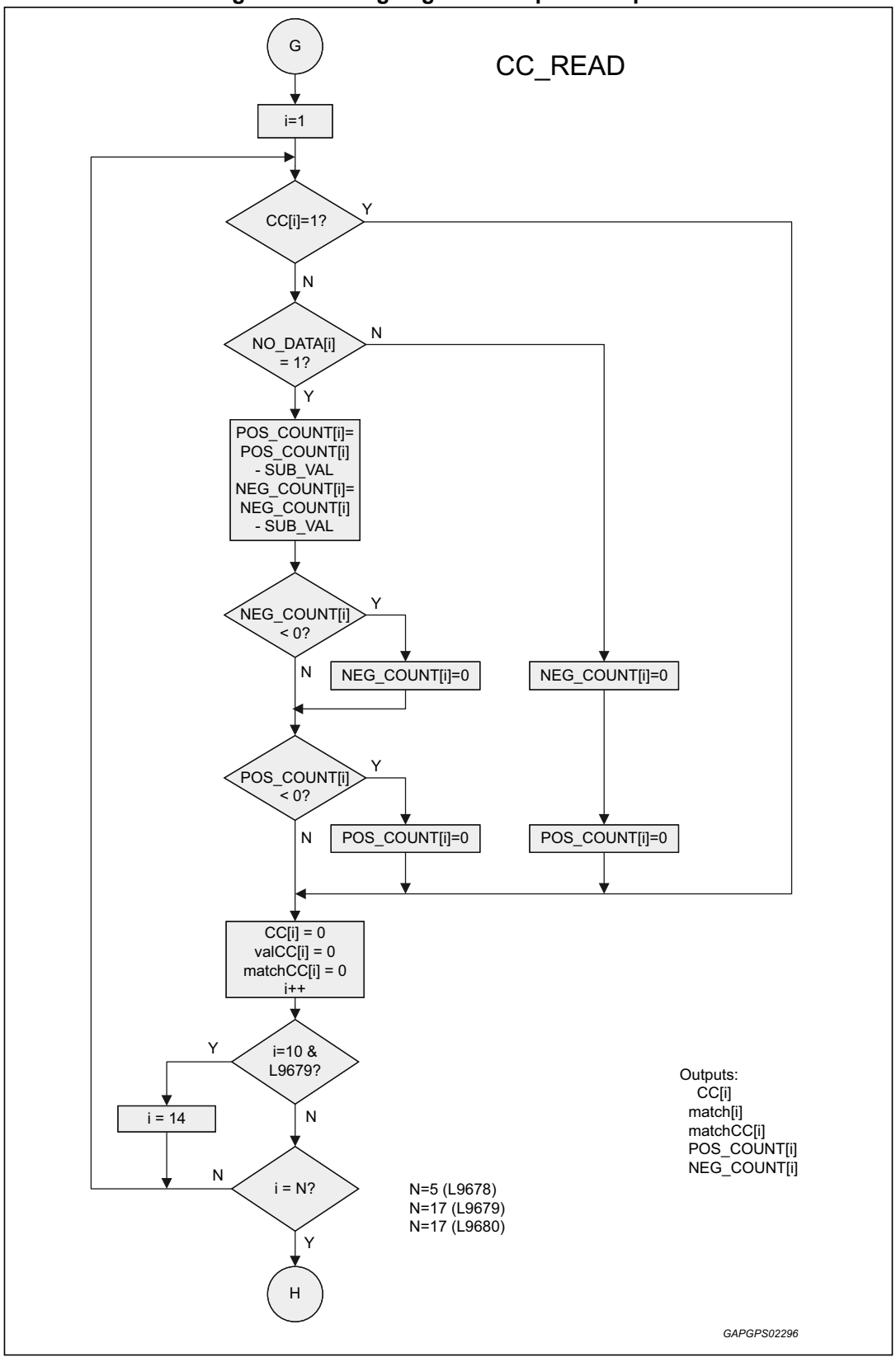


Figure 55. Safing engine - Compare complete



Each safing record has SPI accessible registers defined in the SPI command tables and summarized below:

- Request Mask and Request Target - to understand what sensor the microcontroller is addressing
- Response Mask and Response Target - to identify the sensor response
- Data Mask - to extract relevant sensor data from the response.
  - Sensor data is extracted as a bit-wise AND result of the SAF_DATA_MASKx and monitored RS_MISO data. The configuration of the set bits of the DATAMASK must be contiguous for both 16-bit and 32-bit records. The 32-bit records are comprised of Part1 as MSW and Part2 as LSW.
  - The extracted data is then right justified into a 16/32 bit register for 16/32 bit safing records, respectively, prior to further processing steps which assume data is signed should be "using two's complement representation".
- Safing Threshold - specific value that sets the comparator limit for successful arming
- Control:
  - IF, In Frame - to indicate serial data response is ‘in frame’. There are two types of potential serial data responses, ‘in frame’ and ‘out of frame’.
  - CS - to align safing record with a specific SPI CS. The device contains 5 SPI CS inputs for the safing function (CS_RS, SAF_CSx)
  - ARM - there are four internal arming signals, each active record is assigned or mapped to any arming signal. Several safing records can be mapped to a single arming output. ARMx outputs can be enabled also simultaneously.
  - Dwell - Once an arming condition is detected, the safing record remains armed for the specified dwell time.
  - Comb (Combined Data) - specific solution for dual axis high-g sensors specifically oriented off-axis.
  - LimEn (Limit Enable) - to enable PSI5 out-of-range control.
  - LimSel (Limit Select) - to select PSI5 out-of-range thresholds between 8-bit and 10-bit protocol.
  - SPIFLDSEL (SPI Field Select) - to determine which 16-bit field in long SPI messages (>31 bit) to use for response on MISO of SPI monitor. Don't care for messages less than 32 bits.

If input packet matches multiple safing records, the safing engine should process all of them and treat them independently.

Safing record can only be evaluated on the first matching input packet. Any further data packet matches are ignored (i.e. once CC is set, record can't be processed until CC is cleared)

The En (Record Enable) bit for any record is programmable as on or off at any time and will enable/disable the record itself upon the following SATSYNC.

All CC bits are available in one register (SAF_CC) for access in one single SPI read. After ARMing is achieved and CC is set, no further messages are considered until CC is cleared via read.

Safing Engine must not process sensor data in any state but Safing state (refer to *Figure 10*).

All safing records are cleared on SSM RESET.

Comb (Combined Data) bit allows combining X and Y for off-axis oriented sensors. In this case, it is typical for such orientations to add or subtract the sensor response to translate the sensor signal to an on-axis response. Only couples of 16-bit long records have this feature (i.e. 1&2, 3&4, 5&6, 7&8, 9&10, 11&12).

Records are added and subtracted and results compare against two thresholds. Safing engine will process data as follows:

- Use record(n) and record(n+1), where n = 1, 3, 5, 7, 9, 11.
- The matching inputs used for math combinations are processed only after both are captured.
- The sum of the two matching inputs will be compared to the threshold of record(n).
- The difference of the two records will be compared to the threshold of record(n+1).
- If the Comb feature was enabled on only one of the two records in a couple, math would be performed only on it as shown in *Figure 54*

Example of Combine Function operation:

Table 15. Example of combine function operation

Record #	Combine Bit	Data	Resulting value	Record Threshold	ARMSELx Configuration	ARMINTx Result
Record 1	0	12	12	48	ARMP	0
Record 2	0	50	50	48	ARMP	1
Record 3	0	50	12	48	ARMP	0
Record 4	1	12	50 – 12 = 38	48	ARMP	0
Record 5	1	12	12 + 50 = 62	48	ARMP	1
Record 6	0	50	50	48	ARMP	1
Record 7	1	50	12 + 50 = 62	48	ARMP	1
Record 8	1	12	50 – 12 = 38	48	ARMP	0
Record 9	1	12	50 + 12 = 62	-24	ARMN	0
Record 10	1	50	12 – 50 = -38	-24	ARMN	1

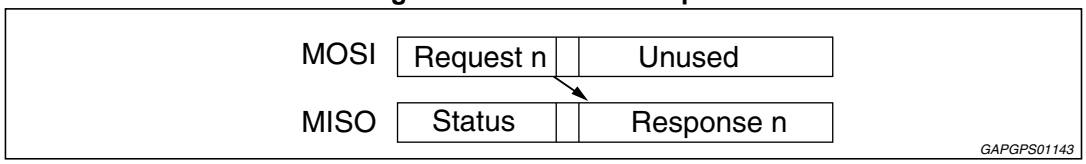
All items in the safing records, except En(Record Enable) bit, can be configured only in Diag state (refer to *Figure 10*). Additionally, the global bit to select internal or external safing engine is set in Init state.

12.3 In-frame and out-of-frame responses

Some sensors will communicate data within the current communication frame while others will send data on the next communication frame. Sometimes this is sensor specific and sometimes this is due to the amount of data to be transmitted. A simplified diagram shows the basic communication differences of in and out of frame responses.

In-frame example:

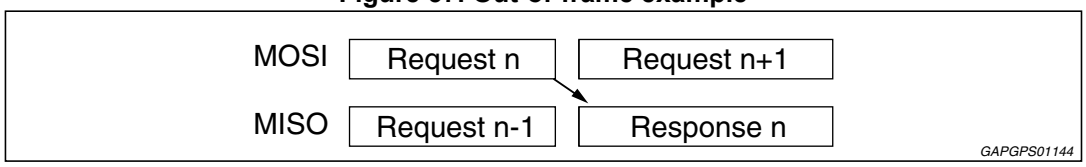
Figure 56. In-frame example



At least one bit needed to allow for synchronization between clock domains (SPI clock and system clock).

Out-of-frame example:

Figure 57. Out-of-frame example



Synchronization between clock domains relies upon inter-frame gap.

12.4 Safing state machine operation

State machine operation is disabled when the safing state machine reset signal is active as described in the power supply diagnostics and controls section of this document. The outputs of the state machine are ARMxREQ. As previously stated, there is a maximum of 16 safing records available to the state machine. Inputs to the safety state machine are programmed safing records and sensor data. The configuration of the state machine is common to all sensors.

12.4.1 Simple threshold comparison operation

In this mode, sensor data received through the sensor SPI interface and validated by the safing record is passed to the safing algorithm. The simple threshold comparison algorithm compares the received data to two thresholds, SAF_TH (positive threshold) and (-SAF_TH) (negative threshold). If the sensor data is greater than SAF_TH or is less than (-SAF_TH) then and event is flagged and the event counter is incremented based on the programmed value of ADD_VAL. If sensor data does not trigger the SAF_TH comparators, the counter is decremented by SUB_VAL. SUB_VAL is programmed by the user and can be same or different than ADD_VAL. This feature allows for an asymmetrical counter function making the system either more or less sensitive to sensor data. Since sensor data can indicate a positive or negative event, the algorithm maintains separate event counters, POS_COUNT and NEG_COUNT. ADD_VAL and SUB_VAL programmed values are the same for both event counters.

On each sensor sample, the event counters, POS_COUNT and NEG_COUNT, are updated based on the SAF_TH comparators. Likewise, each event counter is compared with a corresponding arming threshold. In this case, POS_COUNT value is compared to ARMP_TH and NEG_COUNT to ARMN_TH. ARMP_TH and ARMN_TH are programmable thresholds set by the user. The compared result will set ARMP and ARMN to either ‘1’ or ‘0’ depending on the comparison status. If ARMP_TH or ARMN_TH are set to 0, the arming will be activated immediately entering in safing state.

POS_COUNT and NEG_COUNT are not updated if microcontroller stops reading SAF_CC bits (this must be avoided otherwise ARMING set and reset will not be possible).

By way of the assignment of the ADD_VAL, SUB_VAL, ARMP_TH and ARMN_TH settings, the safing engine can be configured to assert arming for either a simple accumulation of COUNTs in a non-consecutive manner, or it could be set to require some number of consecutive samples.

12.5 Safing engine output logic (ARMxINT)

SPI messages are monitored and mapped to specific safing records. Each safing record is configured with its own threshold, dwell time and the appropriate ARMxINT signal to activate if safing criteria are met.

Any enabled safing record can be programmed to an arming signal. All safing records arming status is logically ‘OR'd’ to its programmed arming signal. For example, if safing records 1, 2, 4 are programmed to ARMINT1 and the records are enabled, any of the records can set the ARMINT1 signal. Configuration of safing record mapping to ARMxINT signals is specified in the in the SAF_CONTROL_x register (refer to *Table 65*).

While in Diag state, L9679P allows diagnostics of the squib driver HS and LS FETs, ARM pins, VSF output and firing timers. The ARM and VSF output tests are mutually exclusive.

For safety purposes, the safing logic circuitry is physically separated from the circuitry that contains the deployment logic.

Figure 58. Safing engine arming flow diagram

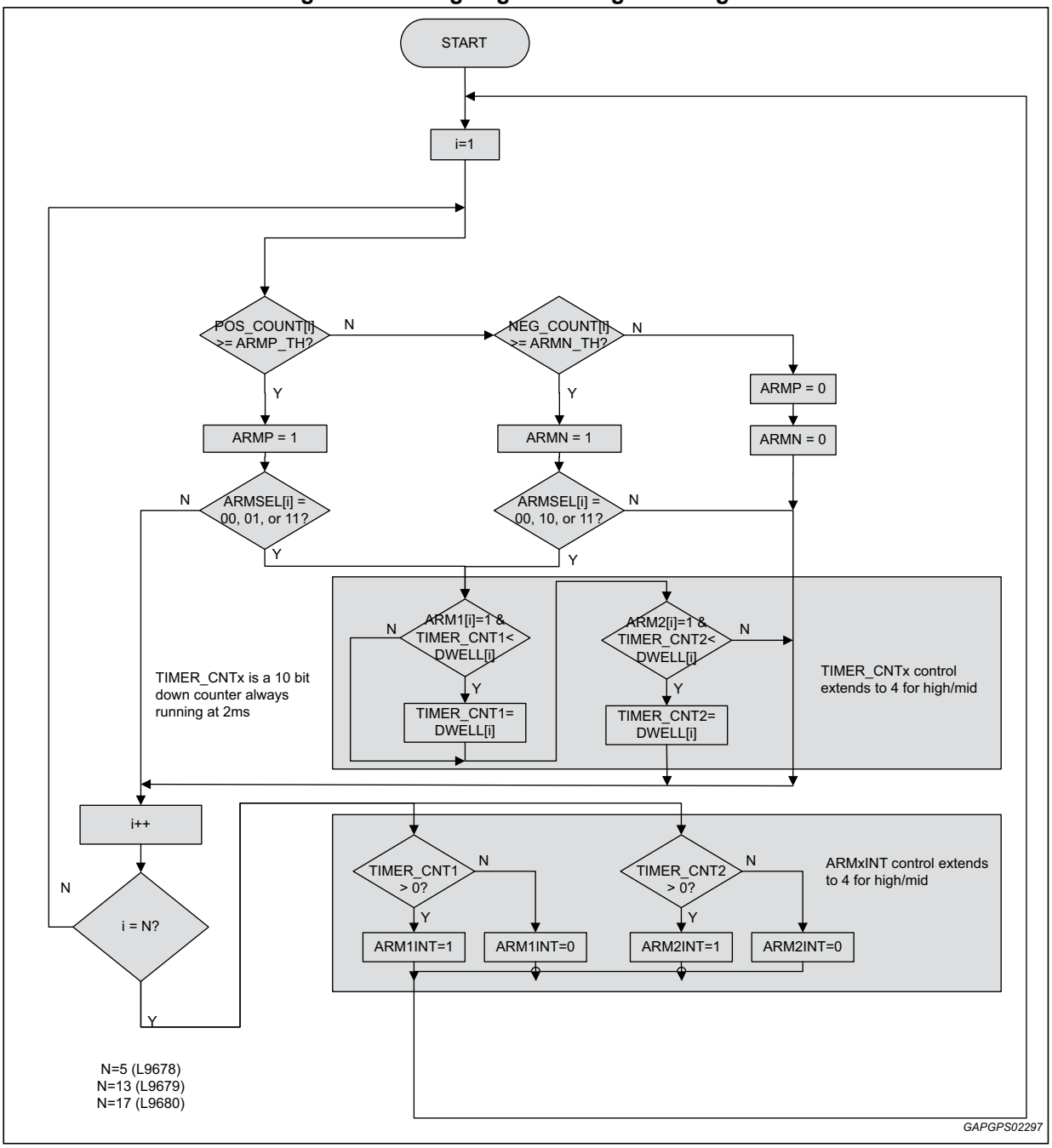
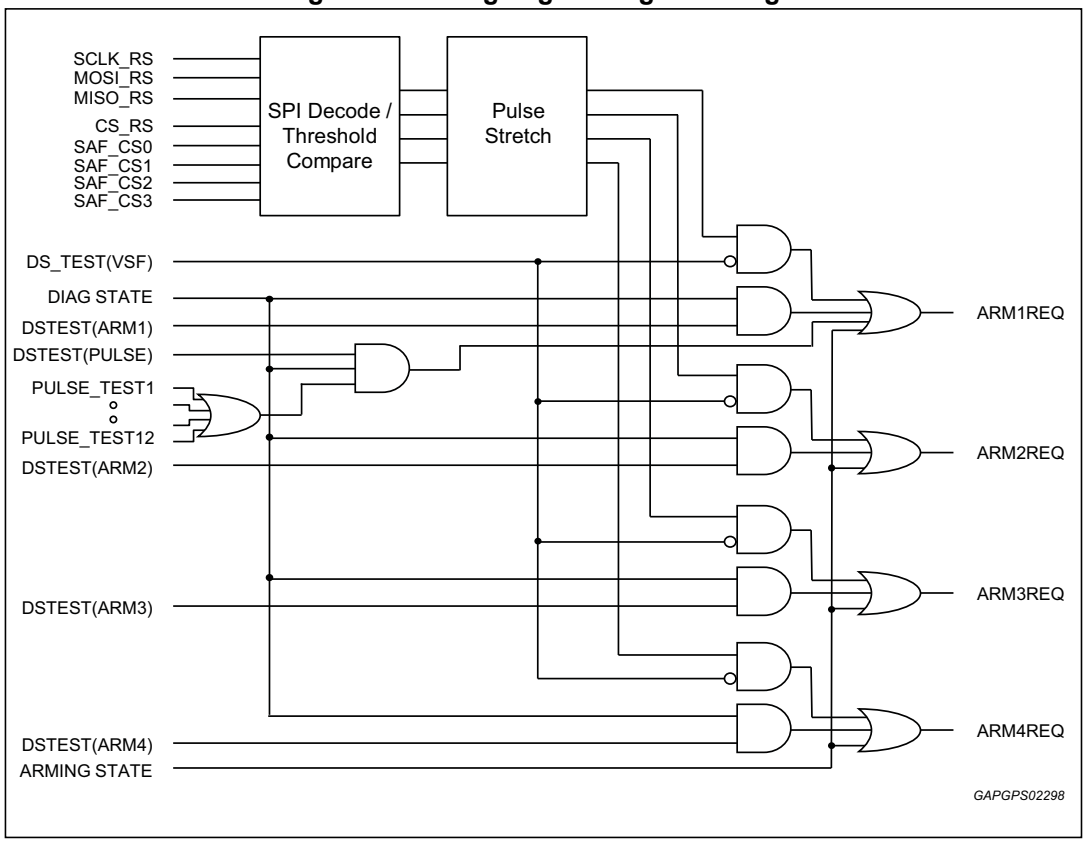


Figure 59. Safing engine diagnostic logic

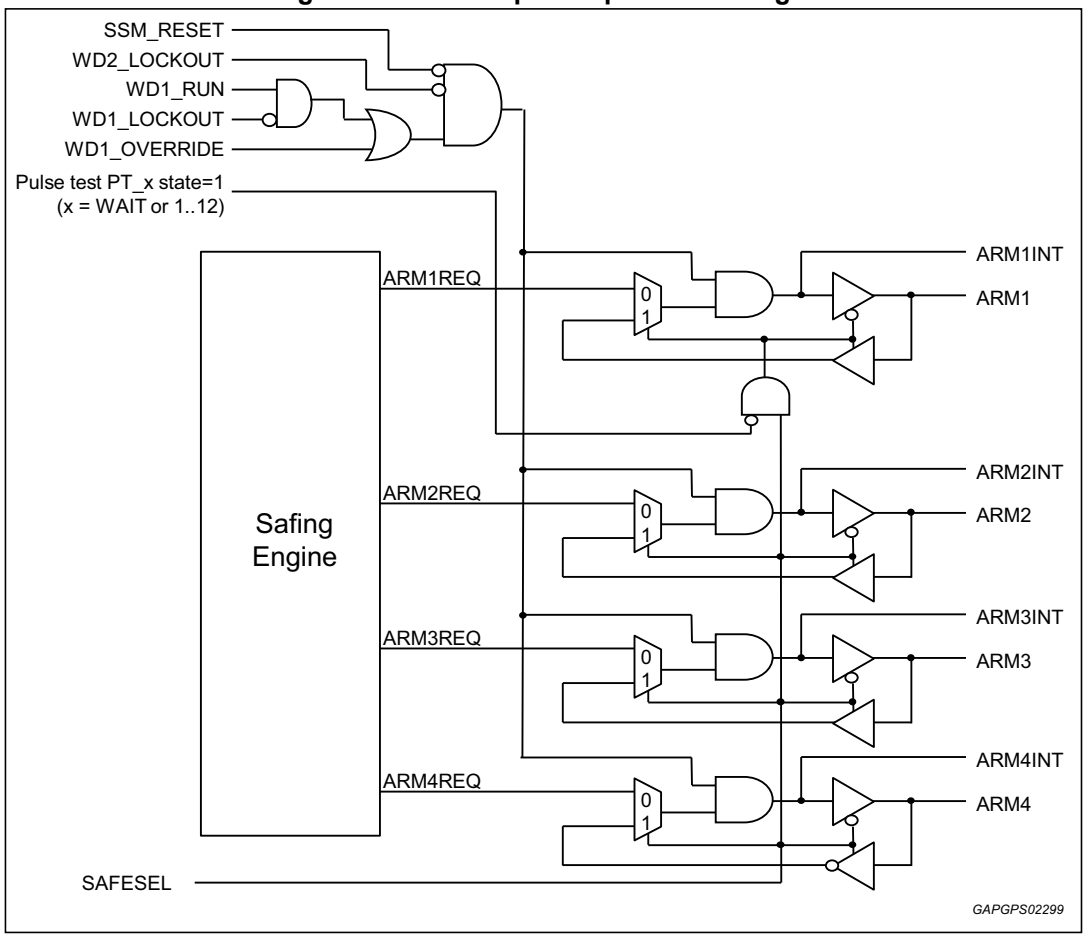


A configurable mask for each internal ARMxINT signal is available for all of the integrated deployment loops. The un-masked ARMxINT signal for each loop will enable the respective loop drivers.

Activation of VSF (regulation rail for High Side Safing FET) occurs upon ARMxINT. Actual High Side Safing FET activation still requires microcontroller signal.

L9679P is able to provide arming signals to external deployment loops by means of four discrete output ARMx pins.

Figure 60. ARMx input/output control logic



12.5.1 Arming pulse stretch

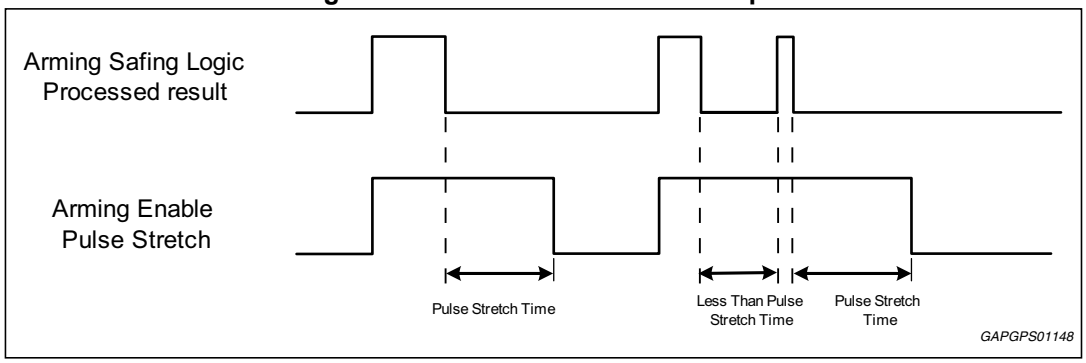
Upon a valid command processed by the safing logic, the Dwell bit to stretch the arming time assertion (dwell time) applies to each safing record and is used to help safe the deployment sequence to avoid undesired behaviour.

Once dwell time has started, it will continue, regardless of the En (Record Enable) bit. Dwell will be truncated in case of SSM reset. Dwell values in the safing records are transferred to the ARMx signals. A dedicated counter is designed for each ARMx output pin. If different dwell values are assigned to the same ARMx, the longer value is used. Dwell times can only be extended, not reduced. If the remaining dwell time is less than the new dwell extension setting, the new setting will be loaded into the dwell counter.

Dwell times are user programmable.

The behaviour of the pulse stretch timer is shown below.

Figure 61. Pulse stretch timer example



The Arming Enable Pulse Stretch Timer status is available in the AEPSTS register.

12.6 Additional communication line

The ACL pin is the Additional Communication Line input that provides a means of safely activating the arming outputs (ARMx and VSF) for disposal of restraints devices at the end of vehicle life.

The handshake sequence for activating the Arming outputs is illustrated in *Figure 62*. The strategy involves generation of a seed value from within the L9679P device using a free-running 8-bit counter running at f_{SCRAP_SEED} rate, where it can be read by the microcontroller. The microcontroller uses it to generate an 8-bit key value. When the seed value is read (SPI SCRAP_SEED command), L9679P also freezes the seed value and computes its own key, which is used for comparison to the key subsequently submitted by the microcontroller. The key value is submitted by the microcontroller using the SCRAP_KEY command, and successful reception of this command with a key value matching the internally calculated key allows the successful completion of the first handshake. After that, in case a second handshake (seed-key) completes successfully and if a valid ACL is detected (as described below) the L9679P transitions from Scrap state to Arming state. To remain in Arming state the microcontroller must periodically refresh L9679P with the SCRAP_KEY command containing the correct key value in the data field of the command, and L9679P must also receive the correct ACL signal. This must occur before the scrap timeout timer expires ($T_{SCRAP\_TIMEOUT}$). The scrap key is derived from the seed value using a simple logical inversion on the even-numbered bits (0, 2, 4, 6). From a logical standpoint, this is equivalent to a bit-wise XOR of the seed value with 0x55.

While the SSM is in Arming state, the arming outputs are asserted (ARMx=1, VSF on). If the periodic scrap key is incorrect, or not received before the timeout expires, or the ACL is not correctly received, the SSM reverts back to the Scrap state, and the arming outputs are deactivated.

Figure 62. Scrap SEED-KEY state diagram

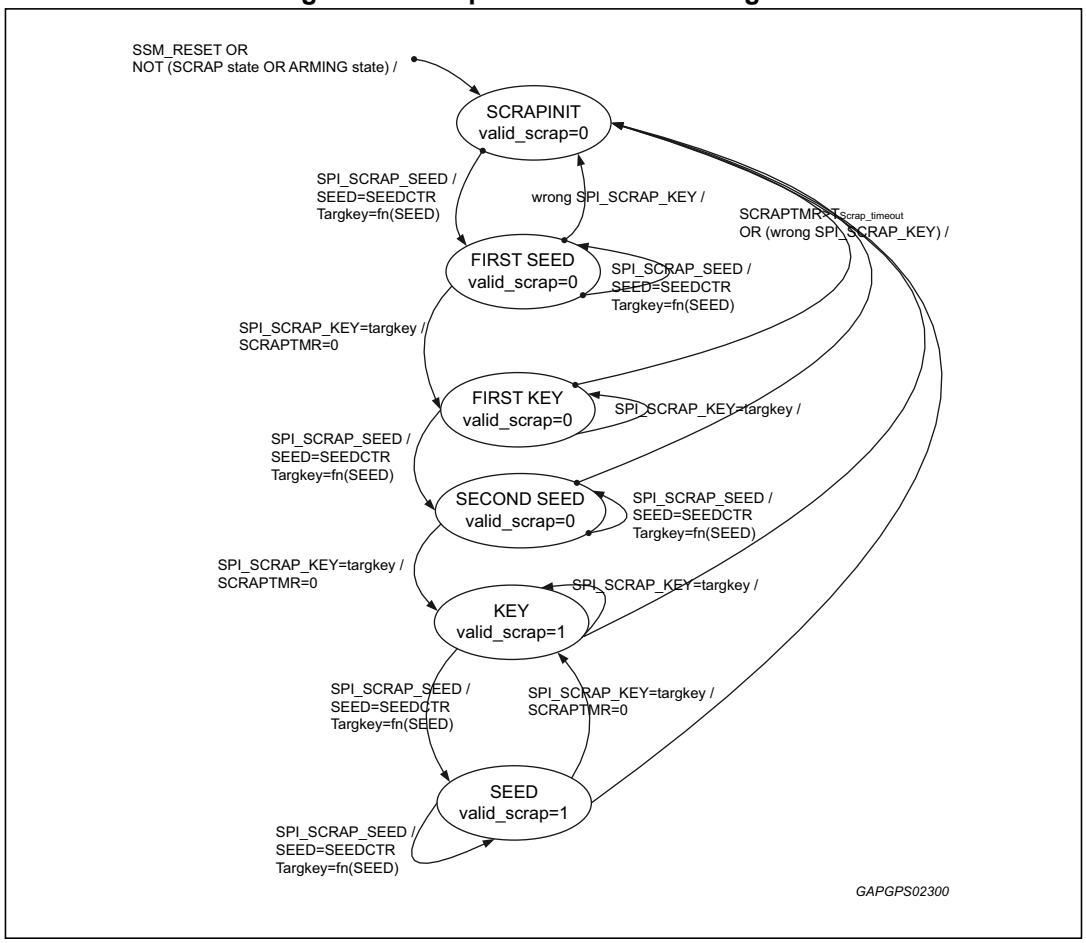
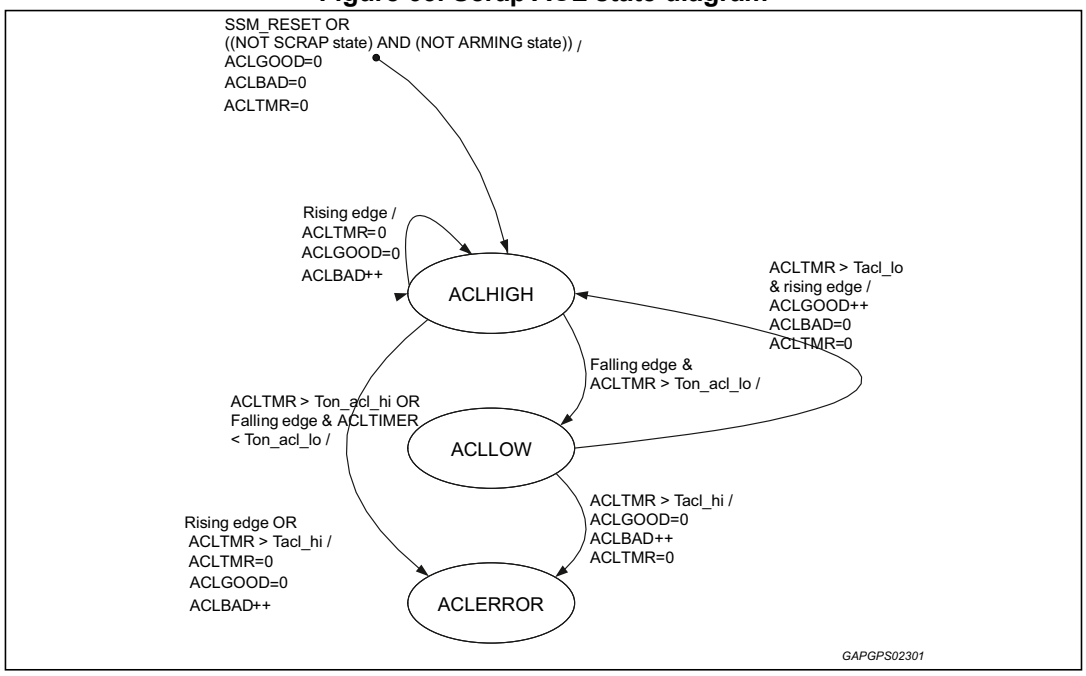


Figure 63. Scrap ACL state diagram

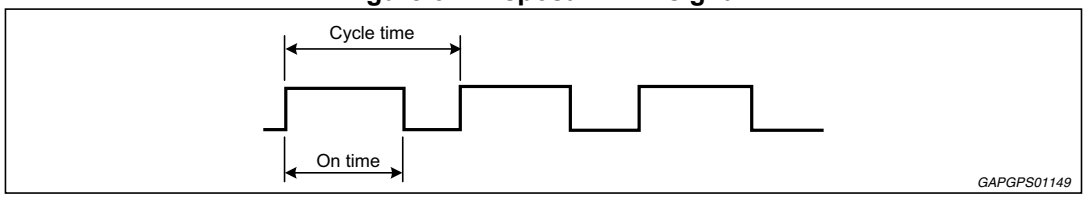


A specific waveform needs to be present on ACL input in order to instruct L9679P to arm all deployment loops. L9679P is designed to support the Additional Communication Line (ACL) aspect of the ISO-26021 standard, which requires an independent hardwired signal (ACL) to implement the scrapping feature. The disposal signal may come from either the vehicle's service connector, or the systems main microcontroller, depending on the end customer's requirements.

The arming function monitors the disposal PWM input (ACL pin) for a command to arm all loops for vehicle end-of-life airbag disposal. The disposal signal characteristic is shown in *Figure 64*. To remain in Arming state, at least three cycles of the ACL signal must be qualified (in addition to the periodic KEY value being received from the microcontroller). For the device to qualify the periodic ACL signal, the period and duty cycle are checked. Two consecutive cycles of invalid disposal signal are to be received to disqualify the ACL signal.

If the logic detects that the signal is incorrect or missing while in Scrap state, the device will stay in Scrap state; would it happen in Arming state, it will transition to Scrap state immediately.

Figure 64. Disposal PWM signal



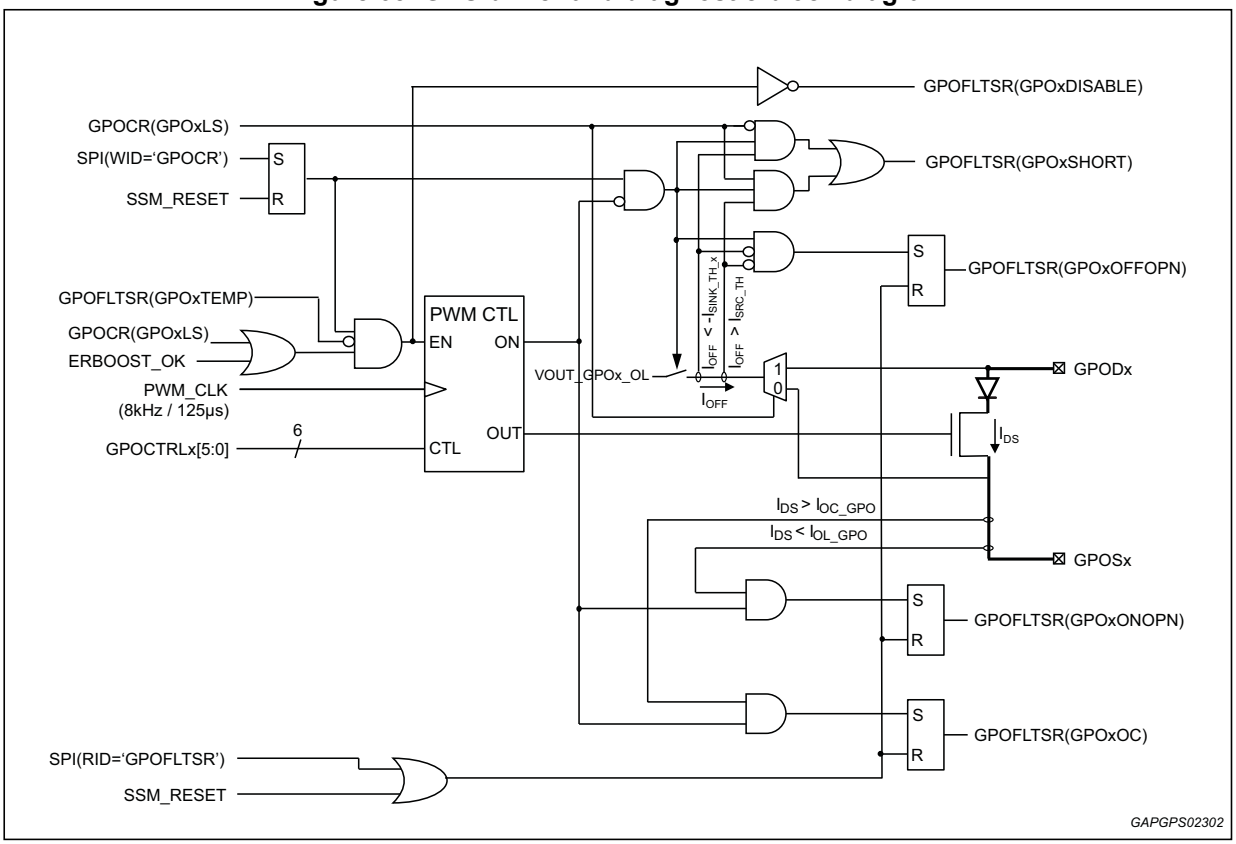
The disposal PWM signal cycle time and on time parameters can be found in the electrical parameters tables.

13 General purpose output (GPO) drivers

The L9679P contains three General Purpose Output (GPO) drivers configurable either as high-side or low-side modes. The drivers can be independently controlled in ON-OFF mode or in PWM mode setting the desired duty cycle value through the GPO Control Register (GPOCTRLx).

For low side driver configuration, the GPODx pin is the drain connection of an internal MOSFET and is the current sink for the output driver. The GPOSx pin is the source connection of the internal MOSFET and is externally connected to ground. For high side driver configuration, the GPODx pin will be connected to battery and GPOSx pin will be connected to load's high side.

Figure 65. GPO driver and diagnostic block diagram



The drivers are configured in one of the two modes through the GPO Configuration Register (GPOCR) register. This hardware configuration is only allowed during the Init and Diag states.

When configured as high-side, the drivers need ER Boost voltage to be above the V_{ERBST_OK} threshold to be enabled.

The default state of all drivers is off. The drivers can be independently activated via SPI control bits on GPO Control Register (GPOCTRLx). In addition, a set point on the GPOCTRLx will control the output drivers in PWM with a 125Hz frequency. If PWM control is desired, user should set the needed set point in the GPOxPWM bits of the GPOCTRLx while activating the interface. When all bits are set to '0', the GPOx output will be disabled.

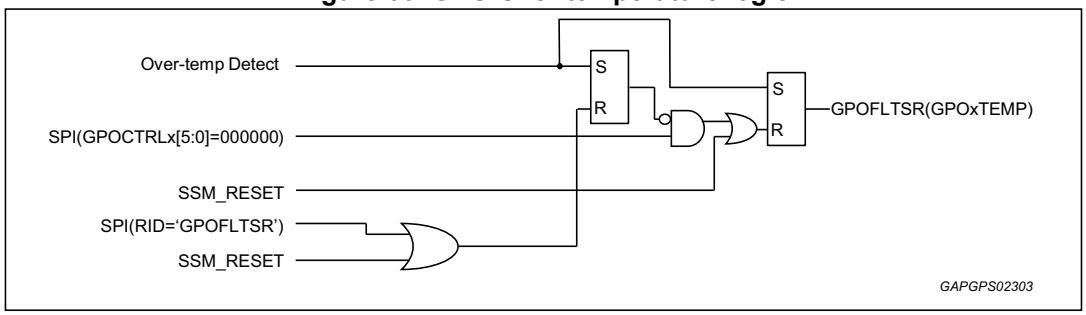
PWM control is based on a 125Hz frequency. 6 bits of GPOCTRLx are reserved to this mode, in order to control the drivers with 64 total levels from a 0% to a full 100% duty cycle.

When both GPO channels are used in PWM Mode at the same frequency they are synchronized to provide parallel configuration capability.

PWM control is implemented through a careful slew rate control to mitigate EMC emissions while operating the interface. The driver output structure is designed to stand -1V on its terminals and a +1V reverse voltage across source and drain.

The GPO driver is protected against short circuits and thermal overload conditions. The output driver contains diagnostics available in the GPO Fault Status Register (GPOFLTSR). All faults except for thermal overload will be latched until the GPOFLTSR register is read. Thermal overload faults will remain active after reading the GPOFLTSR register should the temperature remain above the thermal fault condition. For current limit faults, the output driver will operate in a linear mode (ILIM) until a thermal fault condition is detected.

Figure 66. GPO Over temperature logic



The device offers also an open load diagnostics while in ON state. The diagnostics is run comparing the current through the output stage with a reference threshold $I_{OpenLoad}$: should the output current be lower than the threshold, the open detection flag is asserted.

The device is also able to detect a fault condition during the OFF state by means of the Voltage Regulator Current Monitor (VRCM) block. During the OFF state the VRCM block tries to force a voltage $V_{OUT\_GPOx\_OL}$ (2.5 V) on GPOD pin if LS mode is selected (with a current limitation of $I_{LIM\_GPOD\_SRC/SINK}$) or on GPOS pin if the HS mode is selected (with a current limitation of $I_{LIM\_GPOS\_SRC/SINK}$) and, at the same, it compares the current sourced or sunk in order to detect if a fault on GPO pins is present. The diagnostic in OFF state is able to detect the open load in both HS and LS modes, the short to ground fault in LS mode and the short to battery fault in HS mode:

Table 16. Short to ground fault in LS mode

	LS MODE		
	GPOxSHORT	**GPOxOFFOPN**	**Interpretation**
$\mathbf{I_{OFF}} > I_{SRC\_TH}$	1	0	Short to ground
$-I_{SINK\_TH\_LS} < \mathbf{I_{OFF}} < I_{SRC\_TH}$	0	1	Open
$\mathbf{I_{OFF}} < -I_{SINK\_TH\_LS}$	0	0	Normal

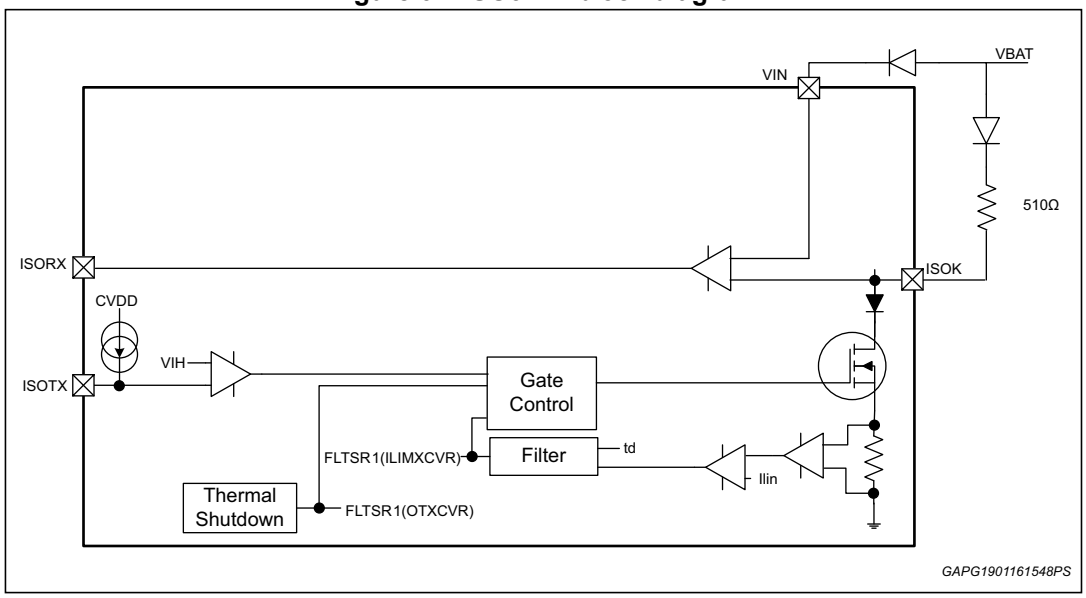
Table 17. Short to battery fault in HS mode

	HS MODE		
	GPOxSHORT	**GPOxOFFOPN**	**Interpretation**
$I_{OFF} > I_{SRC\_TH}$	0	0	Normal
$-I_{SINK\_TH\_HS} < I_{OFF} < I_{SRC\_TH}$	0	1	Open
$I_{OFF} < -I_{SINK\_TH\_HS}$	1	0	Short to battery

14 ISO9141 Transceiver (K-Line)

A block diagram of the function is shown below. Data transmitted by the main microcontroller is sent via the ISOTX pin and data is received via the ISORX pin. The bus output is ISOK.

Figure 67. ISO9141 block diagram



When the ISOTX pin is asserted, logic high, the ISOK output will be disabled (pulled up by an external resistor). When the ISOTX pin is logic low, the ISOK output will be enabled (pulled down by the internal driver). This input pin contains an internal pull-up to command the output to the disabled state in the event of an open circuit condition.

The ISORX pin has a push-pull output stage referenced to VDDQ voltage. This output is asserted high when the voltage on the ISOK pin is above the ISOK input receiver threshold, VBATMON, as defined in the electrical tables, while it is low when the voltage on the ISOK pin is below the ISOK input receiver threshold with hysteresis.

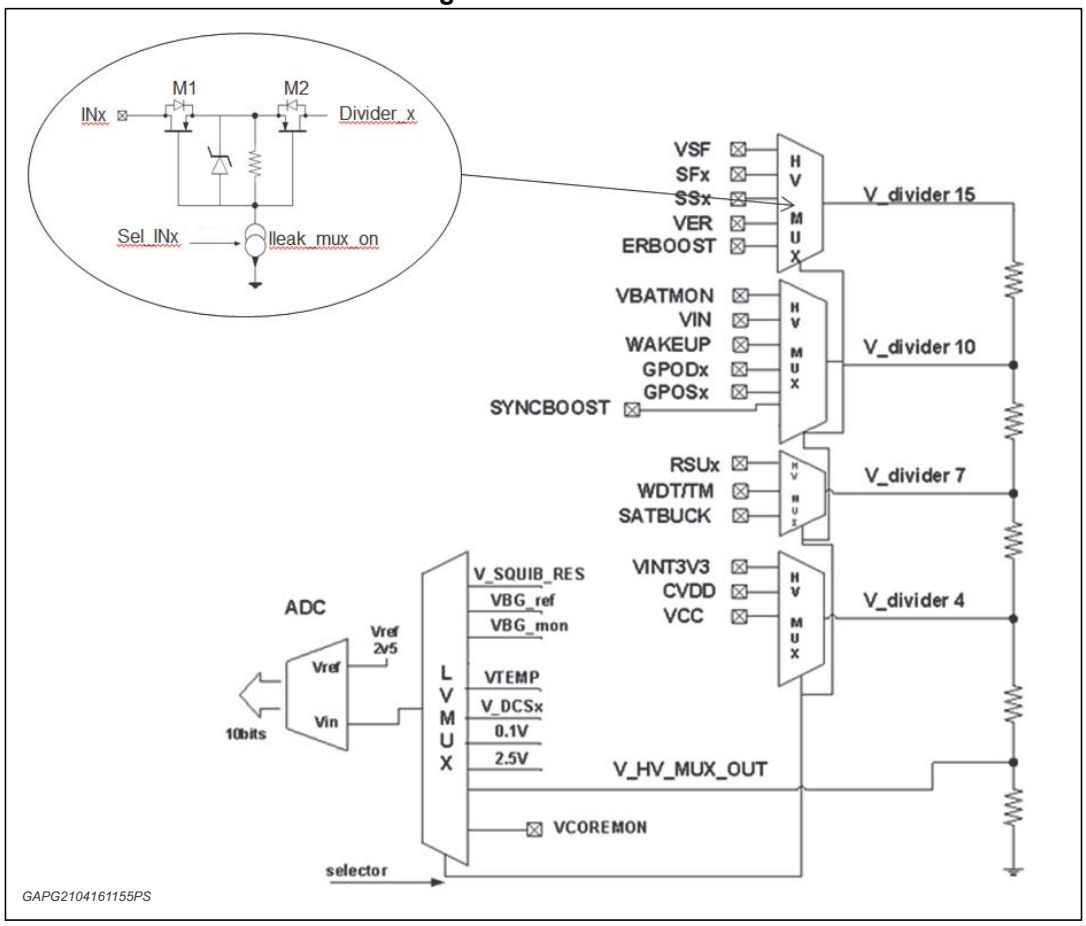
ISOK output is a low side driver compatible with ISO9141 physical layer.

The output stage is protected against short circuits and diagnostics provide feedback for current limit and thermal shutdown. While in current limit, the output stage will continue to function until thermal limit is reached. If the thermal limit occurs, the output stage will shut down until the temperature decreases below the limit threshold with hysteresis. The fault status is reported in the ISO9141 Fault Status Register (ISOFLTSR).

15 System voltage diagnostics

L9679P has an integrated dedicated circuitry to provide diagnostic feedback and processing of several inputs. These inputs are addressed with an internal analog multiplexer and made available through the SPI digital interface with the Diagnostic Data commands. In order to avoid saturation of high voltage internal signals, an internal voltage divider is used.

Figure 68. ADC MUX



The diagnostics circuitry is activated by four SPI Diagnostics Control commands (DIAGCTRLx); each of them can address all the available nodes to be monitored, except for what mentioned in *Table 18*.

DIAGCTRLx SPI command bit fields are structured in the following way:

DIAGCTRL_A (ADDRESS HEX 3A)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					x	x	x	x	x	x	x	x	x	ADCREQ_A[6:0]						
MISO	NEWDATA_A	0	0	ADCREQ_A[6:0]							ADCRES_A[9:0]									

DIAGCTRL_B (ADDRESS HEX 3B)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					x	x	x	x	x	x	x	x	x	ADCREQ_B [6:0]						
MISO	NEWDATA_B	0	0	ADCREQ_B [6:0]							ADCRES_B [9:0]									

DIAGCTRL_C (ADDRESS HEX 3C)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					x	x	x	x	x	x	x	x	x	ADCREQ_C [6:0]						
MISO	NEWDATA_C	0	0	ADCREQ_C [6:0]							ADCRES_C [9:0]									

DIAGCTRL_D (ADDRESS HEX 3D)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					x	x	x	x	x	x	x	x	x	ADCREQ_D [6:0]						
MISO	NEWDATA_D	0	0	ADCREQ_D [6:0]							ADCRES_D [9:0]									

ADCREQ[A-D] bit fields, used to address the different measurements offered, are listed in *Table 18* for reference.

L9679P diagnostics is structured to take four automatic conversions at a time. In order to get four measurements, four different SPI commands have to be sent (DIAGCTRL_A, DIAGCTRL_B, DIAGCTRL_C and DIAGCTRL_D), in no particular order.

In case the voltage to be measured is not immediately available, the desired inputs for conversion have to be programmed by SPI in advance, to allow them to attain a stable voltage value. This case applies to the squib resistance measurement and diagnostics (refer to *Loop diagnostics control and results registers*) and to the DC sensor measurement (refer to *Section 11*).

CONVRDY_0 bit in GSW is equal to (NEWDATA_A or NEWDATA_B), while CONVRDY_1 bit in GSW corresponds to (NEWDATA_C or NEWDATA_D).

Each NEWDATAx flag is asserted when conversion is finished and cleared when result is read out. However result is cleared only when new result for that register is available.

When a new request is received it is queued if other conversions are ongoing. The conversions are executed in the same order as their request arrived. The queue is 4 measures long so it's possible to send all 4 requests at the same time and then wait for the results. If a DIAGCTLRx command is received twice, the second conversion request will overwrite the previous one.

Requests are sent to the L9679P IC via the ADC measurement Registers (ADCREQx) as shown in *Table 18*. All diagnostics results are available on the ADCRESx registers, when addressed by the related ADCREQx register (e.g. data requested by ADCREQA would be written to ADCRESA).

Table 18. Diagnostics control register (DIAGCTRLx)

ADC Request (ADCREQx)								Voltage Measurement Selection	ADC Results (ADCRESx)
Bit[6:0]							Hex		Bit[9:0]
0	0	0	0	0	0	0	$00	Unused	
0	0	0	0	0	0	1	$01	ADC ground reference	V_{ADC_GROUND}
0	0	0	0	0	1	0	$02	ADC Test Pattern 2	$V_{ADC\_FULLSCALE}$
0	0	0	0	0	1	1	$03	DC Sensor ch. selected, Voltage	DCSV_selected
0	0	0	0	1	0	0	$04	DC Sensor ch. selected, Current	DCSI_selected
0	0	0	0	1	0	1	$05	DC Sensor ch. selected, Resistance(1)	DCSV and DCSI selected
0	0	0	0	1	1	0	$06	Squib measurement loop selected	Voutx
0	0	0	0	1	1	1	$07	Internal reference Voltage	VBGR
0	0	0	1	0	0	0	$08	Internal reference monitor Voltage	VBGM
0	0	0	1	0	0	1	$09		
0	0	0	1	0	1	0	$0A	Temperature Measurement	TEMP
0	0	0	1	0	1	1	$0B	DC Sensor ch 0, Voltage	DCSV_0
0	0	0	1	1	0	0	$0C	DC Sensor ch 1, Voltage	DCSV_1
0	0	0	1	1	0	1	$0D	DC Sensor ch 2, Voltage	DCSV_2
0	0	0	1	1	1	0	$0E	DC Sensor ch 3, Voltage	DCSV_3
0	0	0	1	1	1	1	$0F	DC Sensor ch 4, Voltage	DCSV_4
0	0	1	0	0	0	0	$10	DC Sensor ch 5, Voltage	DCSV_5
0	0	1	0	0	0	1	$11	DC Sensor ch 6, Voltage	DCSV_6
0	0	1	0	0	1	0	$12	DC Sensor ch 7, Voltage	DCSV_7
0	0	1	0	0	1	1	$13	DC Sensor ch 8, Voltage	DCSV_8
0	0	1	0	1	0	0	$14	V_B voltage of ER ESR measure(2)	V_B
0	0	1	0	1	0	1	$15	V_A voltage of ER ESR measure(2)	V_A
0	0	1	0	1	1	0	$16	V_C voltage of ER ESR measure(2)	V_C
0	0	1	0	1	1	1	$17	Unused	
0	0	1	1	0	0	0	$18	Unused	
0	0	1	1	0	0	1	$19	Unused	
0	0	1	1	0	1	0	$1A	Unused	
0	0	1	1	0	1	1	$1B	Unused	
0	0	1	1	1	0	0	$1C	Unused	
0	0	1	1	1	0	1	$1D	Unused	
0	0	1	1	1	1	0	$1E	Unused	
0	0	1	1	1	1	1	$1F	Unused	
0	1	0	0	0	0	0	$20	VBATMON pin voltage	VBATMON

Table 18. Diagnostics control register (DIAGCTRLx) (continued)

ADC Request (ADCREQx)								Voltage Measurement Selection	ADC Results (ADCRESx)
Bit[6:0]							Hex		Bit[9:0]
0	1	0	0	0	0	1	$21	VIN pin voltage	VIN
0	1	0	0	0	1	0	$22	Internal analog supply voltage (VINT3V3)	VINT3V3
0	1	0	0	0	1	1	$23	Internal digital supply voltage (CVDD)	CVDD
0	1	0	0	1	0	0	$24	ERBOOST pin voltage	ERBOOST
0	1	0	0	1	0	1	$25	SYNCBOOST pin voltage	SYNCBOOST
0	1	0	0	1	1	0	$26	VER pin voltage	VER
0	1	0	0	1	1	1	$27	SATBUCK voltage	SATBUCK
0	1	0	1	0	0	0	$28	VCC voltage	VCC
0	1	0	1	0	0	1	$29	WAKEUP pin voltage	WAKEUP
0	1	0	1	0	1	0	$2A	VSF pin voltage	VSF
0	1	0	1	0	1	1	$2B	WDTDIS pin voltage	WDTDIS
0	1	0	1	1	0	0	$2C	GPOD0 pin voltage	GPOD0
0	1	0	1	1	0	1	$2D	GPOS0 pin voltage	GPOS0
0	1	0	1	1	1	0	$2E	GPOD1 pin voltage	GPOD1
0	1	0	1	1	1	1	$2F	GPOS1 pin voltage	GPOS1
0	1	1	0	0	0	0	$30	GPOD2 pin voltage	GPOD2
0	1	1	0	0	0	1	$31	GPOS2 pin voltage	GPOS2
0	1	1	0	0	1	0	$32	RSU0 pin Voltage	RSU0
0	1	1	0	0	1	1	$33	RSU1 pin Voltage	RSU1
0	1	1	0	1	0	0	$34		
0	1	1	0	1	0	1	$35		
0	1	1	0	1	1	0	$36	SS0 pin voltage	SS0
0	1	1	0	1	1	1	$37	SS1 pin voltage	SS1
0	1	1	1	0	0	0	$38	SS2 pin voltage	SS2
0	1	1	1	0	0	1	$39	SS3 pin voltage	SS3
0	1	1	1	0	1	0	$3A	SS4 pin voltage	SS4
0	1	1	1	0	1	1	$3B	SS5 pin voltage	SS5
0	1	1	1	1	0	0	$3C	SS6 pin voltage	SS6
0	1	1	1	1	0	1	$3D	SS7 pin voltage	SS7
0	1	1	1	1	1	0	$3E		
0	1	1	1	1	1	1	$3F		
1	0	0	0	0	0	0	$40		
1	0	0	0	0	0	1	$41		

Table 18. Diagnostics control register (DIAGCTRLx) (continued)

ADC Request (ADCREQx)								Voltage Measurement Selection	ADC Results (ADCRESx)
Bit[6:0]							Hex		Bit[9:0]
1	0	0	0	0	1	0	$42	Unused	-
1	0	0	0	0	1	1	$43	Unused	-
1	0	0	0	1	0	0	$44	Unused	-
1	0	0	0	1	0	1	$45	Unused	-
1	0	0	0	1	1	0	$46	SF0 pin voltage	SF0
1	0	0	0	1	1	1	$47	SF1 pin voltage	SF1
1	0	0	1	0	0	0	$48	SF2 pin voltage	SF2
1	0	0	1	0	0	1	$49	SF3 pin voltage	SF3
1	0	0	1	0	1	0	$4A	SF4 pin voltage	SF4
1	0	0	1	0	1	1	$4B	SF5 pin voltage	SF5
1	0	0	1	1	0	0	$4C	SF6 pin voltage	SF6
1	0	0	1	1	0	1	$4D	SF7 pin voltage	SF7
1	0	0	1	1	1	0	$4E		
1	0	0	1	1	1	1	$4F		
1	0	1	0	0	0	0	$50		
1	0	1	0	0	0	1	$51		

1. The DC sensor resistance measurement can only be addressed through DIAGCRTL_A command. Results are available through DIAGCTRL_A and DIAGCTRL_B, where ADCRES_A will contain DCSI and ADCRES_B will contain DCSV.
2. Valid only for ADCREQ_x field of MISO response when ESR measure results are available.

Proper scaling is necessary for various measurements. The divider ratios vary by measurement and are summarized by function in the table below.

Table 19. Diagnostics divider ratios

Measurements	Divider Ratio				
	15:1	10:1	7:1	4:1	1:1
VER	X				
ERBOOST	X				
VSF	X				
SSxy	X				
SFx	X				
GPODx		X			
GPOSx		X			
SYNCBOOST		X			
VIN		X			

Table 19. Diagnostics divider ratios (continued)

Measurements	Divider Ratio				
	15:1	10:1	7:1	4:1	1:1
VBATMON		X			
WAKEUP		X			
SATBUCK			X		
WDT/TM			X		
RSUx			X		
VCC				X	
CVDD				X	
VINT				X	
Bandgap (BGR/BGM)					X

For measurements other than voltage (current, resistance, temperature etc.) the ranges are specified in the electrical parameters section of the relevant block.

15.1 Analog to digital algorithmic converter

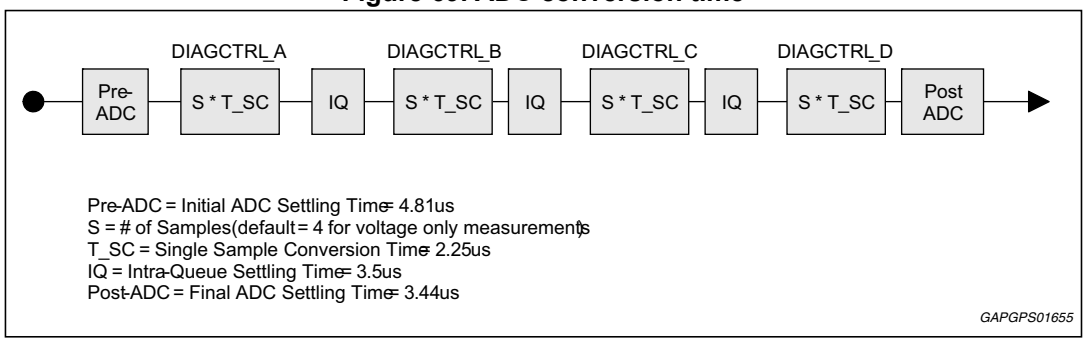
The device hosts an integrated 10 bit Analog to Digital converter, running at a clock frequency of 16 MHz. The ADC output is processed by a D to D converter with the following functions:

- Use of trimming bits to recover additional gain error due to resistor dividers mismatch;
- Digital low-pass filtering;
- Conversion from 12 to 10 bits.

10 bits data are filtered inside the digital section. The number of samples that are filtered vary depending on the chosen conversion. As per *Section 7.3.2*, the number of used samples in converting DC sensor, squib or temperature measurements defaults to 8. The number of samples for all other measurements defaults to 4. The sample number can be configured by accessing the SYS_CFG register. After low pass filter, the residual total error is ±4 LSB. This error figure applies to the case of a ideal reference voltage: the spread of reference voltage causes a proportional error in the conversion output. The reference voltage of the ADC is set to 2.5 V.

The conversion time is comprised of several factors: the number of measurements loaded into the queue, the number of samples taken for any one measurement, and the various settling times. An example of conversion time calculation for a full ADC request queue is reported in *Figure 69*. The timings reported in *Figure 69* are nominal ones, min/max values can be obtained by considering the internal oscillator frequency variation reported in the DC characteristics section.

Figure 69. ADC conversion time



16 Temperature sensor

The L9679P provides an internal analog temperature sensor. The sensor is aimed to have a reference for the average junction temperature on silicon surface. The sensor is placed far away from power dissipating stages and squib deployment drivers. The output of the temperature sensor is available via SPI through ADC conversion, as shown in *Table 18*. The formula to calculate temperature from ADC reading is the following one:

$$T(°C) = 180 - \left\{\left(\frac{220}{1.652}\right) \cdot \left[\left(\frac{ADC_{REF}}{2^{ADC_{RES}}} \cdot DIAGCTRLn(ADCRESn)\right) - 0.739\right]\right\}$$

@ DIAGCTRLn(ADCREQn) = $0A_{hex}$

All parametric requirements for this block can be found in specification tables.

17 Electrical characteristics

Every parameter in this chapter is fulfilled down to $VIN_{GOOD(max)}$.

No device damage is granted to occur down to VIN_{BAD}(min).

GNDA pin is used as ground reference for the voltage measurements performed within the device, unless otherwise stated.

All table or parameter declared ‘Design Info’ are not tested during production testing

17.1 Configuration and control

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C.

Table 20. Configuration and control DC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	V_{NOV}	Normal Operating Voltage	Design Info Depending on power supply configuration	6	13	18	V
2	V_{JSV}	Jump Start Voltage	Design Info 40°C ≤ Ta ≤ 50°C	18	-	26	V
3	V_{LDV}	Load Dump Voltage	Transient Design Info	26.5	-	40	V
4	WU_mon	WAKEUP Monitor threshold	GNDSUBx as ground reference Vin =5.5 V and 35 V	-	-	1.5	V
5	WU_off	WAKEUP Off threshold	GNDSUBx as ground reference Vin =5.5 V and 35 V	2	2.5	3	V
6	WU_on	WAKEUP On threshold	GNDSUBx as ground reference	4	4.5	5	V
7	WU_{RPD}	WAKEUP Pull-down Resistor	GNDSUBx as ground reference	120	300	480	kΩ
8	VB_{GOOD0}	VBATMON Thresholds	SYS_CTL(VBATMON_TH_SEL)=00 or 11	5.5	5.75	6	V
9	VB_{BAD0}		SYS_CTL(VBATMON_TH_SEL)=00 or 11	5	5.25	5.5	V
10	VB_{GOOD1}		SYS_CTL(VBATMON_TH_SEL)=01	6.45	6.7	6.95	V
11	VB_{BAD1}		SYS_CTL(VBATMON_TH_SEL)=01	5.95	6.2	6.45	V
12	VB_{GOOD2}		SYS_CTL(VBATMON_TH_SEL)=10	7.5	7.75	8	V
13	VB_{BAD2}		SYS_CTL(VBATMON_TH_SEL)=10	7	7.25	7.6	V

Table 20. Configuration and control DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
13b	ΔV_{BGOOD2_VBBAD2}	VBATMON delta thresholds	V_{BGOOD2_VBBAD2}	300	-	600	mV
14	$I_{LKG\_VBATMON\_OFF}$	VBATMON input leakage	Device OFF	-5	-	5	µA
15	$I_{LKG\_VBATMON\_ON}$		Device ON Design Info	20	24	30	µA
16	$R_{PD\_VBATMON}$	VBATMON pull-down resistance	Device ON VBATMON < 10V Design Info	125	250	375	kΩ
17	$I_{LKG\_VBATMON\_TOT}$	VBATMON total input leakage	$I_{LKG\_VBATMON\_ON}$ + R_{PD_VBATMO} VBATMON = 18V	35	-	180	µA
18	VIN_{GOOD0}	VIN Good and VIN Bad Thresholds	SYS_CTL(VIN_TH_SEL)=0	5	5.25	5.5	V
19	VIN_{BAD0}		SYS_CTL(VIN_TH_SEL)=0	4.5	4.75	5	V
20	VIN_{GOOD1}		SYS_CTL(VIN_TH_SEL)=1	6.05	6.3	6.55	V
21	VIN_{BAD1}		SYS_CTL(VIN_TH_SEL)=1	5.55	5.8	6.05	V
22	$VIN_{FASTSLOPE\_H}$	VIN Thresholds used to change Boost regulator transition time	-	9.3	9.8	10.3	V
23	$VIN_{FASTSLOPE\_L}$		-	9	9.5	10	V
24	$VIN_{FASTSLOPE\_HYS}$		-	0.2	0.3	0.4	V
25	$VIN_{SYNC\_DIS\_L}$	VIN SyncBoost Disable Thresholds	SYS_CTL(SYBST_V) =0	12.2	-	13.6	V
26	$VIN_{SYNC\_DIS\_H}$		SYS_CTL(SYBST_V) = 1	15	-	16.2	V
27	$VIN_{SYNC\_DIS\_LYS}$ $VIN_{SYNC\_DIS\_HYS}$		SYS_CTL(SYBST_V) = 0 / 1 Guaranteed by design	5	-	300	mV
28	$I_{LKG\_VIN\_OFF}$	VIN input current	Device OFF VIN = 40V	-10	-	10	µA
29	I_{VIN_ON}	VIN current consumption	Device ON VIN = 12V	-	-	40	mA
30	C_{VIN}	External VIN capacitor	Design Info	1	-	13(1)	µF

Table 20. Configuration and control DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
31	$I_{LKG\_VER\_OFF}$	VER Input Leakage	Device OFF VER = 40V	-5	-	50	µA
32	$I_{LKG\_VER\_ON\_L}$		Device ON ERBOOST > VER ER Charge OFF	50	-	200	µA
33	$I_{LKG\_VER\_ON\_H}$		Device ON ERBOOST < VER ER Charge OFF	100	-	500	µA
34	V_{WDTDIS_TH}	WDT/TM threshold	Test go no go	10	12	14	V
35	V_{WDTDIS_HYST}	WDT/TM hysteresis	Design Info	0.2	0.4	0.5	V
36	I_{PD_WDTDIS}	WDT/TM Pull Down Resistance	$V_{WDTDIS} \leq 5V$	20	45	70	µA
37	$V_{TH2\_H\_VCCSEL\_}$	VCCSEL Input Voltage Thresholds 2	-	5.9	6.4	6.9	V
38	$V_{TH2\_L\_VCCSEL}$		-	5.6	6.1	6.6	V
39	V_{HYS2_VCCSEL}		-	0.2	-	-	V
40	I_{PD_VCCSEL}	VCCSEL Pull Down Current	VCCSEL= SATBUCK	20	45	70	µA
41	I_{TOTLKG_BAT}	Battery Line Total Input Leakage	Room Temp WAKEUP = 0 All following pins at 13V: VBATMON, VIN, ERBSTSW, ERBOOST, SYNCBSTSW, SYNCBOOST Guaranteed by design	-	-	35	µA
42	T_J	Junction Temperature	Design Info	-	-	150	°C

1. Bigger capacitor can be used in case an external switch is used in parallel to the ER-Switch.

Table 21. Configuration and control AC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	$T_{FLT\_VBATMONTH}$	VBATMON thresholds deglitch filter time	-	26	30	34	µs
2	$T_{FLT\_VINGOOD\_UP}$	VIN Good thresholds deglitch filter time rising edge	-	3	3.5	4	µs
3	$T_{FLT\_VINGOOD\_DOWN\_L}$	VIN Good thresholds deglitch filter time falling edge	SYS_CFG(VINGOOD_FILT_SEL) = 0	-	1	-	µs
4	$T_{FLT\_VINGOOD\_DOWN\_H}$	VIN Good thresholds deglitch filter time falling edge	SYS_CFG(VINGOOD_FILT_SEL) = 1	3	3.5	4	µs
6	$T_{FLT\_VINBAD\_DOWN}$	VIN Bad thresholds deglitch filter time falling edge	-	3	3.5	4	µs
7	$T_{FLT\_VINBAD\_UP}$	VIN Bad thresholds deglitch filter time rising edge	-	26	30	34	µs
8	$T_{VINGOOD\_BLK}$	VIN Good Thresholds blanking time	-	26	30	34	µs
9	$T_{FLT\_VINSYNCDIS\_DOWN}$	VIN SyncBoost Disable deglitch filter time falling edge	-	3.3	-	4.2	µs
10	$T_{FLT\_VINSYNCDIS\_UP}$	VIN SyncBoost Disable deglitch filter time rising edge	-	9.5	-	11	µs
11	T_{FLT_WAKEUP}	Wakeup deglitch filter time	-	0.95	1.05	1.15	ms
12	T_{LATCH_WAKEUP}	Wakeup latch time	-	9.7	10.8	11.9	ms
13	T_{PWRUP}	Power-up Delay Time – Wake-up to RESET released	-	-	-	10	ms

Table 22. Open ground detection DC specifications

No	Symbol	Parameter	Conditions / Comments	Min	Typ	Max	Unit
1	$GNDA_{OPEN}$	GNDA open threshold	GNDSUBx=0	100	200	300	mV
2	$GNDD_{OPEN}$	GNDD open threshold	GNDSUBx=0	100	200	300	mV
3	$BSTGND_{OPEN}$	BSTGND open threshold	GNDSUBx=0	100	200	300	mV
4	I_{PU_BSTGND}	BSTGND pull-up current	ER BOOST OFF and SYNC BOOST OFF	130	-	270	µA
5	$SATGND_{OPEN}$	SATGND open threshold	GNDSUBx=0	100	200	300	mV
6	I_{PU_SATGND}	SATGND pull-up current	SATBUCK OFF	80	120	160	µA
7	$VCCGND_{OPEN}$	VCCGND open threshold	GNDSUBx=0	100	200	300	mV
8	I_{PU_VCCGND}	VCCGND pull-up current	VCC BUCK OFF	80	120	160	µA

Table 23. GND_OPEN_AC - Open ground detection DC specifications

No	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$T_{FLT\_GNDREFOPEN}$	GNDA and GNDD Open Deglitch Filter Time	-	7	11	16	µs
2	$T_{FLT\_GNDREGOPEN}$	BSTGND, SATGND, VCCGND Open Deglitch Filter Time	-	1.9	2.3	2.7	µs

17.2 Internal analog reference

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ Ta ≤ +95 °C

$VIN_{BAD0(min)}$ ≤ VIN ≤ 35 V

Table 24. Internal analog reference

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	V_{BG1}	Bandgap reference	-	-1%	1.2	+1%	V
2	V_{BG2}	Bandgap monitor	-	-1%	1.2	+1%	V
3	V_{ADC_GROUND}	ADC Ground reference	ADC total error included	90	104	120	mV
4	$V_{ADC\_FULLSCALE}$	ADC Full scale reference	-	-1.5%	2.5	+1.5%	V

17.3 Internal regulators

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V

Table 25. Internal regulator DC specifications

No	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$V_{OUT\_VINT3V3}$	VINT3V3 output voltage	Vin =5.5 V, 12 V and 35 V	3.14	3.3	3.46	V
2	$V_{OV\_VINT3V3}$	VINT3V3 over voltage	-	3.47	-	3.7	V
3	$V_{UV\_VINT3V3}$	VINT3V3 under voltage	-	2.97	-	3.13	V
4	V_{OUT_CVDD}	CVDD output voltage	Vin =5.5 V, 12 V and 35 V	3.14	3.3	3.46	V
5	I_{OUT_CVDD}	CVDD current capability	External load is not allowed	-	-	50	mA
6	I_{LIM_CVDD}	CVDD current limit	Vin =5.5 V, 12 V and 35 V	80	-	-	mA
7	V_{OV_CVDD}	CVDD over voltage	-	3.47	-	3.7	V
8	V_{UV_CVDD}	CVDD under voltage	-	2.7	-	2.9	V
9	C_{CVDD}	CVDD output capacitance	Design info	60	100	140	nF

Table 26. Internal regulators AC specifications

No	Symbol	Parameter	Comment	Min	Typ	Max	Unit
1	$T_{FLT\_VINT\_CVDD\_OV}$	Internal regulator over voltage deglitch filter time	-	7	11	16	µs
2	$T_{FLT\_VINT\_CVDD\_UV}$	Internal regulator under voltage deglitch filter time	-	7	11	16	µs

17.4 Watchdog

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V

Table 27. Temporal watchdog timer AC specifications (WD1)

No	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$T_{WDT1\_TIMEOUT}$	Temporal watchdog timeout	-	-	-	2.00	ms
				-	-	16.3	ms
2	T_{WDT1_RST}	Temporal watchdog reset time	-	0.9	1.0	1.1	ms

Table 28. Algorithmic watchdog timer DC specifications (WD2)

No	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$V_{OH\_WD2LCKOUT}$	WD2LockOut output voltage	I_{LOAD} = -0.5 mA	VCC-0.6	-	VCC	V
2	$V_{OL\_WD2LCKOUT}$		I_{LOAD} = 2.0 mA	0	-	0.4	V

Table 29. Algorithmic watchdog timer AC specifications (WD2)

No	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$T_{WDT2\_TIMEOUT}$	Algorithmic watchdog timeout	-	45	50	55	ms
2	T_{WDT2_RST}	Algorithmic watchdog reset time	-	0.9	1.0	1.1	ms
3	$T_{RISE\_WD2LCKOUT}$	WD2LockOut rise time	50 pF load, 20%-80%	-	-	1.0	µs
4	$T_{FALL\_WD2LCKOUT}$	WD2LockOut fall time	50 pF load, 20%-80%	-	-	1.0	µs
5	f_{WD2_SEED}	WD2 Seed Counter Rate	-	-	$\frac{f_{osc}}{512}$	-	MHz

17.5 Oscillators

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ Ta ≤ +95 °C, $V_{INGOOD0}$(max) ≤ VIN ≤ 35 V.

Table 30. Oscillators specifications

N #	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	f_{OSC}	Main oscillator average frequency	-	15.2	16	16.8	MHz
2	f_{MOD_OSC}	Main oscillator modulation frequency	SPI_CLK_CNF(MAIN_SS_DIS=0) Design Info	-	$\frac{f_{osc}}{128}$	-	MHz
3	I_{MOD_OSC}	Main oscillator modulation index	SPI_CLK_CNF(MAIN_SS_DIS=0)	2	4	6	%
4	f_{AUX}	Aux oscillator average frequency	-	7.125	7.5	7.875	MHz
5	f_{MOD_AUX}	Aux oscillator modulation frequency	SPI_CLK_CNF(AUX_SS_DIS=0) Design Info	-	$\frac{f_{osc\_AUX}}{128}$	-	MHz
6	I_{MOD_AUX}	Aux oscillator modulation index	SPI_CLK_CNF(AUX_SS_DIS=0)	2	4	6	%
7	$f_{OSC\_LOW\_TH}$	Main oscillator low frequency detection threshold	-	$\frac{128}{68} \cdot f_{AUX\_MIN}$	-	$\frac{128}{68} \cdot f_{AUX\_MAX}$	MHz
8	$f_{OSC\_HIGH\_TH}$	Main oscillator high frequency detection threshold	-	$\frac{79}{32} \cdot f_{AUX\_MIN}$	-	$\frac{79}{32} \cdot f_{AUX\_MAX}$	MHz

17.6 Reset

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V, VCCx(min) ≤ VCCx ≤ VCCx(max), VCC = 3.3 V or 5 V

Table 31. Reset DC specifications

No	Symbol	Parameter	Comment	Min	Typ	Max	Unit
1	V_{OH_RESET}	RESET output voltage	I_{LOAD} = -1. mA	VCC-0.4	-	VCC	V
2	V_{OL_RESET}		I_{LOAD} = 2.0 mA	0	-	0.4	V
3	R_{PD_RESET}	RESET pull down resistance	-	65	100	135	kΩ

Table 32. Reset AC specifications

No	Symbol	Parameter	Comment	Min	Typ	Max	Unit
1	T_{RISE_RESET}	Rise time	50 pF load, 20%-80%	-	-	1.00	µs
2	T_{FALL_RESET}	Fall time		-	-	1.00	µs
3	T_{HOLD_RESET}	Reset hold time	-	0.45	0.5	0.55	ms

17.7 SPI interface

All electrical characteristics are valid for both Global and Remote Sensor SPI and for the following conditions unless otherwise noted:

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V, VCCx(min) ≤ VCCx ≤ VCCx(max), VCC = 3.3 V or 5 V

Table 33. Global and remote sensor SPI DC specifications

No	Symbol	Parameter	Comment	Min	Typ	Max	Unit
1	$V_{IH\_CS\_G}$ $V_{IH\_CS\_RS}$	CS_x High level Input Voltage	-	2	-	-	V
2	$V_{IL\_CS\_G}$ $V_{IL\_CS\_RS}$	CS_x Low level Input Voltage	-	-	-	0.8	V
3	$I_{PU\_CS\_G}$ $I_{PU\_CS\_RS}$	CS_x Pull Up Current	CS_x = 0V	-70	-45	-20	µA
4	$V_{IH\_MOSI\_G}$ $V_{IH\_MOSI\_RS}$	MOSI_x High level Input Voltage	-	2	-	-	V
5	$V_{IL\_MOSI\_G}$ $V_{IL\_MOSI\_RS}$	MOSI_x Low level Input Voltage	-	-	-	0.8	V
6	$I_{PD\_MOSI\_G}$ $I_{PD\_MOSI\_RS}$	MOSI_x Pull Down Current	MOSI_x = VCC	20	45	70	µA
8	$V_{IH\_SCLK\_G}$ $V_{IH\_SCLK\_RS}$	SCLK_x High level Input Voltage	-	2	-	-	V

Table 33. Global and remote sensor SPI DC specifications (continued)

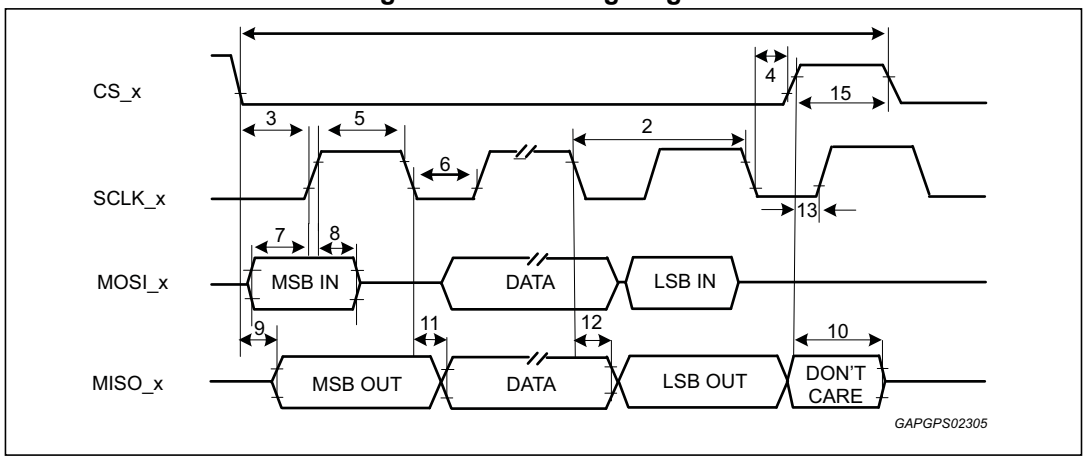
No	Symbol	Parameter	Comment	Min	Typ	Max	Unit
9	$V_{IL\_SCLK\_G}$ $V_{IL\_SCLK\_RS}$	SCLK_x Low level Input Voltage	-	-	-	0.8	V
10	$I_{PD\_SCLK\_G}$ $I_{PD\_SCLK\_RS}$	SCLK_x Pull Down Current	SCLK_x = VCC	20	45	70	µA
12	$V_{OH\_MISO\_G}$ $V_{OH\_MISO\_RS}$	MISO_x High level Output Voltage	I_{LOAD} = -800 µA	VCC -0.5	-	VCC	V
13	$V_{OL\_MISO\_G}$ $V_{OL\_MISO\_RS}$	MISO_x Low level Output Voltage	I_{LOAD} = 2.0 mA	-	-	0.4	V
14	$I_{LKG\_MISO\_G}$ $I_{LKG\_MISO\_RS}$	MISO_x Output Leakage	Tri-state leakage	-10	-	10	µA
15	$V_{IH\_MISO\_RS}$	MISO_RS High level Input Voltage	-	2	-	-	V
16	$V_{IL\_MISO\_RS}$	MISO_RS Low level Input Voltage	-	-	-	0.8	V

Table 34. SPI AC specifications

No	Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
1	F_{SCLK}	SPI transfer frequency	-	-	8	8.08	MHz
2	T_{SCLK}	SCLK_x period	-	123.8	-	-	ns
3	T_{LEAD}	Enable lead time	-	250	-	-	ns
4	T_{LAG}	Enable lag time	-	50	-	-	ns
5	T_{HIGH_SCLK}	SCLK_x high time	-	40	-	-	ns
6	T_{LOW_SCLK}	SCLK_x low time	-	40	-	-	ns
7	T_{SETUP_MOSI}	MOSI_x input setup time	-	20	-	-	ns
8	T_{HOLD_MOSI}	MOSI_x input hold time	-	20	-	-	ns
9	T_{ACC_MISO}	MISO_x access time	80 pF load	-	-	60	ns
10	T_{DIS_MISO}	MISO_x disable time		-	-	100	ns
11	T_{VALID_MISO}	MISO_x output valid time		-	-	30	ns
12	T_{HOLD_MISO}	MISO_x Output Hold Time	80 pF load; Design Info	0	-	-	ns
13	T_{NODATA}	SCLK_x hold time	-	20	-	-	ns
14	T_{FLT_CS}	CS_x noise glitch rejection time	-	50	-	300	ns
15	T_{NODATA}	SPI interframe time	-	400	-	-	ns
16	$T_{SETUP\_MISO\_RS}$	MISO_RS Input Setup Time	-	20	-	-	ns
17	$T_{HOLD\_MISO\_RS}$	MISO_RS Input Hold Time	-	20	-	-	ns

Note: All timing is shown with respect to 10% and 90% of the actual delivered VCC voltage.

Figure 70. SPI timing diagram



17.8 ERBoost regulator

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V.

Table 35. ERBoost regulator DC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	V_{O_ERBST}	Boost output voltage	Across all line and I_{O_BST} load (steady state) SYS_CTL(ER_BST_V)=0	22.6	23.8	25	V
2			Across all line and I_{O_BST} load (steady state) 1SYS_CTL(ER_BST_V)=1	31.65	33	35	V
3	I_{O_ERBST}	Boost output current	-	0.1	-	70	mA
4	dV_{SR_ac}	Line transient response	All line, load; dt=100us; BST33V = 0/1 Design Info	-8%	-	8%	%
5	dV_{LR_ac}	Load transient response	All line, load; dt=100us; BST33V = 0/1 Design Info	-8%	-	8%	%
6	R_{DSON_ERBST}	Power switch resistance	-	-	-	1	Ω
7	I_{OC_ERBST}	Over current detection	-	650	-	1350	mA
8	$I_{OC\_ERBST\_ERON}$		ER Switch activated AND SW_REGS_CONF(LOW_ERBST_ILIM_ERON) = 1	125	-	600	mA

Table 35. ERBoost regulator DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
9	$I_{LKG\_ERBST\_OFF}$	ERBOOST input current	ERBOOST=40V Power-off or Sleep Mode	-5	-	+5	µA
10	$I_{LKG\_ERBST\_ON}$		Active or Passive Mode ERBoost reg. enabled ERBSTSW > ERBoost > VER ER Charge OFF VSF regulator OFF Any GPO channel not enabled Guarantee by design	60	-	200	µA
11	$I_{LKG\_ERBST\_ON\_wGPO}$		Active or Passive Mode ERBoost reg. enabled ERBSTSW > ERBoost > VER ER Charge OFF VSF regulator OFF All GPO channel activated	1.5	-	2.4	mA
12	V_{ERBST_OK}	ERBOOST voltage threshold	BST33V = 0	18	20	22	V
13			BST33V = 1	26	28	30	V
14	V_{ERBST_OV}	ERBOOST Over Voltage threshold	SYS_CTL(ER_BST_V) = 0	22.6	-	25	V
15			SYS_CTL(ER_BST_V) = 1	31.65	-	35	V
16	$V_{ERBST\_DIS\_TH}$	Voltage difference between VIN and ERBOOST to deactivate the ER Boost regulator	VIN – ERBOOST Vin = 5.5 V, 12 V and 35 V	1.6	2.2	2.5	V
17	$V_{ERBST\_CLAMP\_EN\_TH}$	Voltage difference between ERBSTSW and ERBOOST to activate the ER Boost CLAMP	$V_{ERBSTSW} - V_{ERBOOST}$	2.7	3.3	3.7	V
18	T_{JSD_ERBST}	Thermal shutdown	-	150	175	190	°C
19	$T_{HYS\_TSDERBST}$		-	5	10	15	°C

Table 36. ERBoost regulator AC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	F_{SW_ERBST}	ERBOOST switching frequency	-	1.8	1.882	2.0	MHz
2	$T_{RISE\_ERBSTSW\_SLOW}$ $T_{FALL\_ERBSTSW\_SLOW}$	ERBSTSW transition time	10% to 90% voltage on ERBSTSW VIN ≥ $VIN_{FASTSLOPE\_H}$ = 10.3 V I_{load} = 6 0mA SYS_CTL(ER_BST_V) = 1 Guaranteed by Design	15	-	35	ns
3	$T_{RISE\_ERBSTSW\_FAST}$ $T_{FALL\_ERBSTSW\_FAST}$		10% to 90% voltage on ERBSTSW VIN = $VIN_{FASTSLOPE\_L}$ =9 V	5	-	15	ns
4	T_{ON_ERBST}	ERBOOST charge-up time	$C_{ERBOOST}$ = 2.2 µF Vin =12V, I_{O_ERBST}= 5mA SYS_CTL(ER_BST_V) = 1 Measured from CS_G edge to V_{O_ERBST}(min)	50	-	500	µs
5	$T_{SOFTST\_IOC\_ERBST}$	ERBOOST over current threshold soft start time	Not tested	-5%	1024	+5%	µs
6	$T_{FLT\_VIN\_ERBST\_COMP}$	Deglitch filter on VIN_ERBoost comparator	-	27	30	33	µs
7	$T_{FLT\_TSD\_ERBST}$	Thermal shutdown filter time	-	-	-	10	µs
8	T_{SOFTST_ERBST}	ERBOOST Soft-start Time	Design Info. Time from activation of ERBOOST when overcurrent is 40% of I_{OC_ERBST} ($I_{OC\_ERBST\_ERON}$) to instant when overcurrent is 100% of I_{OC_ERBST} ($I_{OC\_ERBST\_ERON}$)	-	-	1075	µs

Table 37. ERBOOST Converter external components design info

No	Symbol	Component	Conditions	Min	Typ	Max	Unit
1	L_{ERBST}	Inductance	-	8	10	12	µH
2	ESL_{ERBST}	Inductance resistance	-	-	-	0.1	Ω
3	C_{BLK_ERBST}	Output bulk capacitance to ensure regulator stability	Min cap value including derating factors	1	2.2	-	µF
4	ESR_{CBLK_ERBST}	Bulk capacitor ESR	-		-	50	mΩ

Table 37. ERBOOST Converter external components design info (continued)

No	Symbol	Component	Conditions	Min	Typ	Max	Unit
5	V_{FSTR_ERBST}	Steering diode forward voltage	I_F=100 mA	-	-	0.85	V
6	I_{LKGSTR_ERBST}	Steering diode reverse leakage	Ta = 95 °C	-	-	3	mA

17.9 ER CAP current generators and diagnostic

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V, 8 V ≤ ERBOOST.

Table 38. ER CAP current generators and diagnostic DC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	I_{ER_CHARGE}	ER charge current	ERBOOST ≥ 8 VERBOOST - VER ≥2V ERBOOST = 24 V and 35 V	60	65	70	mA
2	$I_{ER\_DISCHARGE\_LOW}$	ER discharge low level current	VER ≥ 6V	60	65	70	mA
3	$I_{ER\_DISCHARGE\_HIGH}$	ER discharge high level current	VER ≥ 8V	589	640	691	mA
4	$R_{DSON\_ERCHARGE}$	ER charge power resistance	$(V_{ERBOOST} - V_{VER})/I_{VER}$ I_{VER} = 10mA	-	-	20	Ω
5	VER_{RANGE}	VER voltage measurement range	-	20	-	35	V
6	VER_{ACC}	VER voltage measurement accuracy	VER_{RANGE}	-8	-	+8	%
7	$ERCAP_{RANGE}$	Energy reserve capacitor measurement range	Design Info	-	-	10	mF
8	$ERCAP_{ACC}$	Energy reserve capacitor measurement accuracy	ΔVERMIN = 2 V	-7	-	+7	%
9	$ERCAP\_ESR_{RANGE}$	Energy reserve capacitor ESR measurement range	-	200	-	600	mΩ
10	$ERCAP\_ESR_{ACC}$	Energy reserve capacitor ESR measurement accuracy	All errors included except the offset one (OFF_{ER_ESR})	-20		+20	%
11	G_{ER_ESR}	Energy Reserve Capacitor ESR Measurement Gain	-	-13%	3	+13%	V/V
12	OFF_{ER_ESR}	Energy Reserve Capacitor ESR Measurement Offset	Design Info	70	-	160	mΩ

Table 38. ER CAP current generators and diagnostic DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
13	T_{JSD_ERBST}	ER charge thermal shutdown	-	150	175	190	°C
14	$T_{HYS\_TSDERBST}$		-	5	10	15	°C
15	$V_{VER\_VBATMON\_TH}$	Voltage difference between VER and VBATMON to activate the ER Discharge in passive mode	VER - VBATMON	1.6	2.2	2.5	V

Table 39. ER CAP current generators and diagnostic AC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	T_{ON_ERCAP}	Energy reserve capacitor charge-up time	$C_{VER} \leq$ 10mF nominal, BST33V = 0, Design Info	-	-	4	s
2	T_{ESR_DIAG}	ER CAP ESR diagnostic duration	Total duration time from SPI command to ADC results availability	-5%	225	+5%	µs
3	$T_{FLT\_TSD\_ERCHARGE}$	Thermal shutdown filter time	-	-	-	10	µs

17.10 ER switch

All electrical characteristics are valid for the following conditions unless otherwise noted: -40 °C ≤ Ta ≤ +95 °C, $VIN_{GOOD0} \leq$ VIN ≤ 35 V.

Table 40. ER Switch DC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	R_{DSON_ERSW}	Power switch resistance	Vin = 5.5 V and 35 V	0.5	-	3	Ω
2	I_{LIM_ERSW}	ER switch current limit	V_{ER} = 17 V@ Vin = 12 V and V_{ER} = 35 V@ V_{IN} = 31 V	600	810	980	mA
3	$V_{ER\_SW\_OV\_TH}$	ER switch Over Voltage threshold	Test go / no go ER switch turned off when Vin > V_{ER} + $V_{ER\_SW\_OV\_TH}$ Vin = 12 V and 35 V	10	-	200	mV
4	T_{JSD_ERSW}	Thermal shutdown	-	150	175	190	°C
5	$T_{HYS\_TSDERSW}$		-	5	10	15	°C

Table 41. ER Switch AC specifications

No	Symbol	Parameter	Conditions	Min		Max	Unit
1	T_{ON_ERSW}	ER turn-on time (time to reach either R_{DSON_ERSW} or I_{LIM_ERSW})	C_{VIN} = 10 µF	-	-	5	µs
2	$T_{FLT\_TSD\_ERSW}$	Thermal shutdown filter time	-	-	-	10	µs
3	T_{BLK_ERSW}	ER switch activation blanking time after thermal shutdown	-	-	1	-	ms

17.11 COVRACT

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V; VIN_{GOOD}(max) ≤ VIN ≤ 35 V;
VCCx(min) ≤ VCCx ≤ VCCx(max); VCC = 3.3 V or 5 V

Table 42. COVRACT DC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	$V_{OH\_COVRACT}$	COVRACT output voltage	I_{LOAD} = -0.5 mA	VCC -0.6	-	VCC	V
2	$V_{OL\_COVRACT}$		I_{LOAD} = 2.0 mA	0	-	0.4	V
3	$I_{REV\_COVRACT}$	Reverse current short high voltage	COVRACT = 40 V VCC = 3.3 V	-	-	1	mA

Table 43. COVRACT AC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	$T_{RISE\_COVRACT}$	Rise time	50 pF load, 20%-80%	-	-	1.00	µs
2	$T_{FALL\_COVRACT}$	Fall time	50 pF load, 20%-80%	-	-	1.00	µs

17.12 SYNCBOOST converter

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ $VIN_{SYNC\_DIS\_X}$(min)

Table 44. SYNCBOOST converter DC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	$V_{O\_SYNCBST}$	SYNCBOOST output voltage	Across all line and load, steady state SYS_CTL(SYBST) = 0	11.40	12	-	V
2			Across all line and load (steady state) SYS_CTL(SYBST) = 1	14.00	14.75	-	V

Table 44. SYNCBOOST converter DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
3	$I_{O\_SYNCBST\_VL\_IH}$	SYNCBOOST output current	SYS_CTL(SYBST_V) = 0 SYS_CFG(LOW_POWER_MODE) = 0	20	-	360	mA
4	$I_{O\_SYNCBST\_VL\_IL}$		SYS_CTL(SYBST_V) = 0 SYS_CFG(LOW_POWER_MODE) = 1	20	-	240	mA
5	$I_{O\_SYNCBST\_VH\_IH}$		SYS_CTL(SYBST_V) = 1 SYS_CFG(LOW_POWER_MODE) = 0	20	-	290	mA
6	$I_{O\_SYNCBST\_VH\_IL}$	SYNCBOOST output current	SYS_CTL(SYBST_V) = 0 SYS_CFG(LOW_POWER_MODE) = 1	20	-	190	mA
7	dV_{SR_ac}	Line transient response	All line, load; dt = 100 µs; SYS_CTL(SYBST) = 0/1 Design Info	-8%	-	8%	%
8	dV_{LR_ac}			-8%	-	8%	%
9	$R_{DSON\_SYNCBST}$	Power switch resistance	-	-	-	0.5	Ω
10	$I_{OC\_SYNCBST\_HIGH}$	Over current detection of integrated MOS	SYS_CFG(LOW_POWER_MODE) = 0	1.6	-	3.2	A
11	$I_{OC\_SYNCBST\_LOW}$		SYS_CFG(LOW_POWER_MODE) = 1	1.5	-	2.6	A
12	$I_{LKG\_SYNCBOOST}$	SYNCBOOST leakage	SYNCBOOST=40V Device off	-	-	10	µA
13	$I_{LKG\_SYNCBSTSW}$	SYNCBSTSW leakage	SYNCBSTSW=40V Device off	-	-	20	µA
14	$V_{SYNCBST\_OK}$	SYNCBOOST voltage threshold	-	9	10	11	V
15	$V_{SYNCBST\_OV}$	SYNCBOOST Over Voltage threshold	-	22	23	24	V
16	$V_{SYNCBST\_DIS\_TH}$	Voltage difference between VIN and SYNCBOOST to deactivate the SYNC Boost regulator	VIN – SYNCBOOST	1.6	2.2	2.5	V
17	$V_{SYNCBST\_CLAMP\_EN\_TH}$	Voltage difference between SYNCBSTSW and SYNCBOOST to activate the SYNC Boost CLAMP	$V_{SYNCBSTSW} - V_{SYNCBOOST}$	2.7	3.3	3.7	V
18	$V_{VIN\_SYNCBST\_RESTART\_TH}$	Voltage threshold to restart Syncboost regulator during ER State	SYS_CTL(RESTART_SYBST_SEL) = 0 Voltage threshold on VIN pin	9	-	10.3	V
19	$V_{SYNCBST\_RESTART\_TH}$		SYS_CTL(RESTART_SYBST_SEL) = 1 Voltage threshold on SYNCBOOST pin	19	20	21	V

Table 44. SYNCBOOST converter DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
20	$T_{JSDERSYNCBST}$	Thermal shutdown	-	150	175	190	C
21	$T_{HYS\_TSDSYNCBST}$	Thermal shutdown hysteresis	-	5	10	15	°C

Table 45. SYNCBOOST converter AC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	$F_{SW\_SYNCBST}$	SYNCBST switching frequency	-	1.8	1.882	2.0	MHz
2	$T_{RISE\_SYNCBSTSW\_SLOW}$ $T_{FALL\_SYNCBSTSW\_SLOW}$	SYNCBSTSW transition time	10% to 90% voltage on SYNCBSTSW VIN = $VIN_{FASTSLOPE\_H}$ Design Info	15	-	30	ns
3	$T_{RISE\_SYNCBSTSW\_FAST}$ $T_{FALL\_SYNCBSTSW\_FAST}$		10% to 90% voltage on SYNCBSTSW VIN = $VIN_{FASTSLOPE\_L}$ Design Info	5	-	20	ns
4	$T_{SOFTST\_SYNCBST}$	SYNCBST Soft-start Time	Design Info. Time from activation of SYNCBOOST when overcurrent is 40 % of $I_{OC\_SYNCBST\_HIGH}$ ($I_{OC\_SYNCBST\_LOW}$) to instant when overcurrent is 100% of $I_{OC\_SYNCBST\_HIGH}$ ($I_{OC\_SYNCBST\_LOW}$)	-	-	1075	µs
5	$T_{SOFTST\_OC\_SYNCBST}$	ERBOOST $_{Over\ Current}$t threshold soft start time	Not tested	-5%	1024	+5%	µs
6	$T_{FLT\_TSD\_SYNCBST}$	Thermal shutdown filter time	-	-	-	10	µs
7	T_{BLK_SYNCSW}	Sync boost activation blanking time after thermal shutdown	-	-	1	-	ms

Table 46. SYNCBOOST converter external components design info

No	Symbol	Component	Conditions	Min	Typ	Max	Unit
1	$L_{SYNCBST}$	Inductance	Min 4.7 µH nominal	3.76	-	-	µH
2	$ESL_{SYNCBST}$	Inductance resistance	-	-	-	0.1	Ω
3	$C_{BLK\_SYNCBST}$	Output bulk capacitance	Min 2.2 µF nominal	1.76	-	-	µF
4	$ESR_{CBLK\_SYNCBST}$	Bulk capacitor ESR	-	-	-	50	mΩ

Table 46. SYNCBOOST converter external components design info (continued)

No	Symbol	Component	Conditions	Min	Typ	Max	Unit
5	V_{FSTR}	Steering diode forward voltage	I_F = 1 A	-	-	0.5	V
6	I_{LKGSTR}	Steering diode reverse leakage	Ta = 95 °C	-	-	3	mA

17.13 SATBUCK converter

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35V, $V_{SYNCBST\_OK}$ ≤ SYNCBOOST

Table 47. SATBUCK converter DC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	V_{O_SATBCK}	SATBUCK output voltage	Across all line and load, steady state SAT_V = 0	6.92	7.2	7.48	V
2			Across all line and load, steady state SAT_V = 1	8.64	9	9.36	V
3	$I_{O\_SATBCK\_VH\_IH}$	SATBUCK output current	SAT_V =0 LOW_POWER_MODE = 0	20	-	450	mA
4	$I_{O\_SATBCK\_VH\_IL}$		SAT_V =0 LOW_POWER_MODE = 1	20	-	300	mA
5	$I_{O\_SATBCK\_VL\_IH}$		SAT_V =1 LOW_POWER_MODE = 0	20	-	390	mA
6	$I_{O\_SATBCK\_VL\_IL}$		SAT_V =1 LOW_POWER_MODE = 1	20	-	240	mA
7	dV_{SR_ac}	Line transient response	All line, load; dt=100 µs; SAT_V = 0/1 Design Info	-4%	-	4%	%
8	dV_{LR_ac}	Load transient response	All line, load; dt=100 µs; SAT_V = 0/1 Design Info	-4%	-	4%	%
9	$R_{DSON\_SATBCK\_HS}$	High side power switch resistance	SyncBoost = 12 V and 35 V	-	-	1.4	Ω
10	$R_{DSON\_SATBCK\_LS}$	Low side power switch resistance	SyncBoost = 12 V and 35 V	-		1	Ω
11	$I_{OC\_HS\_SATBCK\_HI}$	High side over current detection	LOW_POWER_MODE = 0	0.83	1.1	1.37	A
12	$I_{OC\_HS\_SATBCK\_LO}$		LOW_POWER_MODE = 1	0.53	0.7	0.9	A
13	$I_{OCP\_LS\_SATBCK\_LO}$	Low side positive over current detection	$V_{SATBCKSW}$ ≥ 0 $V_{SYNCBST}$ < $V_{SYNCBST\_RESTART\_TH}$	1	-	100	mA
14	$I_{OCP\_LS\_SATBCK\_HI}$		$V_{SATBCKSW}$ ≥ 0 FAST SLOPE	100	240	350	mA

Table 47. SATBUCK converter DC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
15	$I_{OCN\_LS\_SATBCK\_HI}$	Low side negative over current detection	$V_{SATBCKSW}$ = 0 LOW_POWER_MODE = 0	0.94	1.25	1.56	A
16	$I_{OCN\_LS\_SATBCK\_LO}$		$V_{SATBCKSW}$ = 0 LOW_POWER_MODE = 1	0.64	0.85	1.06	A
17	$V_{SATBCK\_OK\_LOW}$	SATBUCK voltage threshold	SYS_CTL(SAT_V) = 0	6.2	6.5	6.8	V
18	$V_{SATBCK\_OK\_HIGH}$		SYS_CTL(SAT_V) = 1	7.7	8.1	8.5	V

Table 48. SATBUCK converter AC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Units
1	F_{SW_SATBCK}	SATBUCK switching frequency	-	1.8	1.882	2.0	MHz
2	$T_{RISE\_SATBCKSW\_SLOW}$ $T_{FALL\_SATBCKSW\_SLOW}$	SATBCKSW transition time	10% to 90% voltage on SATBCKSW $V_{SYNCBST}$ < $V_{SYNCBST\_RESTART\_TH}$ Design Info	10	-	25	ns
3	$T_{RISE\_SATBCKSW\_FAST}$ $T_{FALL\_SATBCKSW\_FAST}$		10% to 90% voltage on SATBCKSW $V_{SYNCBST}$ > $V_{SYNCBST\_RESTART\_TH}$ Design Info	5	-	15	
4	T_{SOFTST_SATBCK}	SATBUCK soft start time	From 10% to 90%	0.50	-	2	ms

Table 49. SATBUCK converter external components design info

No	Symbol	Component	Conditions	Min	Typ	Max	Unit
1	L_{SATBCK}	Inductance	Min 4.7 µH nominal	3.76	-	-	µH
2	$ESR_{LSATBCK}$	Inductance Resistance	-	-	-	0.25	Ω
3	C_{BLK_SATBCK}	Output Bulk Capacitance	Min 4.7 µH nominal	3	-	30	µF
4	ESR_{CBLK_SATBCK}	Bulk Capacitor ESR	-	-	-	50	mΩ

17.14 VCC regulator

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V, V_{SATBCK_OK} ≤ SATBUCK

Table 50. VCC converter DC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Units
1	V_{O_VCC}	VCCBUCK Output Voltage	Across all line and load, steady state VCCSEL < $V_{TH1\_L\_VCCSEL}$	3.20	3.3	3.40	V
2			Across all line and load, steady state VCCSEL = > $V_{TH1\_H\_VCCSEL}$	4.85	5	5.15	V
3	$I_{O\_VCC3V\_HI}$	VCCBUCK output current	VCCSEL < $V_{TH1\_L\_VCCSEL}$ LOW_POWER_MODE = 0	20	-	420	mA
4	$I_{O\_VCC3V\_LO}$		VCCSEL < $V_{TH1\_L\_VCCSEL}$ LOW_POWER_MODE = 1	20	-	230	mA
5	$I_{O\_VCC5V\_HI}$		VCCSEL > $V_{TH1\_H\_VCCSEL}$ LOW_POWER_MODE = 0	20	-	270	mA
6	dV_{SR_ac}	Line transient response	All line, load; dt=100 µs; Design Info	-4%	-	4%	%
7	dV_{LR_ac}	Load transient response	All line, load; dt=100 µs; Design Info	-4%	-	4%	%
8	$R_{DSON\_VCCBCK\_HS}$	High side power switch resistance	SATBUCK = 6.92 V and 9.36 V	-	1.4	0.6	Ω
9	$R_{DSON\_VCCBCK\_LS}$	Low side power switch resistance	SATBUCK = 6.92 V and 9.36 V	-	1.4	0.6	Ω
10	$I_{OC\_HS\_VCCBCK\_HI}$	High side over current detection	SYS_CFG(LOW_POWER_MODE) = 0	0.59	0.75	0.9	A
11	$I_{OC\_HS\_VCCBCK\_LO}$		SYS_CFG(LOW_POWER_MODE) = 1	0.4	0.56	0.7	A
12	$I_{OCP\_LS\_VCCBCK}$	Low side positive over current detection	$V_{VCCBCKSW}$ > 0 SYS_CFG(LOW_POWER_MODE) = 0 / 1	1	-	100	mA
13	$I_{OCN\_LS\_VCCBCK\_HI}$	Low side negative over current detection	$V_{VCCBCKSW}$ = 0 LOW_POWER_MODE = 0	0.67	0.9	1.13	A
14	$I_{OCN\_LS\_VCCBCK\_LO}$		$V_{VCCBCKSW}$ = 0 LOW_POWER_MODE = 1	0.49	0.65	0.82	A
15	I_{OF_VCC}	Open feedback current on VCC	-	100	150	200	µA
16	VCC_{OV3V}	VCC over voltage detection	VCCSEL < $V_{TH2\_L\_VCCSEL}$	3.43	-	3.6	V
17	VCC_{OV5V}		VCCSEL > $V_{TH2\_H\_VCCSEL}$	5.25	-	5.50	V

Table 50. VCC converter DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Units
18	VCC_{UV3V}	VCC under voltage detection high	VCCSEL < $V_{TH2\_L\_VCCSEL}$	3.0	-	3.17	V
19	VCC_{UV5V}		VCCSEL > $V_{TH2\_H\_VCCSEL}$	4.5	-	4.75	V
20	VCC_{UVL}	VCC under voltage detection low	-	1.8	2	2.2	V

Table 51. VCC converter AC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Units
1	F_{SW_VCCBCK}	VCCBUCK switching frequency	-	1.8	1.882	2.0	MHz
2	$T_{RISE\_VCCBCKSW}$ $T_{FALL\_VCCBCKSW}$	VCCBCKSW transition time	10% to 90% voltage on VCCBCKSW Design Info	8	-	20	ns
3	T_{SOFTST_VCCBCK}	VCCBUCK soft start time	From 10% to 90%	0.5	-	2	ms
4	T_{FLT_VCCOV}	VCC over voltage detection deglitch filter time	-	27	30	33	µs
5	$T_{FLT\_VCCOV\_RAMPUP}$	VCC Over voltage detection deglitch filter time during VCC_RAMPUP state	VCC reg in VCC_RAMPUP state	1.5	2	2.5	µs
6	T_{FLT_VCCUV}	VCC under voltage detection deglitch filter time	-	27	30	33	µs
7	T_{FLT_VCCUVL}	VCC under voltage low detection deglitch filter time	-	1.5	2	2.5	µs

Table 52. VCC converter external components design info

No	Symbol	Component	Conditions	Min	Typ	Max	Unit
1	L_{VCCBCK}	Inductance	Min 4.7 µH nominal	3.76	-	-	µH
2	$ESR_{LVCCBCK}$	Inductance resistance	-	-	-	0.25	Ω
3	C_{BLK_VCCBCK}	Output bulk capacitance	Min 4.7 µF nominal	3	-	30	µF
4	ESR_{CBLK_VCCBCK}	Bulk capacitor ESR	-	-	-	50	mΩ

17.15 VSF regulator

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35V, VSF + 2V ≤ ERBOOST

Table 53. VSF regulator DC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	VSF	Output voltage	All line, load, IO_VSF up to 6mA SYS_CGF(VSF_V)= 0	18	20	22	V
2			All line, load, IO_VSF up to 6mA Only in case SYS_CTL(ER_BST_V)=1 SYS_CGF(VSF_V) = 1	23	25	27	V
3	I_{LIM_VSF}	Output load current limit	VSF = 0	7	10	13	mA
4	V_{DO_VSF}	Drop-out voltage	V(ERBOOST-VSF)	-	-	2	V
5	C_{VSF}	Output capacitance	Design Info	2.9	-	14	nF
6	$I_{LKG\_VSF\_OFF}$	VSF input leakage	Device OFF	-5	-	5	µA
7	R_{PD_VSF}	VSF pull-down resistance	Device ON VSF regulator OFF; VSF = 25V	60	125	220	kΩ
8	I_{PD_VSF}	VSF pull-down current	Device ON VSF regulator ON; Design Info	34	40	46	µA
9	$I_{PD\_VSF\_TOT}$	VSF total pull-down current	Device ON VSF regulator ON VSF = 25V SYS_CGF(VSF_V)= 1	147	230	462	µA

Table 54. VSF regulator AC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	T_{ON_VSF}	VSF turn on time	C_{VSF} = 14 nF Measured from VSF_EN=1 to VSF inside regulation limits	-	-	100	µs

17.16 Deployment drivers

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35V, 6V ≤ SSxy ≤ 35V, SSxy - SFx ≤ 25V.

Table 55. Deployment drivers – DC specifications

No	Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
1	I_{DEPL_LO}	Deployment Current	R = 2 ohms Considering 9mA as not detected leakage with a 1kOhm equivalent resistance from SFx to GND	1.33	1.4	1.6	A
2	I_{DEPL_HI}		R = 2 ohms, 9V ≤ SSxy Considering 13.5mA as not detected leakage with a 1kOhm equivalent resistance from SFx to GND,	1.94	1.99	2.3	A
3	I_{TH_DEPL}	Deployment Current Counter Threshold	-	I_{DEPL} x * 90%	-	-	A
4	I_{OC_SR}	Low side Over Current Detection	-	2.2	3.1	4.0	A
5	I_{LIM_SR}	Low side Current Limitation	-	2.2	3.1	4.0	A
6	$\Delta I_{LIM\_OC\_SR}$	Difference between Current Limitation and OC Threshold	I_{LIM_SR} - I_{OC_SR}	0.1	-	-	mA
7	R_{DSON_HSLS}	Combined High side MOS + Low side MOS On Resistances	Ta = 95°C	-	-	2	Ω
8	I_{REV_SF}	Reverse Current on SFx	Without device malfunction(1) Not to be tested in series production	-	-	-100	mA

Table 55. Deployment drivers – DC specifications (continued)

No	Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
9	$I_{LKG\_SS\_OFF}$	SSxy leakage current	Device OFF SSxy ≤ 35 V SFx=SFy=0	-10	-	10	µA
10	$I_{LKG\_SS\_ON\_1CH}$		Device ON SSxy ≤ 35 V SFx = 0 SSxy Leakage current of each channel Not Tested	70	100	130	µA
11	$I_{LKG\_SS\_ON}$		Device ON SSxy ≤ 35 V SFx = SFy = 0 Total SSxy leakage current with both x and y channels NOT armed (= 2 * 100µA)	140	200	260	µA
12	$I_{LKG\_SS\_CH\_ARMED}$		Device ON SSxy ≤ 35 V SFx = 0 Total SSxy leakage current with only one channel armed (=520 + 100 µA)	450	620	850	µA
13	$I_{LKG\_SS\_2CH\_ARMED}$		Device ON SSxy ≤ 35 V SFx = SFy = 0 Total SSxy leakage current with both x and y channels armed (= 2* 520 µA) Not Tested	884	1040	1196	µA
14	$I_{LKG\_SF\_ON\_0V}$	SF Leakage Current	Device ON, SYNCBOOST = SSxy = 35V, SFx = 0V	-5	-	5	µA
15	$I_{LKG\_SF\_ON\_35V}$		Device ON, SYNCBOOST = SSxy = 35V, SFx = 35V	-5	-	50	µA
16	$I_{LKG\_SF\_OFF\_0V}$		Device OFF SYNCBOOST = open, SSxy = open but all SSxy pins connected, SFx = 0V	-5	-	5	µA
17	$I_{LKG\_SF\_OFF\_35V}$		Device OFF SYNCBOOST = open, SSxy = open but all SSxy pins connected, SFx = 35V	-5	-	50	µA

Table 55. Deployment drivers – DC specifications (continued)

No	Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
18	$I_{LKG\_SR\_ON}$	SR Leakage Current	Device ON, SYNCBOOST = SSxy = 35V, SRx = 0V-35	-	-	50	µA
19	$I_{LKG\_SR\_OFF}$		DEVICE OFF, SYNCBOOST = open, SSxy = open but all SSxy pins connected, SRx pull down current OFF SRx=0V-20V	-	-	50	µA
20			DEVICE OFF, SYNCBOOST = open, SSxy = open but all SSxy pins connected, SRx pull down current OFF SRx=35V	-	-	30	µA
21	V_{SR_CLAMP}	SR voltage clamp	-	35	-	40	V
22	L_{DEPL}	Load Inductance	Maximum load inductance Design Info(2)	0	-	56	µH
23	C_{SFx}	Load Capacitance	Maximum capacitance to GND Design Info	13	-	455	nF
24	C_{SRx}			13	-	455	nF
25	C_{SSxy}	SSxy Capacitance	Maximum capacitance to GND connected directly to SSxy pin Design Information	-	-	10	nF
26	R_{SFLx}	Load Impedance	Design Info	-	-	6.5	Ω
27		Wire Length	Squib Loops containing a clock spring shall be limited to a maximum length of 3m	1	-	10	m
28	R_{Wirex}	Wire Resistance	Design Info	16.8	-	63.4	mΩ/m
29	L_{Wirex}	Wire Inductance	Design Info	0.6	-	1.8	µH/m
30	R_{CSx}	Clock Spring Resistance	Maximum number of clock springs is 3 for any IC Design Info	0	-	0.7	Ω

Table 55. Deployment drivers – DC specifications (continued)

No	Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
31	L_{CSx}	Clock Spring Inductance	Design Info	0	-	42.9	µH
32	$k_{L\_CS1 – L\_CS2}$	Clock Spring Coupling	Design Info	0.739	-	0.903	-
33	L_{EMI}	Squib EMI protection	Design Info	0	-	7.7	µH

1. In case of an unsupplied device and shorted deployment pins (e.g. to battery voltage), the dynamic reverse current through the high side power stage depends on C_{SSxy}.
2. L_{DEPL} could be calculated in the following way:

   Non-Clock Spring Loops: $L_{DEPL}(max) = L_{Wire}(10m*2) + L_{EMI} = (3.6uH/m * 10m) + 7.7uH = 43.7uH$

   Clock Spring Loops: $L_{Wire}(3m*2) + 2*L_{CSx} + L_{EMI} - (2*k_{L_CX}*SQRT(L_CS1*L_CS2)) = = (3.6uH/m * 3m) + 2 * 42.9uH + 7.7uH - (2 * 0.739 * 42.9uH) = 40.9uH$Clock Spring Loops with short to ground
   $L_{DEPL}(max) = L_{Wire}(3m) + L_{CSx} + L_{EMI} = (1.8uH/m * 3m) + 42.9uH + 7.7uH = 56uH.$

Figure 71. Deployment drivers diagram

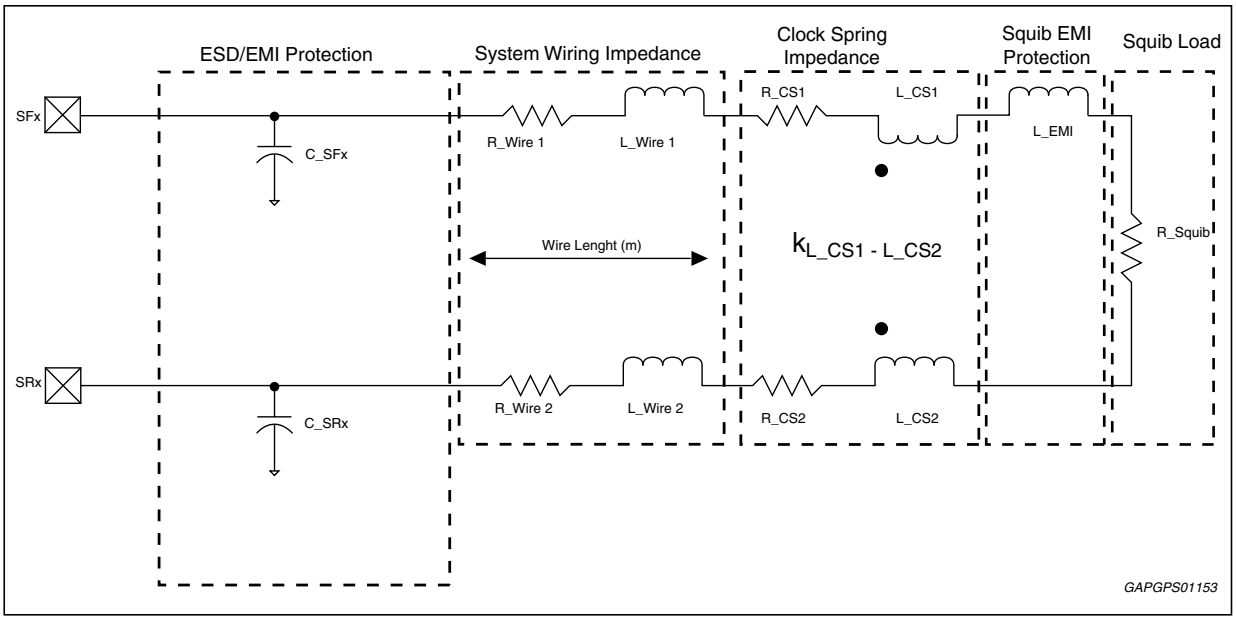


Table 56. Deployment drivers – AC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1 2 3	T_{DEPL}	Deployment time	DCR_x(Dep_Current) = I_{DEPL_LO} ≥1.209A rising to 1.209A falling; T_{DEPL} = DCR_x(Deploy_Time)* $T_{DEP\_TIME\_RES}$ - TDEL_IDEP	- DCR_x(Deploy_Time)* TDEP_TIME_RES - 65 -	-	DCR_x(Deploy_Time)* $T_{DEP\_TIME\_RES}$ -	ms
4	$T_{DEP\_TIME\_RES}$	DCR_x Deploy_Time resolution	-	-	$\frac{1024}{f_{osc}}$	-	µs
5	$T_{DEP\_CC\_RES}$	Deployment current counter resolution	-	-	$\frac{256}{f_{osc}}$	-	µs
6	T_{RISE_IDEPL}	Rise time 10% - 90% of I_{DEPL}	SSxy = 25 V, R_{SQ} = 2.2 ohm, C = 22 nF L = 44 µH	-	-	32	µs
7	T_{DEL_IDEP}	Delay time SPI_CS to 90% I_{DEPL}		-	-	65	µs
8	T_{FALL_IDEPL}	Fall time 90% - 10% I_{DEPL}		-	-	32	µs
9	$T_{DEL\_SD\_LS}$	Low side shutdown delay time (with respect to high-side deactivation)	-	50	-	-	µs
10	$T_{FLT\_ILIM\_LS}$	Low side overcurrent to low side deactivation deglitch time in short to battery condition	-	80	100	120	µs
11	$T_{FLT\_OS\_LS}$	Low side overcurrent to high side deactivation deglitch time in case of intermittent open to squib condition	-	-	-	20	µs
12	$T_{OFF\_OS\_HS}$	High side OFF time in case of intermittent open to squib condition	-	4	-	12	µs

17.17 Deployment driver diagnostic

17.17.1 Squib resistance measurement

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0}(max) ≤ VIN ≤ 35 V, 6 V ≤ SSxy ≤ 35 V, 7 V ≤ SYNCBOOST ≤ 35 V.

Table 57. Deployment drivers diagnostics - Squib resistance measurement

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	$R_{SQ\_RANGE\_1}$	Squib resistance range 1	LPDIAGREQ(ISRC_CURR_SEL) = 0	0	-	10.0	Ω
2	$R_{SQ\_RANGE\ 2}$	Squib resistance range 2	LPDIAGREQ(ISRC_CURR_SEL) = 1	0	-	50.0	Ω
3	G_{RSQ}	Squib resistance measurement Differential amplifier gain	$V_{OUT\_RSQ} = G_{RSQ}$ x [(V_{SF} - V_{SR})] + V_{off_RSQ}	-2%	5.2	+2%	V/V
4	V_{off_RSQ}	Squib resistance measurement Differential amplifier offset	$V_{OUT\_RSQ} = G_{RSQ}$ x [(V_{SF} – V_{SR})] + V_{off_RSQ}	200	-	400	mV
5	$I_{SRC\_HI\_SF}$ $I_{SRC\_HI\_SR}$	Squib resistance measurement High current source	LPDIAGREQ(ISRC_CURR_SEL) = 0 LPDIAGREQ(ISRC) = “01” or “10” SyncBoost = 11.5 V and 35 V	-5%	40	+5%	mA
6	$I_{SRC\_LO\_SF}$ $I_{SRC\_LO\_SR}$	Squib resistance measurement Low current source	LPDIAGREQ(ISRC_CURR_SEL) = 1 LPDIAGREQ(ISRC) = “01” or “10” SyncBoost = 11.5 V and 35 V	-10%	8	+10%	mA
7	I_{SRC_DELTA}	Squib Resistance Measurement Delta Current Source	$I_{SRC\_HI\_x}$ - $I_{SRC\_LO\_x}$	-5%	32	+5%	mA
8	SR_{ISRC}	Squib resistance measurement current source slew-rate	-	3	7.5	12	mA/µs
9	V_{SRx_RM}	SRx voltage during resistance measurement	LPDIAGREQ(ISRC)=”01” or “10” LPDIAGREQ(ISINK)=1	0.4	0.7	1.2	V
10	$I_{SINK\_HI\_SR}$	SRx current sink limit high	LPDIAGREQ(ISRC_CURR_SEL) = 0 LPDIAGREQ(ISINK) = 1	50	75	100	mA
11	$I_{SINK\_LO\_SR}$	SRx current sink limit low	LPDIAGREQ(ISRC_CURR_SEL) = 1 LPDIAGREQ(ISINK) = 1	10	17.5	25	mA
12	$I_{PD\_SR\_L}$	SRx current pull down	SYS_CTL(PD&VRCM_SEL) = 0	0.7	1	1.3	mA
13	$I_{PD\_SR\_H}$		SYS_CTL(PD&VRCM_SEL) = 1	4.5	6	7.5	mA
14	R_{LKG_SF}	SFx leakage resistance	Design info	1	-	-	kΩ

Table 57. Deployment drivers diagnostics - Squib resistance measurement (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
15	V_{LKG_SF}	SFx leakage voltage source	Design info	-1	-	18	V
16	R_{SQ_ACC}	Squib resistance measurement accuracy	After software calculation All errors included R_{SQ} between 1.0 Ω and 10.0 Ω With High Current Source (40 mA)	-8%	-	+8	%
17	-	EMI input low-pass filter	Design Info	50	-	100	kHz

17.17.2 Squib leakage test (VRCM)

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V

Table 58. Squib Leakage Test (VRCM)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	V_{OUT_VRCM}	Output Voltage on SF or SR pins during Leakage test	I_{OUT} = 0 mA	-10%	2.5	+10%	V
2			I_{OUT} = 6.6 mA	1.9	-	2.5	V
3	$R_{LKG\_GSG\_TH}$	Detection threshold, leakage to GND	Leakage detected if R_{LKG_GSG} ≤ 1 kΩ and not detected if R_{LKG_GSG} ≥ 10 kΩ Design Info	1	-	10	kΩ
4a	$I_{LKG\_GSQ\_TH\_L}$		Equivalent to resistance range SYS_CTL(PD&VRCM_SEL) = 0 -25 °C ≤ T_j ≤ +150 °C guaranteed by design/characterization	-15.5 %	450	+15.5 %	µA
4b			Equivalent to resistance range SYS_CTL(PD&VRCM_SEL) = 0 -40 °C ≤ T_j ≤ +150 °C	-17%	450	+15.5 %	µA
5	$I_{LKG\_GSQ\_TH\_H}$		SYS_CTL(PD&VRCM_SEL) = 1	-15%	2	15%	mA
6	T_{FLT_LKG}	Leakage to GND deglitch filter time	-	17	20	23	µs
7	$R_{LKG\_BSQ\_TH}$	Detection threshold, leakage to battery	Leakage detected if R_{LKG_GSG} ≤ 1 kΩ and not detected if R_{LKG_GSG} ≥ 10 kΩ Design Info	1	-	10	kΩ
8a	$I_{LKG\_BSQ\_TH}$		Equivalent to resistance range -25 °C ≤ T_j ≤ +150 °C guaranteed by design/characterization	-12%	1.8	+15%	mA
8b			-40 °C ≤ T_j ≤ +150 °C	-17%	1.8	+15%	mA

Table 58. Squib Leakage Test (VRCM)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
9	T_{FLT_LKG}	Leakage to BAT deglitch filter time	-	17	20	23	µs
10	$I_{LIM\_VRCM\_SRC}$	VRCM current limitation	-	-20	-	-10	mA
11	$I_{LIM\_VRCM\_SINK}$		-	10	-	20	mA
12	V_{SHIFT}	External ground or battery shift	Design Info	-1	-	+1	V
13	$R_{SQ\_LOW\_TH}$	Detection threshold for “resistance too low”	Design Info	200	-	500	Ω
14a	$I_{RSQ\_LOW\_TH}$		Equivalent to resistance range -25 °C ≤ T_j ≤ +150 °C guaranteed by design/characterization	-12%	6	+12%	mA
14b			-40 °C ≤ T_j ≤ +150 °C	-17%	6	+12%	mA
15	T_{FLT_RLOW}	“Resistance too low” deglitch filter time	-	12	15	18	µs
16	R_{SQ_HIGH}	Detection Threshold for “resistance too high”	Design Info	2	-	5	kΩ
17a	I_{RSQ_HIGH}		Equivalent to resistance range -25 °C ≤ Tj ≤ +150 °C guaranteed by design/characterization	-17%	700	+17%	µA
17b			-40 °C ≤ Tj ≤ +150 °C	-17%	700	+22%	µA
18	T_{FLT_RHIGH}	“Resistance too high” deglitch filter time	-	12	15	18	µs
19	$T_{delay\_STG\_selection}$	Time needed to change the VRCM STG thresholds (450 µA-to-2 mA or 2 mA-to-450 µA)	guaranteed by design	-	-	2	µs

17.17.3 High/low side FET test

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0}(max) ≤ VIN ≤ 35 V, 6 V ≤ SSxy ≤ 35 V, 7 V ≤ SYNCBOOST ≤ 35 V.

Table 59. High/low side FET test

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	$I_{HS\_FET\_TH}$	Detection threshold high side FET test	-	-12%	1.8	+12%	mA
2	$I_{LS\_FET\_TH}$	Detection threshold low side FET test	SYS_CTL(PD&VRCM_SEL) = 0	-15.5%	450	+15.5%	µA
3	$I_{LS\_FET\_TH\_HIGH}$		SYS_CTL(PD&VRCM_SEL) = 1	-15%	2	+15%	mA
4	E_{FET_TEST}	Energy transferred to squib during HS/LS FET tests	Design Info	-	-	170	µJ
5	T_{DRIVER_DIS}	Driver Disable time	Guarantee by design	-	-	1.5	µs
6	$T_{TOT\_FETTEST\_ACTIVE}$	Total FET test activation time in case of no fault condition	Guarantee by design	-	-	4	µs
7	$T_{FETTIMEOUT}$	HS/LS FET test timeout	-	190	200	210	µs
8	$T_{FLT\_LKGB\_FT}$	Deglitch filter time during FET test on $I_{HS\_FET\_TH}$ / $I_{LS\_FET\_TH}$ current thresholds	-	0.8	1	1.2	µs
9	$I_{LIM\_HS\_FET}$	HS FET current in HS driver diagnostics	Not tested because of item # 1 in errata sheet	40	50	60	mA
10	$SGxy_{OPEN}$	Squib open ground detection	GNDSUBx as ground reference	300	450	600	mV
11	T_{FLT_SGOPEN}	Squib open ground detection filter time	-	46	50	54	µs

17.17.4 Deployment timer test

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V.

Table 60. Deployment timer test - AC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	t_{PULSE_PERIOD}	Deployment timer pulse test period time	SYSDIAGREQ(DSTEST)=PULSE	7	8	9	ms
2	I_{PULSE_HIGH}	Deployment timer pulse test high time		-	DCR_x(Deploy_Time)* $T_{DEP\_TIME\_RES}$	-	µs

17.18 Remote sensor interface

All electrical characteristics are valid for the following conditions unless otherwise noted:
40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V, $V_{SATBUCK}$(min) ≤ VSATBUCK, $V_{SYNCBOOST}$(min) ≤ VSYNCBOOST

17.18.1 PSI-5 interface

Table 61. PSI-5 satellite transceiver - DC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	I_{RSU}	Interface quiescent current	-	-35	-	-4	mA
2	V_{RSU_MAX}	Max. output voltage excluding sync. pulse	(internal regulation, VSATBUCK = VSYNCBOOST)	-	-	11	V
3	$V_{RSU\_SYNC\_MAX}$	Max. output voltage including sync. pulse	(internal regulation, VSYNCBOOST = VIN) Syncboost = 12 V, 14.75 V, 18 V and 35 V	-	-	16.5	V
4	R_{RSU}	RSU output resistance	From I_{RSU} = -4 mA to -65 mA	3	-	9.5	Ω
5	I_{STB_TH}	Static reverse current into SATBUCK or SYNCBOOST pin (V_{SUPPLY})	V_{RSUx} > V_{SUPPLY} + V_{RSU_STB}	0.0	-	10	mA
6	V_{RSU_STB}	Output short to battery threshold	-	10.0	-	100	mV
7	I_{OCTH_PSI5}	Over current detection threshold	Interface disabled after $T_{FLT\_OCTH\_PSI5}$	-130	-	-66	mA
8	I_{LIM_PSI5}	Output current limit	I_{RSUx}	-130	-	-80	mA
9	$\Delta I_{LIM\_OC\_PSI5}$	Difference between current limitation and OC threshold	ABS(I_{LIM_RSU}) - ABS(I_{OCTH_RSU})	1	-	-	mA
10	I_{BO}	Base current	Default value	-15%	-15	+15%	mA
11	I_{THGND}	Leakage to ground fault current detection	To ground; detected by I_B	-50.4	-42	-35	mA
12a	I_{THOPEN}	Output open load detection threshold	V_{RSUx} = open or leakage to battery -25 °C ≤ T_j ≤ +150 °C guaranteed by design/characterization	-3.5	-	-0.5	mA
12b			-40 °C ≤ T_j ≤ +150 °C	-3.9	-	-0.2	mA
13	I_{OL}	Output open load detection threshold	V_{RSUx} = open	I_{LKGB} (min)	-	I_{LKGB} (max)	mA
14	DAC_{RES}	DAC resolution	-	-	10	-	Bit
15	I_{LSB}	LSB current	Design Info	-	93.75	-	µA

Table 61. PSI-5 satellite transceiver - DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
16	V_{t2}	Sync pulse amplitude	I_{RSU} = 4 - 35 mA Referred to V_{RSUx} voltage before sync pulse Syncboost = 12 V, 14.75 V, 18 V and 35 V	3.8	-	-	V
17	$V_{SYNCDROP}$	Sync drop-out voltage	$V_{SYNCBOOST}$ - V_{RSUx}	1	-	-	V
18	$I_{LIM\_SYNC\_LS}$	Sync pulse current limit (LS driver)	-	50	-	80	mA
19	I_{LIM_SYNC}	Static current limitation for each transceiver output RSUx	During sync pulse generator $V_{RSUx=GND}$	-240	-	-120	mA
20	C_1	Capacitor on RSUx Regulator	22 nF nominal Design Info	13	-	-	nF
21	R_{E2}	RSU damping resistance	Design info	-	2.5	-	Ω
22	C_2	ECU pin capacitance	5 nF nominal Design Information, not tested	4	-	6	nF
23	-	Total number of sensors connected to bus	Design info	1	-	3	-

Table 62. PSI-5 satellite transceiver - AC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	T_{Bit_125k}	Bit time (125kbps mode)	At the sensor connector	7.6	8	8.4	µs
2	T_{Bit_189k}	Bit time (189kbps mode)	At the sensor connector	5	5.3	5.6	µs
3	$T_{FLT\_OCTH\_PSI5}$	Over Current Detection deglitch filter time	Normal operation	500	-	600	µs
4	$T_{BLK\_OCTH\_PSI5}$	Over Current Detection Blanking Time	At interface power on (BLKTxSEL = 0)	4.6	-	5.4	ms
5			At interface power on (BLKTxSEL = 1)	9.4	-	10.8	ms
6	T_{STBTH}	Reverse Battery Blocking Enable Time	-	12	-	16	µs
7	t_0	Reference time	@0.5 V on top of V(RSUx) Syncboost = 12 V, 14.75 V, 18 V and 35 V	-	0	-	-
8	t_1	Start delay time	From t_0 to SATSYNC Syncboost = 12 V, 14.75 V, 18 V and 35 V	-3	-	-	µs

Table 62. PSI-5 satellite transceiver - AC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
9	t_2	Sync signal sustain start	@ VRSU+3.8 V relative to t_0 Syncboost = 12 V, 14.75 V, 18 V and 35 V	-	-	7	µs
10	SR_{RISE_RSU}	Sync slope rising slew rate		0.43	-	1.5	V/µs
11	SR_{FALL_RSU}	Sync slope falling slew rate		-1.5	-	-	V/µs
12	t_3	Sync signal sustain time	Design Info	16	-	-	µs
13	t_4	Discharge time limit	Design Info	-	-	35	µs
14	T_{BLANK}	Decoder blanking time (decoding disabled)	Design Info	-	-	42	µs
15	T_{SYNC}	Time between two sync pulses	Design Info	400	500	-	µs
16	$T_{FLT\_PSI5\_HF}$	PSI5 Deglitch filter time	F = 189 kbaud Configurable by SPI (4bits)	1	-	2	µs
17	$T_{FLT\_PSI5\_LF}$	PSI5 Deglitch filter time	F = 125 kbaud Configurable by SPI (4bits)	1.5	-	2.5	µs
18	T_{ES_1}, T_{LS_1}	Message start time, Slot 1	Related to t0, Sensor Side, P8P-500-3L	44	-	58.6	µs
19			Related to t0, Sensor Side, P8P-500-3H	44	-	58.6	µs
20			Related to t0, Sensor Side, P8P-500-4H	44	-	58.6	µs
21			Related to t0, Sensor Side, P10P-500-3L	44	-	58.6	µs
22			Related to t0, Sensor Side, P10P-500-3H	44	-	58.6	µs
23			Related to t0, Sensor Side, P10P-500-4H	44	-	58.6	µs
24	T_{ES_2}, T_{LS_2}	Message start time, Slot 2	Related to t0, Sensor Side, P8P-500-3L	181.3	-	210.4	µs
25			Related to t0, Sensor Side, P8P-500-3H	181.3	-	210.4	µs
26			Related to t0, Sensor Side, P8P-500-4H	139.5	-	164.2	µs
27			Related to t0, Sensor Side, P10P-500-3L	181.3	-	210.4	µs
28			Related to t0, Sensor Side, P10P-500-3H	181.3	-	210.4	µs
29			Related to t0, Sensor Side, P10P-500-4H	139.5	-	164.2	µs

Table 62. PSI-5 satellite transceiver - AC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
30	$T_{\_ES\_3}$, $T_{\_LS\_3}$	Message start time, Slot 3	Related to t0, Sensor Side, P8P-500-3L	328.9	-	373.5	µs
31			Related to t0, Sensor Side, P8P-500-3H	328.9	-	373.5	µs
32			Related to t0, Sensor Side, P8P-500-4H	245.5	-	281.3	µs
33			Related to t0, Sensor Side, P10P-500-3L	328.9	-	373.5	µs
34			Related to t0, Sensor Side, P10P-500-3H	328.9	-	373.5	µs
35			Related to t0, Sensor Side, P10P-500-4H	245.5	-	281.3	µs
36	$T_{\_s1\_end\_open}$	Slot 1 End valid window, opening time	Related to t_0, Sensor Side, P8P-500-3L	107.2	-	127.6	µs
37			Related to t_0, Sensor Side, P8P-500-3H	82	-	99.4	µs
38			Related to t_0, Sensor Side, P8P-500-4H	82	-	99.4	µs
39			Related to t_0, Sensor Side, P10P-500-3L	121	-	142.8	µs
40			Related to t_0, Sensor Side, P10P-500-3H	91	-	109.4	µs
41			Related to t_0, Sensor Side, P10P-500-4H	91	-	109.4	µs
42	$T_{\_s1\_end\_closure}$	Slot 1 End valid window, closure time	Related to t0, Sensor Side, P8P-500-3L	151	-	174.6	µs
43			Related to t0, Sensor Side, P8P-500-3H	119.8	-	139.9	µs
44			Related to t0, Sensor Side, P8P-500-4H	119.8	-	139.9	µs
45			Related to t0, Sensor Side, P10P-500-3L	167.8	-	193	µs
46			Related to t0, Sensor Side, P10P-500-3H	131	-	152.5	µs
47			Related to t0, Sensor Side, P10P-500-4H	131	-	152.5	µs
48	$T_{\_s2\_end\_open}$	Slot 2 End valid window, opening time	Related to t0, Sensor Side, P8P-500-3L	231.6	-	264.9	µs
49			Related to t0, Sensor Side, P8P-500-3H	206	-	236.7	µs
50			Related to t0, Sensor Side, P8P-500-4H	168	-	194.9	µs
51			Related to t0, Sensor Side, P10P-500-3L	245.4	-	280.1	µs
52			Related to t0, Sensor Side, P10P-500-3H	215.5	-	246.7	µs
53			Related to t0, Sensor Side, P10P-500-4H	177.5	-	205	µs
54	$T_{\_s2\_end\_closure}$	Slot 2 End valid window, closure time	Related to t0, Sensor Side, P8P-500-3L	302.8	-	342.1	µs
55			Related to t0, Sensor Side, P8P-500-3H	271.6	-	308	µs
56			Related to t0, Sensor Side, P8P-500-4H	225.4	-	256.5	µs
57			Related to t0, Sensor Side, P10P-500-3L	319.6	-	360.5	µs
58			Related to t0, Sensor Side, P10P-500-3H	282.7	-	320	µs
59			Related to t0, Sensor Side, P10P-500-4H	236.5	-	260	µs

Table 62. PSI-5 satellite transceiver - AC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
60	$T_{\_s3\_end\_open}$	Slot 3 End valid window, opening time	Related to t0, Sensor Side, P8P-500-3L	365.1	-	412.5	µs
61			Related to t0, Sensor Side, P8P-500-3H	339.4	-	384.3	µs
62			Related to t0, Sensor Side, P8P-500-4H	263.9	-	300.9	µs
63			Related to t0, Sensor Side, P10P-500-3L	378.9	-	427.7	µs
64			Related to t0, Sensor Side, P10P-500-3H	348.5	-	394.3	µs
65			Related to t0, Sensor Side, P10P-500-4H	273	-	311	µs
66	$T_{\_s3\_end\_closure}$	Slot 3 End valid window, closure time	Related to t0, Sensor Side, P8P-500-3L	465.9	-	522.7	µs
67			Related to t0, Sensor Side, P8P-500-3H	434.7	-	488	µs
68			Related to t0, Sensor Side, P8P-500-4H	342.5	-	386.1	µs
69			Related to t0, Sensor Side, P10P-500-3L	482.7	-	541.1	µs
70			Related to t0, Sensor Side, P10P-500-3H	445.9	-	500	µs
71			Related to t0, Sensor Side, P10P-500-4H	353.7	-	398.2	µs
72	$T_{SYNC\_DLY\_SHORT}$	Sync Pulse Start Delay	SYS_CFG(RSU_SYNCPULSE_SHIFT_CONF)=0 Related to Start of Sync Pulse on ch. N-1	-	$\frac{160}{f_{osc}}$	-	µs
73	$T_{SYNC\_DLY\_LONG}$		SYS_CFG(RSU_SYNCPULSE_SHIFT_CONF)=1 Related to Start of Sync Pulse on ch. N-1	-	$\frac{288}{f_{osc}}$	-	µs
74	$T_{FLT\_OPEN\_RSU}$	Open Detection Deglitch Filter Time	-	10	-	15	µs
75	$T_{FLT\_LKG\_RSU}$	Leakage Deglitch Filter Time	-	10	-	15	µs
76	$T_{WRITE\_EN\_DELAY\_LF}$	Data register write delay	Design Info F = 125 kbaud Calculated from transition of last sensor bit to when data is available in SPI register	-	-	19	µs
77	$T_{WRITE\_EN\_DELAY\_HF}$		Design Info F = 189 kbaud Calculated from transition of last sensor bit to when data is available in SPI register	-	-	14	µs

17.19 DC sensor interface

All electrical characteristics are valid for the following conditions unless otherwise noted:
40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V, 8.5 V ≤ SYNCBOOST ≤ 35 V.

Table 63. DC Sensor interface specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	V_{OUT_DCSREG}	DCS output voltage regulation mode	DCS regulator enabled SyncBoost = 11.5 V and 35 V	-10%	6.25	+10 %	V
2	I_{LIM_DCSREG}	DCS current limitation regulation mode	DCS regulator enabled SyncBoost = 11.5 V and 35 V	24	27	30	mA
3	V_{DCS_RANGE1}	DCS voltage measurement range1	First voltage measurement (V_{DCS_MEAS1}) to compensate external ground shift and internal offset	-1	-	1.4	V
4	V_{DCS_ACC1}	DCS voltage measurement accuracy 1	V_{DCS} = V_{DCS_RANGE1} Included ADC error	-15	-	15	%
5	V_{DCS_RANGE2}	DCS voltage measurement range 2	-	1.5	-	10	V
6	V_{DCS_ACC2}	DCS voltage measurement accuracy 2	V_{DCS} = V_{DCS_RANGE2} Included ADC error	-8	-	+8	%
7	I_{DCS_RANGE1}	DCS Current measurement range 1	-	1	-	2	mA
8	I_{DCS_ACC1}	DCS current measurement accuracy 1	I_{DCS} = I_{DCS_RANGE1} Included ADC error	-30	-	+30	%
9	I_{DCS_RANGE2}	DCS current measurement range 2	-	2	-	22	mA
10	I_{DCS_ACC2}	DCS current measurement accuracy 2	I_{DCS} = I_{DCS_RANGE2} Included ADC error	-12	-	+12	%
11	I_{DCS_RANGE3}	DCS current measurement range 3	Regulator in current limitation	-	I_{LIM_DCSREG}	-	mA
12	I_{DCS_ACC3}	DCS Current measurement accuracy 3	V_{DCS} = 0V Included ADC error	-12	-	+12	%
13	R_{DCS_RANGE}	DCS resistance measurement range	Design info	65	-	3000	Ω
14	R_{DCS_ACC}	Accuracy of digital resistance measurement	Performing voltage measurements 1 and 2 After software calculation all errors included	-15	-	15	%

Table 63. DC Sensor interface specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
15a	$I_{PD\_DCS\_OFF}$	DCSx current pull down	$V_{DCS} \geq 1.5$ V All DCS channels OFF Not tested	70	100	130	µA
15b	I_{PD_DCS}		$V_{DCS} \geq 1.5$ V Pull-down current on all DCS channels but the one activated	160	200	250	µA
16	R_{PD_DCS}	DCSx resistance pull down	Device active, DCSx current pull down disabled	90	150	210	kΩ
17a	$I_{PD\_DCS\_TOT}$	DCSx total current pull down	$I_{PD\_DCS\_TOT} = I_{PD\_DCS\_OFF} + R_{PD\_DCS}$ $V_{DCS} = 6.5$ V All DCS channels OFF Not tested	80	140	220	µA
17b	I_{PD_DCS}		$I_{PD\_DCS\_TOT} = I_{PD\_DCS} + R_{PD\_DCS}$ $V_{DCS} = 6.5$ V Total Pull-down current on all DCS channel but the one activated.	180	240	320	µA
18	C_{DCS}	Output capacitance	Design Info	10	-	-	nF
19	I_{REF_DCS}	Internal Current Reference for DCS Current Measurement	-	-5%	300	+5%	µA
20	Ratio_VDCS	Divider ratio for DCSx voltage measurement	-	-3%	7.125	+3%	V/V
21	V_{OFF_DCS}	DCSx internal offset during voltage measurement	-	0.35	0.375	0.39	V

17.20 Safing engine

All electrical characteristics are valid for the following conditions unless otherwise noted:

40 °C ≤ Ta ≤ +95 °C, $VIN_{GOOD0} \leq VIN \leq 35$ V, VCCx(min) ≤ VCCx ≤ VCCx(max), VCC = 3.3 V or 5 V.

Table 64. Arming Interface – DC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	$V_{TH\_H\_ACL}$	ACL input voltage thresholds	-	2.33	-	2.5	V
2	$V_{TH\_L\_ACL}$		-	1.58	-	1.71	V
3	V_{HYS_ACl}	ACL hysteresis	-	0.6	0.75	0.9	V
4	R_{PD_ACL}	ACL pull down resistance	V_{ACL} = 3.3V	150	210	270	kΩ
5	V_{OH_ARM}	ARMx output high voltage	I_{LOAD} = -0.5 mA internal safing selected	VCC-0.60	-	VCC	V

Table 64. Arming Interface – DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
6	V_{OL_ARM}	ARMx output low voltage	I_{LOAD} = 2.0 mA internal safing selected	0	-	0.4	V
7	R_{PD_ARM}	ARMx pull down resistance	-	65	100	135	kΩ
8	V_{IH_ARM}	ARMx high level input voltage	-	2	-	-	V
9	V_{IL_ARM}	ARMx low level input voltage	-	-	-	0.8	V
10	$R_{PD\_ARMx,\ x=1,2,3}$	ARM1,2,3 pull down resistor	External safing selected	60	100	140	kΩ
11	V_{IH_FENL}	FENL high level Input Voltage	-	2	-	-	V
12	V_{IL_FENL}	FENL low level Input Voltage	-	-	-	0.8	V
13	I_{PU_ARM4}	ARM4 pull up current	ARM4 = 0V external safing selected	-100	-75	-50	µA
14	V_{OH_PSINHB}	PSINHB output high voltage	I_{LOAD} = -0.5 mA Internal safing selected	VCC-0.60	-	VCC	V
15	V_{OL_PSINHB}	PSINHB output low voltage	I_{LOAD} = 2.0 mA Internal safing selected	0	-	0.4	V
16	R_{PD_PSINHB}	PSINHB pull down resistance	-	65	100	135	kΩ
17	V_{IH_PSINHB}	PSINHB high level input voltage	-	2	-	-	V
18	V_{IL_PSINHB}	PSINHB low level input voltage	-	-	-	0.8	V
19	$V_{IH\_SAF\_CSx}$	SAF_CSx high level input voltage	-	2	-	-	V
20	$V_{IL\_SAF\_CSx}$	SAF_CSx low level input voltage	-	-	-	0.8	
21	$I_{PU\_SAF\_CSx}$	SAF_CSx pull up current	SAF_CSx = 0 V to $V_{IH\_SAF\_CSx(min)}$	-70	-45	-20	µA

Table 65. Arming interface – AC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	T_{ARM}	Sensor sampling period	-	475	500	525	µs
2	T_{ACL_HI}	ACL period time thresholds	-	213	-	237	ms
3	T_{ACL_LO}		-	168	-	187	ms
4	$T_{ON\_ACL\_HI}$	ACL on-time thresholds	-	154	-	171	ms
5	$T_{ON\_ACL\_LO}$		-	114	-	126	ms

Table 65. Arming interface – AC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
6	T_{VALID_ACL}	Scrap validation T_{ACL} and T_{ON_ACL} valid	-	3	-	-	cycles
7	$T_{INVALID\_ACL}$	Scrap invalid T_{ACL} invalid	-	2	-	-	cycles
8	$T_{SCRAP\_TIMEOUT}$	Scrap timeout timer	-	520	550	580	µs
9	f_{SCRAP_SEED}	Scrap seed counter frequency	-	-	$\frac{f_{osc}}{16}$	-	MHz
10	T_{PULSE_STRECH}	Arming enable pulse stretch time	-	-	-	0	ms
11			-	30	32	34	ms
12			-	242	-	270	ms
13			-	1934	-	2162	ms
14	T_{RISE_ARM}	ARMx rise time	50 pF load, 20% to 80% internal safing selected	-	-	1.00	µs
15	T_{FALL_ARM}	ARMx fall time		-	-	1.00	µs
16	T_{RISE_PSINHB}	PSINHB rise time		-	-	1.00	µs
17	T_{FALL_PSINHB}	PSINHB fall time		-	-	1.00	µs

17.21 General purpose output drivers

All electrical characteristics are valid for the following conditions unless otherwise noted:
40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35V, VGPODx + 5V ≤ VERBOOST.

Table 66. GPO interface DC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	$V_{SAT\_GPO\_L}$	Output saturation voltage	$V_{GPOD} - V_{GPOS}$ I_{LOAD} = 50 mA, ERBOOST = 35 V	-	-	0.5	V
2	$V_{SAT\_GPO\_H}$	Output saturation voltage	$V_{GPOD} - V_{GPOS}$ I_{LOAD} = 70 mA	-	-	0.7	V
3	I_{LIM_GPO}	Driver current limit	$V_{GPOD} - V_{GPOS}$ = 1.5 V ERBOOST = 35 V	73	110	160	mA
4	I_{OC_GPO}	Over current detection	ERBOOST = 35 V	73	110	160	mA
5	$V_{OUT\_GPOD\_OL}$	GPO diag OFF output voltage on GPOD in low side mode in open load condition	GPOxLS = 1 I_{OUT} = 0 mA	-10%	2.5	+10%	V
6	$V_{OUT\_GPOS\_OL}$	GPO diag OFF output voltage on GPOS in high side mode in open load condition	GPOxLS = 0 I_{OUT} = 0 mA	-10%	2.5	+10%	V
7	I_{SRC_TH}	GPO diag OFF state short to ground detection threshold	GPOxLS = 0 / 1	15	27	40	µA
8	$I_{SINK\_TH\_LS}$	GPO Diag OFF state short to battery detection threshold low side mode	GPOxLS = 1 GPOS = 0	15	27	46	µA
9	$I_{SINK\_TH\_HS}$	GPO Diag OFF state short to battery detection threshold high side mode	GPOxLS = 0	170	220	270	µA
10	$I_{LIM\_GPOD\_SRC}$	GPO Diag OFF state low side mode current limitation on GPOD	GPOxLS = 1, GPO Driver OFF, GPOD = 0 V, GPOS = 0 V	-90	-70	-50	µA
11	$I_{LIM\_GPOD\_SINK}$		GPOxLS = 1, GPO Driver OFF, GPOD = 18 V, GPOS = 0 V	50	70	90	µA
12	$I_{LIM\_GPOS\_SRC}$	GPO Diag OFF state high side mode current limitation on GPOS	GPOxLS = 0, GPO Driver OFF, GPOD = 18 V, GPOS = 0 V	-90	-70	-50	µA
13	$I_{LIM\_GPOS\_SINK}$		GPOxLS = 0, GPO driver OFF, GPOD = 18 V,GPOS = 18 V	320	400	480	µA
14	I_{OL_GPO}	Open load current threshold	GPO driver ON	0.5	1	3	mA

Table 66. GPO interface DC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
15	I_{DIAG_GPO}	Diagnostic current on load	Voltage measurement in progress through Analog MUX Increased leakage for a short specified time (32 µs)	-	-	130	µA
16	$I_{LKG\_GPOD\_OFF}$	GPOD output leakage current	V_{GPOD} = 18 V V_{GPOS} = 0 V, ERBOOST = 35 V Power-off or Sleep Mode	-5	-	+5	µA
17	$I_{LKG\_GPOD\_ON}$		V_{GPOD} = 18 V V_{GPOS} = 0 V, ERBOOST = 35 V GPO Driver OFF Active or Passive Mode with GPO un-configured	-5	-	+5	µA
18	$I_{LKG\_GPOS\_OFF}$	GPOS output leakage current	V_{GPOD} = 18 V V_{GPOS} = 0 V, ERBOOST = 35 V Power-off or Sleep Mode	-5	-	+5	µA
19	$I_{LKG\_GPOS\_ON}$		V_{GPOD} = 18 V V_{GPOS} = 0 V, ERBOOST = 35 V GPO Driver OFF Active or Passive Mode with GPO un-configured	-5	-	+5	µA
20	I_{REV_GPO}	Reverse current	V_{GPOS} = V_{GPOD} + 1 V GPO Driver OFF	-	-	1	mA
21	T_{JSD_GPO}	Thermal shutdown	-	150	175	190	°C
22	$T_{HYS\_TSD\_GPO}$		-	5	10	15	°C
23	C_{GPO}	Load capacitor	Design Info	6	-	-	nF

Table 67. GPO driver interface – AC specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	SR_{GPOx}	GPOx output voltage slew rate	30% - 70%; R_{LOAD} = 273 Ω, C_{LOAD} = 100 nF	0.1	0.25	0.4	V/µs
2	T_{FLT_OC}	Over current detection filter time	GPO Driver ON	10	12	14	µs
3	T_{FLT_UC}	Open load detection filter time	GPO Driver ON	8	10	12	µs
4	T_{FLT_STB}	Short to battery detection in OFF state deglitch filter time	GPO Driver OFF	8	10	15	µs
5	T_{FLT_STG}	Short to GND detection in OFF state deglitch filter time	GPO Driver OFF	8	10	15	µs

Table 67. GPO driver interface – AC specifications (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
6	$T_{MASK\_STUP\_ON}$	Diagnostic mask delay after switch ON	C_{GPOX} = 100 nF typ	136	-	200	µs
7	$T_{MASK\_STUP\_OFF}$	Diagnostic mask delay after switch OFF	C_{GPOX} = 100 nF typ	520	-	584	µs
8	T_{FLT_TSD}	Thermal shutdown filter time	-	-	-	10	µs
9	F_{PWM}	GPO PWM frequency	Design Info	-	125		Hz
10	DC_{PWM}	GPO PWM duty cycle	Increment step = 1.6%	0	-	100	%

17.22 ISO9141 Interface (K-LINE)

All electrical characteristics are valid for the following conditions unless otherwise noted:

40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V.

Table 68. ISO9141 interface DC specifications

N°	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	V_{IH_ISOTX}	ISOTX high level input voltage	-	2	-	-	V
2	V_{IL_ISOTX}	ISOTX low level input voltage	-	-	-	0.8	V
3	V_{HYS_ISOTX}	ISOTX hysteresis input voltage	-	150	-	500	mV
4	I_{PU_ISOTX}	ISOTX pull up current	ISOTX = 0	-70	-45	-20	µA
5	C_{IN_ISOTX}	ISOTX input capacitance	Design Info	-	-	5	pF
6	$V_{TH\_DOM\_ISOK}$	ISOK Input Receiver Threshold	ISOTX = 0V	VIN * 0.4	VIN * 0.45	VIN * 0.5	V
7	$V_{TH\_REC\_ISOK}$		ISOTX = VDDQ	VIN * 0.5	VIN * 0.55	VIN * 0.6	V
8	V_{HYS_ISOK}		-	VIN * 0.07	VIN * 0.1	VIN * 0.13	V
9	$V_{O\_DOM\_ISOK}$	ISOK Output Voltage	ISOTX = 0V, I_{ISOK} = 40mA	-	-	1.2	V
10	I_{OC_ISOK}	ISOK Over Current Detection	-	50	-	100	mA
11	I_{LIM_ISOK}	ISOK Current Limitation	-	50	-	100	mA
12	$\Delta I_{LIM\_OC\_ISOK}$	Difference between Current Limitation and OC Threshold	I_{LIM_ISOK} - I_{OC_ISOK}	0.1	-	-	mA

Table 68. ISO9141 interface DC specifications (continued)

N°	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
13	I_{SINK_ISOK}	ISOK sink current capability	Design Info	40	-	-	mA
14	I_{LKG_ISOK}	ISOK input leakage current	VIN < 18V, Driver Off (device is supplied)	-10	-	10	µA
15	V_{OH_ARM}	ISORX output high voltage	I_{LOAD} = -0.5 mA	VDDQ -0.60	-	VDDQ	V
16	V_{OL_ARM}	ISORX output low voltage	I_{LOAD} = 2 mA	0	-	0.4	V
17	C_{IN}	ISOK input capacitance	-	-	-	10	pF
18	T_{JSD_ISOK}	Thermal shutdown	-	150	175	190	°C
19	$T_{HYS\_TSD\_ISOK}$		-	5	10	15	°C

Table 69. ISO9141 interface transceiver AC specifications

N°	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	T_{FLT_TSD}	Thermal shutdown filter time	-	-	-	10	µs
2	T_{BLK_ISOK}	Current limit fault blanking time	-	8	-	12	µs
3	T_{RISE_ISORX}	ISORX rise time	80pF load, 20%-80%	-	-	0.5	µs
4	T_{FALL_ISORX}	ISORX fall time	80pF load, 20%-80%	-	-	0.5	µs
5	-	Baud rate	Design Info	-	62.5	-	kBd
6	T_{PD_ILTX}	Propagation delay transmitter	ISOTX High to Low to ISOK = 70% * $V_{O\_REC\_ISOK}$ R_{ISOK} = 510 Ω, C_{ISOK} = 470 pF	-	-	1	µs
7	T_{PD_IHTX}		ISOTX Low to High to ISOK = 30% * $V_{O\_DOM\_ISOK}$ R_{ISOK} = 510 Ω, C_{ISOK} = 470 pF	-	-	1.5	µs
8	T_{PD_ILRX}	Propagation delay receiver	ISOK = $V_{TH\_DOM\_ISOK}$ to ISORX High to Low R_{ISOK} = 510 Ω, C_{ISOK} = 470 pF	-	-	1.5	µs
9	T_{PD_IHRX}		ISOK = $V_{TH\_REC\_ISOK}$ to ISORX Low to High R_{ISOK} = 510 Ω, C_{ISOK} = 470 pF	-	-	1.5	µs
10	T_{RISE_ISOK}	ISOK rise time	30% to 70% RISOK = 510 Ω, CISOK = 470 pF	-	-	1.5	µs

Table 69. ISO9141 interface transceiver AC specifications (continued)

N°	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	T_{FALL_ISOK}	ISOK fall time	70% to 30% RISOK = 510 Ω, CISOK = 470 pF	-	-	1.5	µs
12	T_{PDW_RX}	Receiver pulse width symmetry	T_{PD_ILRX} - T_{PD_IHRX}	-	-	1	µs
13	T_{PDW_TX}	Transmitter pulse width symmetry	$(T_{PD\_ILTX} + T_{FALL\_ISOK}) - (T_{PD\_IHTX} + T_{RISE\_ISOK})$	-	-	1	µs

17.23 Analog to digital converter

All electrical characteristics are valid for the following conditions unless otherwise noted:

40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V.

Table 70. Analog to digital converter

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	V_{ADC_RANGE}	ADC input voltage range	-	0.1	-	2.5	V
2	V_{ADC_REF}	ADC reference voltage	-	-1.5%	2.5	+1.5%	V
3	ADC_RES	ADC resolution (1)	Design Info	-	10	-	bit
4	DNL	Differential non linearity error (DNL)	Separation between adjacent levels, measured bit to bit of actual and an ideal output step. No missing codes	-1	-	+1	LSB
5	INL	Integral non linearity error (INL)	Maximum difference between the actual analog value at the transition between 2 adjacent steps and its ideal value	-3	-	+3	LSB
6	E_{QUANT}	Quantization error	Design Info	-0.5	-	0.5	LSB
7	TotErr	Total error	Includes INL, DNL, ADC Reference voltage tolerance and quantization error	-15	-	+15	LSB
8	TotErr_0v1	ADC total error for 0.1 V input voltage	-	-5	-	+5	LSB
9	TotErr_2v4	ADC total error for 2.4 V input voltage	-	-15	-	+15	LSB
10	R_{LSB_1}	Reproducibility: conversion result variation for constant input signal	1x sampling measurements. Guaranteed by design	-6	-	6	LSB
11	R_{LSB_4}		4x sampling measurements. Guaranteed by design	-3	-	3	LSB
12	R_{LSB_8}		8x sampling measurements. Guaranteed by design	-2.5	-	2.5	LSB
13	Pre-ADC	Pre-ADC settling time	-	-	4.81	-	µs

Table 70. Analog to digital converter (continued)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
14	T_TSC	Single conversion time	-	-	2.25	-	µs
15	IQ	Intra-queue settling time	-	-	3.5	-	µs
16	Post-ADC	Post- ADC settling time	-	-	3.44	-	µs
17	-	ADC conversion time - voltage	4x sampling for each of the 4 conversions in the queue Design Info	-	54.75	-	µs
18	-	ADC conversion time – current and voltage	8x sampling for DCS, temperature and squib loop resistance measurements + 4x sampling for remaining 2 conversions in the queue Design Info	-	51.25	-	µs

1. LSB = (2.5V / 1024) = 2.44mV

17.24 Voltage diagnostics (Analog MUX)

All electrical characteristics are valid for the following conditions unless otherwise noted:

40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35V.

Table 71. Voltage diagnostics (Analog MUX)

No	Symbol	Parameter	Conditions	Min	Typ	Max	Units
1	Ratio_1	Divider ratios	$V_{IN\_RANGE\_1}$ = 0.1 V to 2.5 V	-	1	-	V/V
2	Ratio_4		$V_{INPUT\_RANGE\_4}$ = 1 V to 10 V	-3%	4	+3%	V/V
3	Ratio_7		$V_{INPUT\_RANGE\_7}$ = 1.5V to 17.5V	-3%	7	+3%	V/V
4	Ratio_10		$V_{INPUT\_RANGE\_10}$ = 2 V to 25 V	-3%	10	+3%	V/V
5	Ratio_15		$V_{INPUT\_RANGE\_15}$ = 3 V to 35 V	-3%	15	+3%	V/V
6	Offset	Divider Offset	High impedance	-10	-	10	mV
7	R_{RATIO_4}	Multiplexer input resistance	Multiplexer input to GNDA	80	-	-	kΩ
8	R_{RATIO_7}		Multiplexer input to GNDA	120	-	-	kΩ
9	R_{RATIO_10}		Multiplexer input to GNDA	160	-	-	kΩ
10	R_{RATIO_15}		Multiplexer input to GNDA	200	-	-	kΩ
11	$I_{LEAK\_MUX\_ON}$	Additional multiplexer on-state input leakage current	For all divider ratio expect ratio_1	-	-	60	µA
12	V_{MEAS_ACC}	Voltage measurement Accuracy	(± 15 LSB) plus divider error (± 3%)				

17.25 Temperature sensor

All electrical characteristics are valid for the following conditions unless otherwise noted:

40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD0} ≤ VIN ≤ 35 V.

Table 72. Temperature sensor specifications

No	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	T_{MON_RANGE}	Monitoring temperature range	-	-40	-	150	°C
2	T_{MON_ACC}	Monitoring temperature accuracy	-	-15	-	15	°C

18 Quality information

18.1 OTP memory

The device contains a 128-bits One-Time Programmable memory. This OTP memory is used for the following purposes:

1. 86 bits data + 3 bits CRC for critical parameters trimming: bandgaps, oscillators, reference currents, firing currents, DC sensor and RSU interface parameters.
2. 18 bits data for other blocks trimming: ADC, ER Cap Measurement
3. 20 bits data for die and wafer traceability
4. 1 bit for debug purpose

User read/write access to the OTP memory via SPI is only possible during production testing and require activation of a special test mode.

During mission mode, the trimming bits are automatically read from OTP and transferred to the related circuits at each POR cycle. During this operation, actual CRC of the protected trimming data is calculated and checked against the expected CRC stored in the OTP. In case of CRC check failure the OTPCRC_ERR flag is set in the FLTSR register.

19 Errata sheet

Table 73. Errata sheet

#	Component Revision	Category / Function	Issue Description
1	L9679BB	Deployment Diagnostic	The high side driver diagnostic, described in section *on page 167*, doesn't work. As consequence, the $I_{LIM\_HS\_FET}$ parameter is not tested in production.
2	L9679BB	Safing engine	The safing records associated with CS_RS validate and process data with matching request/response masks even if these are not coming from CS_RS frames but from frames sniffed on SAF_CSx. This may lead to issues when expansion chip is used and CS_RS frames sent on expansion are sniffed by SAF_CSx at SBC side; the SBC fails to check its own CS_RS and therefore all RSUs safing records CC with matching request/response masks of expansion RSUs safing records will be updated upon the processing of the expansion RSU SPI data. Workaround: use two different values for WID SPI bit when addressing CS_RS at SBC (ie WID=1) and expansion (WID=0) side.

20 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

20.1 TQFP100 (14x14x1.4 mm exp. pad down) package information

Figure 72. TQFP100 (14x14x1.4 mm exp. pad down) package outline

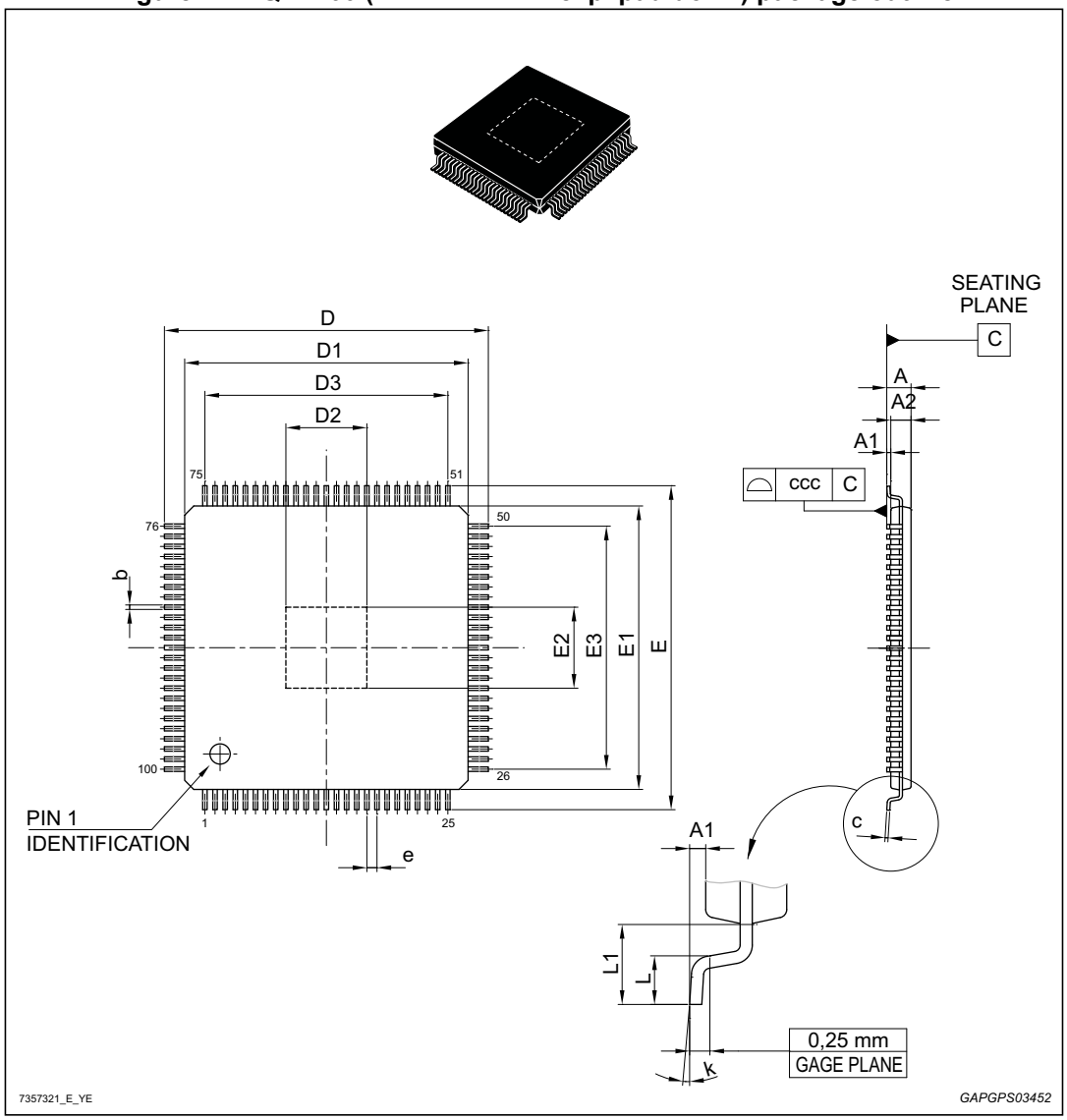


Table 74. TQFP100 (14x14x1.4 mm exp. pad down) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.20	-	-	0.0472
A1	0.05	-	0.15	0.0020	-	0.0059
A2	0.95	1.00	1.05	0.0374	0.0394	0.0413
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	-	0.20	0.0035	-	0.0079
D	15.80	16.00	16.20	0.6220	0.6299	0.6378
D1	13.80	14.00	14.20	0.5433	0.5512	0.5591
D2[2]	5.40	-	8.50	0.2126	-	0.3346
D3	-	12.00	-	-	0.4724	-
E	15.80	16.00	16.20	0.622	0.6299	0.6378
E1	13.80	14.00	14.20	0.5433	0.5512	0.5591
E2[2)]	5.40	-	8.50	0.2126	-	0.3346
E3	-	12.00	-	-	0.4724	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
k	-	3.50	7.00	-	0.1378	0.2756
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The size of exposed pad is variable depending of lead frame design pad size. End user should verify “D2” and “E2” dimensions for each device application.

21 Revision history

Table 75. Document revision history

Date	Revision	Changes
03-May-2016	1	Initial release.
08-Oct-2018	2	– Updated *Figure 2: Device function block diagram on page 23*; – Modified description of the bullet *SSM_RESET on page 50*; – Corrected in *Section 7.3.28* register “RES_MEAS_CHSEL[3:0]” for “0100” from “unused” to “ER cap ESR measure”; – Fixed condition of parameter ΔILIM_OC_PSI5; – Updated *Section 17.21: General purpose output drivers* and *Table 66: GPO interface DC specifications*; – Changed min value of VOH_RESET parameter; – Fixed description in *Section 8.1.2: Deploy command expiration timer*; – Added ISRC_DELTA parameter; – Fixed description in *Section 6.12: Reset control* added min and max values of oscillator Frequency Detection Threshold parameters; – Fixed description for ERSWITCH_LIM_SEL bit in SYS_CTL spi register; – Fixed min value of IPD_VSF_TOT parameter; – Improved ESR ER CAP diagnostic description in *Section 6.5.2: ER CAP ESR measurement*; – Added delta VBgood2 – VBbad2 parameter; – Removed VMEAS_ACC parameter; – Added VSR_CLAMP parameter; – Updated *Figure 10: IC operating state diagram*; – Changed description in *Section 9.1.1: Functional description* to specify better when data registers are updated; added in parameters section TWRITE_EN_DELAY_LF and TWRITE_EN_DELAY_HF; – Replaced 6 bits with 2 bits for deploy expiration timer configuration in *Section 8.1.2: Deploy command expiration timer*; – Updated “CSx[2:0] 100 in *Section 7.3.55: Safing control x registers (SAF_CONTROL_x)*; – Added parameters to specify soft start of erboost and syncboost in *Table 36: ERBoost regulator AC specifications* and *Table 45: SYNCBOOST converter AC specifications*; – Added block diagram of ADC Mux in *Section 15: System voltage diagnostics*; – Added total Voltage Measurement Accuracy in *Table 71: Voltage diagnostics (Analog MUX)*; – Fixed description in *Section 5.2: Deployment drivers*; – Improved the power supply sequences; – Changed AMR of SR pin from 40 V to 35 V; – Added some additional test conditions in electrical tables; – Improved description of PSI5 time slot control. – *Table 73: Errata sheet on page 268*.

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