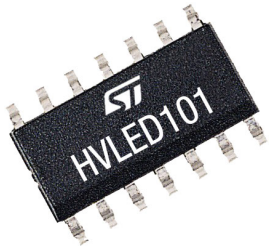
HVLED101

Data brief

Advanced high power factor flyback controller with valley locking and maximum power control



Product status link
HVLED101

Product summary		
Order code	**Package**	**Packaging**
HVLED101	SOP14	Tube
HVLED101TR		Tape and reel

Features

- Quasi-Resonant (QR) topology
- Primary side regulation of output voltage
- Direct optocoupler connection for secondary side regulated loop
- High power factor and low THD in universal and extended range (PF> 0.9 and THD < 5% @ full load and < 10% @ 1/3 load)
- 800 V fast high-voltage startup
- Extremely low input power at no-load and standby conditions
- Integrated input voltage detection for high power factor capabilty, DC rail detection and protection triggering
- Programmable frequency foldback with valley locking for noise free operation
- Programmable brownout and input overvoltage protection
- Latch-free device guarantee by smart Auto Restart Timer (ART)
- Input pin for remote protection with NTC management (threshold hysteresis and linearization)

Application

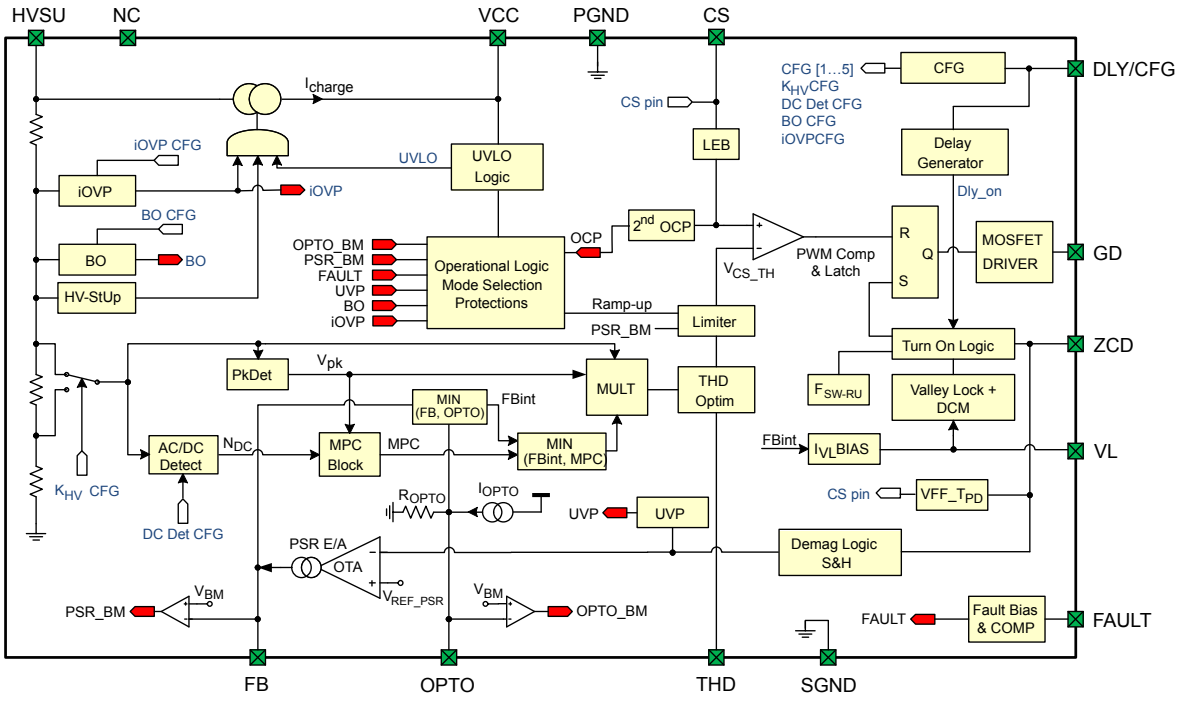
- Single-stage LED drivers with high power factor up to 180 W
- Two-stage LED drivers up to 200 W

Description

The HVLED101 is an enhanced peak current mode controller able to control mainly high power factor (HPF) flyback or buck-boost topologies having an output power up to 180 W. Some other topologies, like buck, boost and SEPIC could also be implemented. Primary Side Regulation of output voltage and Optocoupler control can be applied independently on the chip both exploiting precise regulation and very low standby power during no-load conditions. The innovative ST high-voltage technology allows to directly connect the HVLED101 to the input voltage in order to both start up the device and monitor the input voltage without the need of external components. Abnormal conditions like open circuit, output short-circuit, input overvoltage or undervoltage, external protection circuitries and circuit failures like open loop and overcurrent of the main switch are effectively controlled. A smart Auto Restart Timer (ART) function is built in to guarantee an automatic application recover, without any loss of reliability.

1 Block diagram

Figure 1. **Block diagram**



2 Pin connection and description

Figure 2. **Device pinout**

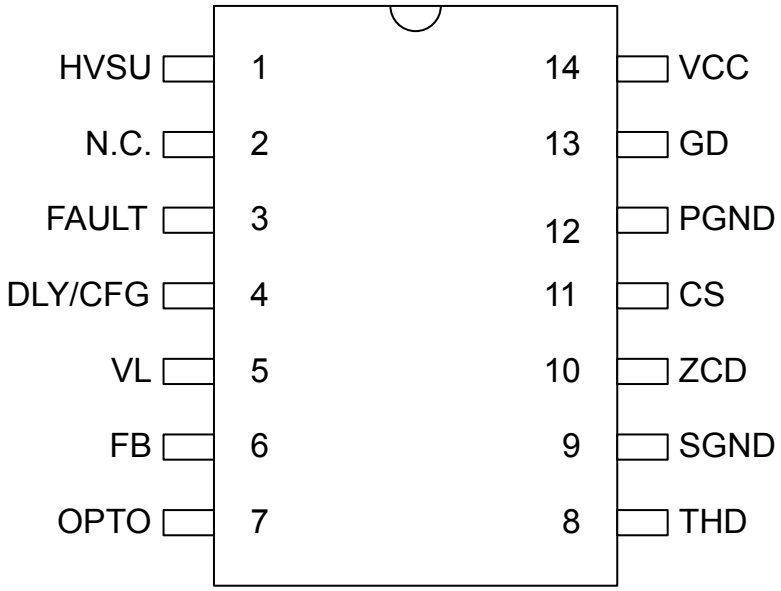


Table 1. **Pin description**

Symbol	Pin	Description
HVSU	1	High-voltage startup and input voltage detection. The pin, able to withstand 800 V, is to be connected to either the DC side of the input rectifier bridge, using a low value resistor (1 kΩ typ), or the AC side of a rectifier bridge with two diodes. It embeds the internal startup unit that quickly charges the capacitor connected between VCC pin and PGND pin during startup and low consumption. During operational mode, this pin measures the input voltage to obtain high power factor and to detect both input overvoltage and undervoltage, according to protection configuration, selected on the DLY/CFG pin.
N.C.	2	Not connected pin for clearance.
FAULT	3	This pin is intended to stop the IC when either the voltage goes below an internal threshold or the pin is left floating. It is suitable to supply an NTC thermistor. The hysteresis of lower disable threshold results in a thermal hysteresis when NTC is connected. When the functionality is unused, connect a 33 kΩ resistor between FAULT pin and SGND.
DLY/CFG	4	The parallel of a resistor and a capacitor is connected between this pin and SGND pin: the value of the resistance sets the delay time between ZCD detection and MOSFET turn-on, while the time constant of the RC network selects the input detection configuration and protection. Recommended values ranges are 22 ÷ 560 kΩ for R and 10 pF ÷ 100 nF for C.
VL	5	The voltage applied to this pin controls valley locking and frequency fold-back operation. It is internally biased with a current that is proportional to the minimum between the voltages that are present at the FB pin and at the OPTO pin (the internal FB_{int} signal). The level of the frequency fold-back depth is set by a resistor connected to SGND. A capacitor between the VL pin and SGND can be used to filter the fluctuations of FB_{int} signal.
FB	6	Output of the primary side regulation error amplifier (OTA). The pin must be connected to the compensation network for Primary Side Regulation. The voltage present at this pin also controls adaptive burst-mode (deep low consumption mode) and is internally connected to the multiplier, together with OPTO pin voltage and MCP voltage in an “OR-ed” structure.

Symbol	Pin	Description
OPTO	7	This pin is intended to be directly connected to the collector of the optocoupler or to the output of the error amplifier of a non-isolated topology: a pull-up current together with gain resistance is embedded in this pin. The OPTO pin voltage is internally connected to the multiplier, together with FB pin voltage and MCP voltage in an “OR-ed” structure. Deep low consumption mode is invoked pulling this pin lower than the V_{BM} threshold that features as burst-mode level when OPTO is used.
THD	8	A ceramic capacitor is placed between this pin and SGND to set the time constant of the THD optimizer unit. It is strongly recommended to use small package ceramic capacitors, placed as close to the above mentioned pins as possible, to avoid any undesired noise injection.
SGND	9	Reference pin for signal’s ground potential.
ZCD	10	Multiple function pin able to detect the zero current instant, to sense the output voltage for primary side regulation (PSR) and to compensate the peak current detection propagation delay (VFF). The delay time between zero current instant detection and MOSFET turn-on is programmed by the resistance between DLY/CFG pin and SGND. An internal starter unit is active to generate the triggering signal when not externally available (for example, at startup). Valley skipping counter is fed by internal ZCD signal processor. Adaptive minimum turn-off time (for example, the blanking after turn-on), larger during UVP condition, is implemented.
CS	11	Input of the current sense comparator for the power regulation. The current sense resistor (R_{CS}, from primary MOSFET source to ground) must be connected to this pin through a series resistance (RFF): this resistor is fed by an internal current, proportional to ZCD pin current during MOSFET on time interval, that creates the offset to compensate for the PWM comparator propagation delay. A leading-edge blanking time avoids false triggering of the MOSFET’s turn-off due to the noise that may be generated after gate driver turn-on.
PGND	12	Reference pin for VCC and gate driver.
GD	13	Gate driver output. The output stage is suitable to directly drive power MOSFETs. An internal pulldown resistor aims to keep the MOSFET off during low power operating modes.
VCC	14	Supply voltage of the IC. Internal UVLO logic prevents the operation at voltages that are insufficient for an efficient gate driving or internal signal processing. Both a bulk capacitor (typically around 22 µF) and a high frequency filter capacitor (100 nF ceramic, mounted as close to the device as possible) should be connected between this pin and PGND.

3 Typical application schematics

Figure 3. **HVLED101 typical PSR application**

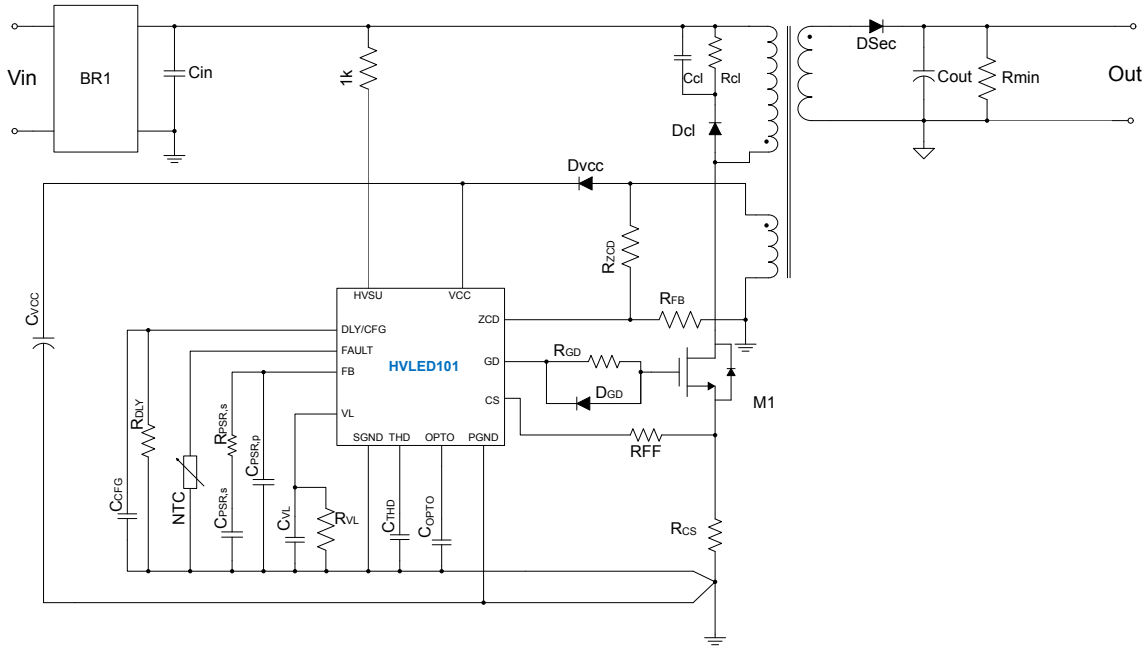
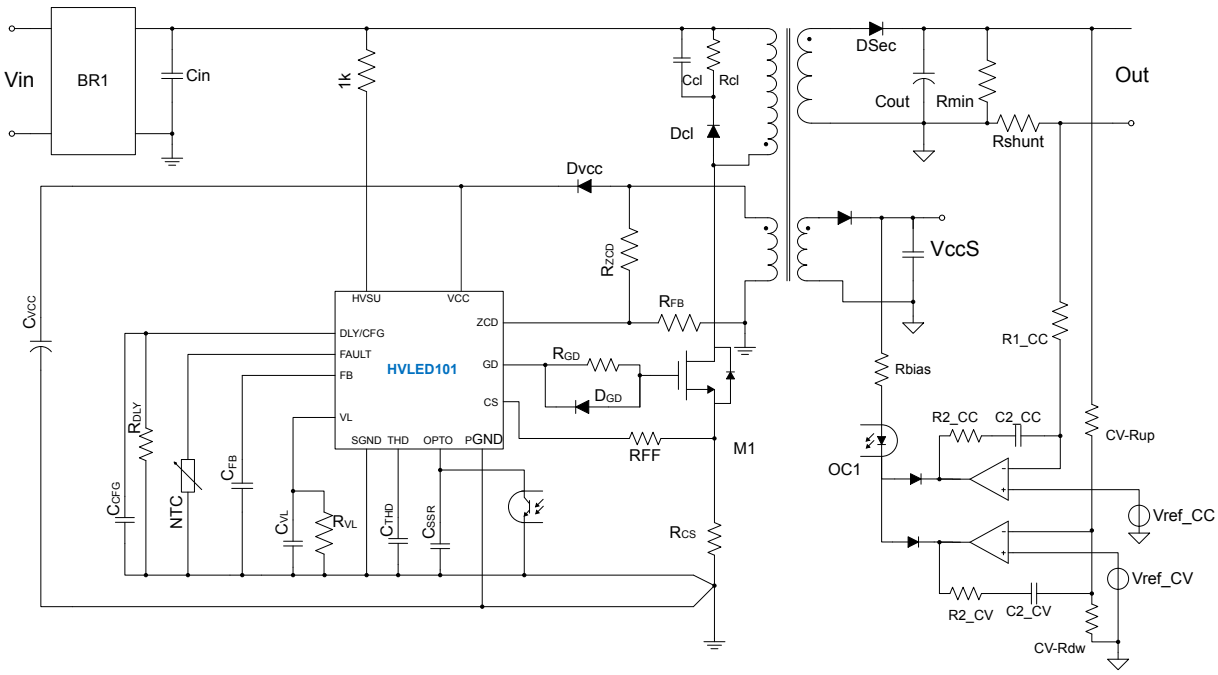


Figure 4. **HVLED101 typical SSR application**



4 Package mechanical data

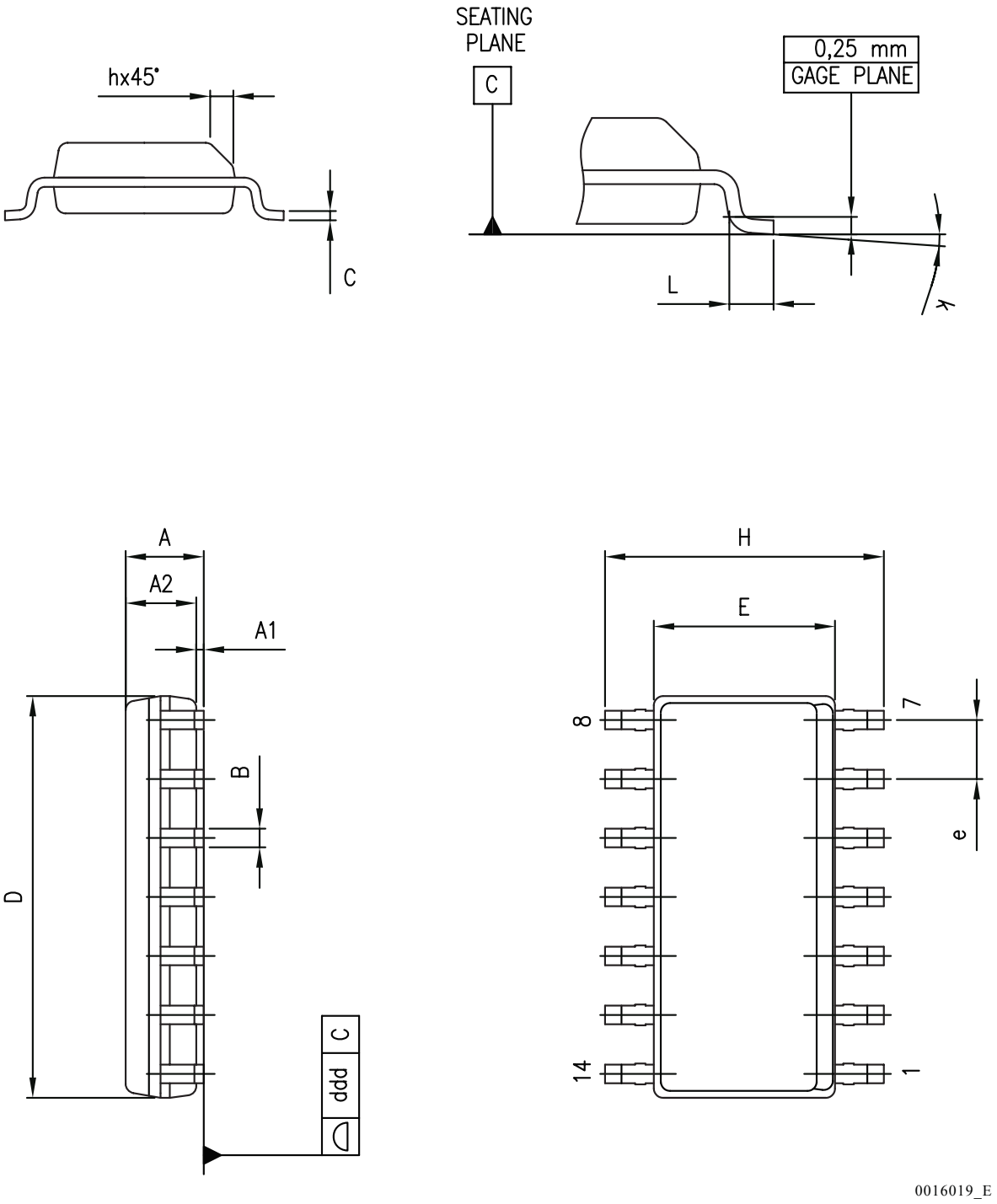
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com.

ECOPACK is an ST trademark.

Table 2. SOP14 mechanical data

Dimensions	mm		
	Min.	Typ.	Max.
A	1.350		1.750
A1	0.100		0.250
A2	1.100		1.650
B	0.330		0.510
C	0.190		0.250
D	8.550		8.750
E	3.800		4.000
e		1.270	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0d		8d
ddd			0.100

Figure 5. **Package dimensions**



Revision history

Table 3. **Document revision history**

Date	Version	Changes
25-Nov-2022	1	Initial release.

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HVLED101TR