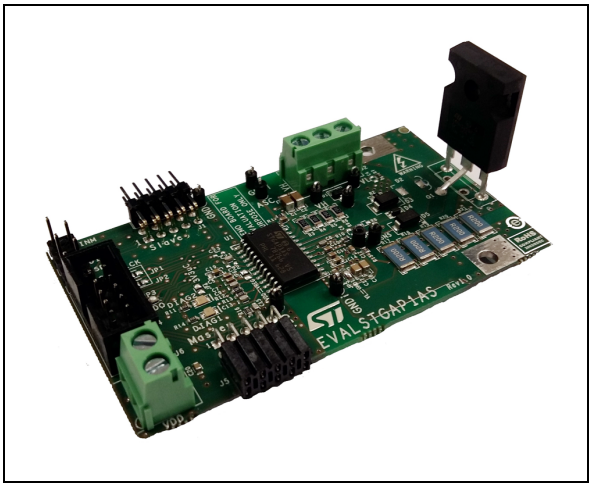
EVALSTGAP1AS

Demonstration board for STGAP1AS galvanically isolated single gate driver

Data brief



Features

- High voltage rail up to 1500 V
- 5 A sink/source driver current capability
- 5 A active Miller clamp
- Gate driving voltage up to 36 V
- Negative gate driving ability
- Desaturation detection
- Overcurrent protection
- Output 2-level turn-off (2LTO) UVLO on each supply voltage
- Overtemperature warning and shut-down protection
- 3.3/5 V logic input interface
- Optimized reference layout
- SPI with daisy chain feature for parameters programming and diagnostic
- Suitable to be used in combination with STEVAL-PCC009V2 and configuration GUI
- Fault LED indicators
- RoHS compliant

Description

The STGAP1AS is a galvanically isolated single gate driver for N-channel MOSFETs and IGBTs with advanced protection, configuration and diagnostic features. The architecture of the STGAP1AS isolates the channel from the control and the low voltage interface circuitry through true galvanic isolation.

The EVALSTGAP1AS board allows evaluating all of the STGAP1AS features while driving a power switch with a voltage rating up to 1500 V. Power switches in both TO-220 or TO-247 packages can be evaluated, and the board allows the connection of a heatsink in order to exploit the ability of the STGAP1AS to handle very high power applications.

In combination with the STEVAL-PCC009V2 communication board and the STGAP1AS evaluation software, the board allows to easily enable, configure or disable all of the driver's protection and control features through the SPI interface. Advanced diagnostic is also available thanks to the driver's status registers that can be accessed through the SPI.

Multiple boards can be connected together and share the same logic supply voltage and control signals in order to evaluate half-bridge, interleaved or even more complex topologies. The board allows implementing the SPI daisy chain when more than one device is used.

Schematic diagrams

Figure 1. EVALSTGAP1AS circuit schematic – connectors and configuration jumpers

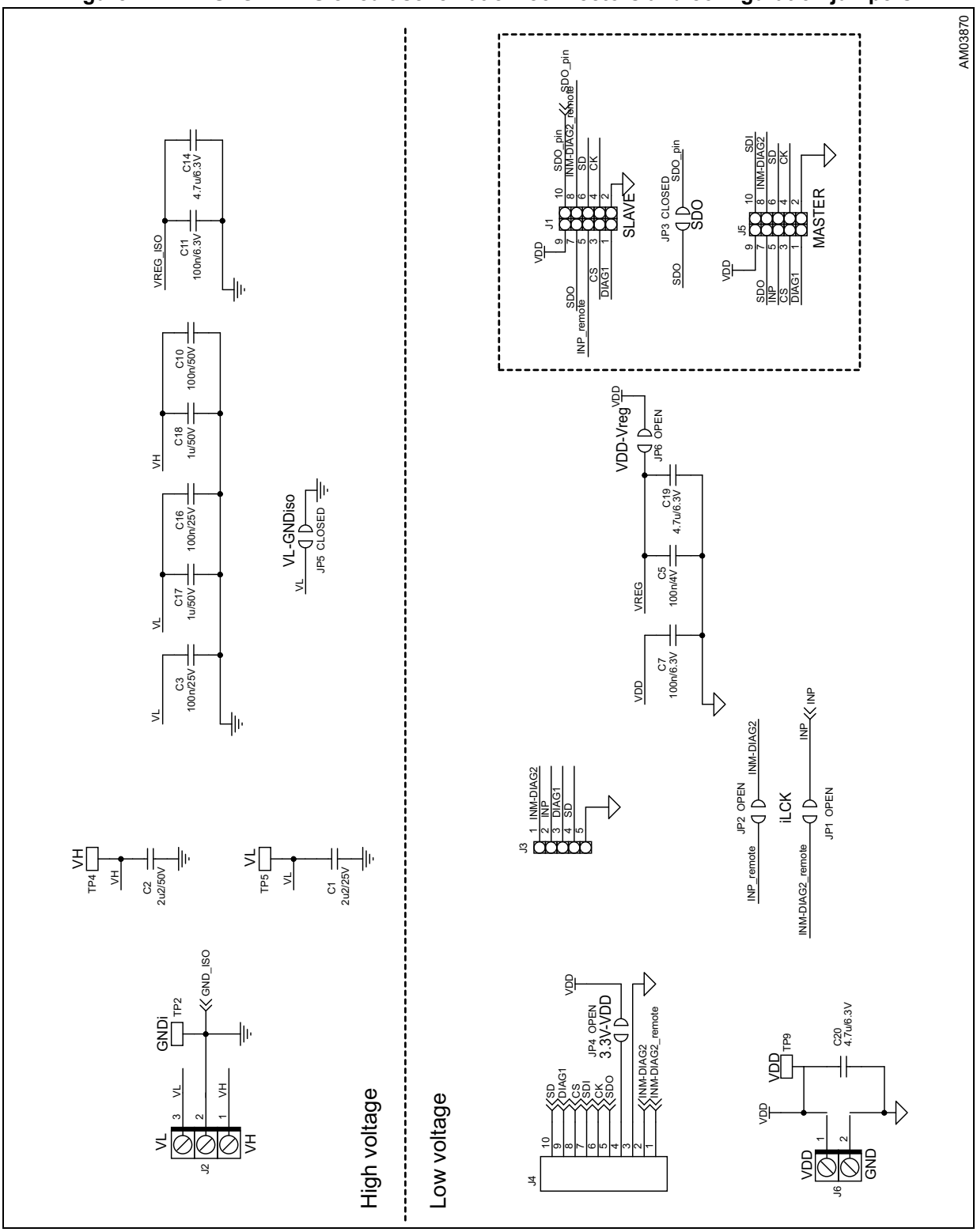


Figure 2. EVALSTGAP1AS circuit schematic – power stage

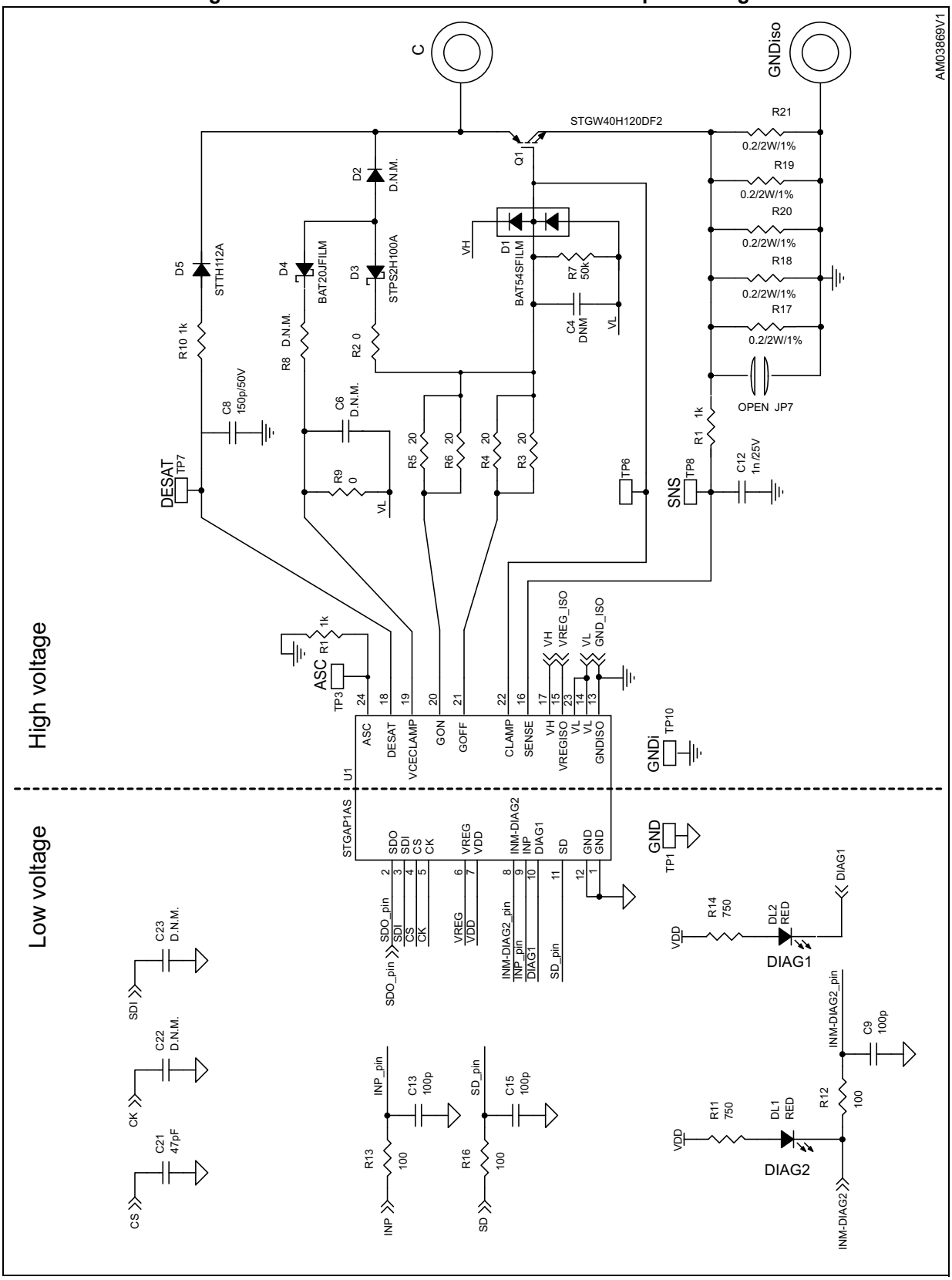


Table 1. STGAP1AS - bill of material

Part reference	Part value	Part description
C1	2.2 µF, 25 V	SMT CERAMIC CAPACITOR, 1206
C2	2.2 µF, 50 V	SMT CERAMIC CAPACITOR, 1206
C3, C16	100 nF, 25 V	SMT CERAMIC CAPACITOR, 0603
C4, C6, C22, C23	D. N. M.	SMT CERAMIC CAPACITOR, 0603
C5	100 nF, 4 V	SMT CERAMIC CAPACITOR, 0603
C7, C11	100 nF, 6.3 V	SMT CERAMIC CAPACITOR, 0603
C8	150 pF, 50 V	SMT CERAMIC CAPACITOR, 0603
C9, C13, C15	100 pF, 6.3 V	SMT CERAMIC CAPACITOR, 0603
C10	100 nF, 50 V	SMT CERAMIC CAPACITOR, 0603
C12	1 nF, 25 V	SMT CERAMIC CAPACITOR, 0603
C14, C19	4.7 µF, 6.3 V	SMT CERAMIC CAPACITOR, 0603
C17,C18	1 µF, 50 V	SMT CERAMIC CAPACITOR, 0805
C20	4.7 µF, 6.3 V	SMT CERAMIC CAPACITOR, 0603
C21	47 pF, 6.3 V	SMT CERAMIC CAPACITOR, 0603
DL1, DL2	Red LED	SMT LED, 0805
D1	BAT54SFILM	SOT-23
D2	D. N. M.	SMB
D3	STPS2H100A	SMA
D4	BAT20JFILM	SOD323
D5	STTH112A	SMA
JP1, JP2, JP4, JP6, JP7	Jumper (OPEN)	JP2SO
JP3, JP5	Jumper (CLOSED)	JP2SO
J1	PIN STRIP	STRIP254P-M-5x2-90
J2	Screw connector	MORSV-508-3P
J3	PIN STRIP 1 x 4	STRIP254P-M-5-split
J4	DIL Male	CON-FLAT-5x2-180M
J5	PIN STRIP	STRIP254P-F-5x2-90
J6	Screw connector	MORSV-508-2P
Q1	STGW40H120DF2	1200 V 40 A N-Ch IGBT, TO-247
Q3A1	D. N. M.	TO-220 footprint for power switch
R10, R15	1 kΩ	SMT RESISTOR, 0603
R2	0 Ω	SMT RESISTOR, 0805
R3, R4, R5, R6	20 Ω	SMT RESISTOR, 1206
R7	50 kΩ	SMT RESISTOR, 0603
R8	D. N. M.	SMT RESISTOR, 0603

Table 1. STGAP1AS - bill of material (continued)

Part reference	Part value	Part description
R1, R9	0 Ω	SMT RESISTOR, 0603
R11, R14	750 Ω	SMT RESISTOR, 0603
R12, R13, R16	100 Ω	SMT RESISTOR, 0603
R17, R18, R19, R20, R21	0.2 Ω, 2W, 1%	SMT RESISTOR, 2512
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	Test point	
U1	STGAP1AS	SO24W

Figure 3. STGAP1AS – layout (top layer)

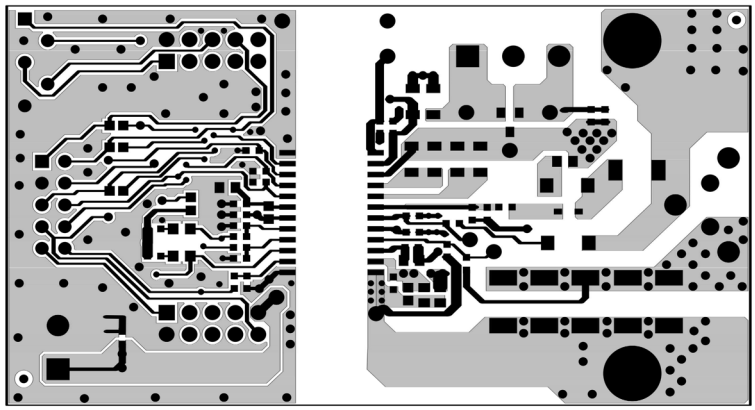


Figure 4. STGAP1AS – layout (bottom layer)

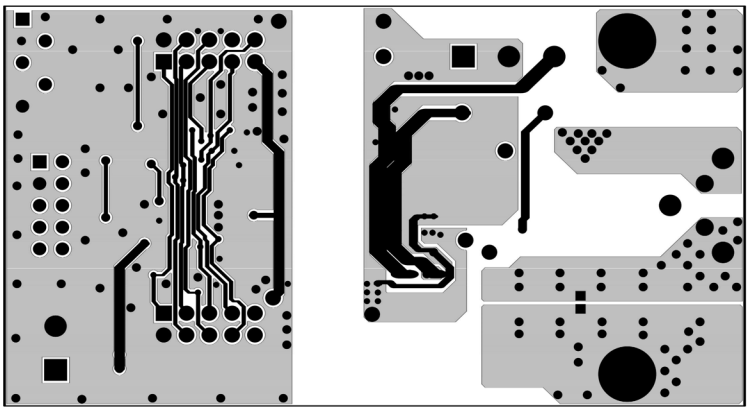
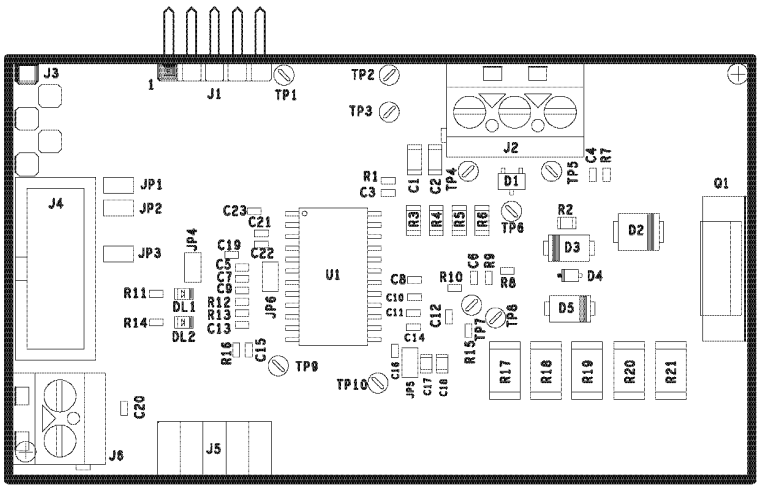


Figure 5. STGAP1AS – layout (component placement view)



Revision history

Table 2. Document revision history

Date	Revision	Changes
02-Nov-2016	1	Initial release.

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